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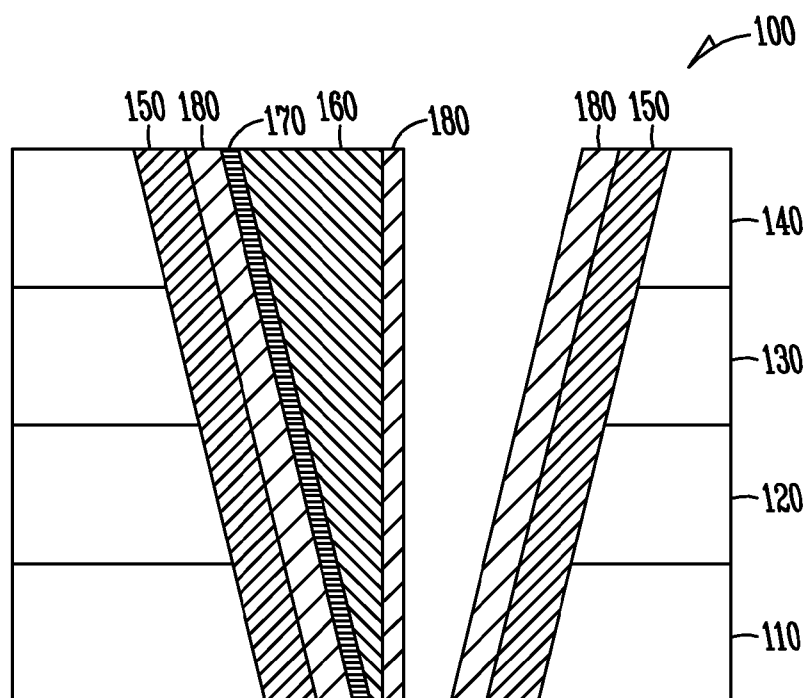


FIG. 1

(57) Abstract: Methods of fabricating 3D charge-trap memory cells are described, along with apparatus and systems that include them. In a planar stack formed by alternate layers of electrically conductive and insulating material, a substantially vertical opening may be formed. Inside the vertical opening a substantially vertical structure may be formed that comprises a first layer, a charge-trap layer, a tunneling oxide layer, and an epitaxial silicon portion. Additional embodiments are also described.



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CHARGE-TRAP BASED MEMORY

RELATED APPLICATION

This patent application claims priority benefit from U.S. Application No.
5 12/548,193 filed 26 August 2009 which is incorporated herein by reference.

BACKGROUND

Non-volatile semiconductor memories (NVSMS) are widely used in
many electronic devices such as personal digital assistants (PDAs), laptop
10 computers, mobile phones, digital cameras, and so on. Some of these memories
operate on the basis of charge trapping.

BRIEF DESCRIPTION OF THE DRAWINGS

Some embodiments are illustrated by way of example and not limitation
15 in the figures of the accompanying drawings in which:

FIG. 1 is a cross sectional view of a portion of a charge-trap based
memory cell, according to various embodiments of the invention;

FIG. 2 is a top view illustrating a charge-trap based memory cell of FIG.
1, according to various embodiments of the invention;

20 FIG. 3 is a three-dimensional (3D) view illustrating a stack of alternate
layers of electrically conductive and insulating materials, in which the charge-
trap based memory cell of FIG. 1 can be formed, according to various
embodiments of the invention;

FIG. 4 is a cross sectional view illustrating an in-process stack of FIG. 3,
25 after forming a first layer on the wall of a vertical opening, according to various
embodiments of the invention;

FIG. 5 is a cross sectional view illustrating an in-process stack of FIG. 4,
after forming a second layer on the first layer, according to various embodiments
of the invention;

30 FIG. 6 is a cross sectional view illustrating an in-process stack of FIG. 5,
after filling a remaining portion of the vertical opening with epitaxial silicon and

removing the sacrificial layer, according to various embodiments of the invention;

FIG. 7 is a cross sectional view illustrating an in-process stack of FIG. 6, after forming a tunneling oxide layer, according to various embodiments of the invention;

FIG. 8 is a cross sectional view illustrating an in-process stack of FIG. 7, after forming a mask for removal of portions of epitaxial silicon, according to various embodiments of the invention;

FIG. 9 is a 3D view illustrating the connection of various contacts used for programming the charge-trap based memory cell of FIG. 1, according to various embodiments of the invention;

FIG. 10 is a flow diagram illustrating a method of forming the charge-trap based memory cell of FIG. 1, according to various embodiments of the invention;

FIG. 11 is a flow diagram illustrating a method of forming the charge-trap based memory cell of FIG. 1, according to various embodiments of the invention; and

FIG. 12 is a diagram illustrating a system, according to various embodiments of the invention.

DETAILED DESCRIPTION

Embodiments of example structures and methods of fabricating a 3D charge-trap based memory cell will now be described. In the following description, for purposes of explanation, numerous examples having example-specific details are set forth to provide a thorough understanding of example embodiments. It will be evident, however, to one skilled in the art that the present examples may be practiced without these example-specific details.

Example embodiments may include forming a substantially vertical opening (hereinafter “vertical opening”) in a planar stack formed by alternate layers of electrically conductive and insulating material. While the term “vertical opening” is used throughout the remainder of this document, it should be noted that such is done only as a matter of convenience. Thus, the broader term “substantially vertical opening” can be used in place of the term “vertical

opening” in every instance.

Inside the vertical opening a substantially vertical structure (hereinafter “vertical structure”) including a first layer (e.g., a blocking dielectric layer), a charge-trap layer, a tunneling oxide layer, and an epitaxial silicon portion may
5 be formed. While the term “vertical structure” is used throughout the remainder of this document, it should be noted that such is done only as a matter of convenience. Thus, the broader term “substantially vertical structure” can be used in place of the term “vertical structure” in every instance.

Similarly, instead of the term “electrically conductive material”, the term
10 “metal” is used throughout the remainder of this document as a matter of convenience. It should be noted that the broader term “electrically conductive material” can be used in place of the term “metal” in every instance. Electrically conductive material may comprise any one or more of the following components, among others: NiSi, Ru, Si, TaN, Ti, TiN, TiSi, WN, and WSi_x.

Finally, instead of the term “insulating material”, the term “oxide” is
15 used throughout the remainder of this document as a matter of convenience. It should be noted that the broader term “insulating material” can be used in place of the term “oxide” in every instance. An insulating material may comprise any one or more of the following components, among others: AlO_x, HfAlO_x,
20 LaAlO_x, LaO_x, SiN, SiO₂, ZrAlO_x, ZrO_x, and ZrSiO_x. In addition, an insulating material may include multiple layers of any one or more of these components.

Some layers that comprise these insulating materials, described in further detail below, may be described as blocking dielectric layers. These include layers having a dielectric layer that includes an inter-poly dielectric (IPD).
25 Some layers that comprise these insulating materials, described in further detail below, may be described as charge-trap layers, such as those that include atomic layer deposition (ALD) SiN. It should be noted that both blocking dielectric layers and charge trap layers may each comprise multiple layers of one or more of the insulating material components listed above, among others.

30 The vertical structure may comprise the dielectric layer, the epitaxial silicon portion partially covered by the tunneling oxide layer, and the charge-trap layer that covers an exposed vertical surface of the epitaxial silicon portion and the tunneling oxide layer. The charge-trap layer may fill a gap between the

tunneling oxide layer and the dielectric layer. It should be noted that, as is the case with blocking dielectric layers and charge trap layers, the tunneling oxide layer may comprise multiple layers, and each of the layers in the tunneling oxide may comprise any one or more of the insulating materials listed above, among
5 others:

This 3D structure may function as a NAND (not AND) charge-trap based (hereinafter “charge-trap”) memory device. In a charge-trap memory device, instead of a floating gate, a charge-trap layer may be formed to store information by trapping charge carriers. The 3D structure comprises a metal-insulator-
10 nitride-oxide-silicon (MINOS) memory device, which includes a gate electrode (e.g., metal layer 120 in FIG. 1), a blocking insulator layer (e.g., IPD layer 150 in FIG. 1), the nitride (e.g., silicon nitride) charge-trap layer (e.g., charge-trap layer 180 in FIG. 1), a tunneling oxide layer (e.g., tunneling oxide layer 170 in FIG. 1), and a silicon channel (e.g., epitaxial silicon 160 in FIG. 1).

15 The silicon nitride layer comprises a material layer in which data are stored. Charge carriers passing through the tunneling oxide layer by tunneling are trapped in the silicon nitride layer. The IPD layer is formed on the silicon nitride layer as a blocking insulating layer for preventing charge carriers trapped in the silicon nitride layer from escaping the silicon nitride layer.

20 FIG. 1 is a cross sectional view illustrating a portion of a charge-trap based memory cell 100, according to various embodiments of the invention. The charge-trap based memory cell 100 (hereinafter “charge-trap memory cell 100”) is formed in the stack 300 of FIG. 3. A portion of the stack 300 shown in FIG. 1 includes metal layers 120 and 140 and oxide layers 110 and 130. It should be
25 noted that while only four total layers of metal and oxide are shown in this figure, as well as in FIGs. 4-8, an actual memory device will have additional layers of metal and oxide. The number of layers has been artificially reduced in FIGs. 1 and 4-8 so that the structure of the layers can be easily seen, and the cell 100 fabrication process can be more easily understood. FIGs. 3 and 9, described
30 below, represent a more practical implementation.

Inside an opening in the stack 300, the vertical structure 190 may be formed. The vertical structure 190 may comprise, a dielectric layer 150, an epitaxial silicon portion (hereinafter “silicon channel”) 160, a tunneling oxide

layer 170 and a charge-trap layer 180. In the memory cell 100, the metal layer 120 and the silicon channel 160 may respectively represent a gate and a channel of a NAND MINOS charge-trap device, in which charge carriers may be trapped in the charge-trap layer 180.

5 FIG. 2 is a top view 200 illustrating a charge-trap memory cell 100 of FIG. 1, according to various embodiments of the invention. The top view 200 shows how the tunneling oxide layer 170, by substantially surrounding the silicon channel 160, allows the charge carriers passing through the silicon channel 160 to tunnel through the tunneling oxide layer 170 so as to be trapped
10 in the charge-trap layer 180. Also the IPD layer 150, as shown in top view 200, substantially surrounds and isolates the charge-trap layer 180 from the metal 140 (also metal layer 120 of FIG. 1), to reduce or prevent the charge carriers from leaking into these metal layers. Various process activities involved in forming the above discussed layers will be described in FIGs. 3-8, discussed below.

15 FIG. 3 is a 3D view illustrating a stack 300 of alternate layers of electrically conductive and insulating materials, in which charge-trap based memory cells can be formed, according to various embodiments of the invention. The shallow trench isolation (STI) 310 may isolate portions of stack 300 where rows of memory cells of a 3D memory arrays may be formed. The memory cells
20 of each row of the memory array may share a common gate contact (e.g., metal layer 120 or 140), which also operates as a word-line contact for the memory array. The oxide layers 110 and 130 insulate metal layers 120 and 140. While six layers of metal and oxide are shown in this figure and in FIG. 9, the total number of layers used in a particular application may vary greatly, from six (as
25 shown) on up to a practically unlimited number. The top metal layer and the bottom metal layer create the select gate in many embodiments. The layers between the top and bottom metal layers form the strings.

 FIG. 4 is a cross sectional view 400 illustrating an in-process stack of FIG. 3, after forming a first layer on the wall of a vertical opening, according to
30 various embodiments of the invention. The process of formation of the charge-trap memory cell 100 of FIG. 1 may begin by forming a vertical opening 410 in the stack 300 of FIG. 3. The vertical openings 410 may be created by an etch process (e.g., wet etch or dry etch, and so on.) following formation of an etch

mask that defines the horizontal position of the openings on the stack 300 of FIG. 3. The walls of the vertical opening 410 may turn out to be only approximately vertical due to limitations of the etch process. FIG. 4 shows two vertical openings 410 that can be used to form to vertical structures. The wall of the vertical openings 410 may be covered with an IPD layer 150. In FIGs. 4-8, only two openings 410 are shown, as part of an array of openings that will typically be much larger in an actual device. The number of openings 410 has been artificially reduced so that the structure of the layers can be easily seen, and the cell fabrication process can be more easily understood.

Deposition of the IPD layer may follow the formation of the vertical opening using the same mask layer as used for defining the horizontal position of the vertical opening. The IPD layer 150 may comprise an insulating material such as silicon dioxide, thermally grown, or deposited using, for example, low-pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). The IPD layer 150 may comprise other insulating materials such an oxide-nitride-oxide (ONO) composite layer, which may be deposited using known methods. The IPD layer 150 may typically have a thickness range of about 10 nm to about 30 nm.

In example embodiments, the IPD layer 18 may comprise a high-k material such as, for example, any of the insulating materials listed above, perhaps deposited using an LPCVD technique or a rapid thermal chemical vapor deposition (RTCVD) process, among others. The IPD layer 150 comprising high-k materials may typically be deposited to a thickness of, for example, about 5 nm to about 30 nm. It is to be noted that the desired thickness is related to the actual k-value of the constituents of the IPD layer 150 and some parameters of the memory cell 100. The IPD layer may insulate the metal layers 120 and 140 from a remaining portion of the vertical structure 190 of FIG. 1, that will be formed in the remaining vertical opening 410 as discussed below.

FIG.5 is a cross sectional view 500 illustrating an in-process stack of FIG. 4, after forming a second layer on the IPD layer 150, according to various embodiments of the invention. The second layer may comprise the sacrificial layer 520, also known by some of ordinary skill in the art as a “spacer layer”. The sacrificial layer 520 may be formed by depositing a layer of dielectric

material using conventional deposition methods such as CVD or physical vapor deposition (PVD) or ALD. The dielectric material may include a nitride such as silicon nitride (SiN) or silicon dioxide (SiO₂). The sacrificial layer 520 may be deposited to a thickness ranging from about 1 nm to about 30 nm. The

5 processing of the remaining vertical opening 510 will now be discussed. The sacrificial layer 520 may also be deposited at the bottom of the opening 510, but can be removed using a spacer etch.

FIG.6 is a cross sectional view 600 illustrating an in-process stack of FIG. 5, after filling remaining portion of the vertical opening with epitaxial
10 silicon and removing the sacrificial layer, according to various embodiments of the invention. At this stage of the process of forming the charge-trap memory cell 100 of FIG. 1, as shown in FIG. 6, the remaining vertical opening 510 of FIG. 5 may be filled by epitaxial silicon material 650. The formation of the epitaxial silicon material 650 may be performed by processes known to those of
15 ordinary skill in the art. In some embodiments, the epitaxial silicon material 650 may be replaced by other forms of silicon material, such as poly-silicon.

After filling the remaining vertical opening with epitaxial silicon material 650, or other substitute silicon material, the sacrificial layer 520 of FIG. 5 may be removed. The removal of the sacrificial layer 520 may be performed by
20 known etch processes, such as wet etch processes. The solvent used in the wet etch process depends on the material used for the sacrificial layer 520. The removal of the sacrificial layer 520 may create an opening 620 between the IPD layer 150 and the epitaxial silicon 160, thus exposing sides of the epitaxial silicon material 650 for further processing as discussed now with respect to FIG.
25 7.

FIG. 7 is a cross sectional view 700 illustrating an in-process stack of FIG. 6, after forming a tunneling oxide layer, according to various embodiments of the invention. The tunneling oxide layer 750 may be formed on the epitaxial silicon material 650 by thermal oxidation of the exposed areas of the epitaxial
30 silicon material 650 located in the opening 620. The thermal oxidation of epitaxial silicon is a well known process and may include, for example, exposing desired areas of epitaxial silicon material 650 to dry oxygen or nitrogen oxide under known conditions. Following the formation of the tunneling oxide layer

750, an opening 720 remains between the tunneling oxide layer 750 and the IPD layer 150, that can be processed as described in FIG. 8.

FIG. 8 is a cross sectional view illustrating an in-process stack of FIG. 7, after forming a mask for removal of portions of epitaxial silicon, according to various embodiments of the invention. The objective of this processing is to form a charge-trap layer 180 shown in FIG. 2. However, in order to allow precursors to flow through the entire opening and substantially fill the opening 720 of FIG. 7, a portion of the epitaxial silicon material 650 of FIG. 7 can be removed. The patterned masks 810 may cover the top of the stack except for exposed areas 830 that allow etching the undesired portions 820 of the epitaxial silicon and portions of the tunneling oxide layer 750 that lies under the exposed areas 830.

Etching of the epitaxial silicon and tunneling oxide may be performed by known etch processes, such as using a dry etch, or combination of dry and wet etch schemes. After completing the etch process, the remaining opening may be filled with charge-trap material to form the charge-trap layer 180 shown in FIGs. 1 and 2. The charge-trap layer 180 may be formed by known processes, such as by ALD, perhaps using silicon nitride (Si_3N_4), or CVD, PVD, and others.

FIG. 9 is a 3D view 900 illustrating the connection of various contacts used for programming the charge-trap memory cell 100 of FIG. 1, according to various embodiments of the invention. The contacts shown in FIG. 9 include word-line (WL) contacts 910, source contacts 950, and bit-line (BL) contacts 960. The source contacts 950 may be formed on a substrate (not shown). After the contacts 910, 950, 960 are connected to various signals known to those of ordinary skill in the art, electrons can be injected into the charge trap layer formed between the oxide layers 935, 945 by tunneling from the substrate, placing a high field on the control gates (e.g., when a positive voltage is applied to a word line coupled to one of the WL contacts 910). These electrons are stored in the trap sites of the charge trap layer (e.g., the charge trap layer 180 of FIG. 1) and alter the threshold voltage V_t of the device. The data represented by the trapped electrons can be erased by tunneling the electrons back into

the substrate, or by tunneling holes into the charge trap layer (e.g., by placing a negative voltage on the word line coupled to one of the WL contacts 910).

FIG. 10 is a high-level flow diagram illustrating a method 1000 for forming the charge-trap memory cell 100 of FIG. 1, according to various embodiments of the invention. At operation 1010, a vertical opening may be formed in the stack 300 of FIG. 3. At operation 1020, as described above with respect to FIGs. 4-8, a vertical structure 190 of FIG. 1 including the first layer (e.g., the IPD layer 150 of FIG. 4), the charge-trap layer 180, the tunneling oxide layer 170, and the epitaxial silicon portion 160, as shown in FIG. 1, is formed.

FIG. 11 is a flow diagram illustrating a method 1100 for forming the charge-trap memory cell 100 of FIG. 1, according to various embodiments of the invention. At operation 1110, a vertical opening may be formed in the stack 300 of FIG. 3. At operation 1120, a first layer (e.g., a blocking dielectric layer such as the IPD layer 150 of FIGs. 4) may be formed on the wall of the vertical opening, as described above with respect to FIG. 4. At operation 1130, a sacrificial layer 520 of FIG. 5 may be formed on the IPD layer 150 (for details, see the description of FIG. 5, above).

The method 1100 may go on to include the activity of operation 1140, which involves filling the remaining vertical opening 510 of FIG. 5 with epitaxial silicon material 650 of FIG. 6 (for details, see the description of FIG. 6, above). At operation 1150, the sacrificial layer 520 may be removed to leave an opening 620, as shown in FIG. 6 (for details, see the description of FIG. 6, above).

At operation 1160, as described above with respect to FIG. 7, the tunneling oxide layer 750 of FIG. 7 can be formed on the epitaxial silicon material 650 of FIG. 7. Portions of the epitaxial silicon material 650 of FIG. 6 may be removed, at operation 1170, to facilitate formation of the charge-trap layer (for details, see the description of FIG. 6). Finally, at operation 1180, the charge-trap layer 180 may be formed to fill the gap between the tunneling oxide layer 170 and the IPD layer 150, and to cover the exposed surfaces of the

epitaxial silicon portion 160 and the IPD layer 150, which are located in the vertical opening.

In some embodiments, the operation 1120, which involves formation of the IPD layer 150, may be postponed to be performed after the operation 1180.

- 5 In this embodiment, the charge-trap layer 180 will cover the tunneling oxide layer 170 and the exposed surface of the epitaxial silicon portion 160. A remaining gap between the charge-trap layer 180 and the wall of the vertical opening may be filled with IPD layer 150 using known processes.

FIG. 12 is a diagram illustrating a system 1200, according to various
10 embodiments of the invention. The system 1200 may include a processor 1210, a memory device 1220, a memory controller 1230, a graphic controller 1240, and an input and output (I/O) controller 1250, a display 1252, a keyboard 1254, a pointing device 1256, and a peripheral device 1258. A bus 1260 couples all of these devices together. A clock generator 1270 provides a clock signal to at least
15 one of the devices of system 1200 via bus 1260. An example of clock generator 1270 may include an oscillator in a circuit board such as a motherboard. Two or more devices shown in system 1200 may be formed in a single chip.

Memory device 1220 may comprise a non-volatile memory including the charge-trap memory cell 100 of FIG. 1. Bus 1260 may be interconnect traces on
20 a circuit board or may be one or more cables. Bus 1260 may also couple the devices of system 1200 by wireless means such as by electromagnetic radiations, for example, radio waves. Peripheral device 1258 may be a printer, an optical device such as a CD-ROM and a DVD reader and writer, a magnetic device reader and writer such as a floppy disk driver, or an audio device such as a
25 microphone.

System 1200 represented by FIG. 12 may includes computers (e.g., desktops, laptops, hand-helds, servers, Web appliances, routers, etc.), wireless communication devices (e.g., cellular phones, cordless phones, pagers, personal digital assistants, etc.), computer-related peripherals (e.g., printers, scanners,
30 monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, camcorders, digital cameras, MP3 (Motion Picture Experts Group, Audio Layer 3) players, video games, watches, etc.), and the like.

Example structures and methods of fabricating a 3D charge-trap memory cell have been described. Although specific embodiments have been described, it will be evident that various modifications and changes may be made to these embodiments. Accordingly, the specification and drawings are to be regarded in
5 an illustrative rather than a restrictive sense.

The Abstract of the Disclosure is provided to comply with 37 C.F.R. §1.72(b), requiring an abstract that allows the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the claims. In addition, in the foregoing
10 Detailed Description, it may be seen that various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as limiting the claims. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

15

CLAIMS

What is claimed is:

1. A method of fabricating a charge-trap memory cell comprising:
5 forming a substantially vertical opening in a planar stack formed by alternate layers of electrically conductive and insulating material; and forming, in the substantially vertical opening, a substantially vertical structure formed at least by a first layer, a charge-trap layer, a tunneling oxide layer, and an epitaxial silicon portion.
10
2. The method of claim 1, wherein the forming of the electrically conductive and insulating materials comprise:
forming a metal comprising any one or more of NiSi, Ru, Si, TaN, Ti, TiN, TiSi, WN, and WSi_x, and forming an oxide comprising any
15 one or more of AlO_x, HfAlO_x, LaAlO_x, LaO_x, SiN, SiO₂, ZrAlO_x, ZrO_x, and ZrSiO_x.
3. The method of claim 1, wherein the forming of the substantially vertical structure by the first layer comprise:
20 forming a dielectric layer including inter-poly dielectric (IPD).
4. The method of claim 1, wherein the forming of the substantially vertical structure by the charge-trap layer comprises:
forming atomic layer deposited (ALD) silicon nitride.
25
5. The method of claim 1, wherein forming of the substantially vertical structure comprises:
filling a portion of the substantially vertical opening as viewed from a top of the substantially vertical opening.
30
6. The method of claim 1, wherein the forming of the substantially vertical structure comprises:

- forming the first layer on a wall of the substantially vertical opening;
- forming a second layer on the first layer;
- filling a remaining portion of the substantially vertical opening with an epitaxial silicon material;
- removing the second layer; and
- forming the tunneling oxide layer on the epitaxial silicon material.
7. The method of claim 6, further comprising:
- removing a portion of the epitaxial silicon material to form the epitaxial silicon portion; and
- forming the charge-trap layer to fill a gap between the tunneling oxide layer and the first layer, and to cover at least one exposed surface of the epitaxial silicon portion and the first layer.
8. The method of claim 7, wherein the second layer comprises a sacrificial layer.
9. The method of claim 7, further comprising:
- forming a bit-line contact and electrically coupling the bit-line contact to the epitaxial silicon portion.
10. The method of claim 1, further comprising:
- forming the planar stack on a source contact formed on a substrate and electrically coupled to the epitaxial silicon portion.
11. The method of claim 1, wherein at least one of the layers of electrically conductive material comprises a word-line for the charge-trap memory cell.
12. The method of claim 1, wherein the first layer comprises a sacrificial layer and the forming of the substantially vertical structure comprises:

- forming the sacrificial layer on a wall of the substantially vertical opening;
- filling a remaining portion of the substantially vertical opening with an epitaxial silicon material;
- 5 removing the sacrificial layer;
- forming the tunneling oxide layer on epitaxial silicon material;
- removing a portion of the epitaxial silicon material to form the epitaxial silicon portion;
- forming the charge-trap layer to cover exposed surfaces of the
- 10 epitaxial silicon portion; and
- forming a dielectric layer to fill a gap between the charge-trap layer and the wall of the substantially vertical opening.
13. The method of claim 1, further comprising:
- 15 forming the planar stack by forming an electrically conductive layer between two insulating layers.
14. A charge-trap memory cell comprising:
- a substantially vertical structure including at least a dielectric
- 20 layer, a charge-trap layer, a tunneling oxide layer, and an epitaxial silicon portion formed inside of a substantially vertical opening created in a planar stack formed by alternate layers of electrically conductive and insulating material.
15. The charge-trap memory cell of claim 14, wherein the dielectric layer
- 25 comprises an inter-poly dielectric (IPD) layer, and wherein the charge-trap layer comprises atomic layer deposited (ALD) silicon nitride.
16. The charge-trap memory cell of claim 14, wherein the substantially vertical structure fills a portion of the substantially vertical opening as viewed
- 30 from a top of the substantially vertical opening and further includes the charge-trap layer filling a gap between the tunneling oxide layer and the dielectric layer.

17. The charge-trap memory cell of claim 14, wherein the substantially vertical structure comprises:
- the dielectric layer substantially covering a wall of the substantially vertical opening and the epitaxial silicon portion partially covered
- 5 by the tunneling oxide layer and the charge-trap layer that covers at least one exposed vertical surface of the epitaxial silicon portion and the tunneling oxide layer.
18. The charge-trap memory cell of claim 14, further comprising:
- 10 a bit-line contact electrically coupled to the epitaxial silicon portion.
19. The charge-trap memory cell of claim 14, further comprising:
- a source contact formed beneath the planar stack and electrically coupled to the epitaxial silicon portion.
- 15
20. The charge-trap memory cell of claim 14, wherein at least one of the layers of electrically conductive material comprises:
- a word-line for the charge-trap memory cell.
- 20 21. A memory comprising:
- a plurality of memory cells, wherein each memory cell of the plurality of memory cells comprises a charge-trap memory cell including
- a substantially vertical structure including at least a dielectric layer, a charge-trap layer, a tunneling oxide layer, and an epitaxial silicon
- 25 portion formed inside of a substantially vertical opening created in a planar stack formed by alternate layers of electrically conductive and insulating material.
22. A method comprising:
- forming a substantially vertical opening in a planar stack formed
- 30 by alternate layers of electrically conductive and insulating material;
- forming a dielectric layer on a wall of the substantially vertical opening;
- forming a sacrificial layer on the dielectric layer;

- filling a remaining portion of the substantially vertical opening with an epitaxial silicon material;
- removing the sacrificial layer;
- forming a tunneling oxide layer on the epitaxial silicon material;
- 5 removing a portion of the epitaxial silicon material to form an epitaxial silicon portion; and
- forming a charge-trap layer to fill a gap between the tunneling oxide layer and the dielectric layer, and to cover at least one exposed surface of the epitaxial silicon portion and the dielectric layer.
- 10
23. The method of claim 22, wherein the forming of the charge-trap layer comprises:
- forming an atomic layer deposited (ALD) silicon nitride.
- 15 24. The method of claim 22, further comprising:
- forming a bit-line contact and electrically coupling the bit-line contact to the epitaxial silicon portion.
25. A method comprising:
- 20 forming a substantially vertical opening in a planar stack formed by alternate layers of electrically conductive and insulating material;
- forming a sacrificial layer on a wall of the substantially vertical opening;
- filling a remaining portion of the substantially vertical opening with an epitaxial silicon material;
- 25 removing the sacrificial layer;
- forming a tunneling oxide layer on the epitaxial silicon material;
- removing a portion of the epitaxial silicon material to form an epitaxial silicon portion;
- 30 forming a charge-trap layer to cover the tunneling oxide layer and exposed surfaces of the epitaxial silicon portion; and

forming a dielectric layer on the wall of the substantially vertical opening to fill a gap between the wall of the substantially vertical opening and the charge-trap layer covering the tunneling oxide layer.

- 5 26. The method of claim 25, wherein the forming of the charge-trap layer comprises:

forming an atomic layer deposited (ALD) silicon nitride.

27. The method of claim 25, further comprising:

10 forming a bit-line contact and electrically coupling the bit-line contact to the epitaxial silicon portion.

28. A system comprising:

a processor;

15 a memory device coupled to the processor, the memory device comprising one or more charge-trap memory cells, each of the charge-trap memory cells comprising:

20 a substantially vertical structure including at least a dielectric layer, a charge-trap layer, a tunneling oxide layer, and an epitaxial silicon portion formed inside of a substantially vertical opening created in a planar stack formed by alternate layers of electrically conductive and insulating material.

29. The system of claim 28, wherein the dielectric layer comprises an inter-poly dielectric (IPD) layer, and wherein the charge-trap layer comprises atomic
25 layer deposited (ALD) silicon nitride.

30. The system of claim 28, wherein the substantially vertical structure includes the charge-trap layer filling a gap between the tunneling oxide layer and the dielectric layer.

30

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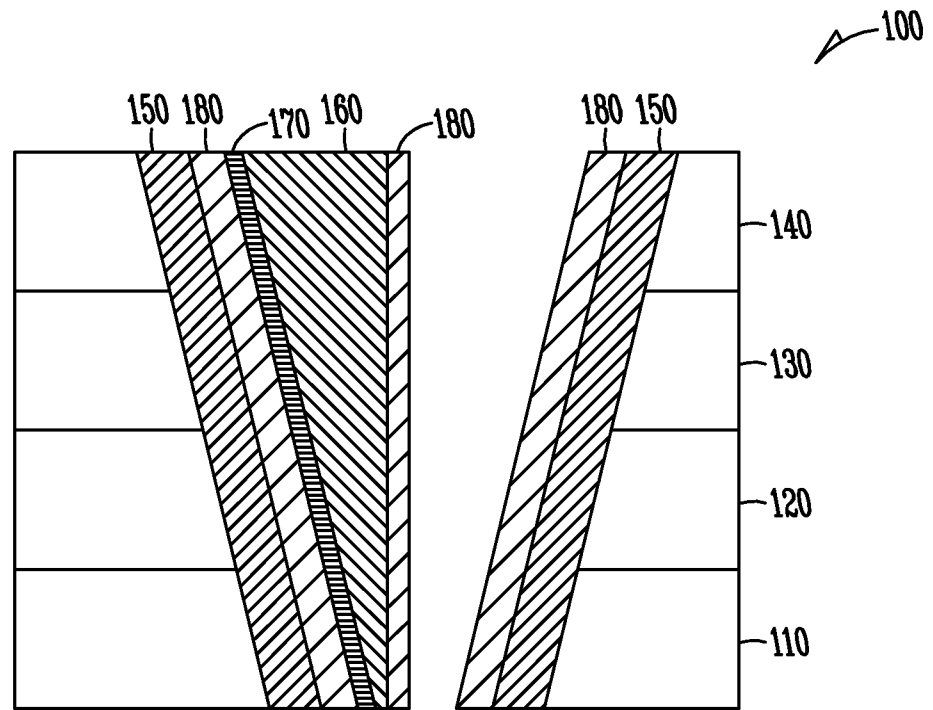


FIG. 1

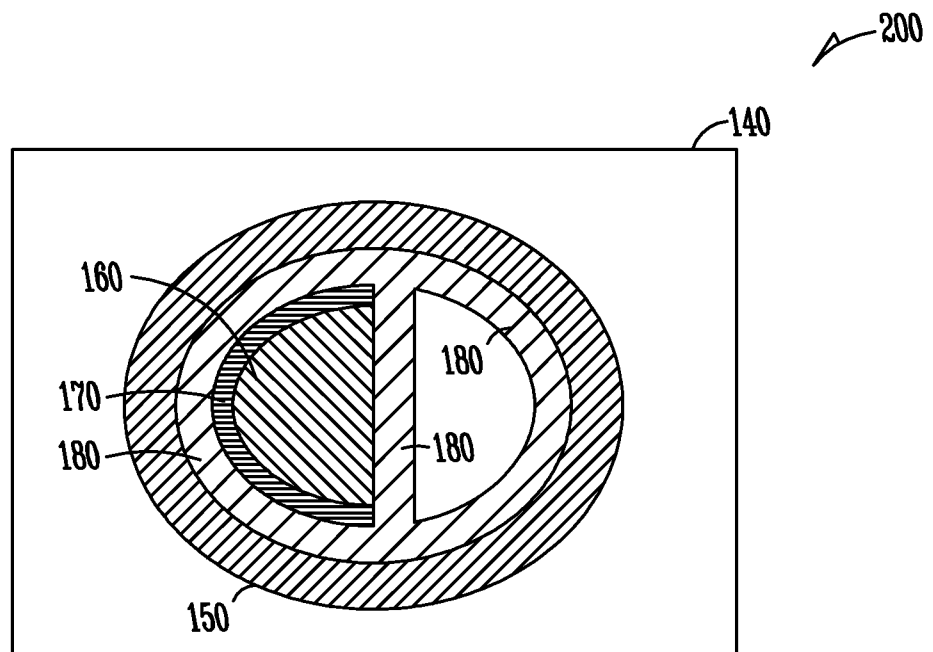


FIG. 2

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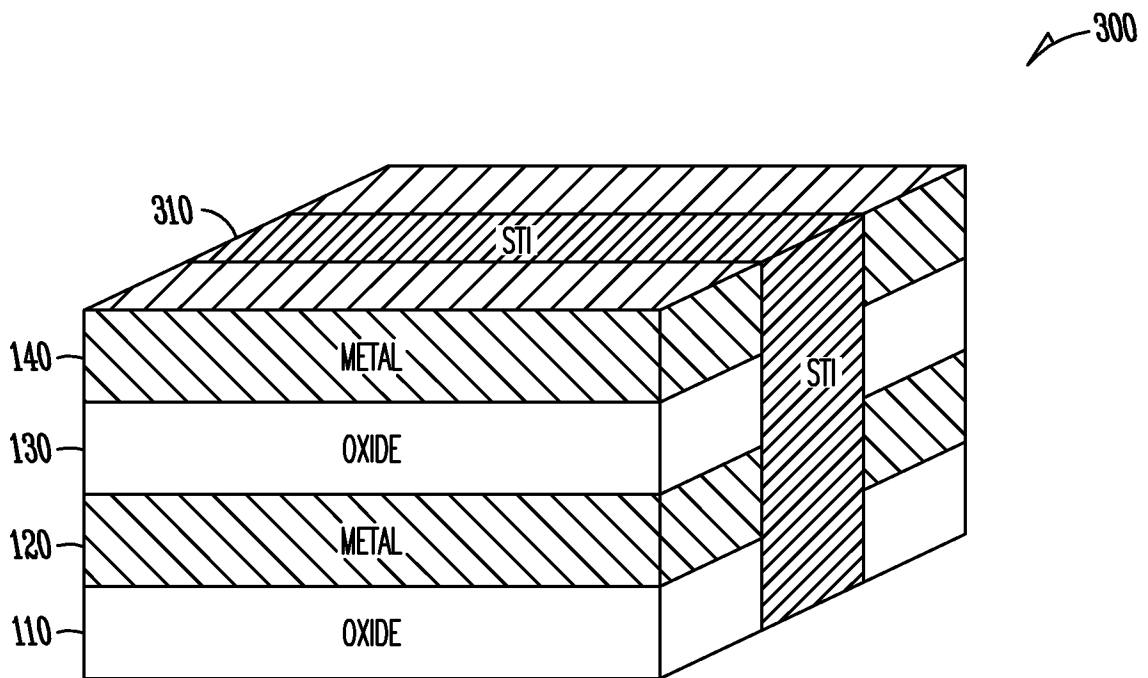


FIG. 3

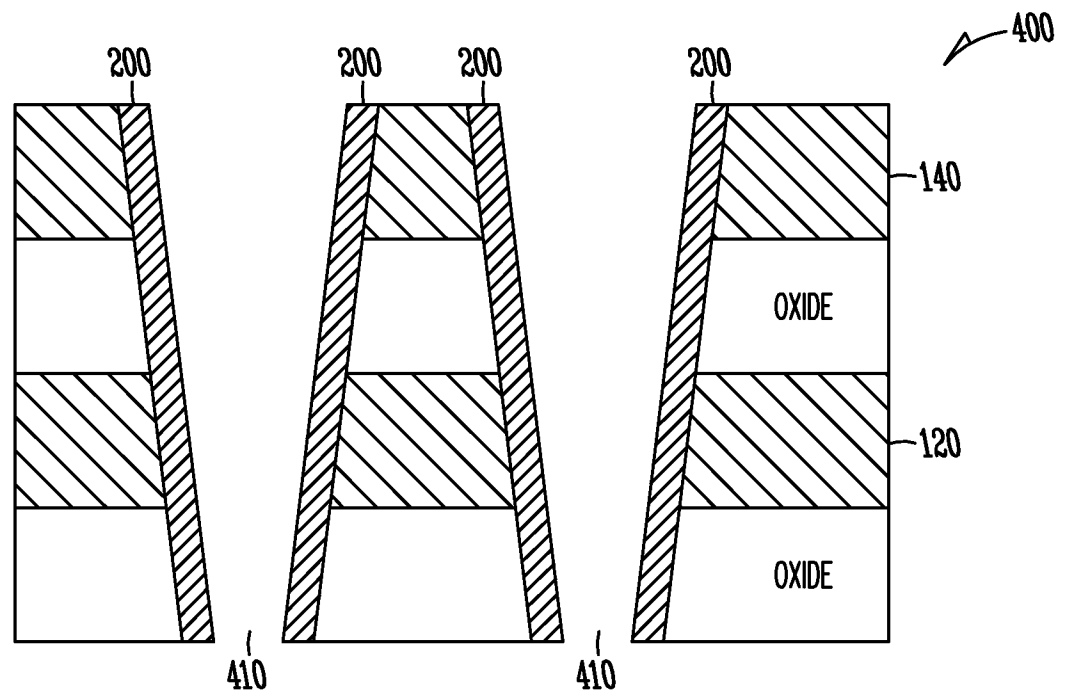


FIG. 4

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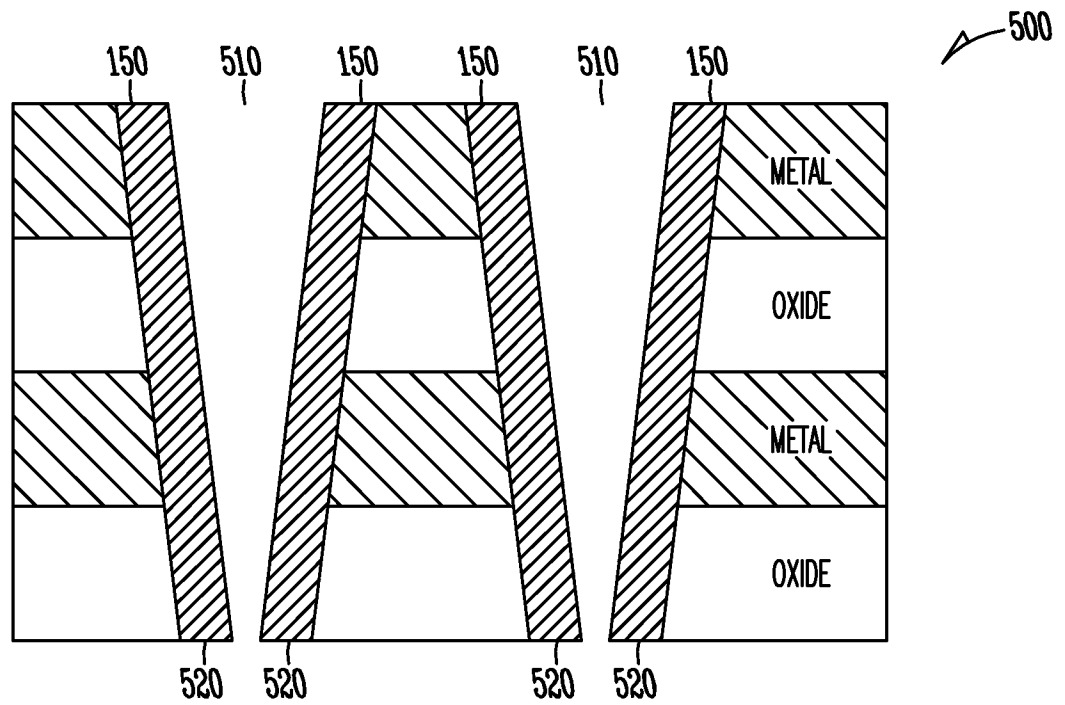


FIG. 5

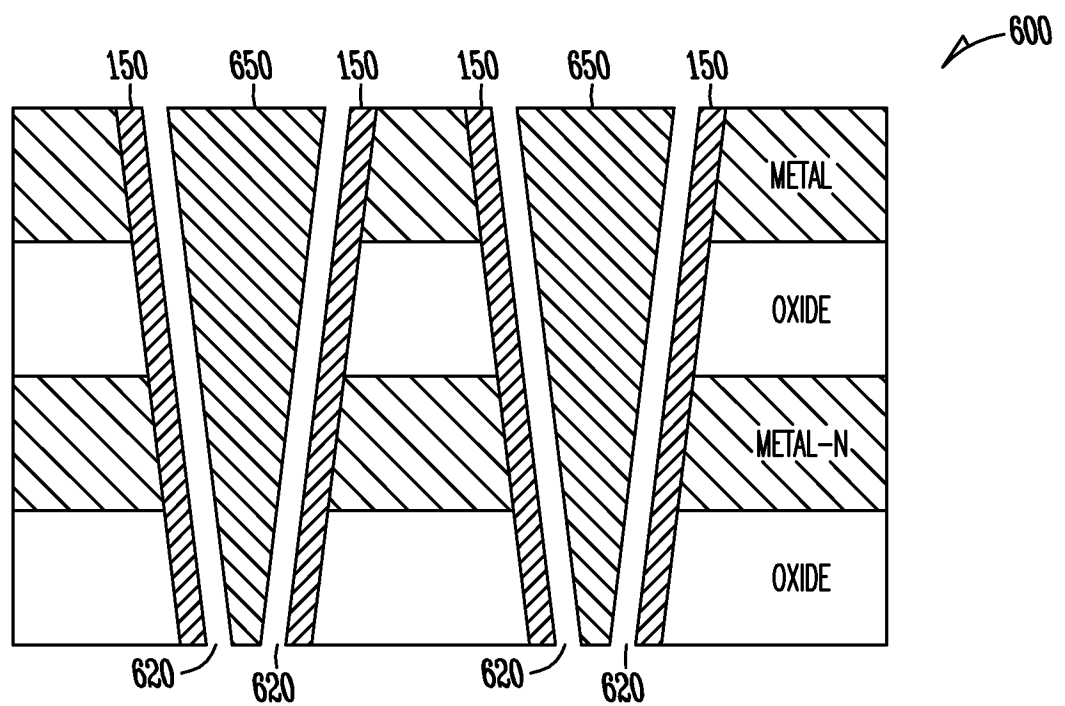


FIG. 6

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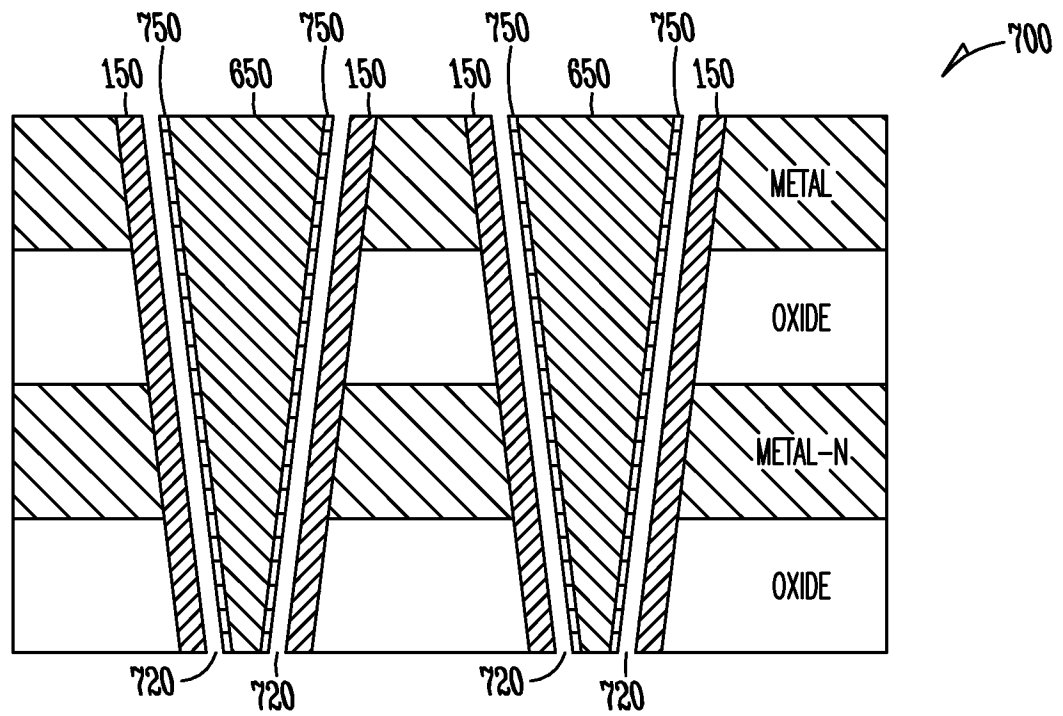


FIG. 7

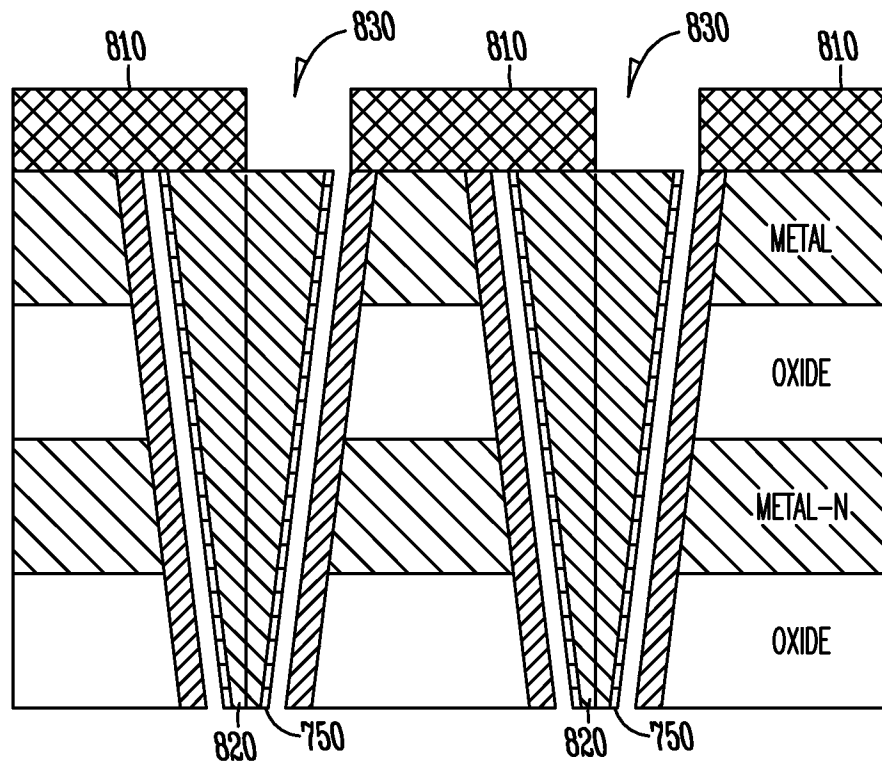


FIG. 8

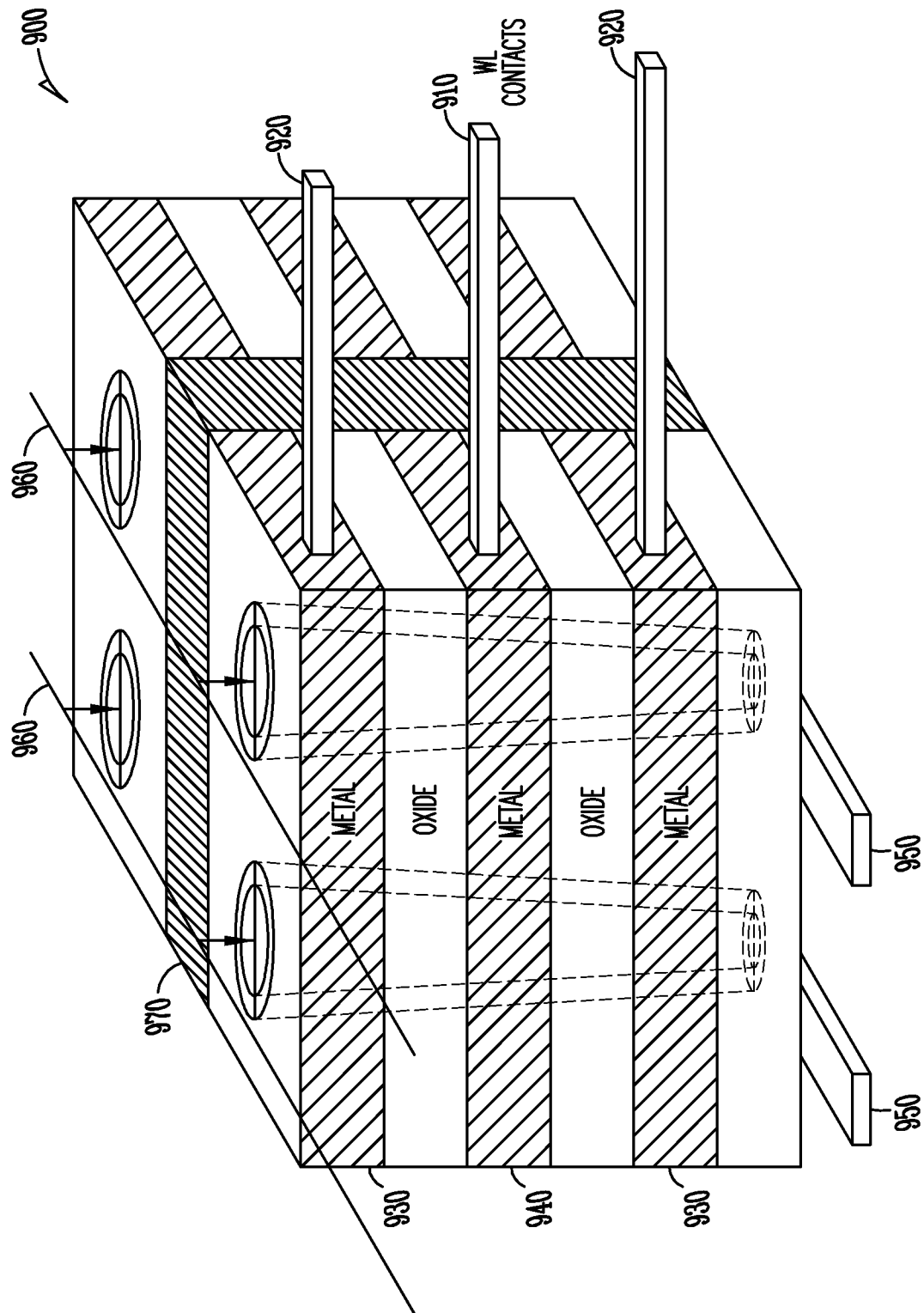
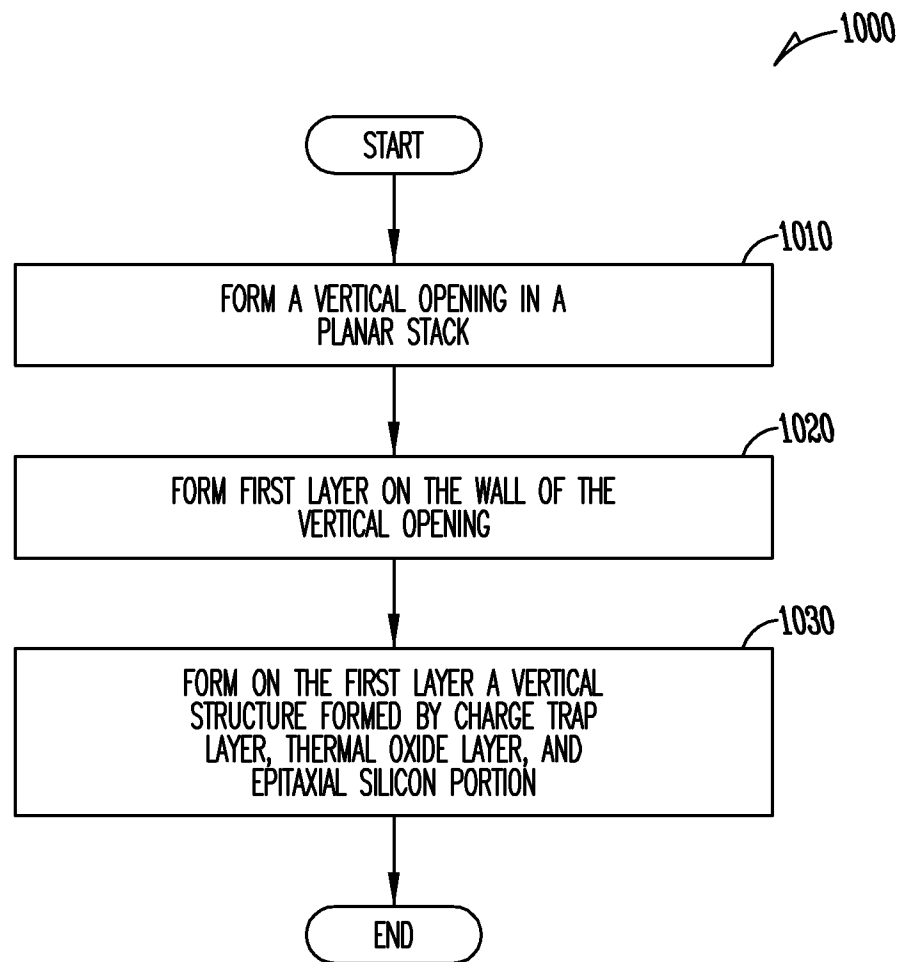
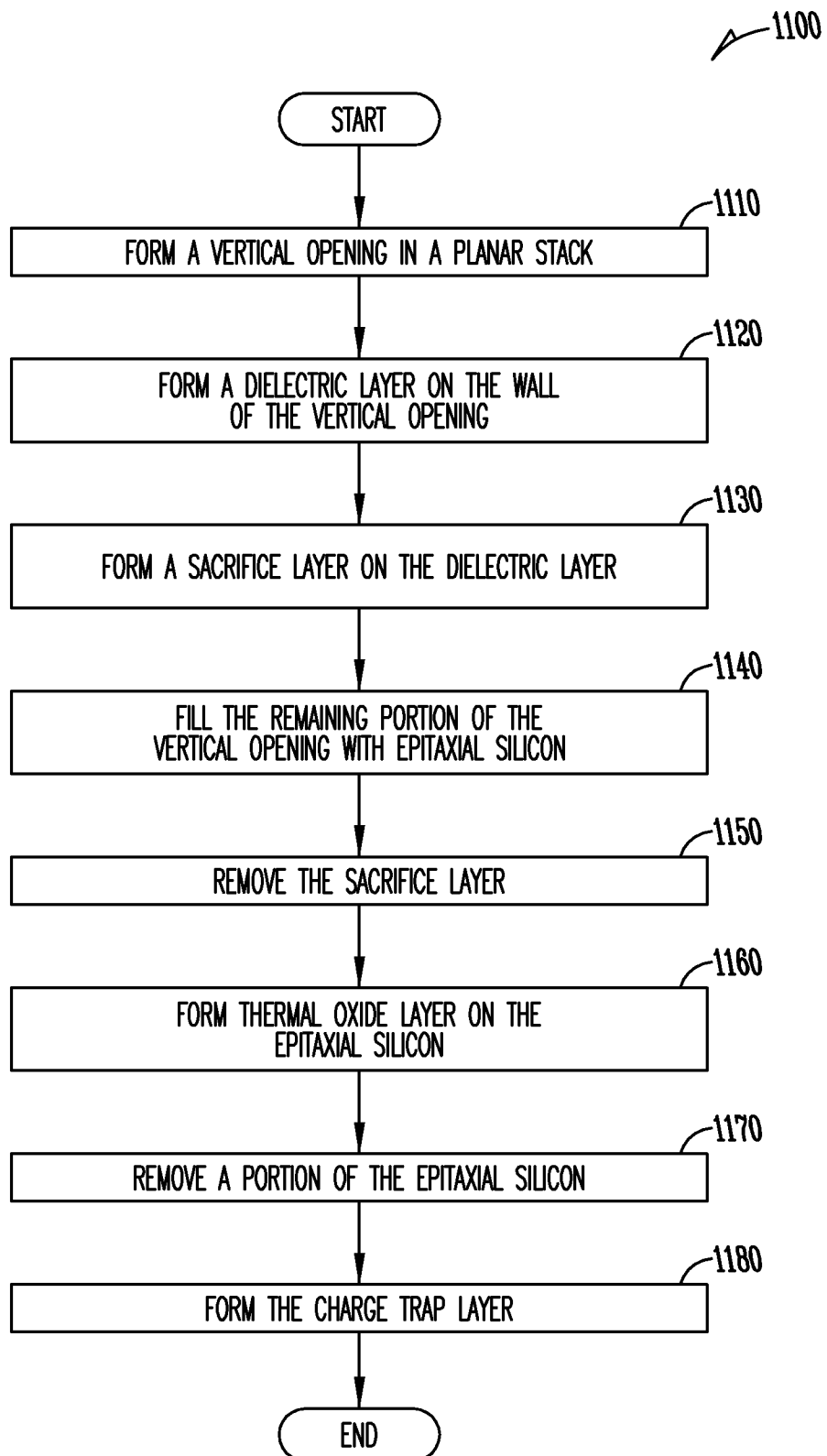


FIG. 9

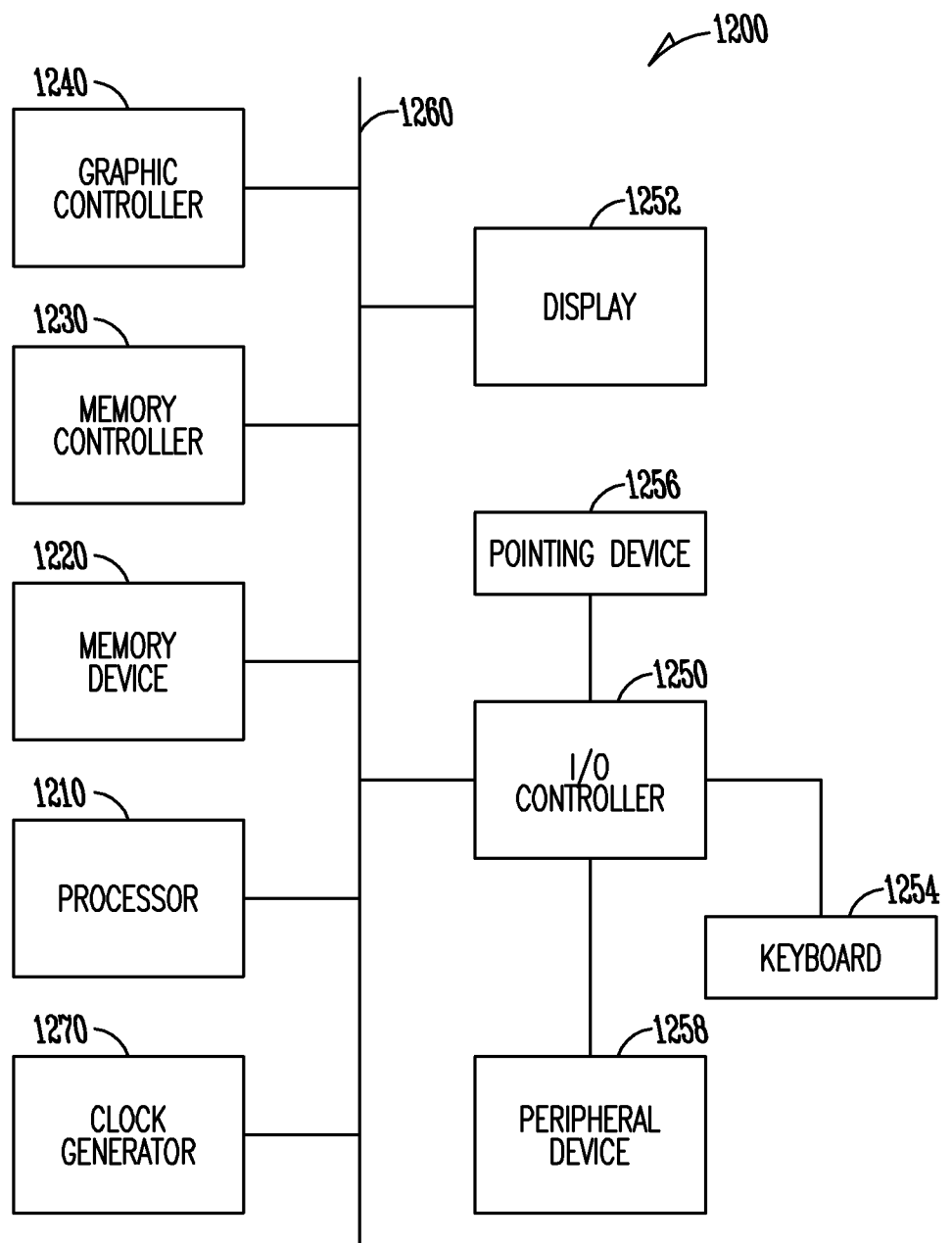
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*FIG. 10*

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*FIG. 11*

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*FIG. 12*