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- (54) **Title:** A METHOD AND APPARATUS FOR GENERATING A CRC VALUE FOR A PACKET

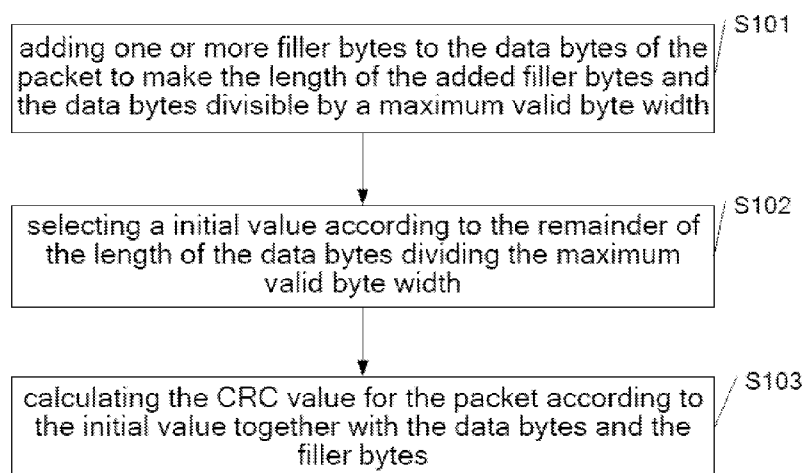


Fig. 3

- (57) **Abstract:** The invention provides a method and apparatus for generating a parallel Cyclic Redundancy Check (CRC) value for a packet, which includes at least one data byte, the method comprising: adding one or more filler bytes to the data bytes of the packet to make the length of the added filler bytes and the data bytes divisible by a maximum valid byte width; selecting a initial value according to the remainder of the length of the data bytes dividing the maximum valid byte width; and calculating the CRC value for the packet according to the initial value together with the data bytes and the filler bytes. The provided method and apparatus may use only one CRC calculation circuit for generating a parallel CRC value for a packet, which may substantially simplify the structure of the circuits.



A METHOD AND APPARATUS FOR GENERATING A CRC VALUE FOR A PACKET

FIELD OF THE INVENTION

5 The present invention generally relates to communication networks. More specifically, relates to a method and apparatus for generating a parallel Cyclic Redundancy Check (CRC) value for a packet.

BACKGROUND

10 When transmitting a packet in the network, such as high-speed Ethernet, in order to reduce the work frequency of the system clock, the packet data parallel width is typically of more than one byte. For example, a packet in the 10G Ethernet has 8 actual packet bytes as input data, a packet in the 100G Ethernet has 80 bytes. However, because the length of the packet in the Ethernet is not fixed, in the end
15 position of the packet, all bytes are not necessarily valid byte. This makes that the algorithm for fixed byte-wide parallel CRC calculation cannot meet the system requirements.

 A traditional approach is to employ a lot of sets of parallel CRC calculation circuit with different input byte wide, which run simultaneously. For example, as
20 shown in Figs. 1 and 2, in 100G Ethernet, there are 80 sets of CRC parallel calculation circuit, which compute one byte, two bytes... up to 80 bytes of input data of the packet respectively. Before the end position of the packet, the CRC value of calculating all bytes is always selected as the current output result. But when asserting end of the packet (EOP), one of all CRC calculation values is selected as a
25 final result according to the data byte number, and then inserted into the frame check sequence (FCS) field of the packet. Disadvantages of this approach are obvious, since many sets of CRC calculation circuit consume a lot of logic resources, which makes the design complicated.

The initial value of the CRC calculation is 0xFFFFFFFF. CRC calculation circuits begin working from the ETH start of the packet (SOP). Before asserting the ETH EOP, the ETH MOD is fixed to the constant binary 1001111 (i.e., decimal 79), which means that all bytes of the packet are valid. Therefore, the CRC circuit output of calculating 80 bytes is always selected. When the ETH EOP is asserted, namely in the end position of the packet, the CRC calculation value is selected to output according to the number of data bytes of the packet as the final result. For example, in the ETH EOP slot, if the ETH MOD is equal to 0, CRC32 (1 Byte) module is selected to output the calculation value as the final CRC result; if 78, then CRC32 (79 Bytes) module is selected to output the calculation value as the final CRC result.

SUMMARY

The present description involves a method and apparatus for generating a parallel CRC value for a packet.

According to a first aspect of the present invention, there is provided a method for generating a parallel CRC value for a packet, which includes at least one data byte, the method comprising:

adding one or more filler bytes to the data bytes of the packet to make the length of the added filler bytes and the data bytes divisible by a maximum valid byte width; selecting a initial value according to the remainder of the length of the data bytes dividing the maximum valid byte width; and

calculating the CRC value for the packet according to the initial value together with the data bytes and the filler bytes.

According to a second aspect of the present invention, there is provided an apparatus for generating a parallel CRC value for a packet, which includes at least one data byte, the apparatus comprising:

an adding means, configured to add one or more filler bytes to the data bytes of the packet to make the length of the added filler bytes and the data bytes divisible by a maximum valid byte width;

a selecting means, configured to select a initial value according to the remainder
5 of the length of the data bytes dividing the maximum valid byte width; and

a calculating unit, configured to the CRC value for the packet according to the initial value together with the data bytes and the filler bytes.

In exemplary embodiments of the present invention, the provided method and apparatus may use only one CRC calculation circuit, much less than 80 sets of CRC
10 parallel calculation circuit as used in the prior art, for generating a parallel CRC value for a packet, which may substantially simplify the structure of the circuits needed, save circuit logic resources for hardware design, such as ASIC or FPGA design.

BRIEF DESCRIPTION OF THE DRAWINGS

15 The invention itself, the preferable mode of use and further objectives are best understood by reference to the following detailed description of the embodiments when read in conjunction with the accompanying drawings, in which:

Fig. 1 illustrates a typical timing diagram for 100G Ethernet packet in the prior art;

20 Fig. 2 illustrates a CRC calculation block diagram of 100G Ethernet packet in the prior art;

Fig.3 is a flowchart illustrating a method for generating a parallel CRC value for a packet in accordance with embodiments of the present invention;

25 Fig. 4 illustrates a typical timing diagram for 100G Ethernet packet in accordance with embodiments of the present invention;

Fig. 5 illustrates a CRC calculation block diagram of 100G Ethernet packet in accordance with embodiments of the present invention; and

Fig.6 exemplarily shows a block diagram for an apparatus for generating a parallel CRC value for a packet in accordance with embodiments of the present invention.

5 DETAILED DESCRIPTION OF THE INVENTION

The embodiments of the present invention are described in detail with reference to the accompanying drawings. Reference throughout this specification to features, advantages, or similar language does not imply that all of the features and advantages that may be realized with the present invention should be or are in any single
10 embodiment of the invention. Rather, language referring to the features and advantages is understood to mean that a specific feature, advantage, or characteristic described in connection with an embodiment is included in at least one embodiment of the present invention. Furthermore, the described features, advantages, and characteristics of the invention may be combined in any suitable manner in one or
15 more embodiments. One skilled in the relevant art will recognize that the invention may be practiced without one or more of the specific features or advantages of a particular embodiment. In other instances, additional features and advantages may be recognized in certain embodiments that may not be present in all embodiments of the invention.

20 As showed in Fig. 3, the present invention provides a method for generating a parallel CRC value for a packet, which includes at least one data byte, the method may comprise following steps: at step S101, adding one or more filler bytes to the data bytes of the packet to make the length of the added filler bytes and the data bytes divisible by a maximum valid byte width, the maximum valid byte width may be set
25 according to the network, for example, the maximum valid byte width may be set to be 8 for 10G Ethernet and 80 for 100G Ethernet, wherein the filler bytes may be such as zero bytes, i.e., "0" bytes, the zero bytes may be all-zero bytes; at step S102, selecting a initial value according to the remainder of the length of the data bytes

dividing the maximum valid byte width, specifically, calculating the remainder of the length of the data bytes of the packet (i.e., the length of the actual valid packet bytes of the packet without the added zero bytes) dividing the maximum valid byte width, and selecting a initial value according to the calculated remainder; and at step S103,
5 calculating the CRC value for the packet according to the initial value together with the data bytes and the filler bytes. Then the calculated CRC value may be added into the FCS field of the packet, and the packet may be sent together with its CRC value to its destination.

In an exemplary embodiment, the CRC value is calculated by only one CRC
10 calculation circuit.

In an exemplary embodiment, the one or more filler bytes are placed ahead of the data bytes in the packet.

Therefore, the provided method may use only one CRC calculation circuit, instead of 80 sets of CRC parallel calculation circuit as used in the prior art, for
15 generating a parallel CRC value for a packet, which may substantially simplify the structure of the circuits, save circuit logic resources for hardware design, such as ASIC or FPGA design. It will be appreciated for those skilled in the art that the present invention may also be applied to calculate the CRC values for more than one packet.

20 At the transmitting side for an Ethernet packet, the length of a packet is usually known to the transmitting side before sending the packet. For example, in the case of generating a new packet at the transmitting side, the packet length is configured from the upper layer software at the transmitting side; in the case of passing through or forwarding packets at the transmitting side, the whole packet has been completely
25 stored in buffer cache, thus, the length of the packet is also known.

Therefore, a set of zero bytes are placed before the actual packet bytes (the number of the zero bytes ranges from 0 to (the maximum valid byte width - 1)), so

that the 'new' length of the packet including the added zero bytes and the actual packet bytes can be divisible by maximum valid byte width. After such processing, the apparatus only requires one set of CRC circuit for calculating CRC value for any number of bytes of a packet. For example, as for 10G Ethernet, only one CRC
5 calculation circuit with 8 input bytes is needed for calculating CRC value for the packet; as for 100G Ethernet, only one CRC calculation circuit with 80 input bytes is needed for calculating CRC value for the packet. The actual packet bytes of the packet may be the valid data of the packet.

In an exemplary embodiment, the step S102 may comprise: finding the initial
10 value in a lookup table having possible numbers of filler bytes and their associated initial values.

In an exemplary embodiment, the initial value is calculated in consideration of the number of the filler bytes and a default initial value which is used when there is no filler byte in the packet.

15 The initial values may be pre-determined and stored in a memory, such as a Read Only Memory (ROM). In fact, the remainder may be corresponding to the number of zero bytes, for example, in 100G Ethernet, if the remainder is 0, no zero byte is added; if the remainder is 1, it means that 79 zero bytes should be added.

IEEE 802.3 protocol defines that the initial value of CRC32 is not all zeros, but
20 0xFFFFFFFF. Accordingly, before calculating CRC value for the data bytes of the packet, the added zero bytes will affect the final calculation result. However, according to the principles of the CRC calculation, the result is the only if the initial CRC value and data bytes of the packet (as input data) have been known. Thus, the system can set different initial values to compensate for the effects because of adding
25 the zero bytes in the packet head. The initial value can be stored in a lookup table in the ROM. When sending a packet, the CRC calculation circuit lookups the table in ROM according to the remainder of the length of the data bytes of the packet dividing the maximum valid byte width, and selects the appropriate initial value. Then CRC

calculation circuit may calculate the final the CRC value for the packet according to the initial value and the data bytes of the packet.

The different initial values may be determined according to a number of algorithms, for example, when the filler bytes are zero bytes, a calculation algorithm may be expressed illustratively by the hardware description language Verilog as follows:

```

task CRC_Init_Calc;
  input    [31:0] Zero_Byte_Num ;
10 //the number of the added zero bytes
  reg      [32:0] Polynomial    ;
  reg      [31:0] Init          ;
  integer   i                  ;
  begin
15   Polynomial = 33'b1_0000_0100_1100_0001_0001_1101_1011_0111;
  //CRC32 generating polynomial
  Init = 32'b1111_1111_1111_1111_1111_1111_1111_1111;
  //CRC32 initial value defined in IEEE 802.3
  for (i=0; i<Zero_Byte_Num*8; i=i+1)
20   begin
    if (Init[0])
      Init = {1'b0, Init[31:1]} ^ Polynomial[32:1];
    else
      Init = {1'b0, Init[31:1]};
25   end
    $display("Insert Zero Byte Number: %d", Zero_Byte_Num, "    Initial
Value: 0x%H", Init);
  end
endtask
30

```

Although the algorithm here is only given for the case of the filler bytes being zero bytes, it will be appreciated that some algorithms may be implemented for other filler bytes based on the teaching of the present invention.

The initial values and corresponding numbers of zero bytes are exemplarily shown in the following table 1.

Table 1

The Numbers of Zero Bytes	CRC Initial Values
0	0xFFFFFFFF
1	0x9BF1A90F
2	0x09B93859
3	0x816474C5
4	0x46AF6449
5	0x339FDE2F
...	...
78	0xCF8B3345
79	0xC48105D5

In an exemplary embodiment, the CRC value may be calculated by only one CRC calculation circuit, instead of 80 sets of CRC calculation circuit as used in the prior art, thereby substantially simplify the structure of the CRC calculation circuit.

5 For example, in 100G Ethernet, there is only CRC circuit of parallel calculating 80 input bytes inside the apparatus. The remainder of the length of the data bytes of the packet dividing 80 is regarded as the read address of lookup table. For example, if the remainder is 0, no zero byte is added and the initial value is all one; if the remainder is 1, it means that 79 zero bytes should be added and calculated together
10 with the data bytes, and initial value is 0xC48105D5.

In an exemplary embodiment, the remainder may be regarded as the read address of corresponding initial value in the lookup table, then the appropriate initial value as required may be found according to the calculated remainder.

15 In an exemplary embodiment, the one or more filler bytes are placed ahead of the data bytes, preferably, the one or more filler bytes are placed at high bit position in the packet, and the at least one data byte is placed at low bit position in the packet.

In an exemplary embodiment, the method according to the present invention may further comprise: prior to the step S101, receiving the packet. Specifically, the
20 step of receiving the packet may further comprise following steps: receiving a first

signal (e.g., CLK signal) which indicates a periodical clock signal; receiving a second signal (e.g., VALID signal) which indicates the data bytes are arriving; asserting a third signal (e.g., SOP signal) which indicates the start of the data bytes when receiving the second signal; receiving a fourth signal (e.g., DATA signal) as the data bytes from the time of asserting the third signal till the time of asserting a fifth signal (e.g., EOP signal) which indicates the end of the data bytes.

Fig. 4 illustrates a typical timing diagram for 100G Ethernet packet in accordance with embodiments of the present invention. As shown in Fig. 4, the timing diagram according to the present invention is changed as compared with that in the prior art shown in fig. 1. Their difference lies in that the signal ETH MOD is no longer needed. In addition, when ETH SOP is asserted, ETH DATA includes the added zero bytes and the data bytes. The zero bytes are placed in the high bit positions of the packet, and the actual packet bytes are placed in the low bit positions of the packet.

Fig. 5 illustrates a CRC calculation block diagram of 100G Ethernet packet in accordance with embodiments of the present invention. It can be seen that the structure of the circuits needed in the present invention is simplified as compared with that in the prior art shown in Fig. 2 since only one CRC calculation circuit is used.

Fig.6 exemplarily shows an apparatus for generating a parallel CRC value for a packet in accordance with embodiments of the present invention.

As shown in Fig. 6, the present invention further provides an apparatus for generating a parallel CRC value for a packet, which includes at least one data byte, the apparatus may comprise: an adding means 610, configured to add one or more filler bytes (such as, "0" bytes) to the data bytes of the packet to make the length of the added filler bytes and the data bytes divisible by a maximum valid byte width, which may be set to be any value according to actual needs, such as 8 or 80; a selecting means 620, configured to select a initial value according to the remainder of

the length of the data bytes dividing the maximum valid byte width; and a calculating means 630, configured to calculate the CRC value for the packet according to the initial value together with the data bytes and the filler bytes.

In an exemplary embodiment, the apparatus may further comprise a lookup table
5 having possible numbers of filler bytes and their associated initial values, wherein the selecting means is configured to find the initial value in the lookup table.

In an exemplary embodiment, the calculating means 630 comprises only one CRC calculation circuit.

In an exemplary embodiment, the initial value is calculated in consideration of
10 the number of the filler bytes and a default initial value which is used when there is no filler byte in the packet.

In an exemplary embodiment, the remainder is regarded as the read address of corresponding initial value in the lookup table.

In an exemplary embodiment, the apparatus may further comprise a receiving
15 means, configured to, receive the packet, which is further configured to: receive a first signal (e.g., CLK signal) which indicates a periodical clock signal; receive a second signal (e.g., VALID signal) which indicates the data bytes are arriving; assert a third signal (e.g., SOP signal) which indicates the start of the data bytes when receiving the second signal; receive a fourth signal (e.g., DATA signal) as the data
20 bytes from the time of asserting the third signal till the time of asserting a fifth signal (e.g., EOP signal) which indicates the end of the data bytes.

In an exemplary embodiment, the one or more filler bytes are placed ahead of the data bytes, preferably, the one or more filler bytes are placed at high bit position in the packet, and the at least one data byte is placed at low bit position in the packet.

25 The structure of the circuit in the apparatus is very simple because of using only one CRC calculation circuit, which can save circuit logic resources for hardware design, such as ASIC or FPGA design.

As long as there is transmitting inside the apparatus and the maximum packet byte width is larger than 1, the method in the present invention is advantageous to the user. Besides the high-speed Ethernet, this method may be applied to any other network, especially when the packet length is variable and the initial value is not
5 zero.

At least one of the adding means 610, the selecting means 620, the calculating means 630, and the receiving means is assumed to comprise program instructions that, when executed, enable the apparatus to operate in accordance with the exemplary embodiments, as discussed above. Any of the adding means 610, the selecting means
10 620, the calculating means 630, and the receiving means as discussed above may be integrated together or implemented by separated components, and may be of any type suitable to the local technical environment, and may comprise one or more of general purpose computers, special purpose computers, microprocessors, digital signal processors (DSP) and processors based on multi-core processor architectures, as
15 non-limiting examples. The ROM mentioned above may be of any type suitable to the local technical environment and may be implemented using any suitable data storage technology, such as semiconductor based memory devices, flash memory, magnetic memory devices and systems, optical memory devices and systems, fixed memory and removable memory.

In general, the various exemplary embodiments may be implemented in
20 hardware or special purpose circuits, software, logic or any combination thereof. For example, some aspects may be implemented in hardware, while other aspects may be implemented in firmware or software which may be executed by a controller, microprocessor or other computing device, although the invention is not limited
25 thereto. While various aspects of the exemplary embodiments of this invention may be illustrated and described as block diagrams, flowcharts, or using some other pictorial representation, it is well understood that these blocks, apparatus, systems, techniques or methods described herein may be implemented in, as non-limiting

examples, hardware, software, firmware, special purpose circuits or logic, general purpose hardware or controller or other computing devices, or some combination thereof.

It will be appreciated that at least some aspects of the exemplary embodiments of the inventions may be embodied in computer-executable instructions, such as in one or more program modules, executed by one or more computers or other devices. Generally, program modules include routines, programs, objects, components, data structures, etc. that perform particular tasks or implement particular abstract data types when executed by a processor in a computer or other device. The computer executable instructions may be stored on a computer readable medium such as a hard disk, optical disk, removable storage media, solid state memory, random access memory (RAM), and etc. As will be realized by one of skill in the art, the functionality of the program modules may be combined or distributed as desired in various embodiments. In addition, the functionality may be embodied in whole or in part in firmware or hardware equivalents such as integrated circuits, field programmable gate arrays (FPGA), and the like.

Although specific embodiments of the invention have been disclosed, those having ordinary skill in the art will understand that changes can be made to the specific embodiments without departing from the spirit and scope of the invention. The scope of the invention is not to be restricted therefore to the specific embodiments, and it is intended that the appended claims cover any and all such applications, modifications, and embodiments within the scope of the present invention.

CLAIMS

What is claimed is:

- 5 1. A method for generating a parallel Cyclic Redundancy Check (CRC) value for a packet, which includes at least one data byte, the method comprising:
 - adding one or more filler bytes to the data bytes of the packet to make the length of the added filler bytes and the data bytes divisible by a maximum valid byte width;
 - selecting a initial value according to the remainder of the length of the data bytes
 - 10 dividing the maximum valid byte width; and
 - calculating the CRC value for the packet according to the initial value together with the data bytes and the filler bytes.
2. The method according to claim 1, wherein the step of selecting comprising:
 - 15 finding the initial value in a lookup table having possible numbers of filler bytes and their associated initial values.
3. The method according to claim 1 or 2, wherein the filler byte is "0" byte.
- 20 4. The method according to any one of claims 1 to 3, wherein the initial value is calculated in consideration of the number of the filler bytes and a default initial value which is used when there is no filler byte in the packet.
5. The method according to any one of claims 1 to 4, wherein the CRC value is
- 25 calculated by only one CRC calculation circuit.
6. The method according to any one of claims 1 to 5, wherein the remainder is regarded as the read address of corresponding initial value in the lookup table.

7. The method according to claim any one of claims 1 to 6, further comprising:
prior to the step of adding, receiving the packet, which further comprising:
receiving a first signal which indicates a periodical clock signal;
receiving a second signal which indicates the data bytes are arriving;
5 asserting a third signal which indicates the start of the data bytes when receiving
the second signal;
receiving a fourth signal as the data bytes from the time of asserting the third
signal till the time of asserting a fifth signal which indicates the end of the data bytes.
- 10 8. The method according to claim any one of claims 1 to 7, wherein the one or more
filler bytes are placed ahead of the data bytes.
9. The method according to claim 8, wherein the one or more filler bytes are placed
at high bit position in the packet, and the at least one data byte is placed at low bit
15 position in the packet.
10. An apparatus for generating a parallel Cyclic Redundancy Check (CRC) value
for a packet, which includes at least one data byte, the apparatus comprising:
an adding means, configured to add one or more filler bytes to the data bytes of
20 the packet to make the length of the added filler bytes and the data bytes divisible by
a maximum valid byte width;
a selecting means, configured to select a initial value according to the remainder
of the length of the data bytes dividing the maximum valid byte width; and
a calculating means, configured to calculate the CRC value for the packet
25 according to the initial value together with the data bytes and the filler bytes.
11. The apparatus according to claim 10, wherein the apparatus further comprising a
lookup table having possible numbers of filler bytes and their associated initial values,

wherein the selecting means is configured to find the initial value in the lookup table.

12. The apparatus according to claim 10 or 11, wherein the filler byte is “0” byte.

5 13. The apparatus according to any one of claims 10 to 12, wherein the initial value is calculated in consideration of the number of the filler bytes and a default initial value which is used when there is no filler byte in the packet.

14. The apparatus according to any one of claims 10 to 13, wherein the calculating
10 means comprises only one CRC calculation circuit.

15. The apparatus according to any one of claims 10 to 14, wherein the remainder is regarded as the read address of corresponding initial value in the lookup table.

15 16. The apparatus according to any one of claims 10 to 15, further comprising:
a receiving means, configured to, receive the packet, which is further configured
to:

receive a first signal which indicates a periodical clock signal;

receive a second signal which indicates the data bytes are arriving;

20 assert a third signal which indicates the start of the data bytes when receiving the
second signal;

receive a fourth signal as the data bytes from the time of asserting the third
signal till the time of asserting a fifth signal which indicates the end of the data bytes.

25 17. The method according to any one of claims 10 to 16, wherein the one or more
filler bytes are placed ahead of the data bytes.

18. The apparatus according to claim 17, wherein the one or more filler bytes are

placed at high bit position in the packet, and the at least one data byte is placed at low bit position in the packet.

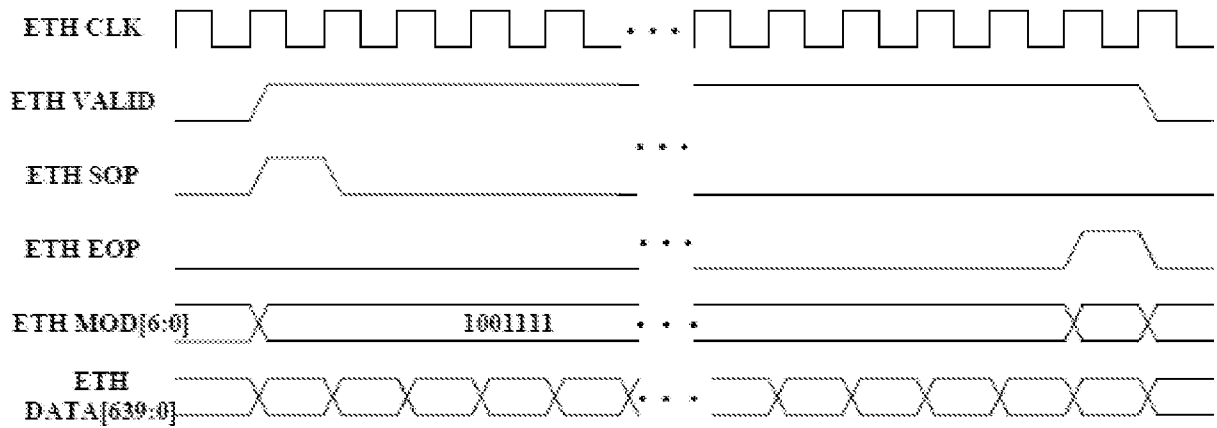


Fig. 1 (prior art)

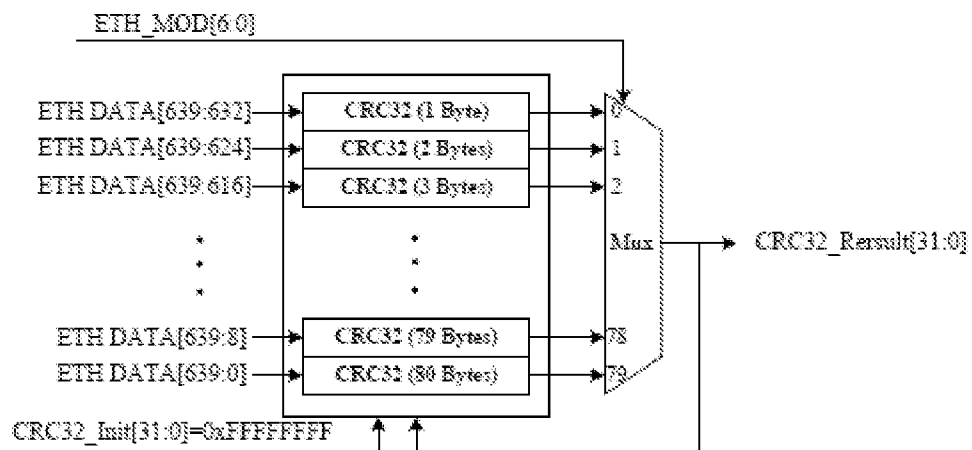


Fig. 2 (prior art)

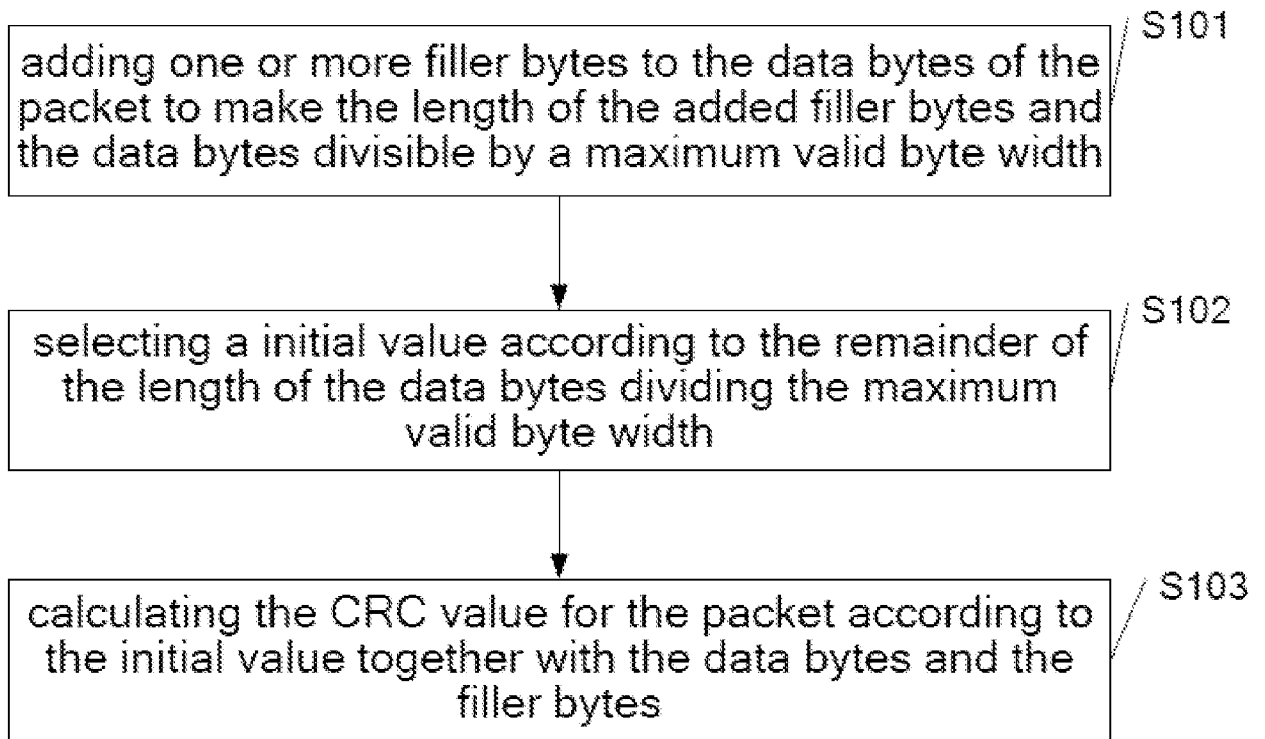


Fig. 3

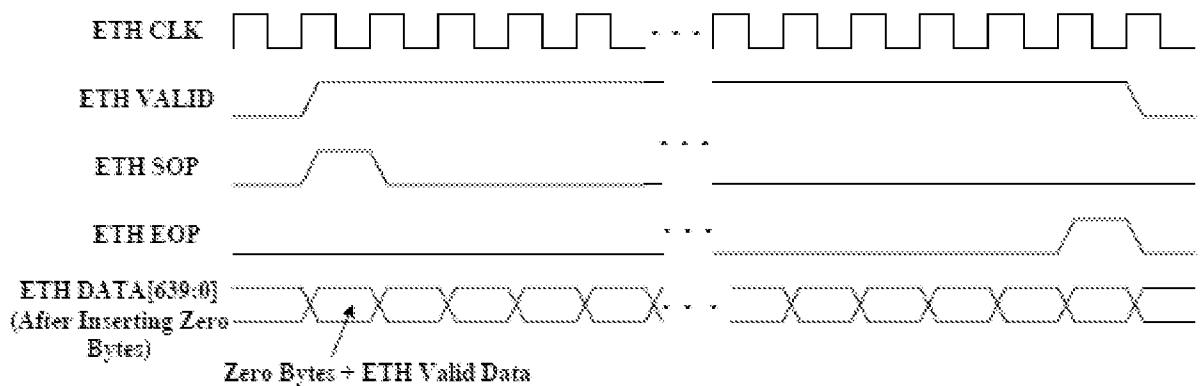


Fig. 4

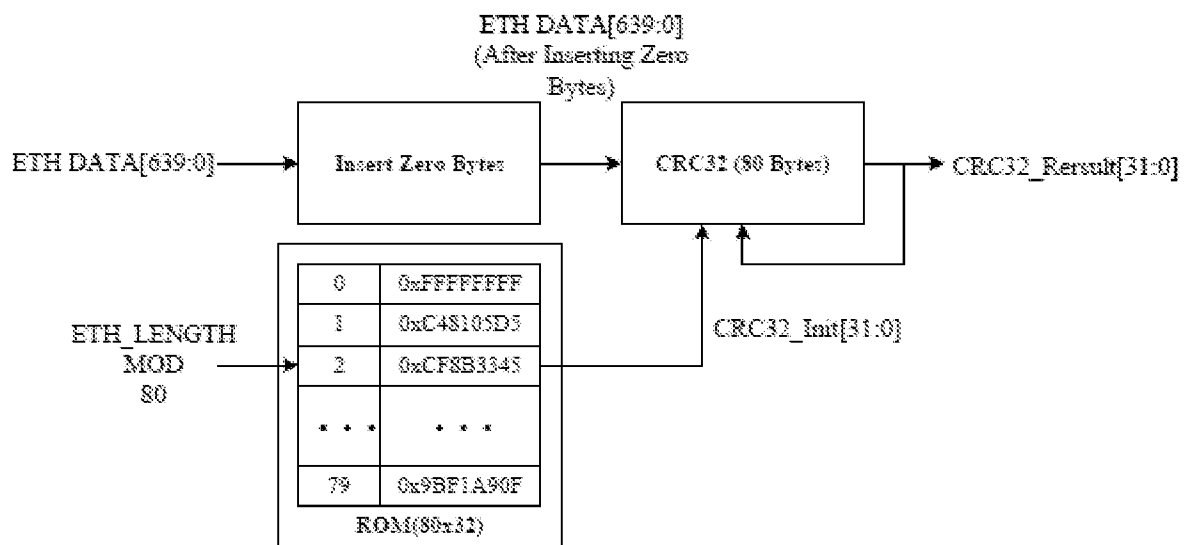


Fig. 5

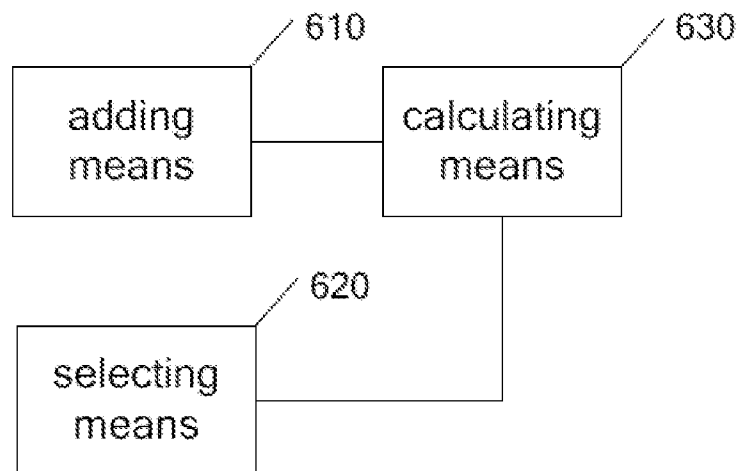


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2015/002256

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04L1/00 H03M13/09
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/067365 A1 (VENKATARAMANA KRISHNAMURTHY B [US] ET AL) 30 March 2006 (2006-03-30) abstract paragraph [0020] - paragraph [0029] paragraph [0051] - paragraph [0069] figures 1,5,6,7 -----	1-18

☐ Further documents are listed in the continuation of Box C.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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