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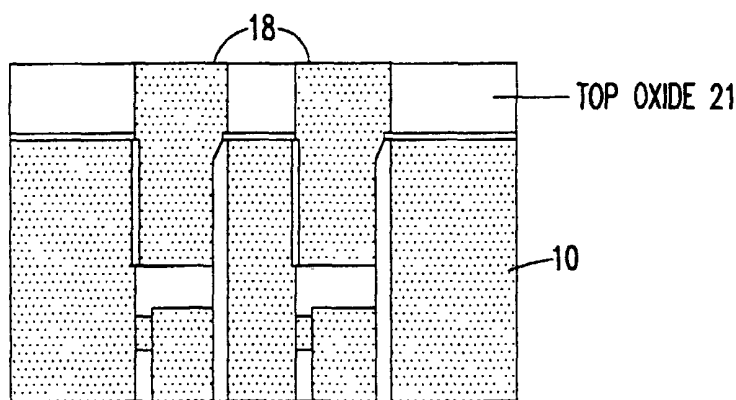
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ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: VERTICAL TRANSISTOR TRENCH CAPACITOR DRAM CELL AND METHOD OF MAKING THE SAME



(57) Abstract: A Top Oxide Method is used to form an oxide layer over an array of vertical transistors as in a trench dynamic random access memory (DRAM) array with vertically stacked access metal oxide semiconductor field effect transistors (MOSFETs). The Top Oxide is formed by first forming the vertical devices with the pad nitride (16) remaining in place. Once the devices have been formed and the gate polysilicon (18) has been planarized down to the surface of the pad nitride, the pad nitride is stripped away leaving the tops of the gate polysilicon plugs extending above the active silicon surface. This pattern of

polysilicon plugs defines the pattern over which the Top Oxide is deposited. The deposited Top Oxide (21) fills the regions between and on top of the polysilicon plugs. The Top Oxide is then planarized back to the tops of the polysilicon plugs so contacts can be made between the passing interconnects and the gates of the vertical devices. The Top Oxide layer serves to separate the passing interconnects from the active silicon thereby reducing capacitive coupling between the two levels and providing a robust etch-stop layer for the reactive ion etch (RIE) patterning of the subsequent interconnect level.



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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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P,X	WO 00 67326 A (RISCH LOTHAR ;WIDMANN DIETRICH (DE); ENDERS GERHARD (US); ILG MATT) 9 November 2000 (2000-11-09) page 7, paragraph 4 -page 11, paragraph 1; figures 4L-4V ---	1-20
Y	EP 0 333 426 A (TOKYO SHIBAURA ELECTRIC CO) 20 September 1989 (1989-09-20) column 12, line 57 -column 14, line 1; figures 3A-3I,5A-5D --- -/--	1-20



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Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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