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(71) **Applicant**: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054-1549 (US).

(72) **Inventors**: **THEN, Han Wui**; 4191 NW 127th Avenue, Portland, Oregon 97229 (US). **DASGUPTA, Sansaptak**; 132 NE Greenridge Terrace, Hillsboro, Oregon 97124 (US). **RADOSAVLJEVIC, Marko**; 3684 NW Loriann Drive, Portland, Oregon 97229 (US).

(74) **Agent**: **GUPTA, Rishi**; Patent Capital Group, 2816 Lago Vista Lane, Rockwall, TX 75032 (US).

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(54) **Title**: GALLIUM NITRIDE TRANSISTORS FOR HIGH-VOLTAGE RADIO FREQUENCY SWITCHES

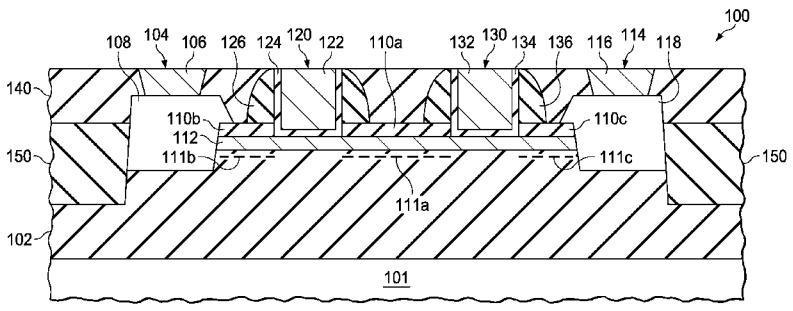


FIG. 1

(57) **Abstract**: Embodiments of this disclosure are directed to a multi-gate gallium nitride (GaN) transistor and methods of making the same. The multi-gate GaN transistor includes a gallium nitride layer. The GaN transistor includes two or more gate electrodes between a drain electrode and a source electrode. A polarization layer is located between the first gate electrode and the second gate electrode, the polarization layer forming a two dimensional electron gas (2DEG) within the GaN layer, the 2DEG electrically coupling the first gate electrode and the second gate electrode.

GALLIUM NITRIDE TRANSISTORS FOR HIGH-VOLTAGE RADIO FREQUENCY SWITCHES

TECHNICAL FIELD

[0001] This disclosure pertains to gallium nitride transistors for high voltage radio frequency switches, and more particularly, to multiple gate enhancement mode gallium nitride transistors with a single source and drain for high-voltage radio frequency switches.

BACKGROUND

[0002] Radio Frequency (RF) switches can be used for switching and routing of high frequency signals. Various materials have been used to form transistors for RF switches. For example, silicon on insulator (SOI) transistors and gallium arsenide (GaAs) pseudomorphic High Electron Mobility Transistors (pHEMT) have been used. Si RF SOI transistors can have high on resistance due to multiple stacking (as many as 14 transistors in series) in order to handle high breakdown voltage. GaAs pHEMT is a depletion mode transistor technology and can use separate supply voltage to the gate to turn the transistor off. The supply voltage in a mobile system is typically limited to either 3.7V (1S battery) or 7.4V (2S battery).

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 is a schematic diagram of a gallium nitride transistor in accordance with embodiments of the present disclosure.

[0004] FIG. 2 is a schematic diagram of a top-down view of a set of multi-gate gallium nitride transistor in accordance with embodiments of the present disclosure.

[0005] FIG. 3A–3L are schematic diagrams illustrating a process flow for fabricating a multi-gate gallium nitride transistor.

[0006] FIG. 4 is an interposer implementing one or more embodiments of the disclosure.

[0007] FIG. 5 is a computing device built in accordance with an embodiment of the disclosure.

[0008] FIG. 6 is a schematic diagram of an example circuit for a radio frequency frontend for a communication device in accordance with embodiments of the present disclosure.

[0009] FIG. 7A–C are a schematic diagrams of example radio frequency circuits with multi-gate transistors in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

[0010] Due to its wide bandgap and high critical breakdown electric field, gallium nitride (GaN) transistors can be used to replace Si RF SOI and GaAs for RF switches. Today's state-of-the-art Si RFSOI and GaAs pHEMT have limitations that can be solved with GaN technology.

[0011] For example, Si RF SOI transistors can have high on-resistances. For example, the on-resistance for an Si RF SOI transistor can be expressed as R(on) = n * R(on_single gate) = n * 2Rcc + n * Rch + n* Rac. Rcc is the contact resistance from N+ Source/Drain to the access region, and Rac is the lateral resistance of the access region from Source/Drain to Channel. The on-resistance for the GaAs transistor can be expressed as R(on) = 2RCC + n * Rch + n * 2Rac.

[0012] Both Si and GaAs transistors have high on resistance, and as a result, very large transistor widths are used to achieve low insertion loss for RF switch application. Moreover, large transistor widths are typically accompanied by large parasitics (capacitance and leakage) which are detrimental to performance and power efficiency.

[0013] This disclosure describes using a multi-gate GaN transistor architecture that uses the low resistance of the 2D electron gas in GaN channel to achieve ON resistance (Ron) that is significantly better than the on-resistances of the Si RF SOI and the GaAs transistors.

[0014] The multiple gates are used to distribute the high gate voltage needed to keep the channel in the off-state under a large RF input voltage swing from Drain to Source. By distributing the gate voltage, the multi-gate GaN RF switch transistor can be used in mobile systems where the supply voltage is typically limited to either 3.7V (1S battery) or 7.4V (2S battery).

[0015] The Rcc components for Si, GaAs and GaN transistors are comparable. The largest resistive contribution to RON in a Si RF SOI MOSFET is Rac due to the lightly-doped Si access region. GaAs pHEMT uses delta-doped quantum-wells and its high electron mobility to achieve a significantly lower Rac than Si, but the charge density is limited to a range from $1 * 10^{12}/cm^2$ to $5 * 10^{12}/cm^2$. GaN offers very high 2DEG charge density in the range from $1 * 10^{13}/cm^2$ to $2 * 10^{13}/cm^2$ and moderately high mobility to enable low sheet resistance for significantly lower Rac than GaAs and Si.

[0016] FIG. 1 is a schematic diagram of a gallium nitride transistor 100 in accordance with embodiments of the present disclosure. The gallium nitride (GaN) transistor 100

includes a GaN layer 102. The GaN layer 102 can reside on a silicon substrate 101 or can be an independent structure. The GaN transistor 100 also includes a drain electrode 104. The drain electrode 104 includes a drain metal 106, which can include for example titanium or tungsten. The drain electrode can also include a doped semiconductor portion 108 between the GaN layer 102 and the drain metal 106. The doped semiconductor portion 108 can include a doped nitride, such as indium gallium nitride ($In_xGa_{1-x}N$, where $5\% < x < 15\%$).

[0017] The GaN transistor 100 also includes a source electrode 114. The drain electrode 114 includes a source metal 116, which can include for example titanium or tungsten. The source electrode can also include a doped semiconductor portion 118 between the GaN layer 102 and the source metal 116. The doped semiconductor portion 118 can include a doped nitride, such as indium gallium nitride ($In_xGa_{1-x}N$, where $5\% < x < 15\%$).

[0018] The GaN transistor 100 also includes a first gate electrode 120. The first gate electrode 120 is located proximate the drain electrode 104. The first gate electrode 120 includes a gate metal 122, which can be titanium nitride for example. The first gate electrode 120 also includes a gate dielectric 124 that is located on the gate metal 122 sidewalls and between the gate metal 122 and the GaN layer 102. A spacer 126 can reside adjacent to the first gate electrode 120 (e.g., contacting the gate dielectride 124). The spacer 126 can be a dielectric material, such as silicon nitride.

[0019] A second gate electrode 130 is located proximate the first gate electrode 120 and proximate the source electrode 114. The second gate electrode 130 includes a gate metal 122, which can be titanium nitride for example. The second gate electrode 130 also includes a gate dielectric 134 that is located on the gate metal 132 sidewalls and between the gate metal 132 and the GaN layer 102. A spacer 136 can reside adjacent to the second gate electrode 130 (e.g., contacting the gate dielectride 134). The spacer 136 can be a dielectric material, such as silicon nitride.

[0020] The GaN transistor 100 also includes a polarization layer 110a located between the first gate electrode 120 and the second gate electrode 130. The polarization layer 110a can form a two dimensional electron gas (2DEG) 111a at an interface between the GaN layer 102 and the polarization layer 110a. In general, a 2DEG can be formed at the heterojunction of two Group III-nitride layers due to the difference in polarization between the two Group III nitride layer. For example, polarizations are inherent in Wurtzite Group III-Nitride crystals. One advantage of GaN transistors over others is that for GaN transistors,

no impurity dopant is needed to form the conductive channel between the source, drain, and gate.

[0021] The presence of the 2DEG is illustrated in FIG. 1 as the dotted lines at the top of the GaN layer 102 and beneath each polarization layer 110a, 110b, and 110c. The 2DEG present at an interface between each polarization layer 110a, 110b, and 110c and the underlying GaN layer. The polarization layer 110a can be referred to as a first polarization layer or an inter-gate polarization layer. The polarization layer 110b that resides between the drain electrode 104 and the first gate electrode 120 can be referred to as a second polarization layer or a drain-side polarization layer. The polarization layer 110c that resides between the source electrode 114 and the second gate electrode 130 can be referred to as a third polarization layer or a source-side polarization layer.

[0022] The 2DEG 111b forms a conductive channel between the drain electrode 104 and the first gate electrode 120. Similarly, the 2DEG 111a forms a conductive channel between the first gate electrode 120 and the second gate electrode 130. The 2DEG 111c forms a conductive channel between the second gate electrode 130 and the source electrode 114.

[0023] The polarization layers 110a, 110b, and 110c, can be formed epitaxially on an aluminum nitride (AlN) interlayer 112. AlN layer 112 can help facilitate growth of the polarization layer 110a, 110b, and 110c. Growth of the polarization layers are discussed further in FIG. 3. Additionally, the AlN layer 112 can act as part of the gate electrode and can enhance the electron mobility in the GaN channel.

[0024] Also shown in FIG. 1 is the interlayer dielectric 140 that isolates the drain electrode from the gate electrodes and the isolates the gate electrodes from the source electrodes and isolates the gate electrodes from themselves.

[0025] Also shown in FIG. 1 is the isolation oxide (such as silicon dioxide) 150 that isolates the entire transistor from other transistors or structures on the substrate / wafer.

[0026] FIG. 1 shows a two-gated, planar GaN transistor but this disclosure contemplates the use of more than two gates. For example, stacking of a large number of gates (N>2) is also contemplated by this disclosure possible. Different transistor architectures, namely, narrow-width or finfet or nanowire/gate-all-around architecture are also possible. Each of these gates can also be of different architecture, with one or more being planar in combination with one or multiple gates being finfets. Finfet and nanowire

GaN could be advantageous in controlling DIBL, short-channel effects and sub-channel punch-through. The advantage of this multi-gate GaN transistor design is that the entire stack incurs the contact resistance of one N+ Source and one N+ Drain (2Rcc). The R(on) for the multi-gate GaN transistor can be expressed as R(on) = 2Rcc + n * Rch + n * 2Rac, where n is the number of gate electrodes.

[0027] FIG. 2 is a schematic diagram of a top-down view of a set of multi-gate gallium nitride transistor 200 in accordance with embodiments of the present disclosure. Transistor 200 includes two gate electrodes: gate 1 206 and gate 2 208, though more than 2 gates can be used.

[0028] The GaN transistor 200 can include a drain 202 and a source 204. The drain 202 can include a plurality of drain electrodes 212a, 212b, 212c, 212d, and 212e. The drain electrodes can be formed to have a common contact point (drain 202). The electrodes can be spaced apart so that a source electrode 214a can be disposed between the electrode 212a and 212b, a source electrode 214b can be disposed between the electrode 212b and 212c, a source electrode 214c can be disposed between the electrode 212c and 212d, and a source electrode 214d can be disposed between the electrode 212d and 212e. The gate electrodes 206 and 208 can be formed. The gate 206 can include a gate electrode 216 that can be disposed in the gaps between each source and drain. The gate 208 can include a gate electrode 218 that can be disposed in the gaps between each source and drain. The gate electrode 216 and the gate electrode 218 are adjacent to each other.

[0029] FIG. 3A–3L are schematic diagrams illustrating a process flow for fabricating a multi-gate gallium nitride transistor. FIG. 3A is a schematic diagram 300 illustrating the forming a polarization layer 304 on a gallium nitride (GaN) layer 302. The GaN layer 302 is formed from a silicon substrate. The polarization layer 304 can include aluminum indium nitride ($Al_xIn_{1-x}N$, where $0.8 < x < 0.9$) or aluminum gallium nitride ($Al_xGa_{1-x}N$, where $0.1 < x < 0.5$). The polarization layer 304 can be grown to a thickness of 5–30 nm. The polarization layer 304 can be grown epitaxially on the GaN layer 302. In some embodiments, an interlayer 306 can be formed on the GaN layer 302. The interlayer 306 can include aluminum nitride (AlN), which can assist in the epitaxial growth of the polarization layer 304. The interlayer 306 can be a 1–2 nm layer of AlN.

[0030] The formation of the polarization layer 304 can cause the formation of a two dimensional electron gas (2DEG) 308 near the surface of the GaN layer 302.

[0031] FIG. 3B is a schematic diagram 310 illustrating the etching of the GaN layer 302. The GaN layer 302 and the polarization layer 304 (and underlying interlayer 306) can be etched using known etching techniques. The substrate is etched at a region that defines the edge of the transistor device. The etched portion of the substrate 312a and 312b are sites for depositing an isolation dielectric material that isolates the GaN transistor from other devices on the substrate.

[0032] FIG. 3C is a schematic diagram 320 illustrating the formation of the isolation dielectric material. The isolation dielectric material 322a and 322b can include silicon dioxide (SiO_2). The isolation dielectric material can be deposited in known ways for forming oxide layers on the gallium nitride.

[0033] FIG. 3D is a schematic diagram 330 illustrating the formation of "dummy" gates 322a and 332b. The dummy gates formed at predetermined locations using lithographic techniques. The dummy gates 332a and 332b are formed to create a positive space around with other components of the transistors can be formed. As will be discussed later, the gate electrodes are formed after other components are formed.

[0034] FIG. 3E is a schematic diagram 340 illustrating the formation of spacer dielectrics 342a and 342b adjacent to the dummy gates 332a and 332b. The spacers 342a and 342b can be formed from lithographic deposition of silicon nitride (SiN) or other dielectric materials. The spacers 342a and 342b facilitate the subsequently described selective removal of the dummy gates 332a and 332b.

[0035] FIG. 3F is a schematic diagram 350 illustrating etching the GaN layer 302 for forming the source and drain. The GaN layer 302 is etched in an area 352a between the isolation dielectric 322a and the dummy electrode 332a (or the spacer 342a if the spacer is formed). The polarization layer 304 (and underlying AlN layer 306) is etched as well as the GaN layer 302. After the etching, a portion of the polarization layer 304 remains between the exposed area 352a and the dummy electrode 332a. After the etching, a portion of the polarization layer 304 remains between the exposed area 352b and the dummy electrode 332b.

[0036] FIG. 3G is a schematic diagram 360 illustrating formation of the source and drain electrodes. A drain semiconductor material 362a is grown for the drain. A source semiconductor material 362b is grown for the source. The drain semiconductor 362a and

source semiconductor 362b can be formed from indium gallium nitride ($In_xGa_{1-x}N$, 5% < x < 15%).

[0037] FIG. 3H is a schematic diagram 370 illustrating forming an interlayer dielectric 372 and planarization. The interlayer dielectric 372 can include a silicon dioxide or other oxide layer. The interlayer dielectric 372 can cover the isolation dielectric 322a and 322b, the drain and source semiconductor 362a and 362b, and the polarization layer 304.

[0038] FIG. 3I is a schematic diagram 380 illustrating forming a contact trench for the source and drain. The drain contact trench 382a can be formed by etching the interlayer dielectric 372 at a location above the drain semiconductor material 362a. The source contact trench 382b can be formed by etching the interlayer dielectric 372 at a location above the drain semiconductor material 362b.

[0039] FIG. 3J is a schematic diagram 390 illustrating forming the drain and source metal for the drain electrode and the source electrode. The drain metal 392a is deposited in the drain contact trench 382a on the drain semiconductor material 362a. The source metal 392b is deposited in the source contact trench 382b on the source semiconductor material 362b. The drain metal 392a and the source metal 392b can include titanium or tungsten.

[0040] FIG. 3K is a schematic diagram 3000 for removing the dummy gates. The dummy electrodes 332a and 332b can be removed by etching. The etching also removes a portion of the polarization layer located below the dummy gates. The resulting structure includes polarization layer 3004a adjacent the drain semiconductor material 362a, the polarization layer 3004c between gate trenches 3002a and 2002b, and the polarization layer 3004b adjacent to the source semiconductor material 362b. The polarization layer 3004a creates a 2DEG 3004a with the GaN layer 302. The 2DEG 3004a extends from the semiconductor material 362a to the edge of the gate trench 3002a. The polarization layer 3004b creates a 2DEG 3004b with the GaN layer 302. The 2DEG 3004b extends from the semiconductor material 362b to the edge of the gate trench 3002b. The 2DEG 3004c extends between the edges of the two gate trenches 3002a and 3002b. In some embodiments, the gate trench is etched to the GaN layer 302. In some embodiments, the gate trench is etched to the AlN layer 306.

[0041] FIG. 3L is a schematic diagram 3100 for forming gate electrodes. A gate dielectric 3104a can be deposited in the gate trench 3002a. A gate metal can be deposited on the gate dielectric 3102a. A gate dielectric 3104b can be deposited in the gate trench 3002b.

A gate metal can be deposited on the gate dielectric 3102b. The polarization layer 3004a creates a 2DEG 3004a with the GaN layer 302. The 2DEG 3004a extends from the semiconductor material 362a to the edge of the gate dielectric 3104a. The polarization layer 3004b creates a 2DEG 3004b with the GaN layer 302. The 2DEG 3004b extends from the semiconductor material 362a to the edge of the gate dielectric 3104b. The 2DEG 3004c extends between the edges of the two gate dielectrics 3104a and 3104b. The gate metal can include titanium nitride.

[0042] FIG. 4 illustrates an interposer 400 that includes one or more embodiments of the disclosure. The interposer 400 is an intervening substrate used to bridge a first substrate 402 to a second substrate 404. The first substrate 402 may be, for instance, an integrated circuit die. The second substrate 404 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 400 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 400 may couple an integrated circuit die to a ball grid array (BGA) 406 that can subsequently be coupled to the second substrate 404. In some embodiments, the first and second substrates 402/404 are attached to opposing sides of the interposer 400. In other embodiments, the first and second substrates 402/404 are attached to the same side of the interposer 400. And in further embodiments, three or more substrates are interconnected by way of the interposer 400.

[0043] The interposer 400 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0044] The interposer may include metal interconnects 408 and vias 410, including but not limited to through-silicon vias (TSVs) 412. The interposer 400 may further include embedded devices 414, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 400.

[0045] In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer 400.

[0046] FIG. 5 illustrates a computing device 500 in accordance with one embodiment of the disclosure. The computing device 500 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die. The components in the computing device 500 include, but are not limited to, an integrated circuit die 502 and at least one communications logic unit 508. In some implementations the communications logic unit 508 is fabricated within the integrated circuit die 502 while in other implementations the communications logic unit 508 is fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 502. The integrated circuit die 502 may include a CPU 504 as well as on-die memory 506, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STT-MRAM).

[0047] Computing device 500 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 510 (e.g., DRAM), non-volatile memory 512 (e.g., ROM or flash memory), a graphics processing unit 514 (GPU), a digital signal processor 516, a crypto processor 542 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 520, an antenna 522, a display or a touchscreen display 524, a touchscreen controller 526, a battery 528 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 528, a compass 530, a motion coprocessor or sensors 532 (that may include an accelerometer, a gyroscope, and a compass), a speaker 534, a camera 536, user input devices 538 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 540 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0048] The non-volatile memory can include a magnetoresistive random-access memory (MRAM) 550. MRAM 550 can include one or more MTJ stacks 552. MTJ stack 552 can be similar to the MTJ stack described in FIG. 2 and include a synthetic antiferromagnet that includes a diffusion barrier between two ferromagnetic layers.

[0049] The communications logic unit 508 enables wireless communications for the transfer of data to and from the computing device 500. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 508 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 500 may include a plurality of communications logic units 508. For instance, a first communications logic unit 508 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communications logic unit 508 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0050] In various embodiments, the computing device 500 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 500 may be any other electronic device that processes data.

[0051] FIG. 6 is a schematic diagram of an example circuit for a radio frequency frontend 600 for a communication device in accordance with embodiments of the present disclosure. The frontend 600 includes a plurality of switches, such as switch 602 or 604. Switch 602 can include one or more multi-gate gallium nitride transistors, such as those described in FIGS. 1 and 2. Additionally, the frontend 600 can include a transmitter 606, which can be a radio transmitter for cellular transmissions. The frontend 600 can also include a receiver 608, which can be a radio receiver. The frontend 600 can also include a wifi and/or Bluetooth transceiver 610.

[0052] FIG. 7A is a schematic diagram of an example radio frequency circuit 700 with a GaN multi-gate transistor 702 in accordance with embodiments of the present

disclosure. The GaN multi-gate transistor 702 includes a RF input 706 and an RF output 708. The RF circuit 700 can be switched by a control element 704. The GaN multi-gate transistor 702 can include a multi-gate transistor as shown in FIG. 1 (or could include more than 2 gates). FIG. 7B is a schematic diagram of an example radio frequency circuit 750 with a multi-gate transistor 712 in accordance with embodiments of the present disclosure. The GaN multi-gate transistor 712 includes a RF input 716 and an RF output 718. The RF circuit 750 can be switched by a control gates 714a and 714b. The GaN multi-gate transistor 712 can include a multi-gate transistor as shown in FIG. 1 (or could include more than 2 gates). FIG. 7C is a schematic diagram of an example radio frequency circuit 700 with a multi-gate transistor 702 in accordance with embodiments of the present disclosure. The GaN multi-gate transistor 722 includes a RF input 726 and an RF output 728. The RF circuit 790 can be switched by a control gates 724a and 724b. An additional control element 724c can be used to provide further control over switching the RF signal. The GaN multi-gate transistor 722 can include a multi-gate transistor as shown in FIG. 1 (or could include more than 2 gates).

[0053] The following paragraphs provide examples of various ones of the embodiments disclosed herein.

[0054] Example 1 is a multi-gate gallium nitride transistor that includes a gallium nitride layer, a drain electrode electrically coupled to the gallium nitride layer, a source electrode electrically coupled to the gallium nitride layer, a first gate electrode located adjacent to the drain electrode, a second gate electrode located between the first gate electrode and the source electrode, and a polarization layer located between the first gate electrode and the second gate electrode.

[0055] Example 2 may include the subject matter of example 1, and may also include a two dimensional electron gas (2DEG) at an interface between the polarization layer and the gallium nitride layer, the 2DEG electrically coupling the first gate electrode and the second gate electrode.

[0056] Example 3 may include the subject matter of any of examples 1 or 2, and may also include a drain-side polarization layer located between the drain and the first gate.

[0057] Example 4 may include the subject matter of example 3, and may also include a 2DEG located between the drain electrode and the first gate electrode at an interface between the drain-side polarization layer and the gallium nitride layer.

[0058] Example 5 may include the subject matter of any of examples 1 or 2 or 3, and may also include a source-side polarization layer located between the source electrode and the second gate electrode.

[0059] Example 6 may include the subject matter of example 5, and may also include a 2DEG located between the second gate electrode and the source electrode at an interface between the source-side polarization layer and the gallium nitride layer.

[0060] Example 7 may include the subject matter of any of examples 1 or 2 , and further include an aluminum nitride layer disposed between the gallium nitride layer and the polarization layer.

[0061] Example 8 may include the subject matter of any of examples 1 or 2 or 7, and also include a first dielectric layer located between the first gate electrode and the polarization layer, and a second dielectric layer located between the second gate electrode and the polarization layer.

[0062] Example 9 may include the subject matter of any of examples 1 or 2 or 3 or 4 or 5 or 6 or 7 or 8, and also include a gallium nitride spacer in contact with sidewalls of the first gate electrode, and a gallium nitride spacer in contact with sidewalls of the second gate electrode.

[0063] Example 10 may include the subject matter of any of examples 1 or 2 or 7 or 8 or 9, wherein one or both of the drain electrode or the source electrode comprises a metal contact located on a doped semiconducting material.

[0064] Example 11 may include the subject matter of example 10, wherein the doped semiconducting material comprises indium gallium nitride.

[0065] Example 12 may include the subject matter of example 1, wherein the polarization layer comprises aluminum indium nitride or aluminum gallium nitride.

[0066] Example 13 may include the subject matter of any of examples 1 or 2 or 7 or 8 or 9 or 10, and also include a third gate electrode residing between the second gate electrode and the source electrode, a fourth polarization layer between the third gate electrode and the source; and a 2DEG at an interface between the fourth polarization layer and the gallium nitride layer and between the third gate electrode and the source electrode.

[0067] Example 14 is a method for fabricating a multi-gate gallium nitride transistor on a gallium nitride layer, the method may include forming an aluminum nitride layer on the gallium nitride surface; forming a polarization layer on the aluminum nitride layer; forming a

first gate electrode on the exposed first portion of the aluminum nitride layer; forming a second gate electrode on the exposed second portion of the aluminum nitride layer; forming a drain electrode proximate the first gate electrode; and forming a source electrode proximate the second gate electrode, the first gate electrode and the second gate electrode formed between the drain electrode and the source electrode.

[0068] Example 15 may include the subject matter of example 14, wherein forming the first gate electrode may include forming a gate dielectric in the exposed first portion of the aluminum nitride layer, and forming a gate metal on the first gate dielectric; and wherein forming the second gate electrode may include forming a second gate dielectric; and forming a second gate metal on the second gate dielectric.

[0069] Example 16 may include the subject matter of any of examples 14 or 15, wherein forming the drain electrode may include forming a doped semiconductor on the gallium nitride layer; and forming a metal electrode on the doped semiconductor; and wherein forming a source electrode may include forming a doped semiconductor on the gallium nitride layer; and forming a metal electrode on the doped semiconductor.

[0070] Example 17 may include the subject matter of any of examples 14 or 15 or 16, wherein forming the doped semiconductor comprises forming indium gallium nitride on the gallium nitride layer; and wherein forming the metal electrode comprises depositing titanium or tungsten on the indium gallium nitride.

[0071] Example 18 may include the subject matter of example 14, wherein forming the polarization layer may include epitaxially growing the polarization layer on the aluminum nitride layer.

[0072] Example 19 may include the subject matter of any of examples 14 or 15, wherein the polarization layer comprises aluminum gallium nitride, aluminum indium nitride, or aluminum gallium indium nitride, or a layered combination of any of aluminum gallium nitride, aluminum indium nitride, or aluminum gallium indium nitride.

[0073] Example 20 is a computing device that includes a processor mounted on a substrate; a communications logic unit within the processor; a memory within the processor; a graphics processing unit within the computing device; an antenna within the computing device; a display on the computing device; a battery within the computing device; a power amplifier within the processor; and a voltage regulator within the processor. The computing device may also include a multi-gate gallium nitride transistor that includes a gallium nitride

layer; a drain electrode electrically coupled to the gallium nitride layer; a source electrode electrically coupled to the gallium nitride layer; a first gate electrode located adjacent to the drain electrode; a second gate electrode located between the first gate electrode and the source electrode; a polarization layer located between the first gate electrode and the second gate electrode.

[0074] Example 21 may include the subject matter of example 20, and may also include a two dimensional electron gas (2DEG) at an interface between the polarization layer and the gallium nitride layer, the 2DEG electrically coupling the first gate electrode and the second gate electrode.

[0075] Example 22 may include the subject matter of any of examples 20 or 21, and may also include a drain-side polarization layer located between the drain and the first gate.

[0076] Example 23 may include the subject matter of example 22, and may also include a 2DEG between the drain electrode and the first gate electrode at an interface between the drain-side polarization layer and the gallium nitride layer.

[0077] Example 24 may include the subject matter of any of examples 20 or 22 or 23, further comprising a source-side polarization layer located between the source electrode and the second gate electrode.

[0078] Example 25 may include the subject matter of example 24, and may also include a 2DEG between the second gate electrode and the source electrode between the source-side polarization layer and the gallium nitride layer.

[0079] Example 26 may include the subject matter of any of examples 20, and may also include an aluminum nitride layer disposed between the gallium nitride layer and the polarization layer.

[0080] Example 27 may include the subject matter of any of examples 20 or 26, and may also include a first dielectric layer located between the first gate electrode and the polarization layer, and a second dielectric layer located between the second gate electrode and the polarization layer.

[0081] Example 28 may include the subject matter of any of examples 20 or 26 or 27, and may also include a gallium nitride spacer in contact with sidewalls of the first gate electrode, and a gallium nitride spacer in contact with sidewalls of the second gate electrode.

[0082] Example 29 may include the subject matter of any of examples 20 or 21 or 22 or 23 or 24 or 25 or 26 or 27 or 28 wherein one or both of the drain electrode or the source electrode comprises a metal contact located on a doped semiconducting material.

[0083] Example 30 may include the subject matter of example 23, wherein the doped semiconducting material comprises indium gallium nitride.

[0084] Example 31 may include the subject matter of example 220, wherein the polarization layer comprises aluminum indium nitride or aluminum gallium nitride.

[0085] Example 32 may include the subject matter of any of examples 20 or 22 or 24, and may also include a third gate electrode residing between the second gate electrode and the source electrode, a fourth polarization layer between the third gate electrode and the source.

[0086] Example 33 may include the subject matter of example 32; and may also include 2DEG at an interface between the fourth polarization layer and the gallium nitride layer between the third gate electrode and the source electrode.

[0087] In the description and claims, the terms coupled and connected, along with their derivatives, may be used. In particular embodiments, connected may be used to indicate that two or more elements are in direct physical or electrical contact with each other. Coupled may mean that two or more elements are in direct physical or electrical contact. However, coupled may also mean that two or more elements may not be in direct contact with each other, but yet may still cooperate or interact with each other.

[0088] Reference in the specification to “one embodiment” or “some embodiments” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least an implementation. The appearances of the phrase “in one embodiment” in various places in the specification may or may not be all referring to the same embodiment.

[0089] Although embodiments have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed subject matter may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.

CLAIMS:

1. A multi-gate gallium nitride transistor comprising:

a gallium nitride layer;

a drain electrode electrically coupled to the gallium nitride layer;

a source electrode electrically coupled to the gallium nitride layer;

a first gate electrode located adjacent to the drain electrode;

a second gate electrode located between the first gate electrode and the source electrode;

a polarization layer located between the first gate electrode and the second gate electrode.

2. The gallium nitride transistor of claim 1, further comprising a two dimensional electron gas (2DEG) at an interface between the polarization layer and the gallium nitride layer, the 2DEG electrically coupling the first gate electrode and the second gate electrode.

3. The gallium nitride transistor of claim 1, further comprising a drain-side polarization layer located between the drain and the first gate.

4. The gallium nitride transistor of claim 3, further comprising a 2DEG between the drain electrode and the first gate electrode at an interface between the drain-side polarization layer and the gallium nitride layer.

5. The gallium nitride transistor of any of claims 1 or 2 or 3, further comprising a source-side polarization layer located between the source electrode and the second gate electrode.

6. The gallium nitride transistor of claim 5, further comprising a 2DEG between the second gate electrode and the source electrode at an interface between the source-side polarization layer and the gallium nitride layer.

7. The gallium nitride transistor of any of claims 1 or 2, further comprising an aluminum nitride layer disposed between the gallium nitride layer and the polarization layer.

8. The gallium nitride transistor of any of claims 1 or 2 or 7, further comprising:

a first dielectric layer located between the first gate electrode and the polarization layer, and

a second dielectric layer located between the second gate electrode and the polarization layer.

9. The gallium nitride transistor of any of claims 1 or 2 or 7 or 8, further comprising:

a gallium nitride spacer in contact with sidewalls of the first gate electrode, and

a gallium nitride spacer in contact with sidewalls of the second gate electrode.

10. The gallium nitride transistor of any of claims 1 or 2 or 7 or 8 or 9, wherein one or both of the drain electrode or the source electrode comprises a metal contact located on a doped semiconducting material.

11. The gallium nitride transistor of claim 10, wherein the doped semiconducting material comprises indium gallium nitride.

12. The gallium nitride transistor of claim 1, wherein the polarization layer comprises aluminum indium nitride or aluminum gallium nitride.

13. A method for fabricating a multi-gate gallium nitride transistor on a gallium nitride layer, the method comprising:

forming an aluminum nitride layer on the gallium nitride surface;

forming a polarization layer on a portion of the aluminum nitride layer;

forming a first gate electrode on the exposed first portion of the aluminum nitride layer;

forming a second gate electrode on the exposed second portion of the aluminum nitride layer;

forming a drain electrode proximate the first gate electrode; and

forming a source electrode proximate the second gate electrode, the first gate electrode and the second gate electrode formed between the drain electrode and the source electrode.

14. The method of claim 13, wherein:

forming the first gate electrode comprises:

forming a gate dielectric in the exposed first portion of the aluminum nitride layer, and

forming a gate metal on the first gate dielectric; and wherein

forming the second gate electrode comprises:

forming a second gate dielectric; and

forming a second gate metal on the second gate dielectric.

15. The method of any of claims 13 or 14, wherein forming the drain electrode comprises:

forming a doped semiconductor on the gallium nitride layer; and

forming a metal electrode on the doped semiconductor; and

wherein forming a source electrode comprises:

forming a doped semiconductor on the gallium nitride layer; and

forming a metal electrode on the doped semiconductor.

16. The method of claim 15, wherein forming the doped semiconductor comprises forming indium gallium nitride on the gallium nitride layer; and

wherein forming the metal electrode comprises depositing titanium or tungsten on the indium gallium nitride.

17. The method of claim 13, wherein forming the polarization layer comprises: epitaxially growing the polarization layer on the aluminum nitride layer.

18. The method of any of claims 13 or 17, wherein the polarization layer comprises aluminum gallium nitride, aluminum indium nitride, or aluminum gallium indium nitride, or a layered combination of any of aluminum gallium nitride, aluminum indium nitride, or aluminum gallium indium nitride.

19. The method of any of claims 13 or 18, wherein the polarization layer comprises aluminum gallium nitride, aluminum indium nitride, or aluminum gallium indium nitride, or a layered combination of any of aluminum gallium nitride, aluminum indium nitride, or aluminum gallium indium nitride.

20. A computing device comprising:

a processor mounted on a substrate;

a communications logic unit within the processor;

a memory within the processor;

a graphics processing unit within the computing device;

an antenna within the computing device;

a display on the computing device;

a battery within the computing device;

a power amplifier within the processor; and

a voltage regulator within the processor;

wherein the computing device comprises:

a multi-gate gallium nitride transistor comprising:

a gallium nitride layer;

a drain electrode electrically coupled to the gallium nitride layer;

a source electrode electrically coupled to the gallium nitride layer;

a first gate electrode located adjacent to the drain electrode;

a second gate electrode located between the first gate electrode and the source electrode;

a polarization layer located between the first gate electrode and the second gate electrode

21. The computing device of claim 20, further comprising a two dimensional electron gas (2DEG) at an interface between the polarization layer and the gallium nitride layer, the 2DEG electrically coupling the first gate electrode and the second gate electrode.

22. The computing device of claim 20, further comprising a drain-side polarization layer located between the drain and the first gate.

23. The computing device of claim 22, further comprising a 2DEG between the drain electrode and the first gate electrode at an interface between the drain-side polarization layer and the gallium nitride layer.

24. The computing device of any of claims 20 or 21 or 22 or 23, further comprising a source-side polarization layer located between the source electrode and the second gate electrode.

25. The computing device of claim 24, further comprising a two dimensional electron gas (2DEG) between the second gate electrode and the source electrode at an interface between the gallium nitride layer and the source side polarization layer.

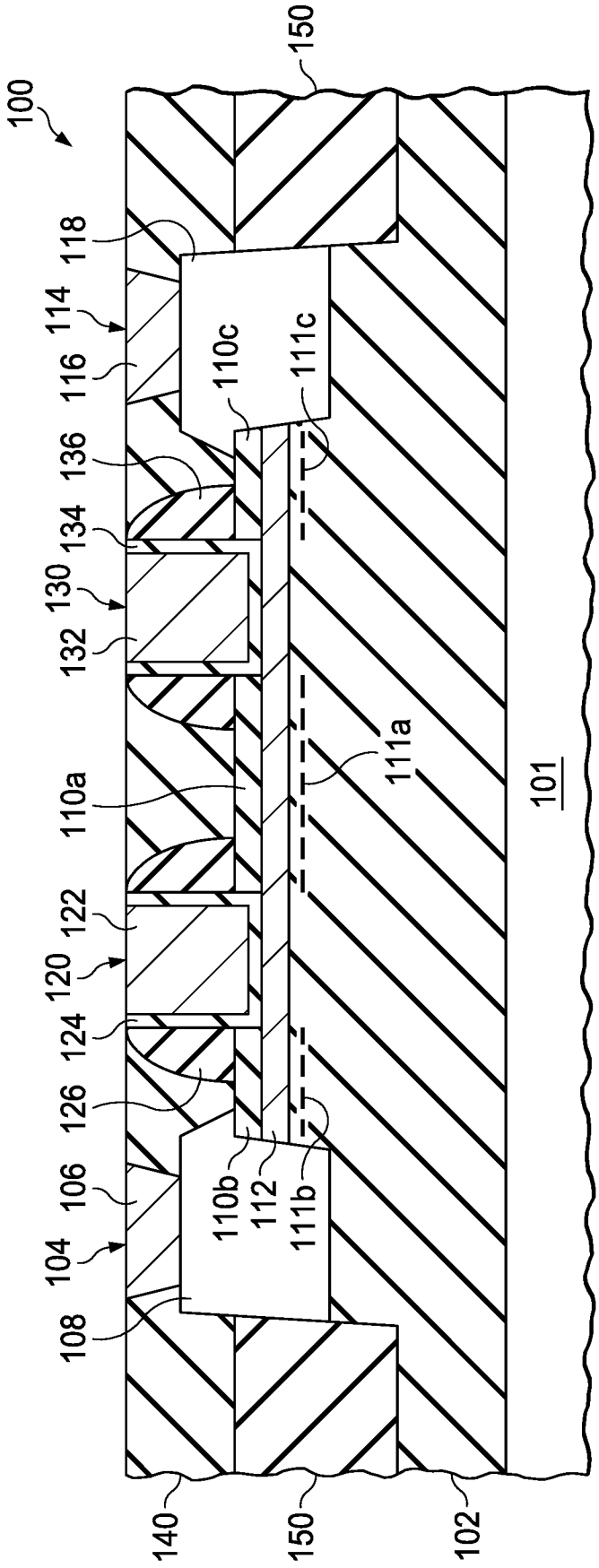

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111c
136
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130
132
110a
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101
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120
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126
106
104
108
110b
112
111b
140
150
102

FIG. 1

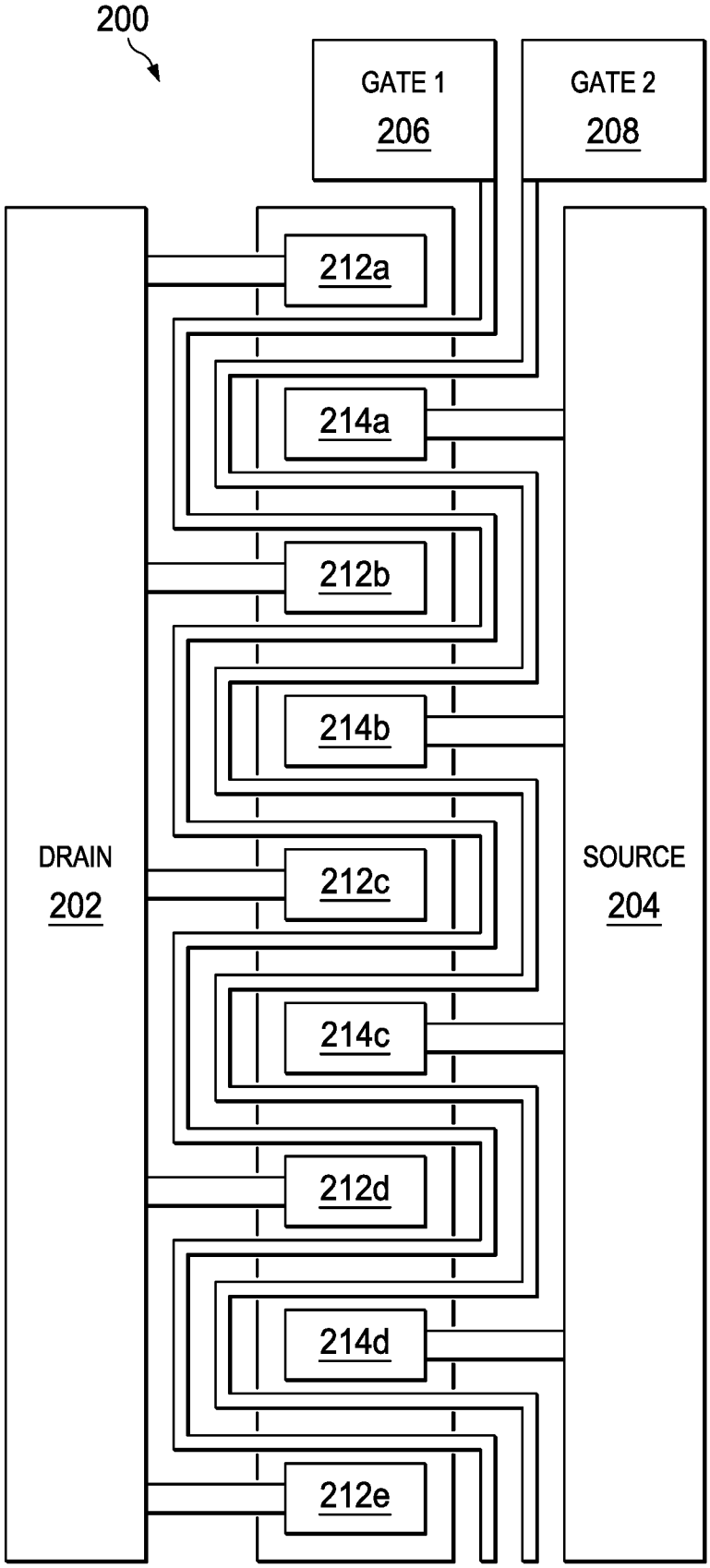

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GATE 1
206
GATE 2
208
212a
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212b
214b
DRAIN
202
212c
SOURCE
204
214c
212d
214d
212e

FIG. 2

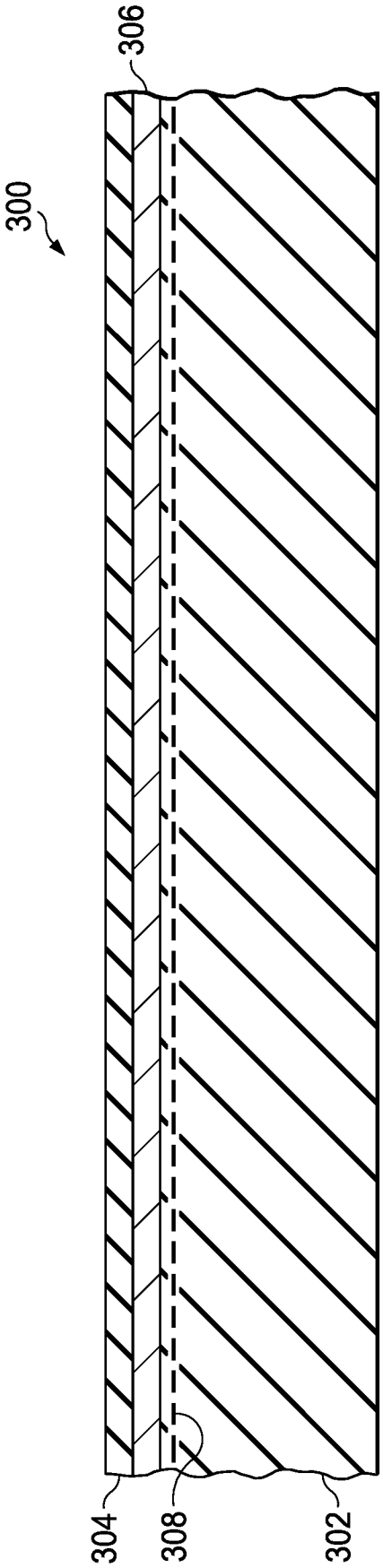


FIG. 3A

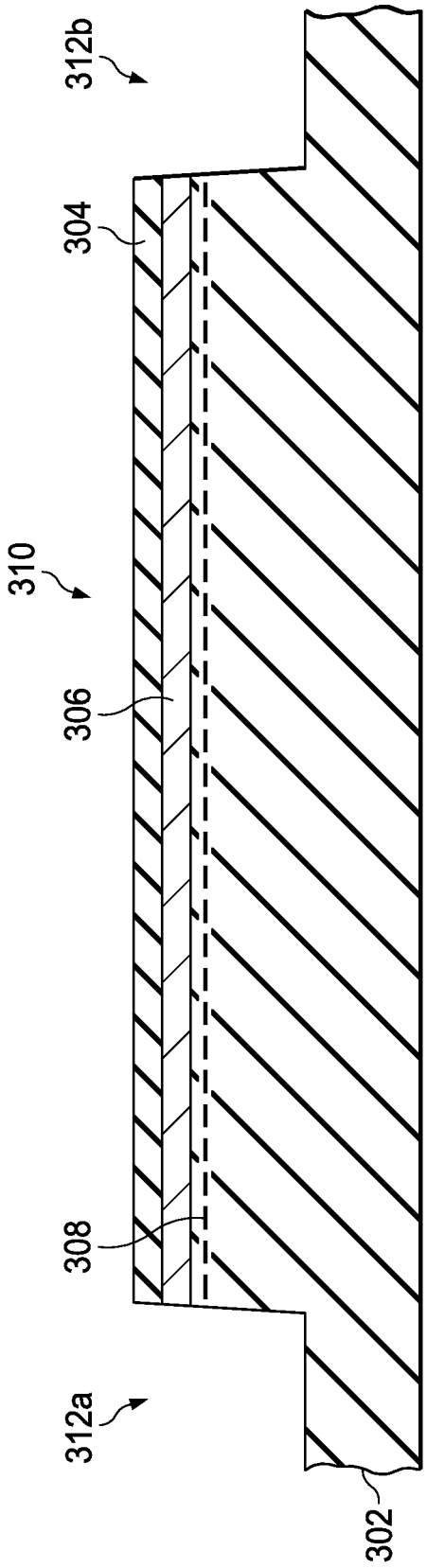


FIG. 3B

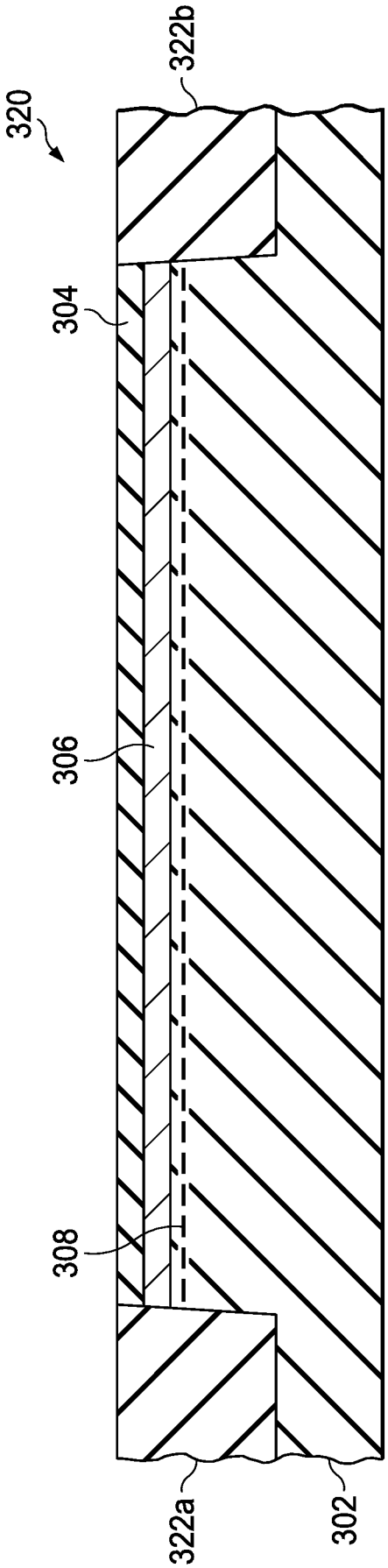

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322b
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306
308
322a
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FIG. 3C

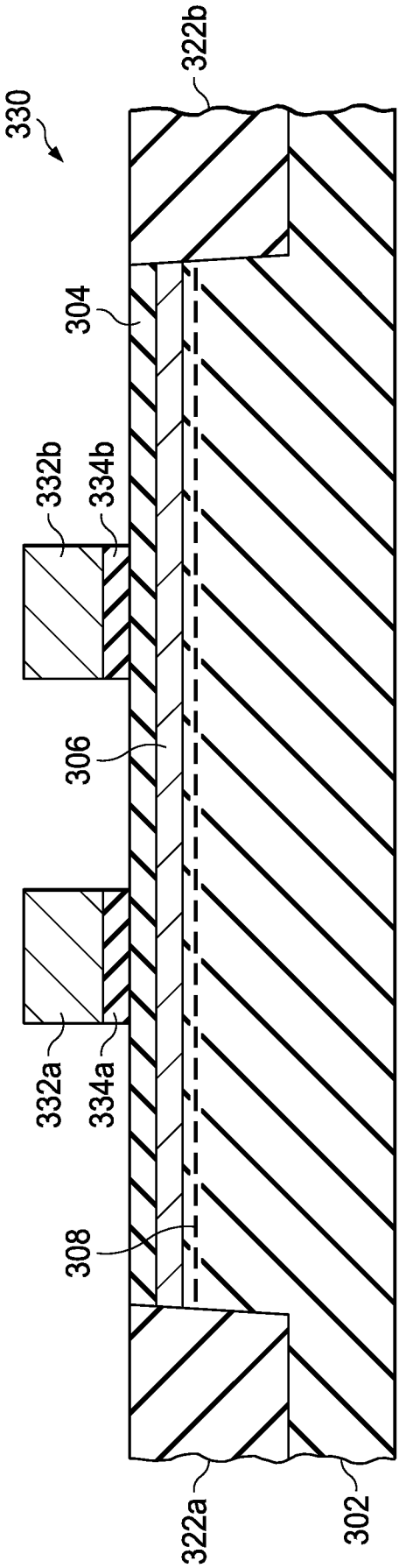

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332b
334b
306
332a
334a
308
322a
302

FIG. 3D

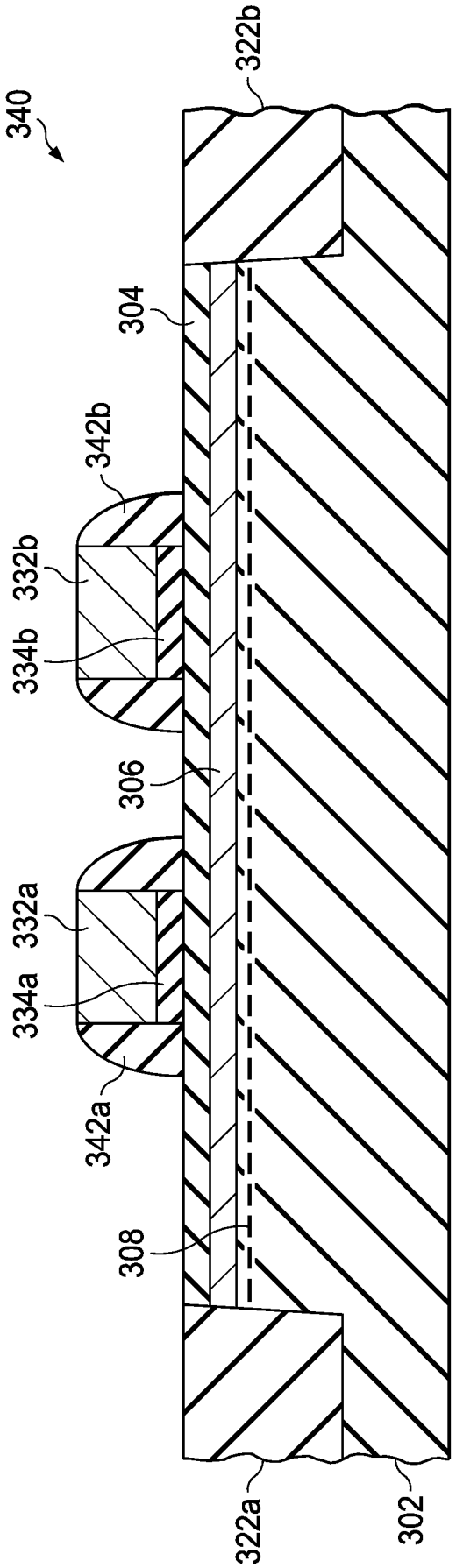

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334b
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332a
334a
342a
308
322a
302

FIG. 3E

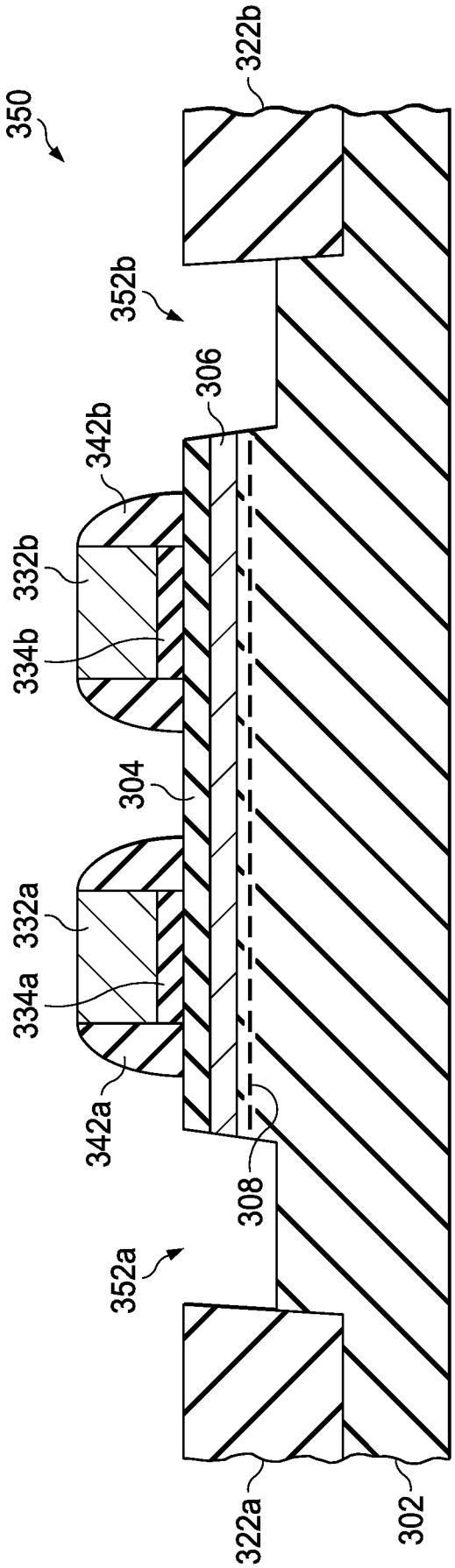

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342b
332b
334b
304
332a
334a
342a
308
352a
322a
302

FIG. 3F

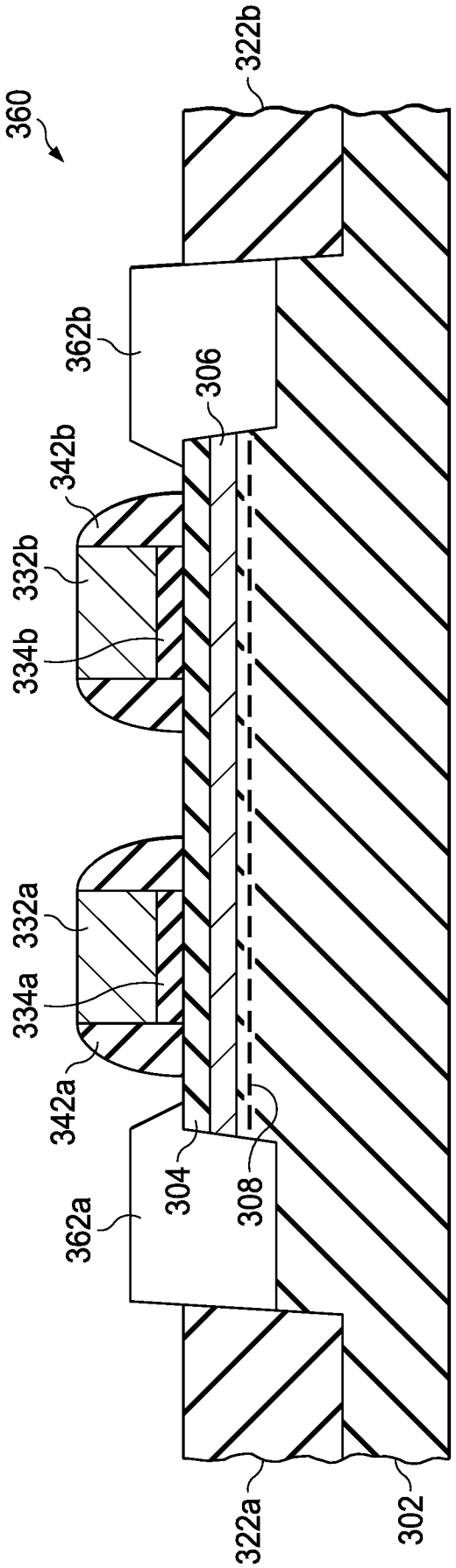

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322b
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334b
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334a
342a
362a
304
308
322a
302

FIG. 3G

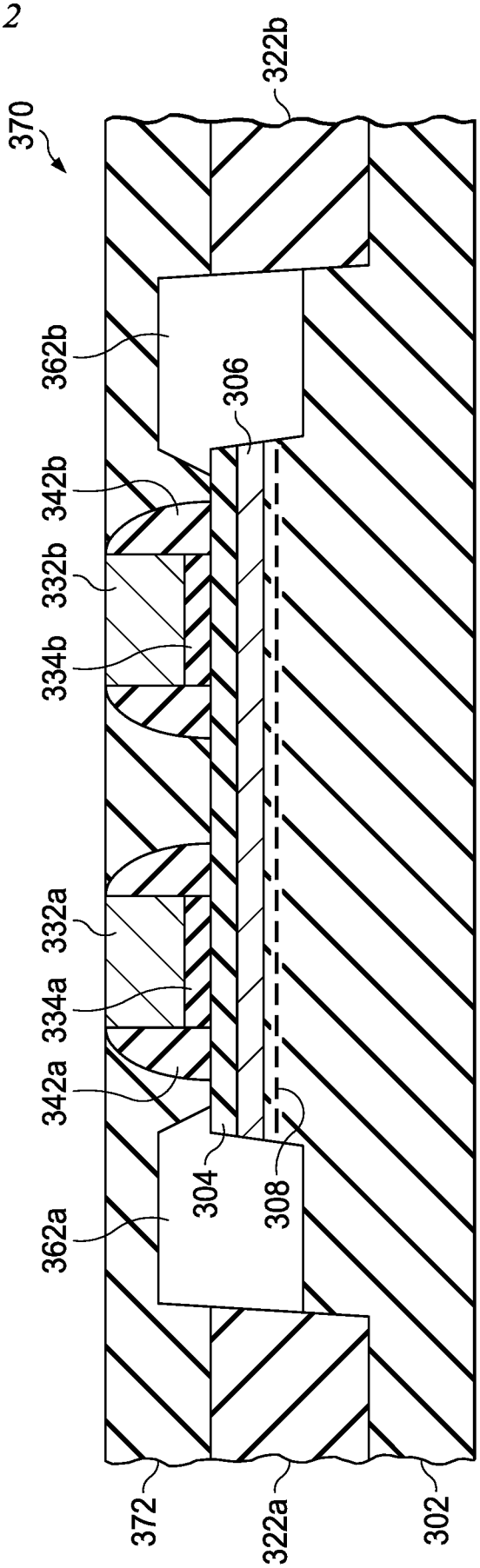

370
322b
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306
342b
332b
334b
332a
334a
342a
362a
304
308
372
322a
302

FIG. 3H

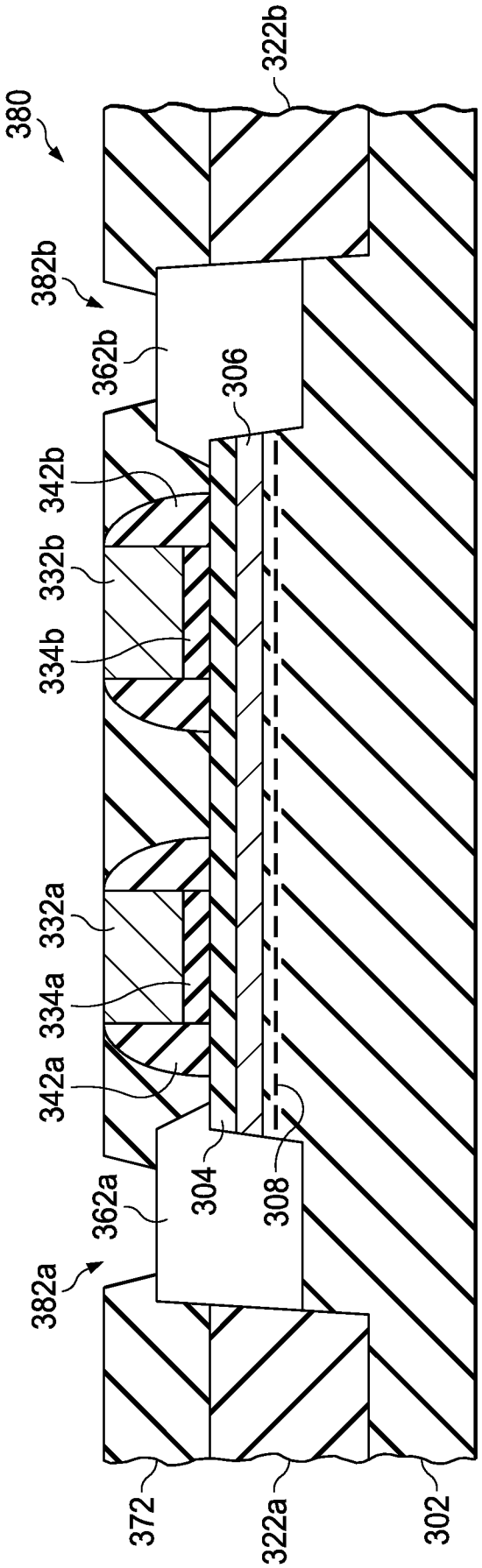

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322b
382b
362b
306
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334a
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362a
304
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382a
372
322a
302

FIG. 3I

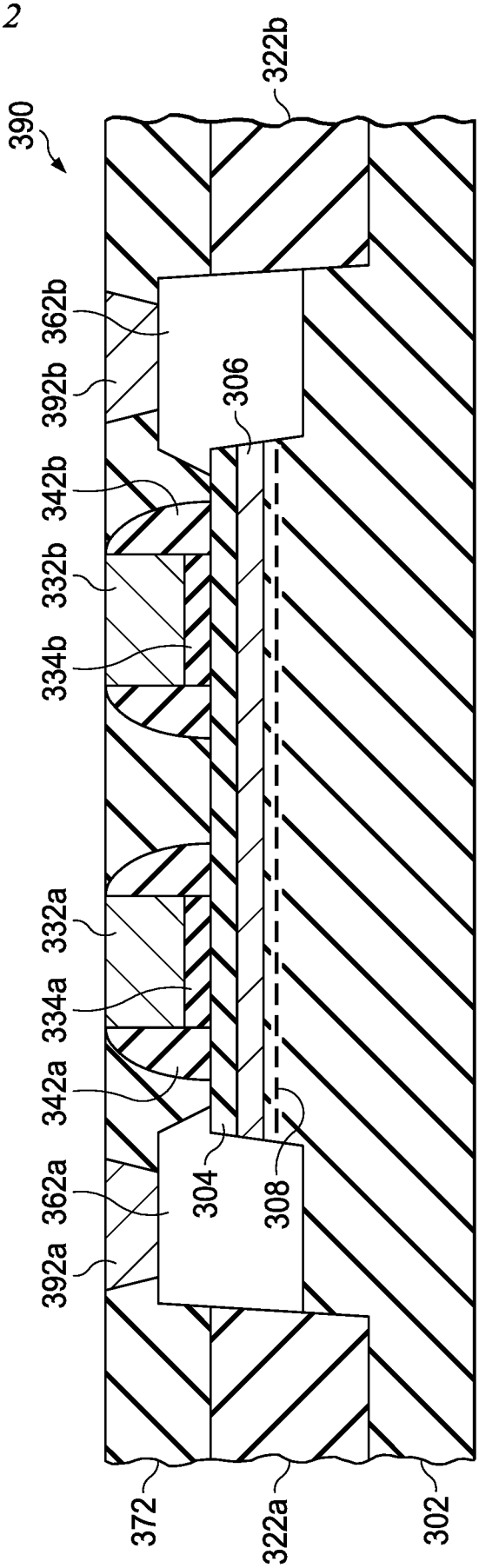

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322a
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FIG. 3J

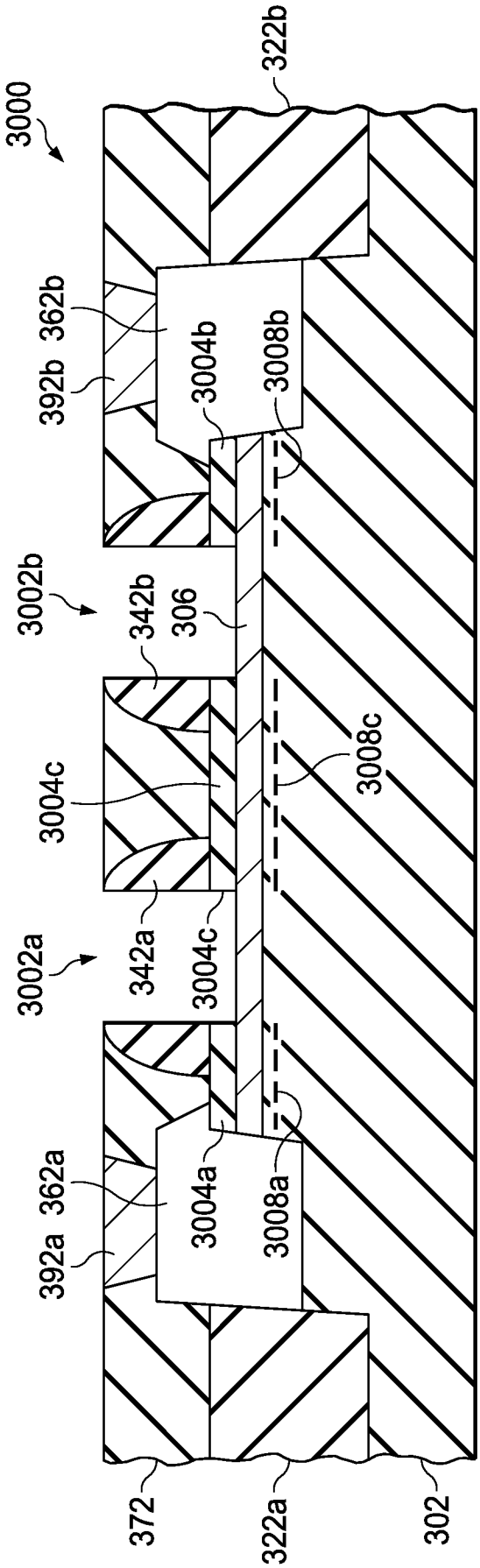

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322b
392b
362b
3004b
3008b
3002b
342b
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3004c
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3002a
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392a
362a
3004a
3008a
372
322a
302

FIG. 3K

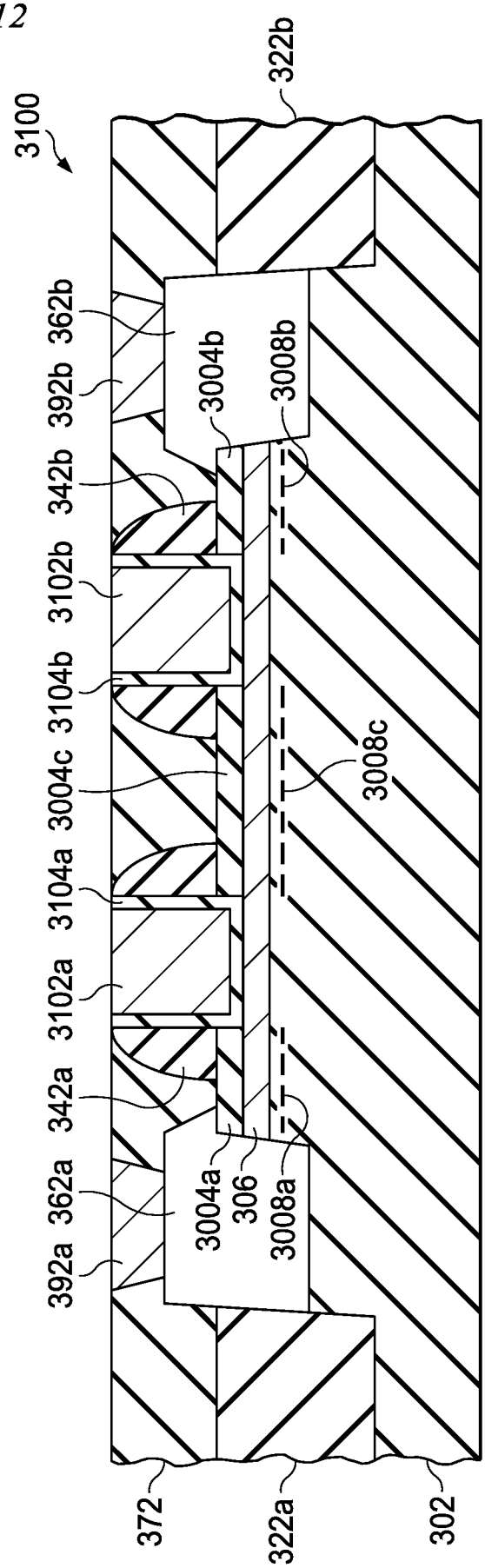

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362b
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3102b
3104b
3004c
3008c
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392a
362a
3004a
306
3008a
372
322a
302

FIG. 3L

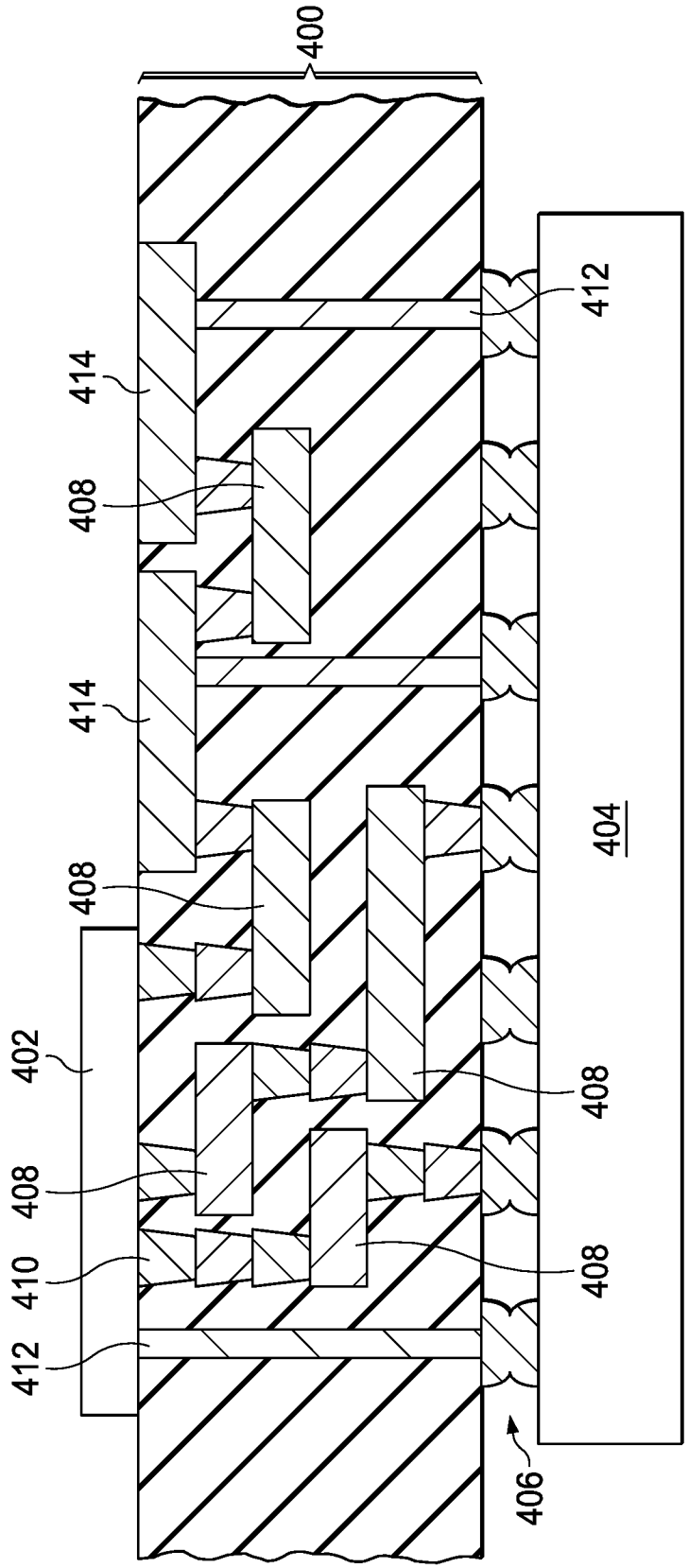


FIG. 4

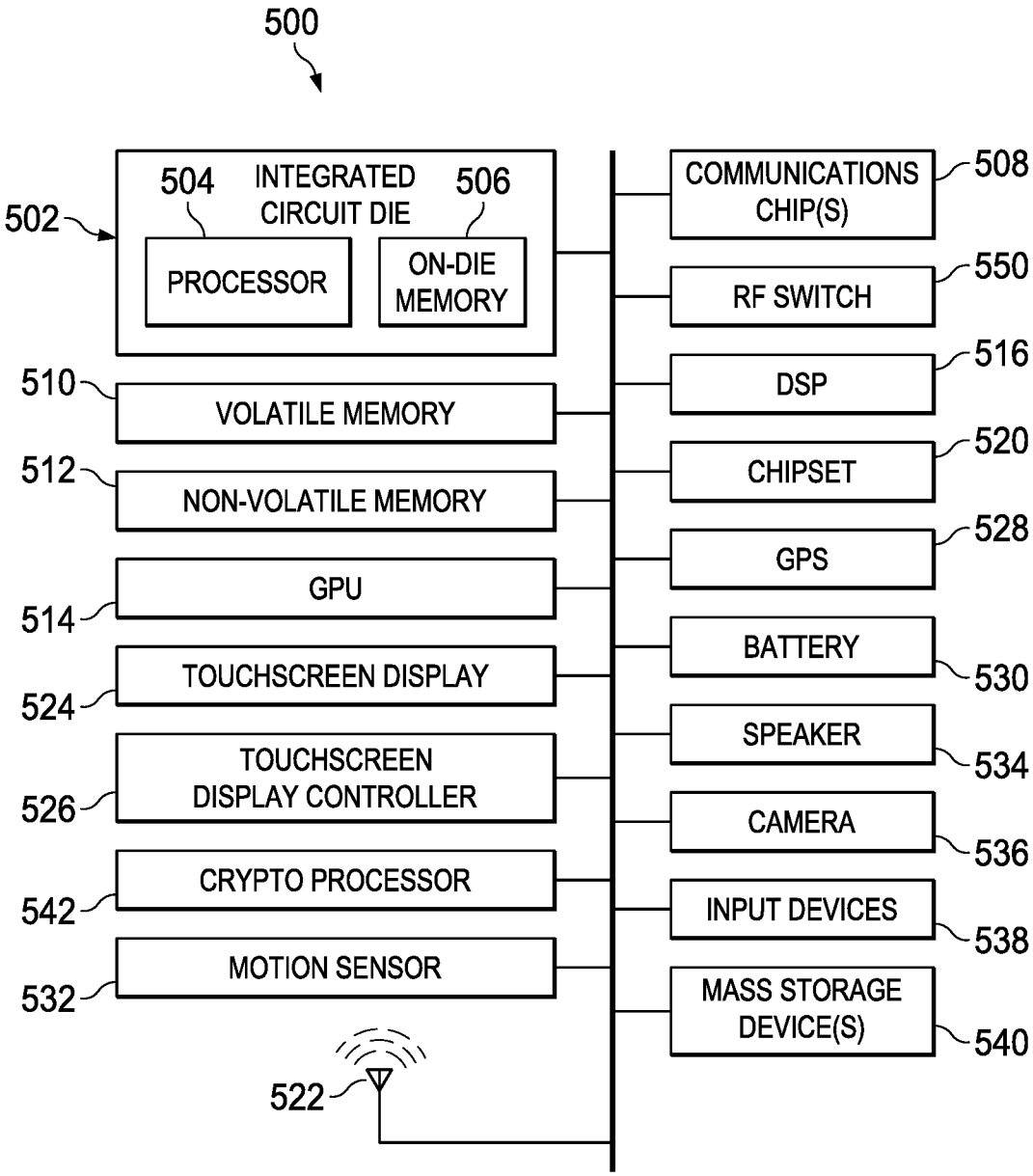

500
502
504
INTEGRATED CIRCUIT DIE
506
PROCESSOR
ON-DIE MEMORY
510
VOLATILE MEMORY
512
NON-VOLATILE MEMORY
514
GPU
524
TOUCHSCREEN DISPLAY
526
TOUCHSCREEN DISPLAY CONTROLLER
542
CRYPTO PROCESSOR
532
MOTION SENSOR
522
COMMUNICATIONS CHIP(S)
508
RF SWITCH
550
DSP
516
CHIPSET
520
GPS
528
BATTERY
530
SPEAKER
534
CAMERA
536
INPUT DEVICES
538
MASS STORAGE DEVICE(S)
540

FIG. 5

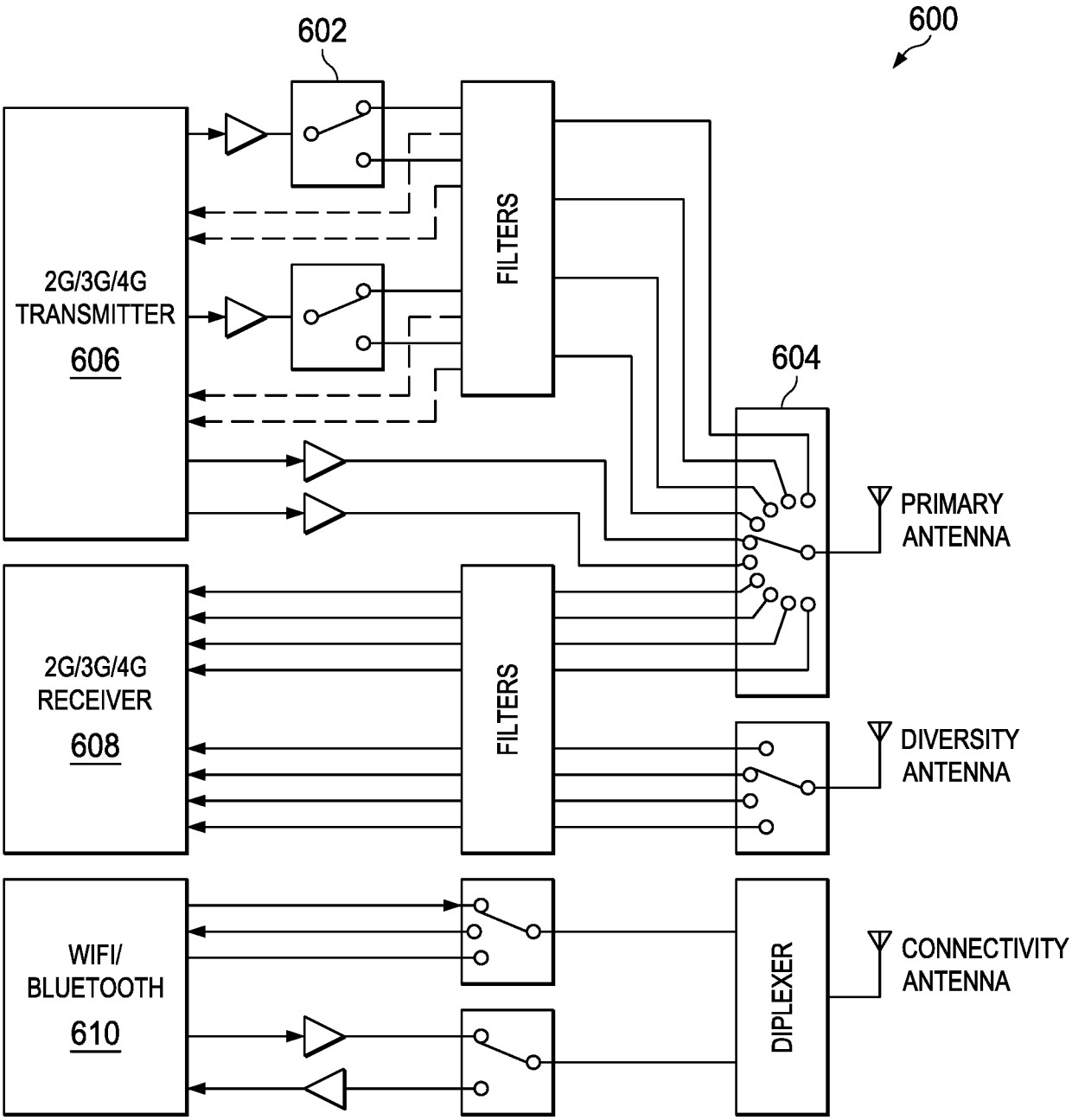

600
602
604
2G/3G/4G
TRANSMITTER
606
FILTERS
PRIMARY
ANTENNA
2G/3G/4G
RECEIVER
608
FILTERS
DIVERSITY
ANTENNA
WIFI/
BLUETOOTH
610
DIPLEXER
CONNECTIVITY
ANTENNA

FIG. 6

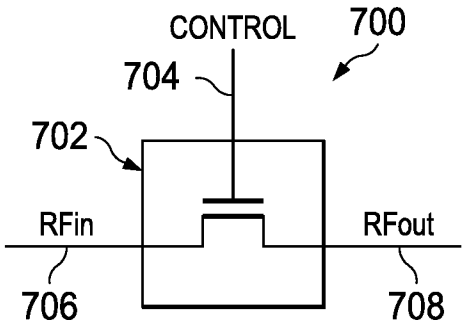


FIG. 7A

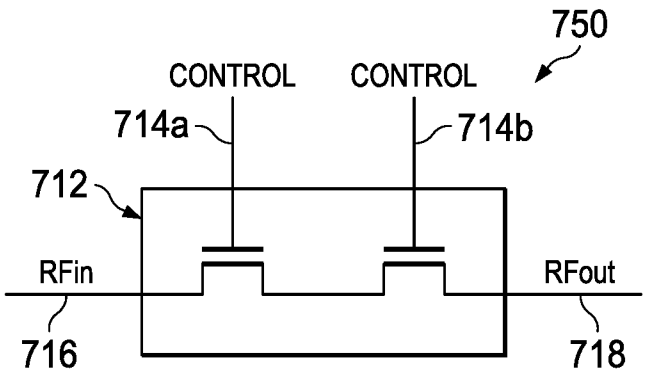


FIG. 7B

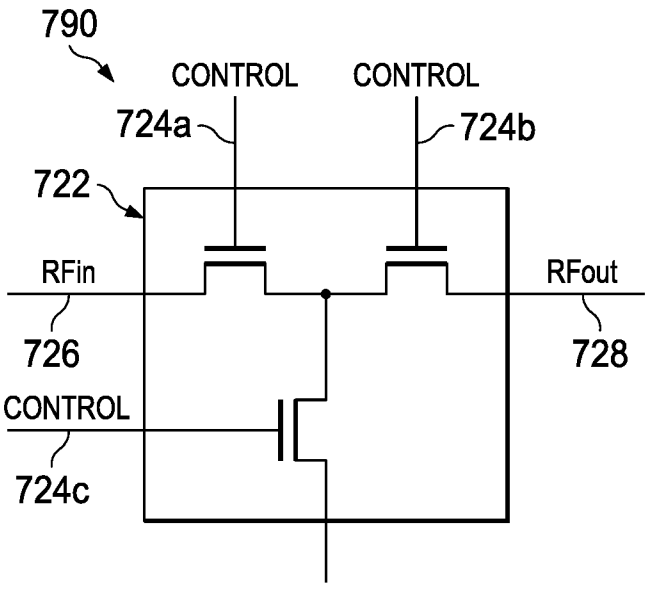


FIG. 7C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/024399

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/778(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/778; H01L 27/088; H01L 21/306; H01L 21/336; H01L 21/332; H01L 29/78; H01L 29/747

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: gate, drain, source, channel, multi, GaN

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0151747 A1 (SAMSUNG ELECTRONICS CO., LTD.) 05 June 2014 See abstract, paragraphs [0044]-[0061] and figures 1-3C.	1-25
A	US 2014-0361343 A1 (CREE, INC.) 11 December 2014 See abstract, paragraphs [0128]-[0129] and figures 19-20.	1-25
A	US 2014-0084331 A1 (ANALOG DEVICES, INC.) 27 March 2014 See abstract, paragraphs [0035]-[0050] and figure 2.	1-25
A	US 2015-0187924 A1 (SANSAPTAK DASGUPTA et al.) 02 July 2015 See abstract, paragraphs [0057]-[0064] and figure 3.	1-25
A	US 2010-0052014 A1 (KEIICHI MATSUSHITA) 04 March 2010 See abstract, paragraphs [0047]-[0090] and figures 3-5.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 December 2016 (20.12.2016)	**20 December 2016 (20.12.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/024399

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