

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
8 January 2009 (08.01.2009)

PCT

(10) International Publication Number
WO 2009/005695 A1

(51) International Patent Classification:
H01L 27/02 (2006.01)

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(21) International Application Number:
PCT/US2008/007975

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(22) International Filing Date: 26 June 2008 (26.06.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/771,565 29 June 2007 (29.06.2007) US

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(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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Published:

— with international search report

(54) Title: ELECTROSTATIC DISCHARGE PROTECTION DEVICES AND METHODS FOR FABRICATING SEMICONDUCTOR DEVICES INCLUDING THE SAME

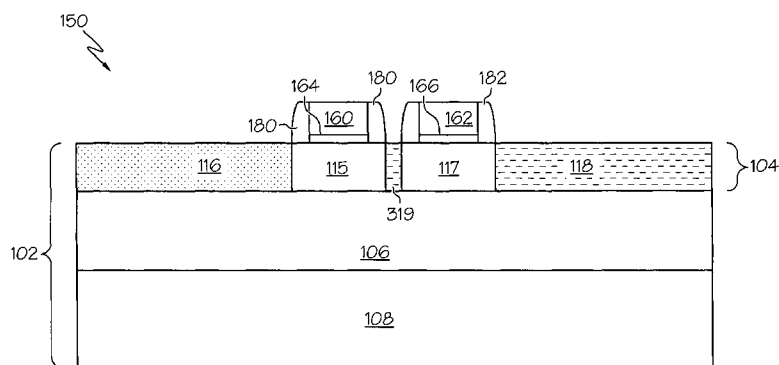


FIG. 8

(57) Abstract: A method for fabricating a semiconductor device (150) is provided. A first gate electrode (160) and a second gate electrode (162) are formed overlying a first portion (114) of a silicon substrate (104). Ions of a first conductivity-type are implanted into a second portion (116) of the silicon substrate (104) to define a first conductivity-type diode region (116) within the silicon substrate (104), and ions of a second conductivity-type are then implanted into a third portion (118) of the silicon substrate (104) to define a second conductivity-type diode region (118) within the silicon substrate (104). During one of the steps of implanting ions of the first conductivity-type and implanting ions of the second conductivity-type, ions are also implanted into at least part (119) of the first portion (114) to define a separation region (119) within the first portion (114) of the silicon substrate (104). The separation region (119) splits the first portion (114) into a first well device region (115) and a second well device region (117), and is formed in series between the first well device region (115) and the second well device region (117).

ELECTROSTATIC DISCHARGE PROTECTION DEVICES AND METHODS FOR FABRICATING SEMICONDUCTOR DEVICES INCLUDING THE SAME

FIELD

- 5 [0001] The present invention generally relates to protection of circuits from electrostatic discharge events, electrostatic discharge protection devices and methods for fabricating semiconductor devices including the same.

BACKGROUND

- 10 [0002] As semiconductor technology advances beyond 130 nm and 90 nm technology towards 65 nm, 45 nm, 32 nm, and even beyond, the electrostatic discharge (ESD) protection for input/output (I/O) pads and their local clamps and supply clamps becomes more challenging. This is especially true for silicon-on-insulator (SOI) technology, which is expected to be preferable over bulk technology.

- 15 [0003] An ESD event refers to a phenomenon of electrical discharge of a current for a short duration during which a large amount of current is provided to a semiconductor structure. During an ESD event, an ESD protection device protects the semiconductor structure. An ideal ESD protection device operates like an open circuit during normal circuit operation, but operates like a short circuit which shunts current caused by the ESD
20 event away from the protected semiconductor structure. While this ideal behavior is not possible in practical implementations, there are ESD protection devices which closely approximate this behavior.

- [0004] Present-day ESD protection devices present a number of drawbacks. For example, some ESD protection circuits are unacceptable because they suffer from high
25 leakage current and high capacitive loading.

- [0005] Accordingly, it is desirable to provide an ESD protection device that exhibits low leakage and low capacitive loading. It also is desirable to provide an ESD protection device that enables a reduction in size of the device. In addition, it is desirable to provide a method for protecting a semiconductor structure from an ESD event using an improved
30 ESD protection device. It is also desirable to provide a method for fabricating an ESD protection device which reduces or eliminates strict fabrication constraints associated with conventional Field Effect Diode (FED) fabrication methods. Furthermore, other desirable features and characteristics of the present invention will become apparent from the

subsequent detailed description of the invention and the appended claims, taken in conjunction with the accompanying drawings and this background of the invention.

SUMMARY

5 [0006] In accordance with an exemplary embodiment of the present invention, a device is provided. The device includes a silicon substrate, a first gate electrode and a second gate electrode. A first conductivity-type diode region is disposed within the silicon substrate. A first well device region is disposed within the silicon substrate in series with the first conductivity-type diode region. A separation region is disposed within the silicon substrate
10 in series with the first well device region. A second well device region is disposed within the silicon substrate in series with the separation region. A second conductivity-type diode region is disposed within the silicon substrate. The second conductivity-type diode region is disposed within the silicon substrate in series with the second well device region. The first gate electrode is disposed overlying the first well device region of the silicon substrate,
15 and the second gate electrode is disposed overlying the second well device region of the silicon substrate.

[0007] In accordance with another exemplary embodiment of the present invention, a method for fabricating a semiconductor device is provided. According to this method, a first gate electrode and a second gate electrode are formed overlying a first portion of a
20 silicon substrate, and ions of a first conductivity-type are implanted into a second portion of the silicon substrate to define a first conductivity-type diode region within the silicon substrate. Ions of a second conductivity-type are implanted into a third portion of the silicon substrate to define a second conductivity-type diode region within the silicon substrate. During one of the steps of implanting ions of the first conductivity-type and
25 implanting ions of the second conductivity-type, ions are also implanted into at least part of the first portion to define a separation region within the first portion. The separation region splits the first portion into a first well device region and a second well device region. The separation region is formed in series between the first well device region and the second well device region.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and wherein:

[0009] FIGS. 1-9 illustrate, in cross section, an ESD protection device and method steps for its fabrication in accordance with various exemplary embodiments of the invention;

[0010] FIG. 10 is a schematic circuit diagram of an input/output (I/O) circuit which implements the ESD protection device of FIG. 9;

5 [0011] FIGS. 1-3 and 11-16 illustrate, in cross section, an ESD protection device and method steps for its fabrication in accordance with other exemplary embodiments of the invention; and

[0012] FIG. 17 is a schematic circuit diagram of an input/output (I/O) circuit which implements the ESD protection device of FIG. 16.

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DETAILED DESCRIPTION

[0013] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any
15 embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments. All of the implementations described below are exemplary implementations provided to enable persons skilled in the art to make or use the invention and are not intended to limit the scope of the invention which is defined by the claims. Furthermore, there is no intention to be bound by any expressed or implied theory
20 presented in the preceding technical field, background, brief summary or the following detailed description.

[0014] FIGS. 1-9 illustrate, in cross section, an ESD protection device 150 and method steps for its fabrication in accordance with various exemplary embodiments of the invention.

25 [0015] As illustrated in FIG. 1, the manufacture in accordance with an embodiment of the invention begins with providing a semiconductor structure 102 in and on which Field Effect Diodes (FEDs) will be fabricated. The semiconductor structure 102 can be either a bulk semiconductor material or a semiconductor-on-insulator (SOI) structure 102 as illustrated in the embodiment of FIG. 1. The SOI structure 102 illustrated in FIG. 1 comprises at least
30 one thin layer of semiconductor material 104 disposed on or overlying a buried oxide insulating layer 106 which, in turn, is supported by a carrier wafer or substrate 108 so that the buried oxide insulating layer 106 is disposed between the carrier wafer 108 and the semiconductor layer 104. The semiconductor layer 104 can be a thin silicon layer, a germanium layer, a gallium arsenide layer, or other semiconductor materials. In one

embodiment, the semiconductor material layer 104 comprises a thin monocrystalline layer of silicon on the buried oxide insulating layer 106. The thin silicon layer may be a relatively pure silicon material, or a layer of silicon material doped with impurity dopant elements such as boron, phosphorus, and arsenic. In one embodiment, the buried oxide
5 insulating layer 106 can be, for example, a silicon dioxide layer, which preferably has a thickness of about 50-200 nm. The thin silicon layer preferably has a resistivity of at least about 1-35 Ohms per square.

[0016] In one embodiment, region 114 of the semiconductor layer 104 can optionally be lightly-doped with P-type conductivity determining impurities such as boron. In an
10 exemplary embodiment of the invention, the P-well device regions 115, 117 are doped with a suitable dopant to a concentration of about 1×10^{16} to about $5 \times 10^{18} \text{ cm}^{-3}$. As described below, region 114 is eventually used to form P-well device regions 115, 117 and the doping of the P-well device regions 115, 117 determines the impedance and conductivity of a non-parasitic leakage current across the semiconductor material layer 104 of the ESD protection
15 device 150.

[0017] As illustrated in FIG. 2, a layer of gate insulating material 164, 166 is formed overlying semiconductor layer 104, and gate electrodes 160, 162 are formed overlying the gate insulating material 164, 166. The layer of gate insulating material 164, 166 can be a layer of thermally grown silicon dioxide or, alternatively, a deposited insulator such as
20 silicon oxide, silicon nitride, or a high dielectric constant (κ) insulator material having a high dielectric constant (κ) relative to silicon dioxide. Examples of "high- κ dielectric" materials include hafnium and zirconium silicates, and their oxides, including, but not limited to, hafnium oxide (HfO_2), hafnium silicate (HfSiO), or the like. Deposited insulators can be deposited, for example, by chemical vapor deposition (CVD), low
25 pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD). The gate insulator layer 164, 166 preferably has a thickness of about 1-10 nm, although the actual thickness can be determined based on the circuit being implemented. The gate electrodes 160, 162 can be formed by depositing, patterning, and etching a layer of metal or polycrystalline silicon, preferably a layer of
30 undoped polycrystalline silicon. The polycrystalline silicon can be deposited, for example, by the reduction of silane (SiH_4) in a CVD reaction such as a low pressure chemical vapor deposition (LPCVD).

[0018] After the gate electrodes 160, 162 have been formed, sidewall spacers 180, 182 are formed on the sidewalls of the gate electrodes 160, 162 as illustrated in FIG. 3. The

sidewall spacers 180, 182 are formed by depositing a layer of insulating material such as silicon oxide and/or silicon nitride and subsequently anisotropically etching the insulating layer, for example by reactive ion etching (RIE). Silicon oxide and silicon nitride can be etched, for example, in a CHF_3 , CF_4 , or SF_6 chemistry. Portions or regions of the semiconductor layer 104 are covered by the gate structures 160, 164, 180 and 162, 166, 182 so that those regions will remain as the P-type semiconductor material 114.

[0019] As illustrated in FIG. 4, layer of masking material, which can be, for example, a layer of photoresist, is applied and patterned to expose portions of semiconductor layer 104 and to cover other portions of the semiconductor layer 104. In this embodiment, the layer of patterned mask material 130 overlies the second gate structure 162, 166, 182 and a first portion of the substrate that is eventually used to create N^+ -type cathode region 118.

[0020] Using this layer of patterned mask material 130 as an ion implantation mask, the exposed portions of the semiconductor layer 104 are impurity doped, as illustrated by arrows, with P-type conductivity determining impurities to create a highly-doped P^+ -type anode region 116 and a highly-doped P^+ -type separation region 119, as illustrated in FIG. 5. The highly-doped P^+ -type separation region 119 is formed in a portion of the P-well device region 114 that is between the gate electrodes 160, 162. In one embodiment, the P^+ -type separation region 119 extends through P-well device region 114 to the buried oxide layer 106. By creating the highly-doped P^+ -type separation region 119, the P-well device region 114 is split into a first P-well device region 115 and a second P-well device region 117. Impurity doping can take place by the implantation and (optionally) subsequent thermal annealing of dopant ions such as boron. The P^+ -type regions are regions having a doping concentration greater than the doping concentration of the P-well device regions 115, 117. In an exemplary embodiment of the invention, the P^+ -type anode region and P^+ -type separation region 119 are doped with a suitable dopant to a concentration of about 10^{20} to about 10^{21} cm^{-3} .

[0021] The highly-doped P^+ -type separation region 119 acts as a barrier which separates P-well device region 115 from P-well device region 117 and helps prevent the bias voltage (that is applied to gate electrodes 160, 162) from influencing the regions under the other gate electrodes 160, 162. This configuration allows the bias voltage applied to the gate electrodes 160, 162 to control the relative conductivity of the device regions 115, 117 without significantly influencing the conductivity of the highly-doped P^+ -type separation region 119. The higher the P^+ doping of separation region 119, the more resistant the highly-doped P^+ -type separation region 119 is to inversion when a bias voltage is applied to

gate electrodes 160, 162 (i.e., it becomes more difficult to invert highly-doped P⁺-type separation region 119).

[0022] Although not shown, after implanting P-type conductivity determining impurities, the patterned mask material 130 is removed. As illustrated in FIG. 6, another layer of masking material 140, which can be, for example, a layer of photoresist, is applied and patterned to expose portions of semiconductor layer 104 and to cover other portions of the semiconductor layer 104. In this embodiment, the layer of patterned mask material 140 overlies the first gate structure 160, 164, 180, at least a portion of the second gate structure 162, 166, 182, anode region 116 and separation region 119 so that the doping of anode region 116 and separation region 119 are not altered by subsequent implantation steps.

[0023] As illustrated in FIG. 7, using this layer of patterned mask material 140 as an ion implantation mask, the semiconductor layer 104 can be impurity doped, as indicated by arrows, with N-type conductivity determining impurities to create N⁺-type cathode region 118. Impurity doping can take place by the implantation and (optionally) subsequent thermal annealing of dopant ions such as phosphorus and/or arsenic. The N⁺-type region has a doping concentration greater than the doping concentration of the P-well device regions 115, 117. In an exemplary embodiment of the invention, the N⁺-type cathode region may be doped with a suitable dopant to a concentration of about 10²⁰ to about 10²¹ cm⁻³.

[0024] As illustrated in FIG. 8, after implanting N-type conductivity determining impurities, the patterned mask material 140 is removed. The resulting structure 150 in FIG. 8 can then (optionally) be annealed, for instance using a Rapid Thermal Annealing (RTA) process to cause outward lateral diffusion of dopants in the highly-doped P⁺-type anode region 116, the highly-doped P⁺-type separation region 119 and the N⁺-type cathode region 118, as illustrated in FIG. 9.

[0025] At the stage of processing shown in FIG. 9, the semiconductor substrate 104 includes a P⁺-type anode region 116, an N⁺-type cathode region 118, and a pair of field effect diodes (FEDs) which are separated from each other via highly-doped P⁺-type separation region 119. The P⁺-type anode region 116 of semiconductor layer 104 is separated from the N⁺-type cathode region 118 by the first P-well device region 115, the highly-doped P⁺-type separation region 119 and the second P-well device region 117. Each FED includes a gate electrode structure formed over a P-well device region 115, 117, where each of the gate electrode structures comprises a gate insulator layer 164, 166, a gate

electrode 160, 162 overlying the gate insulator layer 164, 166, and spacers 180, 182 adjacent a first sidewall and a second sidewall of the gate electrode 160, 162.

[0026] Although not illustrated, the device 150 can be completed, for example, by forming metal silicide contacts on the P⁺-type anode region 116, gate electrodes 160, 162, and N⁺-type cathode region 118, depositing interlayer dielectric layers, planarizing the interlayer dielectric layers, and etching contact vias or openings through the dielectric layer to the metal silicide contacts on the P⁺-type anode region 116, gate electrodes 160, 162, and N⁺-type cathode region 118. Electrical contact to the P⁺-type anode region 116, gate electrodes 160, 162, and N⁺-type cathode region 118 can then be made by contact plugs formed in contact openings and by interconnect metal deposition and patterning. In FIG. 9, the contact plugs are represented by reference numerals 192, 194-196. The contact plugs 195, 196 can eventually be connected to a bias circuit 170 which controls operation of the device 150 during different modes of operation (i.e., ESD operation versus non-ESD operation).

[0027] The bias circuit 170 operates to control a bias voltage applied to gate electrodes 160, 162. The bias voltage which the bias circuit 170 applies to the gate electrodes 160, 162 depends on the operating state of the circuit the ESD protection device 150 is protecting from an ESD event. Depending upon how the gate electrodes 160, 162 are biased, the semiconductor layer 104 of the ESD protection device 150 exhibits different arrangements of P-N junctions. The ESD protection device 150 is a normally-on enhanced field effect diode (FED) meaning that during normal operation, the ESD protection device 150 operates in a biased state, and that during an ESD event biasing stops to protect a core circuit (not shown) against an ESD event. Table 1 summarizes operation of the ESD protection device 150 during its different operating modes.

	SUBSTRATE REGIONS					RESULT
	116	115	119	117	118	
OPERATING MODE						
ESD	P+	P	P+	P	N+	DIODE
NORMAL	P+	N (INVERTS)	P+	N (INVERTS)	N+	SERIES DIODES

Table 1

[0028] During normal circuit operation or “non-ESD operation” when there is not an ESD event, the bias circuit 170 applies a high positive bias voltage to both gate electrodes 160, 162 which initially causes depletion in the P-well device regions 115, 117 underneath gate electrodes 160, 162 and as the high bias voltage increases eventually inverts the surface conductivity of the P-well device regions 115, 117 so that the P-well device regions 115, 117 behave like N-type material. This results in a series P+ N P+ N N+ profile across and within semiconductor layer 104. One PN junction is formed between P⁺-type anode region 116 and device region 115, another PN junction is formed between device region 115 and highly-doped P⁺-type separation region 119, while another PN junction is formed between device region 117 and highly-doped P⁺-type separation region 119. ESD protection device 150 is configured such that P⁺-type anode region 116 is positively biased with respect to N⁺-type cathode region 118. As such, the semiconductor layer 104 is essentially configured like a forward-biased diode 124 in series with another forward-biased diode 126, and the semiconductor layer 104 operates like a PNP (SCR) structure where its turn-on voltage is dependent on an energy barrier height of the central reverse bias PN junction formed between device region 115 and highly-doped P⁺-type separation region 119. Because the ESD protection device 150 operates like two diodes in series (or alternatively as a PNP SCR structure) during normal operation, the ESD protection device 150 has a relatively high impedance and is resistant to conduction of a non-parasitic leakage current across the semiconductor material layer 104 of the ESD protection device 150. The ESD protection device 150 begins to conduct only when the voltage applied across the diodes 124, 126 is greater than 1.4 volts (0.7 volts attributable to each of the diodes 124, 126).

[0029] Because the ESD protection device 150 has two PN junctions in series, the total capacitance of the ESD protection device 150 is reduced since the total capacitance of two diodes in series is lower than each of them individually. Because RF I/O circuits are sensitive to ESD loading capacitance, the low capacitance of the series diodes under normal operation allows the ESD protection device 150 to be used in high speed or RF I/O pads as well as for low leakage/low power pads. During normal operation, the relatively high impedance of ESD protection device 150 causes the ESD protection device 150 to effectively behave like an open circuit with respect to the core circuit being protected.

[0030] By contrast, when an ESD event occurs, the bias circuit 170 stops applying the high bias voltage so that the gate electrodes 160, 162 are left in their unbiased or “electrically floating.” This causes the surface of well device regions 115, 117 under gate

electrodes 160, 162 to return or revert to P-type which results in a series P+ P P+ P N+ profile across semiconductor layer 104 (i.e., semiconductor layer 104 has one PN junction between P⁺-type anode region 116 and the N⁺-type cathode region 118 at the junction between P-well device region 117 and N⁺-type cathode region 118). Therefore, during an ESD event, the ESD protection device 150 behaves as a single forward-biased diode and the on-voltage of ESD protection device 150 is reduced to about 0.7 volts. Accordingly, during an ESD event, the ESD protection device 150 has relatively low impedance and allows conduction of a current across the semiconductor material layer 104 of the ESD protection device 150. As will be described below, the ESD protection device 150 effectively operates like a short circuit which shorts the current resulting from the ESD event to ground thereby protecting the core circuit.

[0031] The device 150 illustrated in FIG. 9 can be fabricated in an alternative complementary conductivity-type embodiment, where at least a portion of the starting substrate is lightly-doped with N-type conductivity determining impurities such as phosphorous or arsenic and is therefore an N-type substrate 104. In this embodiment, the well device regions 115, 117 are N-well device regions 115, 117, and the separation region 119 is doped with N-type impurities to form a highly-doped N⁺-type separation region 119. ESD protection device 150 is configured such that P⁺-type anode region 116 is positively biased with respect to N⁺-type cathode region 118. Table 2 illustrates operation of the normally-on FED 150 when the substrate 104 is an N-type substrate 104, regions 115, 117 are N-type material and the separation region 119 is N⁺-type material.

	SUBSTRATE REGIONS					RESULT
	116	115	119	117	118	
OPERATING MODE						
ESD	P+	N	N+	N	N+	DIODE
NORMAL	P+	P (INVERTS)	N+	P (INVERTS)	N+	SERIES DIODES

Table 2

[0032] During normal circuit operation, the bias circuit 170 applies a high negative bias voltage to both gate electrodes 160, 162 which initially causes depletion in the N-well

device regions 115, 117 underneath gate electrodes 160, 162 and as the high bias voltage increases eventually inverts the surface conductivity of the N-well device regions 115, 117 so that the N-well device regions 115, 117 behave like P-type material. This results in a series P+ P N+ P N+ profile across semiconductor layer 104. One PN junction is formed between device region 115 and highly-doped N⁺-type separation region 119, another PN junction is formed between highly-doped N⁺-type separation region 119 and device region 117 while another PN junction is formed between device region 117 and cathode region 118. As such, during normal operation, the semiconductor layer 104 is configured like two forward-biased diodes in series, and the ESD protection device 150 has a relatively high impedance which makes the ESD protection device 150 more resistant to conduction of a current across the semiconductor material layer 104 of the ESD protection device 150. As such, the ESD protection device 150 effectively behaves like an open circuit with respect to the core circuit being protected.

[0033] By contrast, when an ESD event occurs, the bias circuit 170 stops applying the high bias voltage so that the gate electrodes 160, 162 are left in their unbiased or “electrically floating.” This causes the well device regions 115, 117 under gate electrodes 160, 162 to return or revert to N-type which results in a series P+ N N+ N N+ profile across and within semiconductor layer 104 (i.e., semiconductor layer 104 has one PN junction between P+-type anode region 116 and N-well device region 115). Therefore, during an ESD event, the ESD protection device 150 behaves as a single forward-biased diode and the on-voltage of ESD protection device 150 is reduced to about 0.7 volts. Accordingly, during an ESD event, the ESD protection device 150 has relatively low impedance and allows conduction of a current across the semiconductor material layer 104 of the ESD protection device 150. As such, the ESD protection device 150 effectively operates as a short circuit, which shorts the current resulting from the ESD event to ground thereby protecting the core circuit.

[0034] One implementation of the ESD protection device 150 used as a local clamping circuit will be discussed below with respect to FIG. 10.

[0035] FIG. 10 is a schematic circuit diagram of an input/output (I/O) circuit 200 which implements the ESD protection device 250. The ESD protection device 250 is identical to the ESD protection device 150 in FIG. 9. The I/O circuit 200 includes an I/O pad 252, an ESD diode 240, an ESD protection device 250, a bias circuit 270, a positive (VDD) supply rail 280, a negative (VSS) supply rail 290, a circuit 275 to be protected from an ESD event, and a supply clamp 281.

[0036] In this embodiment, ESD protection device 250 is implemented as a local clamping circuit to provide local clamping of an ESD current to reduce the voltage on the I/O pad 252. Local clamping means the ESD current is shunted to ground at the I/O pad 252. In other words, rail-based clamping is not needed and there is no need to pass the ESD current through the supply rails 280, 290 to the supply clamp 281 and back to ground. In this case, the ESD protection device 250 can provide adequate protection without increasing the I/O pad 252 clamping voltage, and can therefore be implemented in a smaller area in comparison to standard ESD protection devices. To explain further, during an ESD event, the ESD voltage at I/O pad 252 to ground is determined by the resistance of the elements in the path of the ESD current. With local clamping, the ESD voltage is determined only by the resistance of the ESD protection device 250 which is proportional to its width. By contrast, in a rail based clamping scheme, the ESD voltage is determined by the sum of the voltage drop across the diode to the supply rail 280 and the resistance of the supply rail 280 to the supply clamp 281 and the resistance of the supply clamp 281 to ground. To achieve the same voltage at I/O pad 252 for both cases, the ESD protection device in a rail based clamping scheme has to be wider than with local clamping to compensate for the extra resistance in the path.

[0037] As described above, the ESD protection device 250 exhibits different behaviors based on whether the circuit is operating normally or if there is an ESD event. When the circuit is operating normally, the bias circuit 270, which is a PMOSFET in this embodiment, applies a high bias voltage to the gates 260, 262 of the ESD protection device 250. Thus, during normal operation, the ESD protection device 250 operates like two diodes in series which have relatively high impedance and which are resistant to conduction of a current across the semiconductor material layer 104 of the ESD protection device 150. Therefore the ESD protection device 250 does not begin conducting during normal circuit operation (i.e., appears as an open circuit). During a positive ESD event a large voltage is applied to I/O pad 252 which causes a large current to flow. The large voltage causes the ESD protection device 250 to operate in its unbiased state in which the gates 260, 262 of the ESD protection device 250 are not biased (i.e., the gates 260, 262 of the ESD protection device 250 are essentially floating or grounded). Accordingly, as described above, the ESD protection device 250 operates like a single forward-biased diode with relatively low impedance which makes it relatively easy to cause conduction of a current across the semiconductor material layer 104 of the ESD protection device 250. The current caused by

the ESD event flows through from the anode 292 of the diode to the cathode 294 of the diode to ground.

[0038] The ESD diode 240 can be used to provide ESD protection during an opposite polarity situation (i.e., a negative ESD event) where voltage on I/O pad 252 is pulled below ground which forward biases ESD diode 240. In this situation, the ESD protection device 250 is reverse biased and does nothing.

[0039] Although not shown, the ESD protection device 250 can also be implemented within the supply clamp 281 for high voltage supplies. Because the ESD protection device 250 operates as a single forward-biased diode during ESD operation, using the ESD protection device 250 in the supply clamp 281 allows at least one diode to be eliminated in supply clamp 281, thus reducing the area of the supply clamp by 25% to 50%. Moreover, because supply clamp 281 can be implemented using fewer diodes, the voltage drop across the supply clamp 281 during ESD operation is lower or reduced in comparison to conventional supply clamps.

[0040] FIGS. 1-3 and 11-16 illustrate, in cross section, an ESD protection device 350 and method steps for its fabrication in accordance with other exemplary embodiments of the invention.

[0041] FIGS. 1-3 are described above, and for sake of brevity, will not be reiterated here. As illustrated in FIG. 11, a layer of masking material 330, which can be, for example, a layer of photoresist, is applied and patterned to expose portions of semiconductor layer 104 and to cover other portions of the semiconductor layer 104. In this embodiment, the layer of patterned mask material 330 overlies at least a portion of the first gate structure 160, 164, 180, the second gate structure 162, 166, 182 and a first portion of the substrate that is eventually used to create N⁺-type cathode region 318.

[0042] Using this layer of patterned mask material 330 as an ion implantation mask, the exposed portions of the semiconductor layer 104 can be impurity doped with P-type conductivity determining impurities to create a highly-doped P⁺-type anode region 316, as illustrated in FIG. 12. In an exemplary embodiment of the invention, impurity doping can take place as described above with respect to FIG. 5.

[0043] After implanting P-type conductivity determining impurities, the patterned mask material 330 is removed, and another layer of masking material 340, which can be, for example, a layer of photoresist, is applied and patterned to expose portions of semiconductor layer 104 and to cover other portions of the semiconductor layer 104, as illustrated in FIG. 13. In this embodiment, the layer of patterned mask material 340

overlies at least a portion of the first gate structure 160, 164, 180 and the highly-doped P⁺-type anode region 316 so that the doping of highly-doped P⁺-type anode region 316 is not altered during subsequent implantation steps.

[0044] Using this layer of patterned mask material 340 as an ion implantation mask, the exposed portions of the semiconductor layer 104 are impurity doped with N-type conductivity determining impurities to create a highly-doped N⁺-type cathode region 318 and a highly-doped N⁺-type separation region 319, as illustrated in FIG. 14. In an exemplary embodiment of the invention, impurity doping can take place by the implantation as described above with respect to FIG. 7. The highly-doped N⁺-type separation region 319 is formed in a portion of the P-well device region 114 that is between the gate electrodes 160, 162. By creating the highly-doped N⁺-type separation region 319, the P-well device region 114 is split into a first P-well device region 115 and a second P-well device region 117. In one embodiment, the N⁺-type separation region 319 extends through P-well device region 114 to the buried oxide layer 106. The highly-doped N⁺-type separation region 319 acts as a barrier which separates P-well device region 115 from P-well device region 117 and helps prevent the bias voltage (that is applied to gate electrodes 160, 162) from influencing the regions under the other gate electrodes 160, 162. This configuration allows the bias voltage applied to the gate electrodes 160, 162 to control the relative conductivity of the device regions 115, 117 without significantly influencing the conductivity of the highly-doped N⁺-type separation region 319. The higher the N⁺ doping of separation region 319, the more resistant the separation region 319 is to inversion when a bias voltage is applied to the gate electrodes 160, 162 (i.e., makes it more difficult to invert the highly-doped N⁺-type separation region 319).

[0045] As illustrated in FIG. 15, after implanting N-type conductivity determining impurities, the patterned mask material 340 is removed. The resulting structure 350 in FIG. 14 can then (optionally) be annealed, for instance using a Rapid Thermal Annealing (RTA) process to cause outward lateral diffusion of dopants in the highly-doped P⁺-type anode region 116, the highly-doped N⁺-type separation region 119 and the N⁺-type cathode region 118, as illustrated in FIG. 16.

[0046] At the stage of processing shown in FIG. 16, the cross-sectional structure of the ESD protection device 350 is identical to that of the ESD protection device 150 of FIG. 9 except that the doping of the material used for the separation region 319 is different, and therefore the device 350 operates as a “normally-off” enhanced field effect diode (FED). The semiconductor substrate 104 includes a P⁺-type anode region 316 and an N⁺-type

cathode region 318. The P⁺-type anode region 316 of semiconductor layer 104 is separated from the N⁺-type cathode region 318 by the first P-well device region 115, the highly-doped N⁺-type separation region 319 and the second P-well device region 117. A gate electrode structure is formed over each P-well device region 115, 117, where each of the gate electrode structures comprises a gate insulator layer 164, 166, a gate electrode 160, 162 overlying the gate insulator layer 164, 166, and spacers 180, 182 adjacent a first sidewall and a second sidewall of the gate electrode 160, 162.

[0047] Although not illustrated, the device 350 can be completed as described above with respect to FIG. 9. In FIG. 16, the contact plugs are represented by reference numerals 192, 194-196. The contact plugs 195, 196 can eventually be connected to a bias circuit 170 which controls operation of the device 350 during different modes of operation (i.e., ESD operation versus non-ESD operation).

[0048] The bias circuit 170 operates to control a bias voltage applied to gate electrodes 160, 162. The bias voltage which the bias circuit 170 applies to the gate electrodes 160, 162 depends on the operating state of the circuit that the ESD protection device 350 is protecting from an ESD event. Depending upon how the gate electrodes 160, 162 are biased, the semiconductor layer 104 of the ESD protection device 350 exhibits different arrangements of P-N junctions. The ESD protection device 350 is a normally-off enhanced field effect diode (FED) meaning that during normal operation, the ESD protection device 350 operates in its regular, unbiased state, and that during an ESD event biasing of the ESD protection device 350 protects a core circuit (not shown) against an ESD event. Table 3 summarizes operation of the ESD protection device 350 (or the “normally-off enhanced FED”) during its different operating modes when the separation region 319 is N⁺-type material.

	SUBSTRATE REGIONS					RESULT
	316	115	319	117	318	
OPERATING MODE						
ESD	P+	N (INVERTS)	N+	N (INVERTS)	N+	DIODE
NORMAL	P+	P	N+	P	N+	SERIES DIODES

Table 3

[0049] During normal circuit operation or “non-ESD operation” the bias circuit 170 does not apply a bias voltage so that the gate electrodes 160, 162 are unbiased or “electrically floating.” This causes the well device regions 115, 117 under gate electrodes 160, 162 to remain P-type which results in a series P+ P N+ P N+ profile across semiconductor layer 104. One PN junction is formed between device region 115 and highly-doped N⁺-type separation region 319, another PN junction is formed between device region 117 and highly-doped P⁺-type separation region 319, while another PN junction is formed between device region 117 and highly-doped N⁺-type cathode region 318. ESD protection device 150 is configured such that P⁺-type anode region 316 is positively biased with respect to N⁺-type cathode region 318. As such, during normal operation, the semiconductor layer 104 is configured like a forward-biased diode 124 in series with another forward-biased diode 126, and the semiconductor layer 104 operates like a PNPN (SCR) structure where its turn-on voltage is dependent on an energy barrier height of the central reverse bias PN junction formed between device region 115 and highly-doped P⁺-type separation region 119. Because the ESD protection device 150 operates like two diodes in series (or alternatively as a PNPN SCR structure) during normal operation, the ESD protection device 350 has a relatively high impedance and is resistant to conduction of a current across the semiconductor material layer 104 of the ESD protection device 350. As described above, the ESD protection device 350 can be used in high speed or RF I/O pads as well as for low leakage/low power pads. The ESD protection device 350 effectively behaves like an open circuit with respect to the core circuit being protected.

[0050] By contrast, when an ESD event occurs, the bias circuit 170 applies a high positive bias voltage to both gate electrodes 160, 162 which initially causes depletion in the P-well device regions 115, 117 underneath gate electrodes 160, 162 and as the high bias voltage increases eventually inverts the surface conductivity of the P-well device regions 115, 117 so that the P-well device regions 115, 117 behave like N-type material. This results in a series P+ N N+ N N+ profile across semiconductor layer 104 such that semiconductor layer 104 has one PN junction between N-well device region 115 and P⁺-type anode region 316. Therefore, during an ESD event, the ESD protection device 350 behaves as a single forward-biased diode and the on-voltage of ESD protection device 350 is reduced to about 0.7 volts. Accordingly, during an ESD event, it is relatively easy to cause conduction of a current across the semiconductor material layer 104 of the ESD protection device 350 and therefore the ESD protection device 350 effectively operates as a

short circuit which shorts the current resulting from the ESD event to ground thereby protecting the core circuit.

[0051] The device 350 illustrated in FIG. 15 can be fabricated in an alternative complementary conductivity-type embodiment, where the starting substrate is lightly-doped with N-type conductivity determining impurities and is therefore an N-type substrate 104. In this embodiment, the well device regions 115, 117 are N-well device regions 115, 117, and the separation region 319 is doped with P-type impurities to form a highly-doped P⁺-type separation region 319. ESD protection device 350 is configured such that P⁺-type anode region 316 is positively biased with respect to N⁺-type cathode region 318. Table 4 illustrates operation of the normally-off FED 350 when the substrate 104 is an N-type substrate 104, regions 115, 117 are N-type material and the separation region 319 is a highly doped P⁺-type material.

	SUBSTRATE REGIONS					
	316	115	319	117	318	RESULT
OPERATING MODE						
ESD	P+	P (INVERTS)	P+	P (INVERTS)	N+	DIODE
NORMAL	P+	N	P+	N	N+	SERIES DIODES

Table 4

[0052] During normal circuit operation or “non-ESD operation” when there is not an ESD event, the bias circuit 170 applies no bias voltage so that the gate electrodes 160, 162 are unbiased or “electrically floating.” This causes the well device regions 115, 117 under gate electrodes 160, 162 to remain N-type which results in a series P⁺ N P⁺ N N⁺ profile across semiconductor layer 104. One PN junction is formed between P⁺-type anode region 316 and N-type device region 115, another PN junction is formed between N-type device region 115 and highly-doped P⁺-type separation region 319, while another PN junction is formed between device region 117 and highly-doped P⁺-type separation region 319. As such, the semiconductor layer 104 is configured like a forward-biased diode 324 in series with another forward-biased diode 326. Because the impedance of ESD protection device

350 is relatively high, the ESD protection device 350 is resistant to conduction of a current across the semiconductor material layer 104 of the ESD protection device 350. Therefore, the ESD protection device 350 effectively behaves like an open circuit with respect to the core circuit being protected.

5 [0053] By contrast, when an ESD event occurs, the bias circuit 170 applies a high negative bias voltage to both gate electrodes 160, 162 which initially causes depletion in the N-well device regions 115, 117 underneath gate electrodes 160, 162 and as the high bias voltage increases eventually inverts the surface conductivity of the N-well device regions 115, 117 so that the N-well device regions 115, 117 behave like P-type material. This results in a series P+ P P+ P N+ profile across semiconductor layer 104 such that semiconductor layer 104 has one PN junction between P-well device region 117 and N⁺-type cathode region 318. Therefore, during an ESD event, the ESD protection device 350 behaves as a single forward-biased diode and the on-voltage of ESD protection device 350 is reduced to about 0.7 volts. Accordingly, during an ESD event, the ESD protection device 350 has a relatively low impedance and allows conduction of a current across the semiconductor material layer 104 of the ESD protection device 350 which means that the ESD protection device 350 effectively operates as a short circuit which shorts the current resulting from the ESD event to ground thereby protecting the core circuit.

15 [0054] One implementation of the ESD protection device 350 used as a local clamping circuit will be discussed below with respect to FIG. 17.

[0055] FIG. 17 is a schematic circuit diagram of an input/output (I/O) circuit 400 which implements the ESD protection device 450. The ESD protection device 450 is identical to the ESD protection device 350 in FIG. 16. As above, the I/O circuit 400 includes an I/O pad 452, an ESD diode 440, an ESD protection device 450, a bias circuit 470, a positive (VDD) supply rail 480, a negative (VSS) supply rail 490, a circuit 475 to be protected from an ESD event, and a supply clamp 481. In this embodiment, ESD protection device 450 is implemented as a local clamping circuit with respect to the I/O pad 452, as described above.

25 [0056] When the circuit is operating normally, the bias circuit 470, which is an inverter in this embodiment, does not apply any voltage to the gates 460, 462 of the ESD protection device 450 thereby causing the ESD protection device 450 to operate in its unbiased state. Thus, during normal operation, the ESD protection device 450 operates like two diodes in series. The series diodes have a relatively high impedance and are resistant to conduction of a current across the ESD protection device 450. During a positive ESD event a large

voltage is applied to I/O pad 452 which causes a large current to flow towards the ESD protection device 450. During a positive ESD event, the large ESD voltage applied to I/O pad 452 causes the bias circuit 470 to apply a high bias voltage to the gates 460, 462 of the ESD protection device 450 (i.e., the large voltage applied to I/O pad 452 controls the voltage to the gates 460, 462). Accordingly, the ESD protection device 450 operates like a single forward-biased diode and the current flows through from the anode 492 to the cathode 494 to ground. Because the ESD protection device 450 operates like a single forward-biased diode the ESD protection device 450 conducts a current more easily during an ESD event (i.e., effectively appears as a short circuit). The ESD diode 440 is used during an opposite polarity situation (i.e., a negative ESD event) where voltage on I/O pad 452 is pulled below ground which forward biases ESD diode 440. In this situation, the ESD protection device 450 is reverse biased and does nothing. As above the ESD protection device 450 can also be implemented within the supply clamp 481 for high voltage supplies.

[0057] Thus, a number of ESD protection devices (or “enhanced FEDs”) have been disclosed which can be implemented with different I/O circuits. The different embodiments of ESD protection devices disclosed herein can be implemented within different process integration techniques, and are also compatible with the standard SOI fabrication techniques so that no special masks or implants required. The ESD protection devices can provide ESD protection for I/O circuits fabricated on SOI technology which require high speed and low leakage. During normal operation, the ESD protection devices disclosed herein exhibit low loading capacitance and low leakage due to the presence of a PNPN structure. In other words, because two diodes are used in series, the series combination has a capacitance lower than that of a single protection diode. The lower capacitance allows the ESD protection device to be used in conjunction with high speed (i.e., radio-frequency) I/O pads and/or low leakage/ low power I/O pads. The ESD protection devices also provide higher current carrier capability normally associated with conventional diode-based ESD protection devices. The ESD protection devices also make it easier to control the impedance across the ESD protection device without compromising its ESD operation.

[0058] Conventional ESD protection devices used with SOI technology include SOI diodes, NMOS transistors and Silicon Controlled rectifiers (SCR) structures. SOI diodes and SCR structures can handle large current but their turn-on voltage can not be controlled. NMOS transistors can provide controllable turn-on voltage via gate biasing, but can not handle large currents. The ESD protection devices described above can handle large

currents while having a gate controllable impedance which make the ESD protection devices suitable for local clamping over wide range of normal operating voltages.

[0059] While at least one exemplary embodiment has been presented in the foregoing detailed description of the invention, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiment or exemplary embodiments are only examples, and are not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing an exemplary embodiment of the invention, it being understood that various changes may be made in the function and arrangement of elements described in an exemplary embodiment without departing from the scope of the invention as set forth in the appended claims and their legal equivalents.

CLAIMS

What is claimed is:

1. A method for fabricating a semiconductor device (150), the method
5 comprising the steps of:

providing a silicon substrate (104);

forming a first gate electrode (160) and a second gate electrode (162) overlying a
first portion (114) of the silicon substrate (104);

10 implanting ions of a first conductivity-type into a second portion (116) of the
silicon substrate (104) to define a first conductivity-type diode region (116) within the
silicon substrate (104);

implanting ions of a second conductivity-type into a third portion (118) of the
silicon substrate (104) to define a second conductivity-type diode region (118) within the
silicon substrate (104); and

15 during one of the steps of implanting ions of the first conductivity-type and
implanting ions of the second conductivity-type, implanting ions into at least part (119) of
the first portion (114) to define a separation region (119) within the first portion (114),
wherein the separation region (119) splits the first portion (114) into a first well device
region (115) and a second well device region (117), wherein the separation region (119) is
20 formed in series between the first well device region (115) and the second well device
region (117).

2. The method of claim 1, wherein the step of implanting ions into at least part
25 (119) of the first portion (114) takes place during the step of implanting ions of the first
conductivity-type into the second portion (116), and wherein the step of implanting ions of
the first conductivity-type into the second portion (116) further comprises:

implanting ions of a first conductivity-type into at least part (119) of the first
portion (114) and a second portion (116) of the silicon substrate (104) to define a first
30 conductivity-type separation region (119) within the first portion and to define a first
conductivity-type diode region (116) within the silicon substrate (104), wherein the first
conductivity-type separation region (119) splits the first portion (114) into a first well
device region (115) and a second well device region (117).

3. The method of claim 2, wherein the first well device region (115) is formed in series with the first conductivity-type diode region (116) and the first conductivity-type separation region (119), and wherein the second well device region (117) is formed in series with the first conductivity-type separation region (119) and the second conductivity-type diode region (118).

4. The method of claim 2, wherein the silicon substrate (104) comprises a P-type silicon material, wherein the first conductivity-type is P^+ , wherein the first well device region (115) is a first P-well device region (115), wherein the second well device region (117) is second P-well device region (117), and wherein the second conductivity-type is N^+ .

5. The method of claim 2, wherein the silicon substrate (104) comprises a N-type silicon material, wherein the first conductivity-type is P^+ , wherein the first well device region (115) is a first N-well device region (115), wherein the second well device region (117) is second N-well device region (117), and wherein the second conductivity-type is N^+ .

6. The method of claim 1, wherein, wherein the step of implanting ions into at least part (119) of the first portion (114) takes place during the step of implanting ions of the second conductivity-type into the third portion (118) and wherein the step of implanting ions of the second conductivity-type into the third portion (118) further comprises:

implanting ions of a second conductivity-type into at least part (319) of the first portion (114) and a third portion (318) of the silicon substrate (104) to define a second conductivity-type separation region (319) within the first portion (114) and to define a second conductivity-type diode region (318) within the silicon substrate (104), wherein the separation region (319) splits the first portion (114) into a first well device region (115) and a second well device region (117).

7. The method of claim 6, wherein the first well device region (115) is formed in series with the first conductivity-type diode region (116) and the second conductivity-type separation region (319), and wherein the second well device region (117) is formed in series with the second conductivity-type separation region (319) and the second conductivity-type diode region (318).

8. The method of claim 6, wherein the silicon substrate (104) comprises a P-type silicon material, wherein the first conductivity-type is P^+ , wherein the first well device region (115) is a first P-well device region (115), wherein the second well device region (117) is second P-well device region (117), wherein the second conductivity-type is N^+ .

5

9. The method of claim 6, wherein the silicon substrate (104) comprises a N-type silicon material, wherein the first conductivity-type is P^+ , wherein the first well device region (115) is a first N-well device region (115), wherein the second well device region (117) is second N-well device region (117), wherein the second conductivity-type is N^+ .

10

10. A device (200/400), comprising:

a silicon substrate (104), comprising:

a first conductivity-type diode region (116) disposed within the silicon substrate (104);

15

a first well device region (115) disposed within the silicon substrate (104) in series with the first conductivity-type diode region (116);

a separation region (119) disposed within the silicon substrate (104) in series with the first well device region (115);

20

a second well device region (117) disposed within the silicon substrate in series with the separation region (119);

a second conductivity-type diode region (118) disposed within the silicon substrate (104), wherein the second conductivity-type diode region (118) is disposed within the silicon substrate (104) in series with the second well device region (117); and

25

a first gate electrode (160) disposed overlying the first well device region (115) of the silicon substrate (104); and

a second gate electrode (162) disposed overlying the second well device region (117) of the silicon substrate (104).

30

11. The device of claim 10, wherein the first conductivity-type is P^+ , wherein the first well device region (115) is a first P-well device region (115), wherein the second well device region (117) is second P-well device region (117), wherein the second conductivity-type is N^+ , and wherein the separation region (119) is a P^+ -type separation region (119).

12. The device of claim 10, wherein the first conductivity-type is P^+ , wherein the first well device region (115) is a first N-well device region (115), wherein the second well device region (117) is second N-well device region (117), wherein the second conductivity-type is N^+ , and wherein the separation region (119) is a N^+ -type separation region (119).

13. The device of claim 10, wherein the first conductivity-type is P^+ , wherein the first well device region (115) is a first P-well device region (115), wherein the second well device region (117) is second P-well device region (117), wherein the second conductivity-type is N^+ , and wherein the separation region (119) is a N^+ -type separation region (119).

14. The device of claim 10, wherein the first conductivity-type is P^+ , wherein the first well device region (115) is a first N-well device region (115), wherein the second well device region (117) is second N-well device region (117), wherein the second conductivity-type is N^+ , and wherein the separation region (119) is a P^+ -type separation region (119).

15. The device of claim 10, further comprising:
a circuit to be protected from an electrostatic discharge event.

16. The device according to claim 15, further comprising:
a circuit (170) coupled to the first gate electrode (160) and the second gate electrode (162), wherein the circuit (170) designed to: apply a first bias voltage to the first gate electrode (160) and the second gate electrode (162) during normal operation; and stop applying the first bias voltage to the first gate electrode (160) and the second gate electrode (162) in response to an electrostatic discharge event.

17. The device according to claim 15, wherein the electrostatic discharge protection circuit further comprises:

a circuit (170) coupled to the first gate electrode (160) and the second gate electrode (162), wherein the circuit (170) designed to: apply a first bias voltage to the first gate electrode (160) and the second gate electrode (162) in response to an electrostatic discharge event.

18. A method of operating a device (200) comprising a circuit (200) to be protected from an electrostatic discharge event, a bias circuit (270), and an electrostatic discharge protection device (250) comprising a silicon substrate (104), comprising: a first conductivity-type diode region (116) disposed within the silicon substrate (104); a first well device region (115) disposed within the silicon substrate (104) in series with the first conductivity-type diode region (116); a separation region (119) disposed within the silicon substrate (104) in series with the first well device region (115); a second well device region (117) disposed within the silicon substrate in series with the separation region (119); a second conductivity-type diode region (118) disposed within the silicon substrate (104) , wherein the second conductivity-type diode region (118) is disposed within the silicon substrate (104) in series with the second well device region (117); and a first gate electrode (260) disposed overlying the first well device region (115) of the silicon substrate (104); and a second gate electrode (262) disposed overlying the second well device region (117) of the silicon substrate (104), the method comprising:

applying, via the bias circuit (270), a first bias voltage to the first gate electrode (160) and the second gate electrode (162) during normal operation to configure the silicon substrate (104) as a pair of forward biased diodes; and

removing the first bias voltage applied to the first gate electrode (260) and the second gate electrode (262) in response to the electrostatic discharge event to configure the silicon substrate (104) as a single forward biased diode.

19. A method of operating a device (400) comprising a circuit (400) to be protected from an electrostatic discharge event, a bias circuit (470), and an electrostatic discharge protection device (450) comprising a silicon substrate (104), comprising: a first conductivity-type diode region (116) disposed within the silicon substrate (104); a first well device region (115) disposed within the silicon substrate (104) in series with the first conductivity-type diode region (116); a separation region (119) disposed within the silicon substrate (104) in series with the first well device region (115); a second well device region (117) disposed within the silicon substrate in series with the separation region (119); a second conductivity-type diode region (118) disposed within the silicon substrate (104) , wherein the second conductivity-type diode region (118) is disposed within the silicon substrate (104) in series with the second well device region (117); and a first gate electrode (460) disposed overlying the first well device region (115) of the silicon substrate (104);

and a second gate electrode (462) disposed overlying the second well device region (117) of the silicon substrate (104), the method comprising:

applying, via the bias circuit (470), a first bias voltage to the first gate electrode (460) and the second gate electrode (462) in response to the electrostatic discharge event to configure the silicon substrate (104) as a forward biased diode.

5

150 ↗

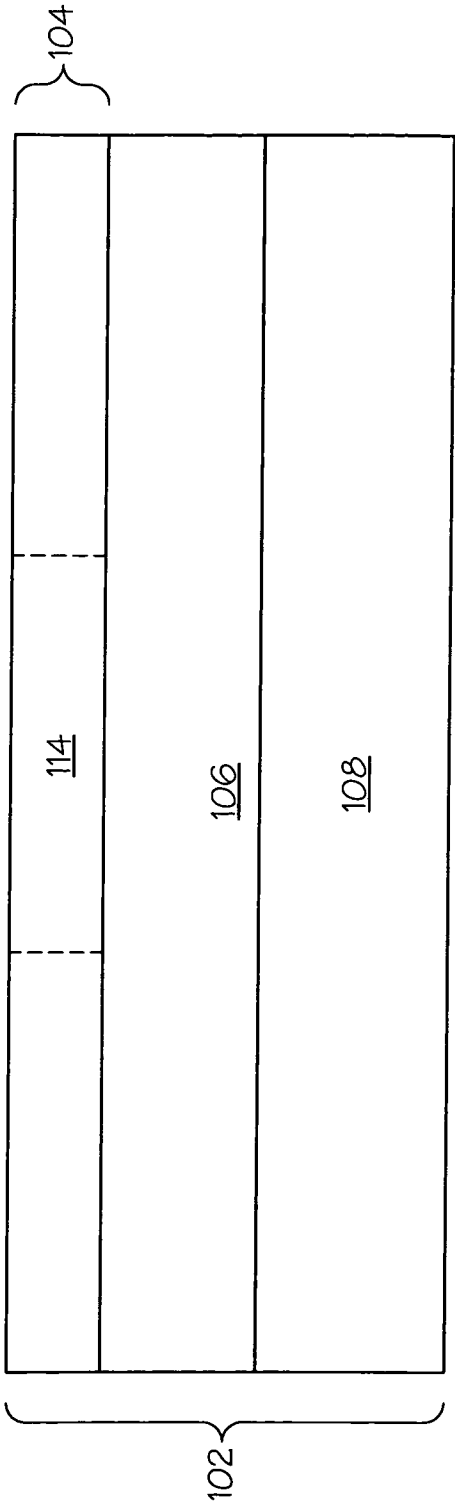


FIG. 1

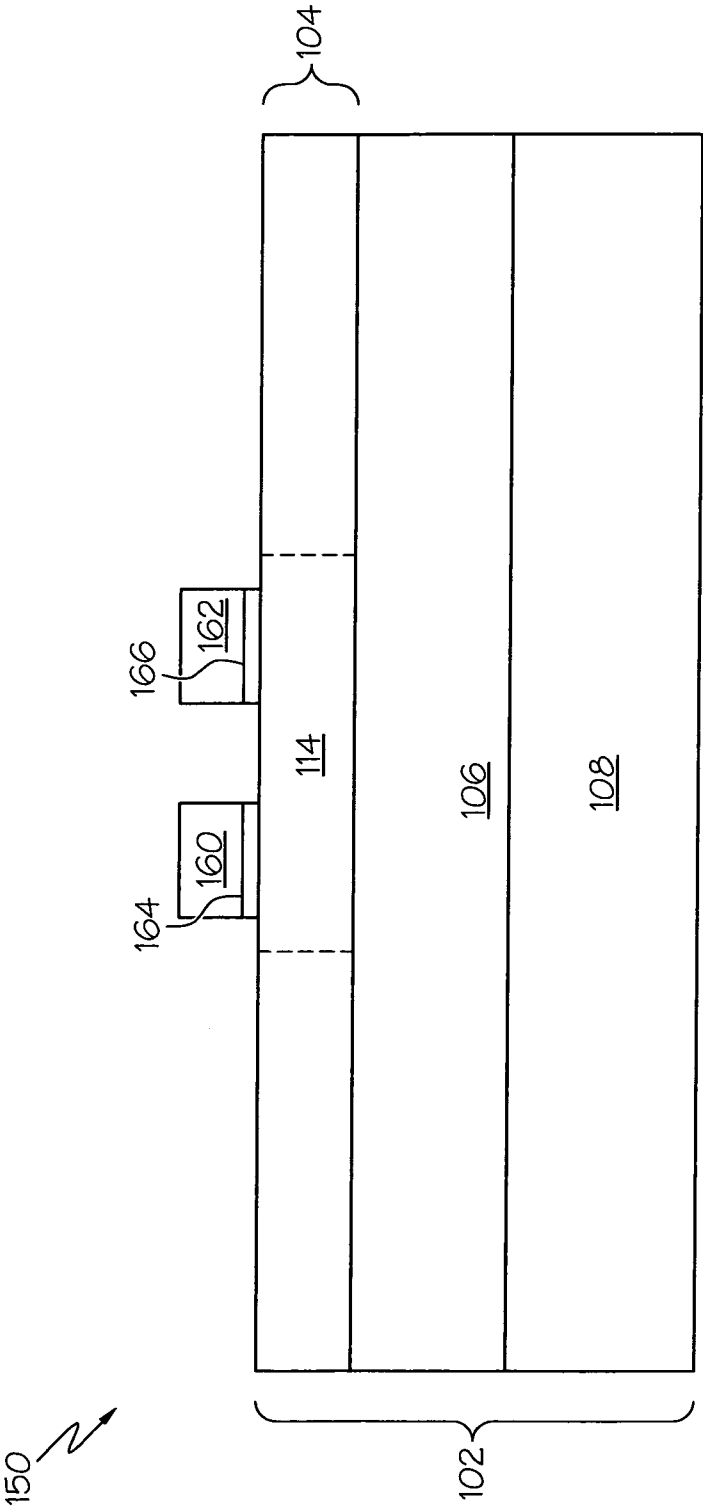


FIG. 2

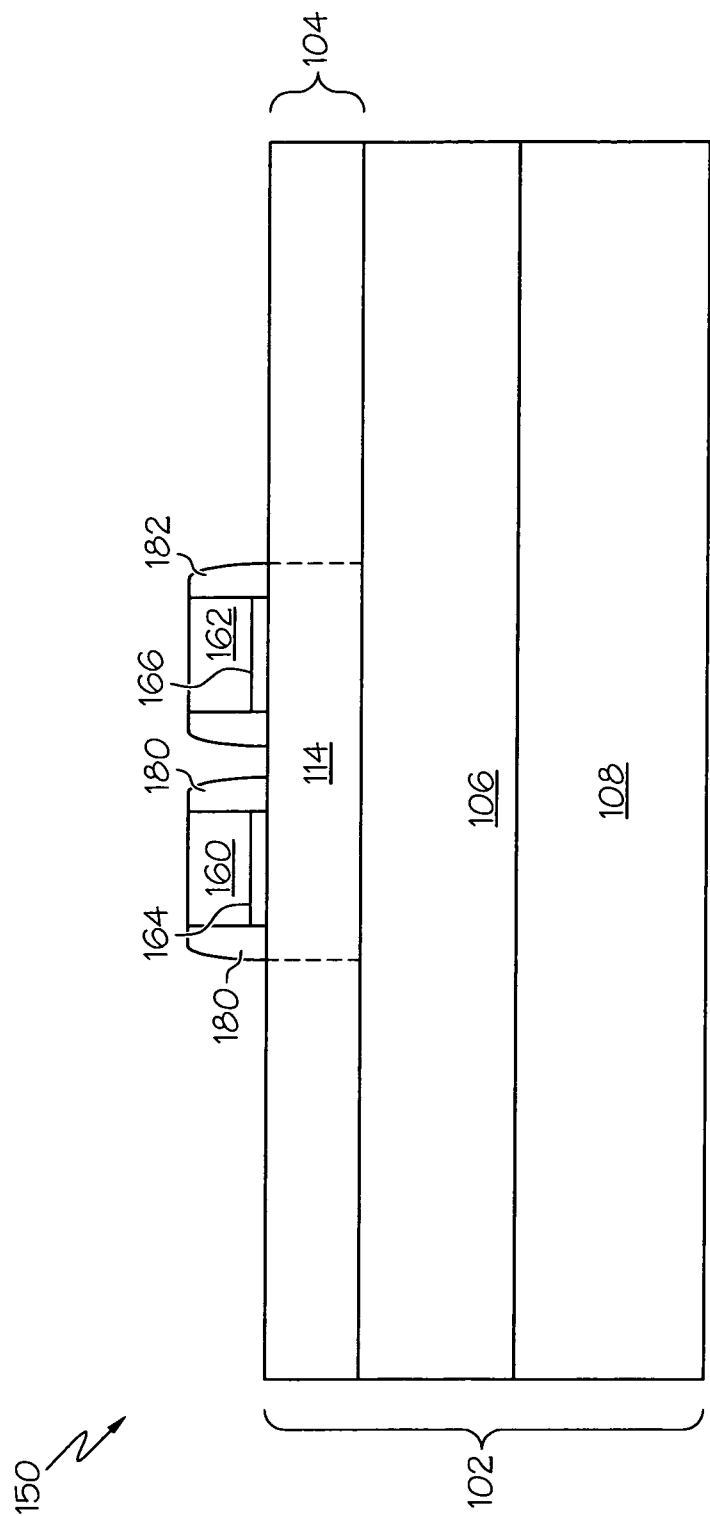


FIG. 3

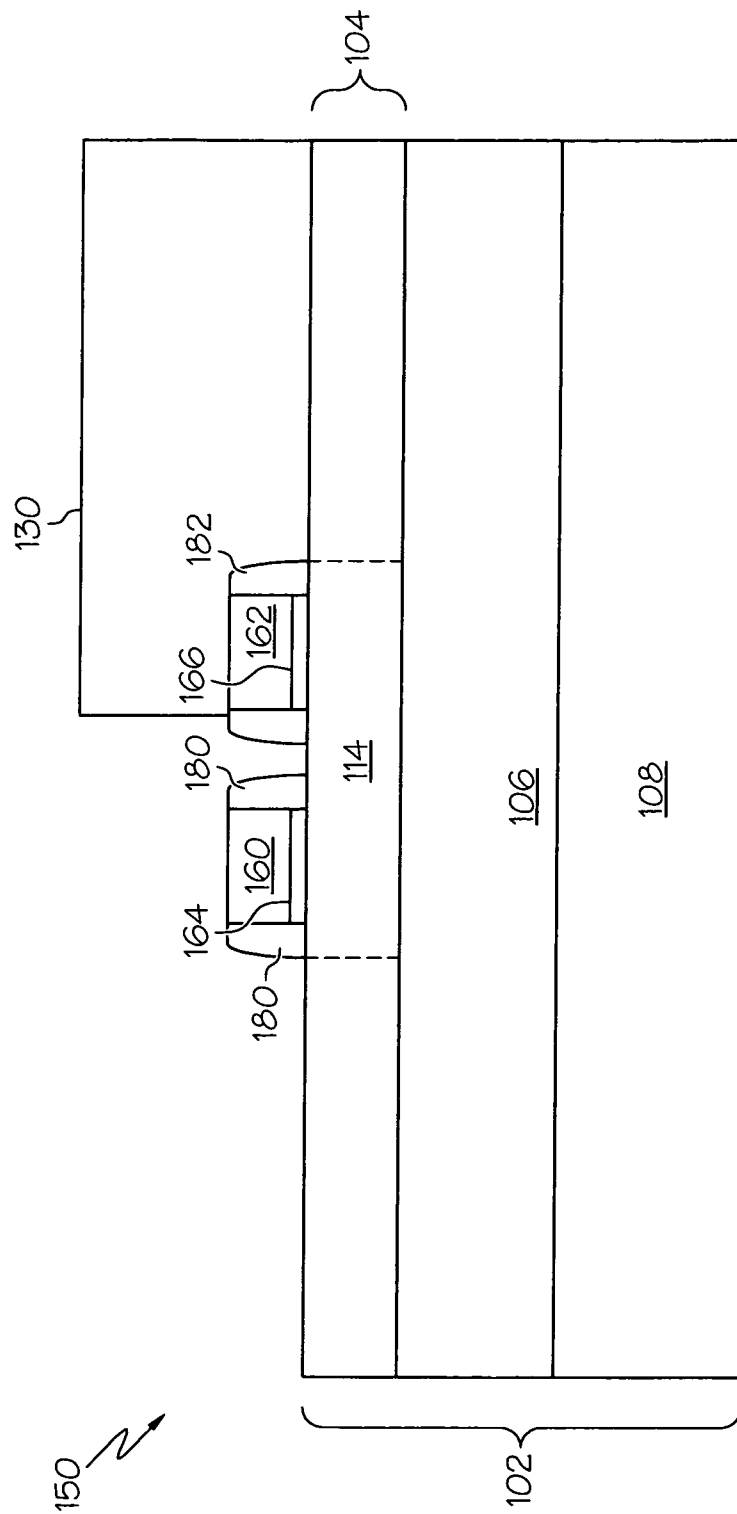


FIG. 4

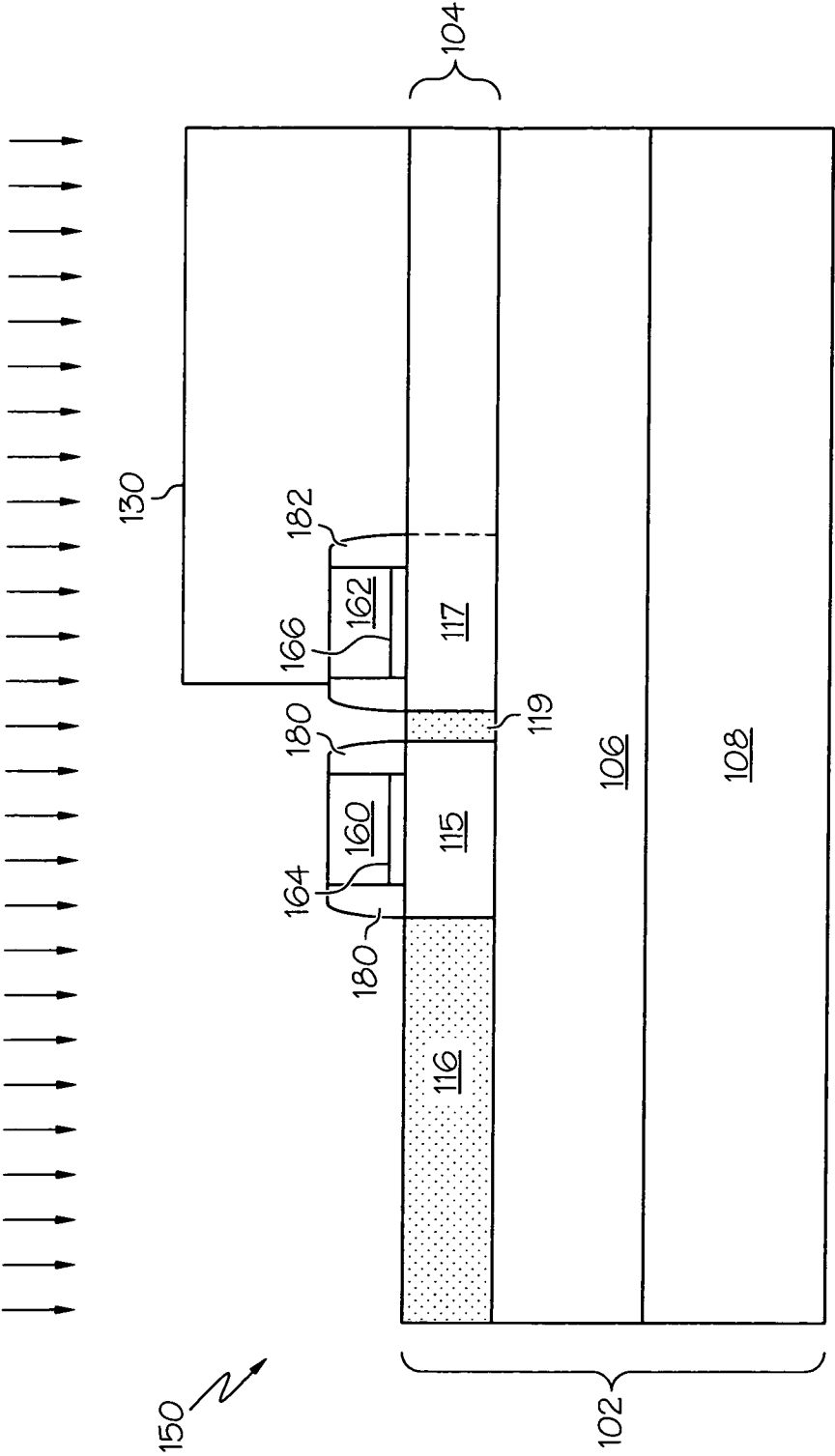


FIG. 5

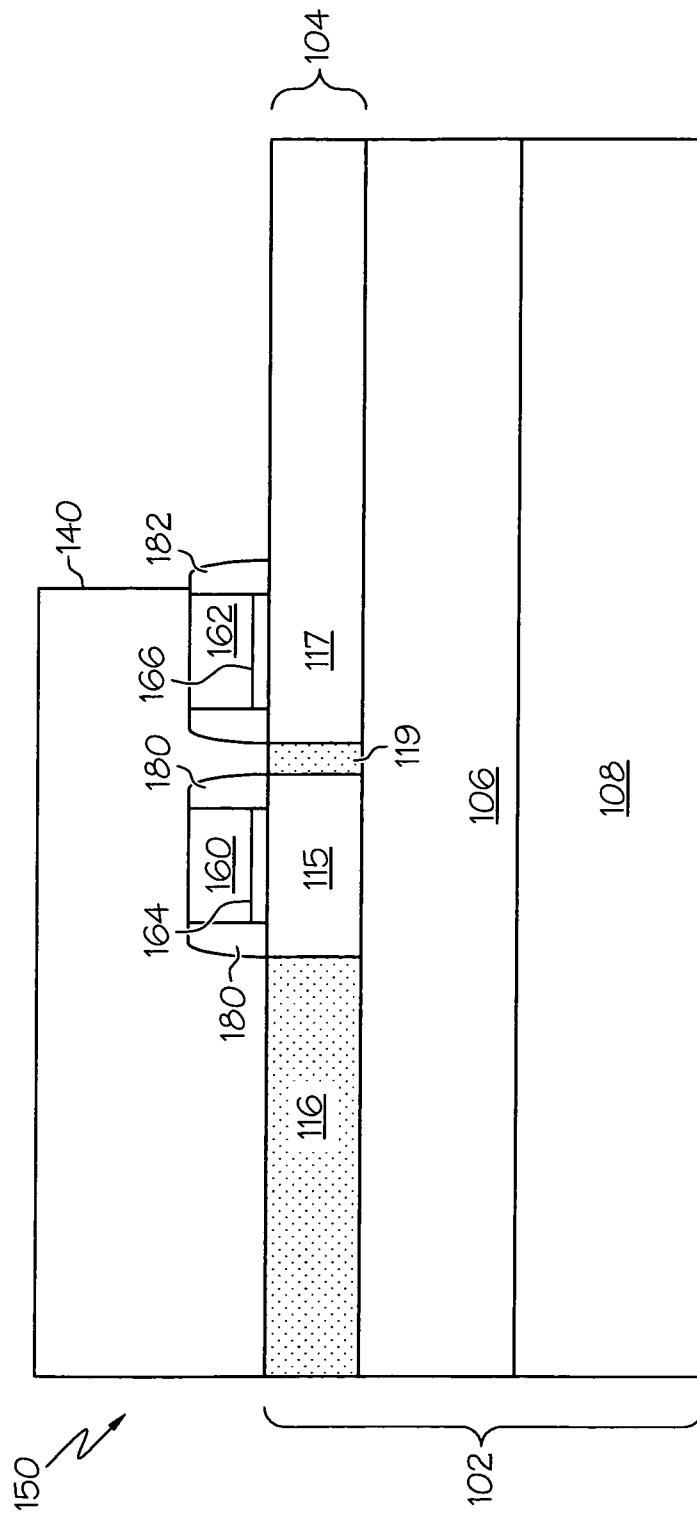


FIG. 6.

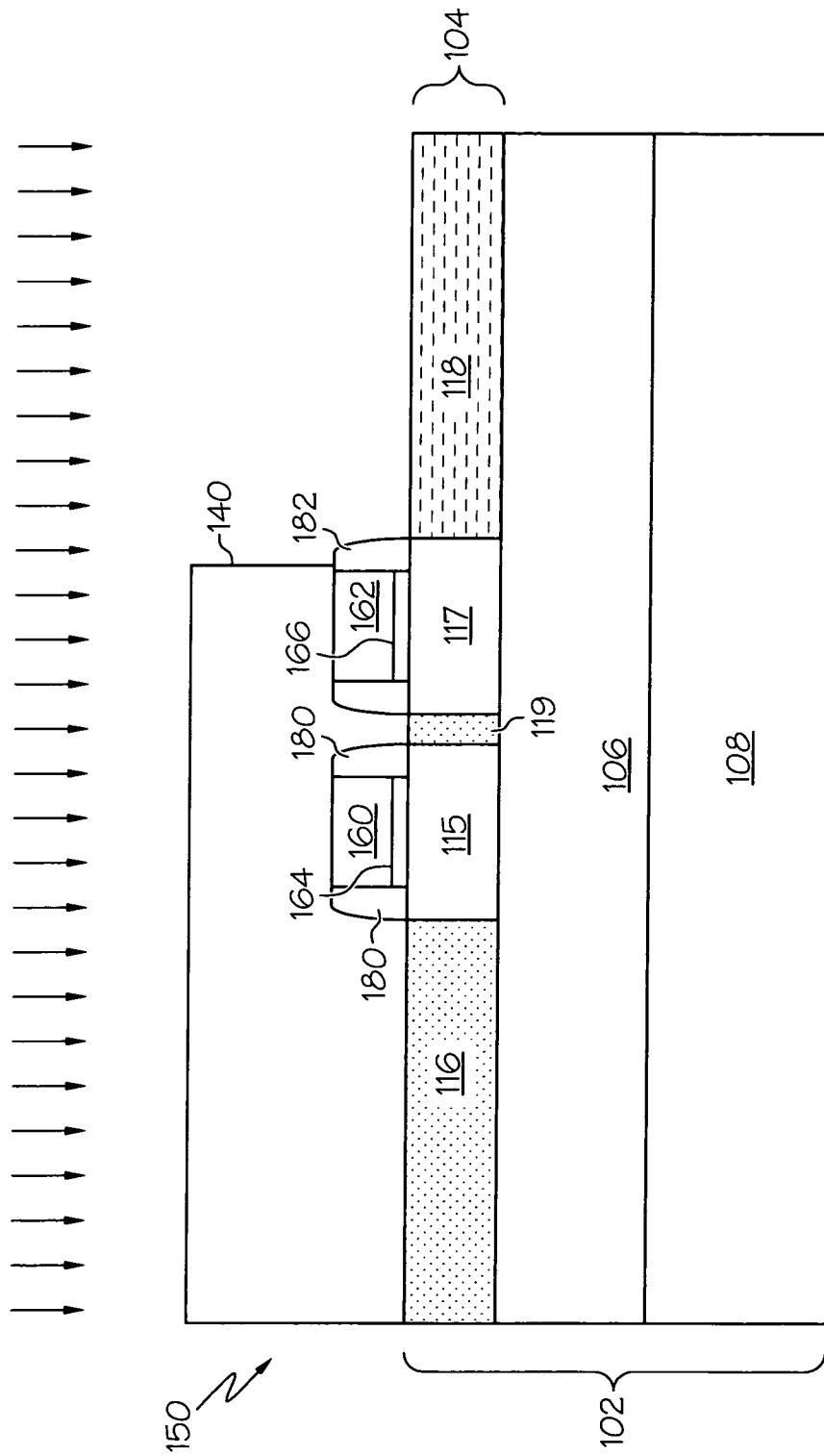


FIG. 7

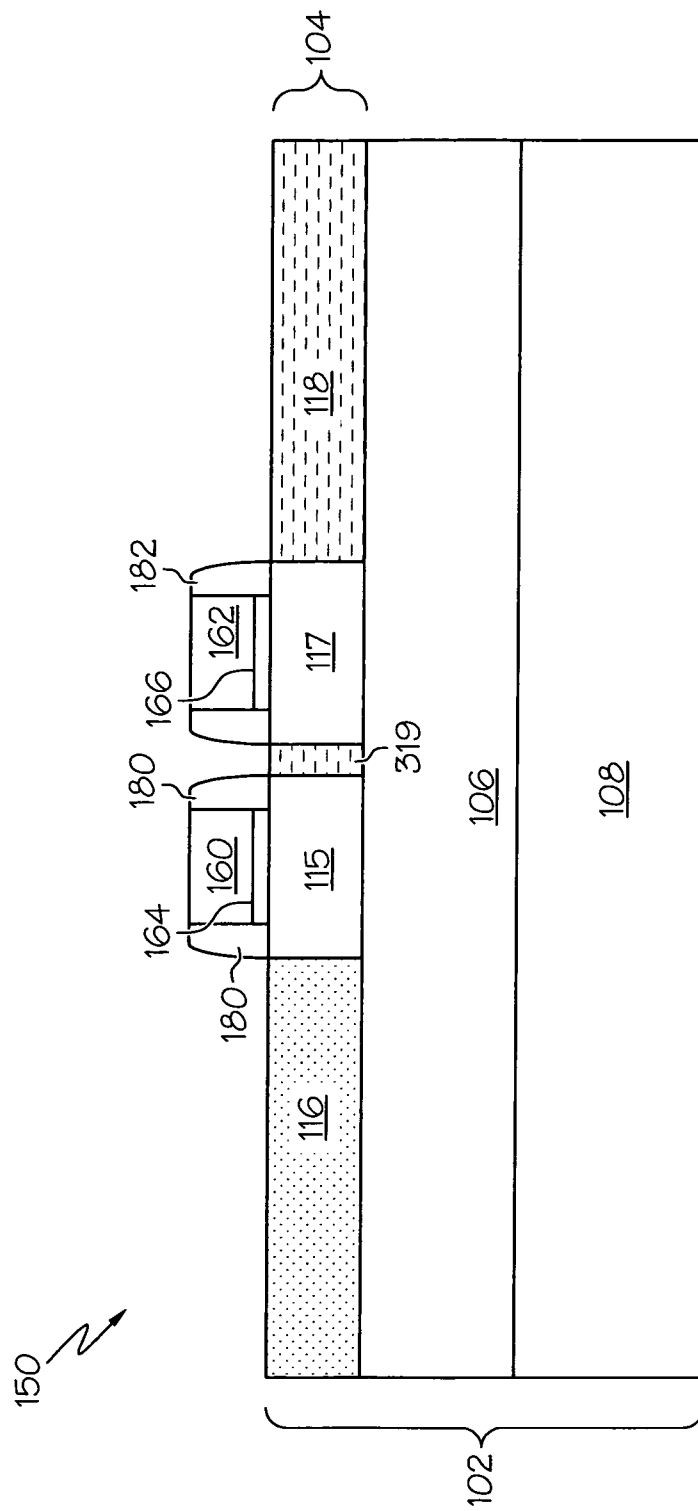


FIG. 8

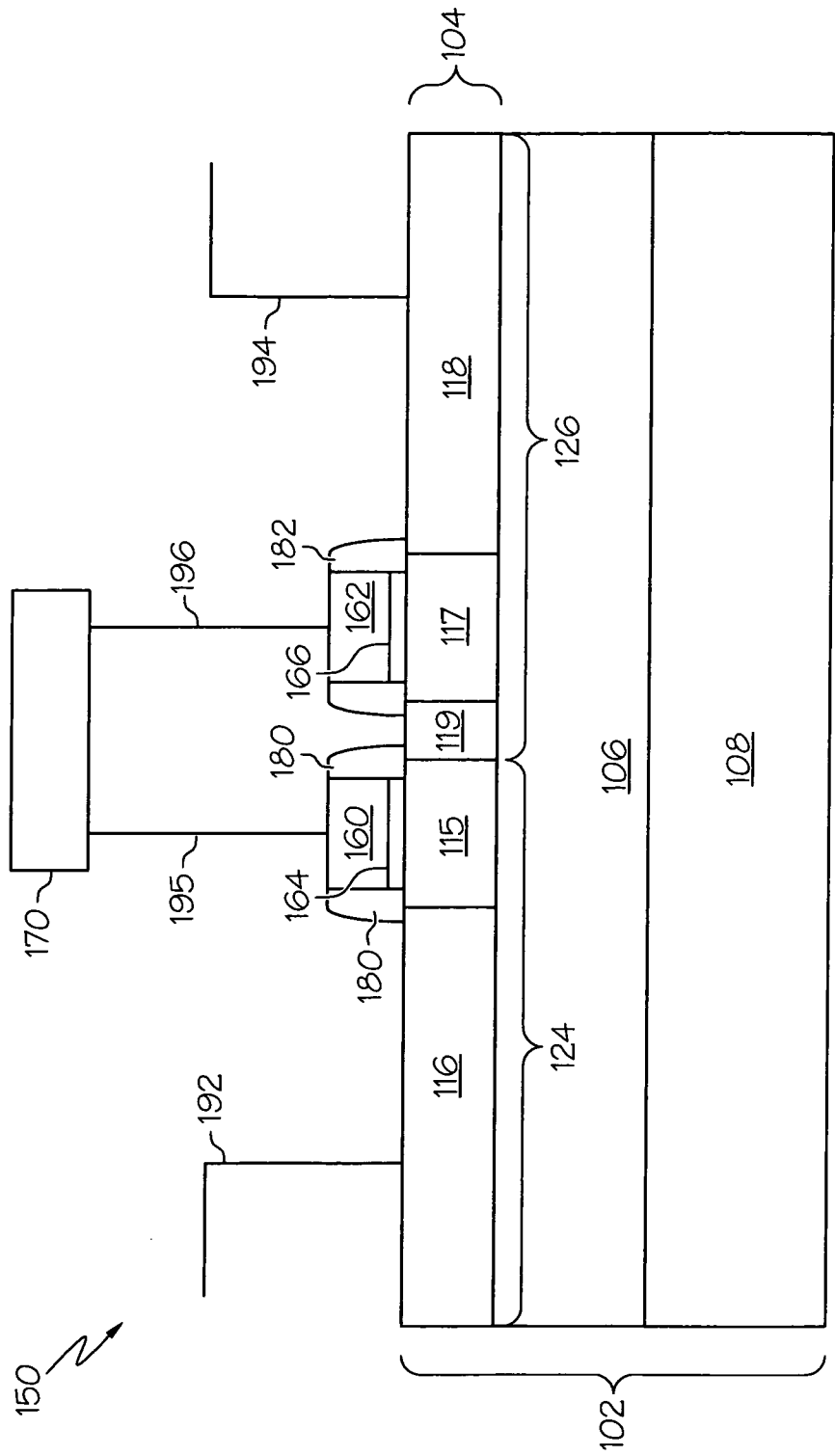


FIG. 9

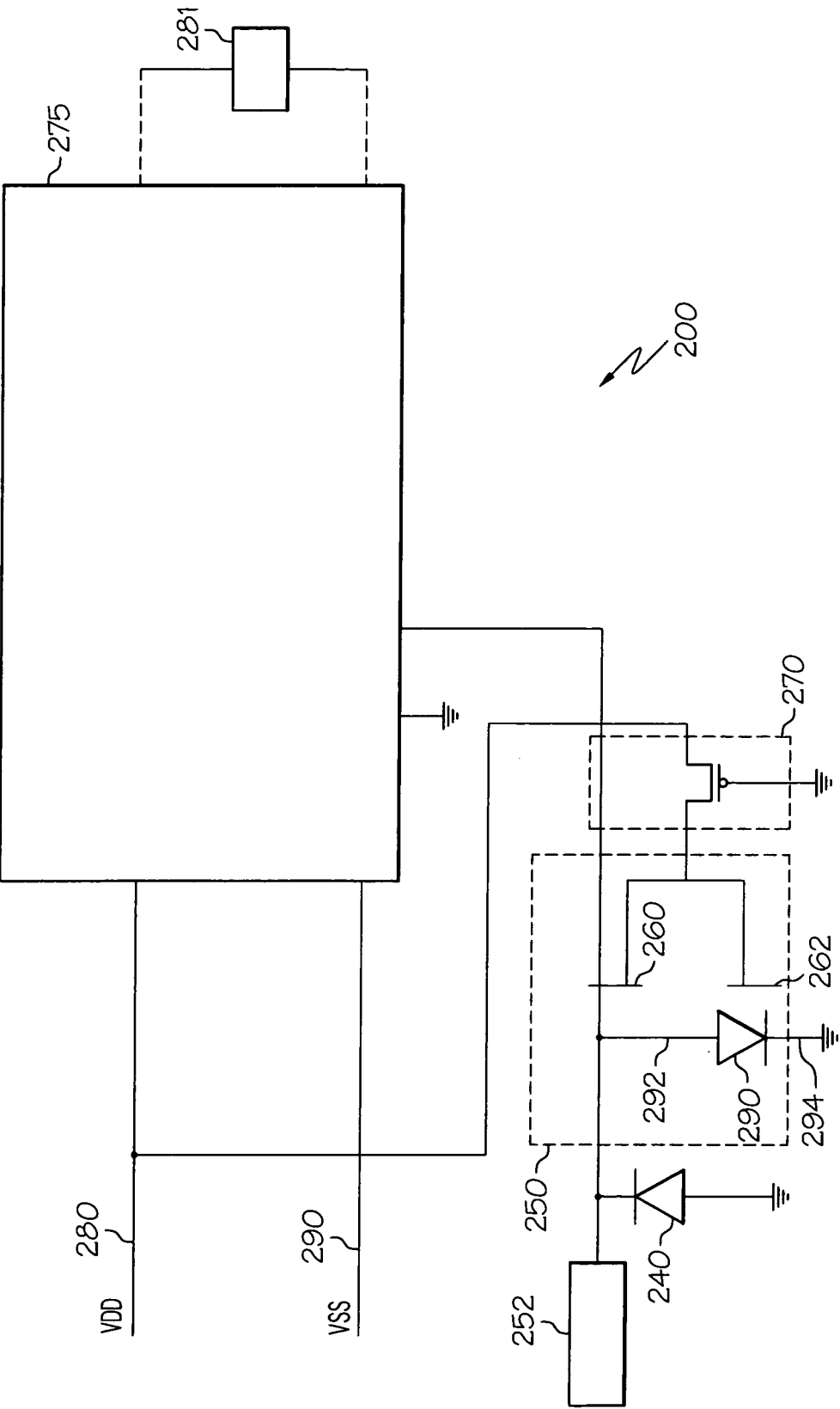


FIG. 10

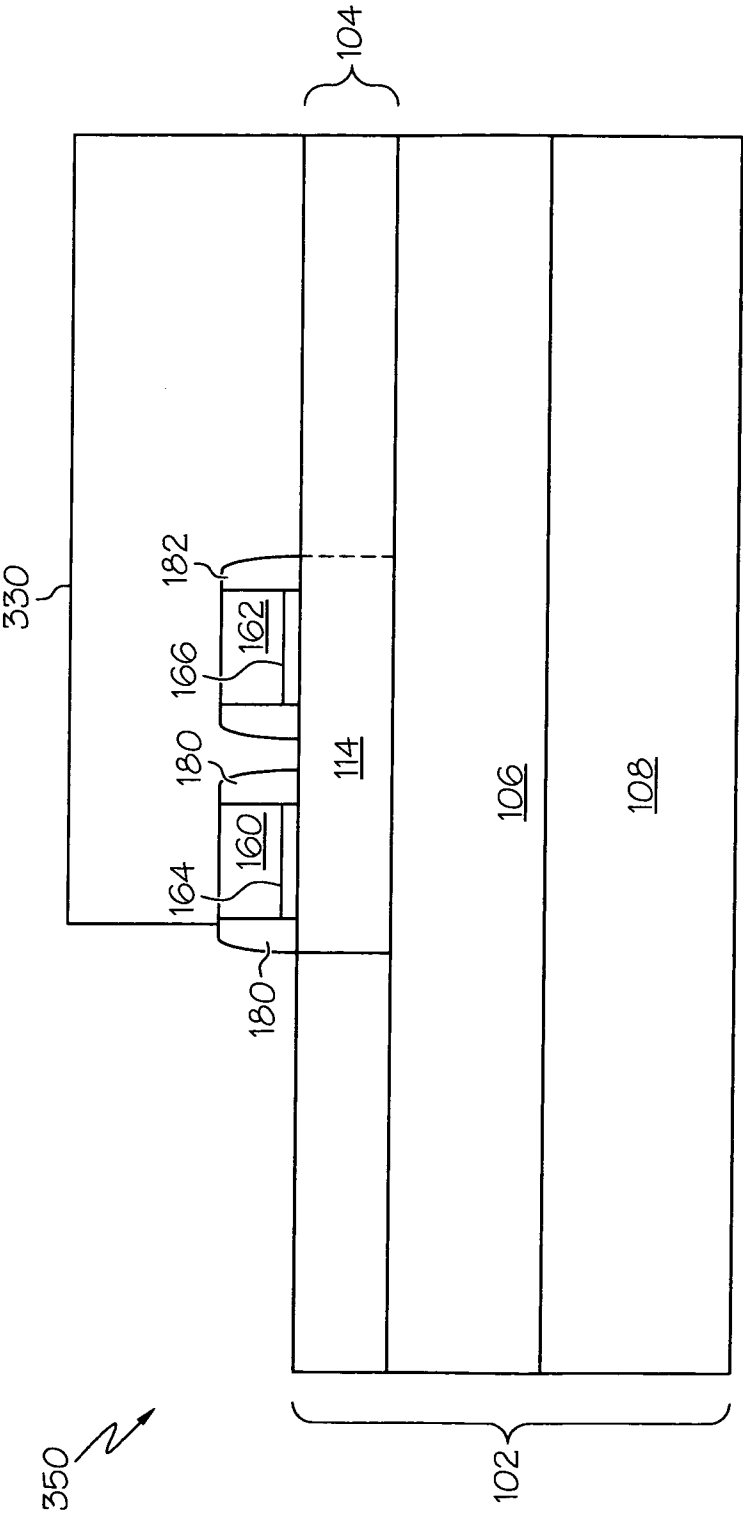


FIG. 11

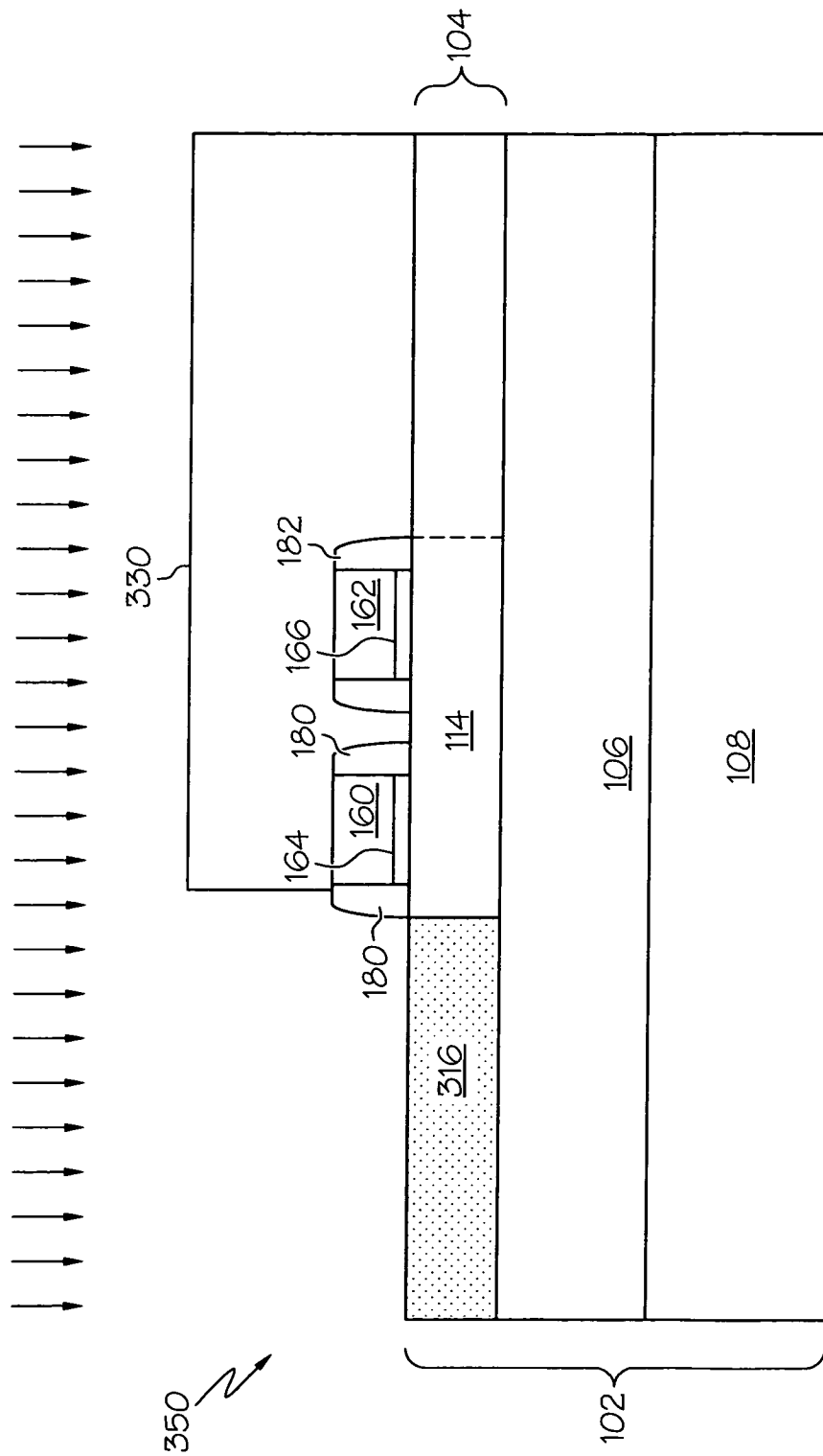


FIG. 12

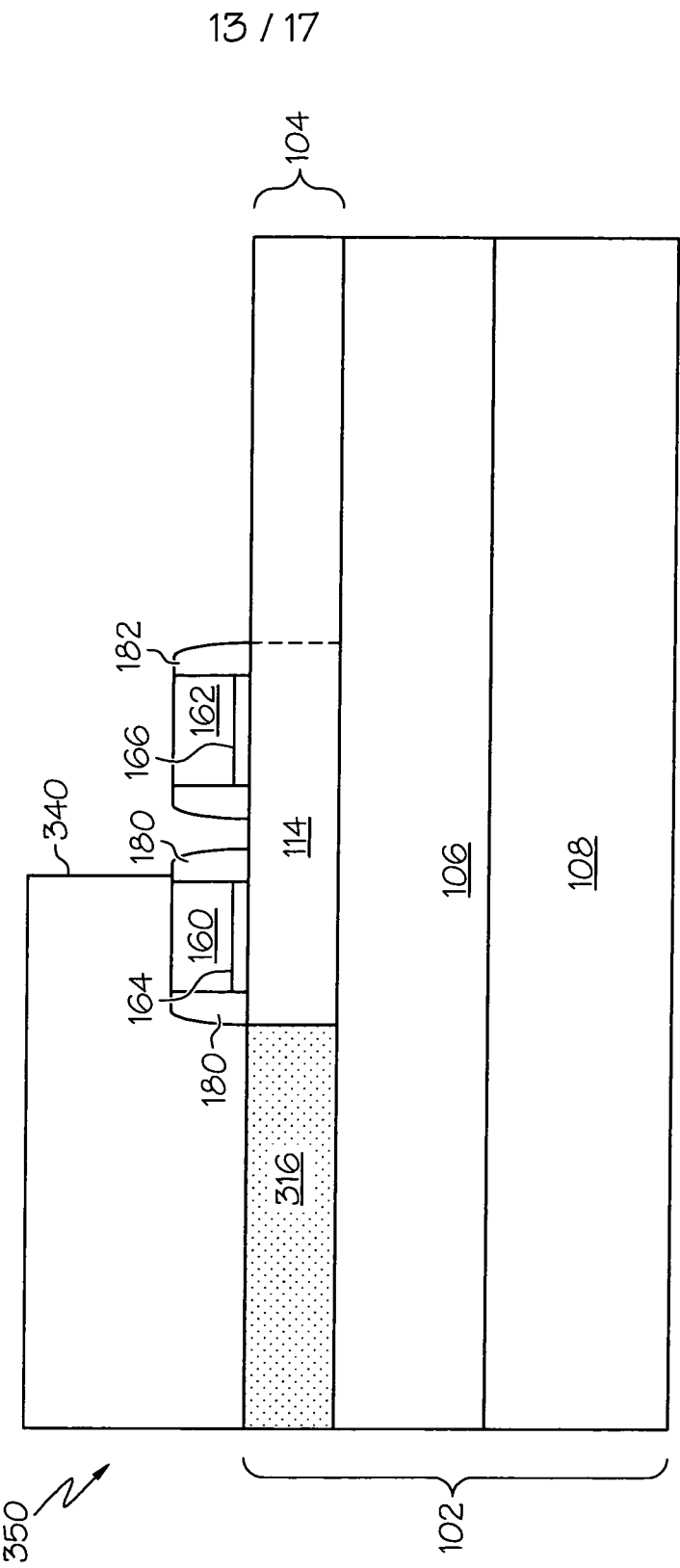


FIG. 13

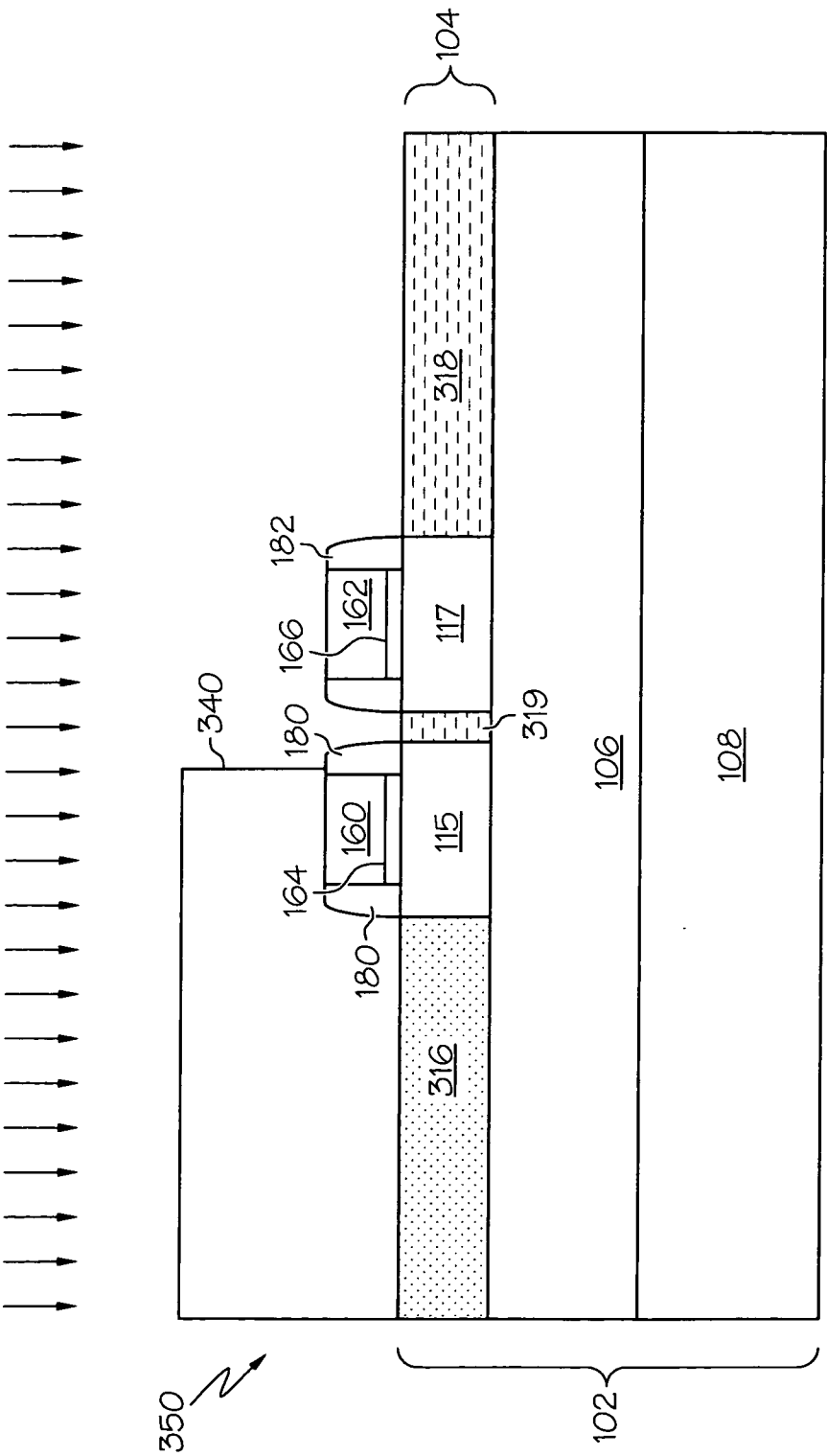


FIG. 14

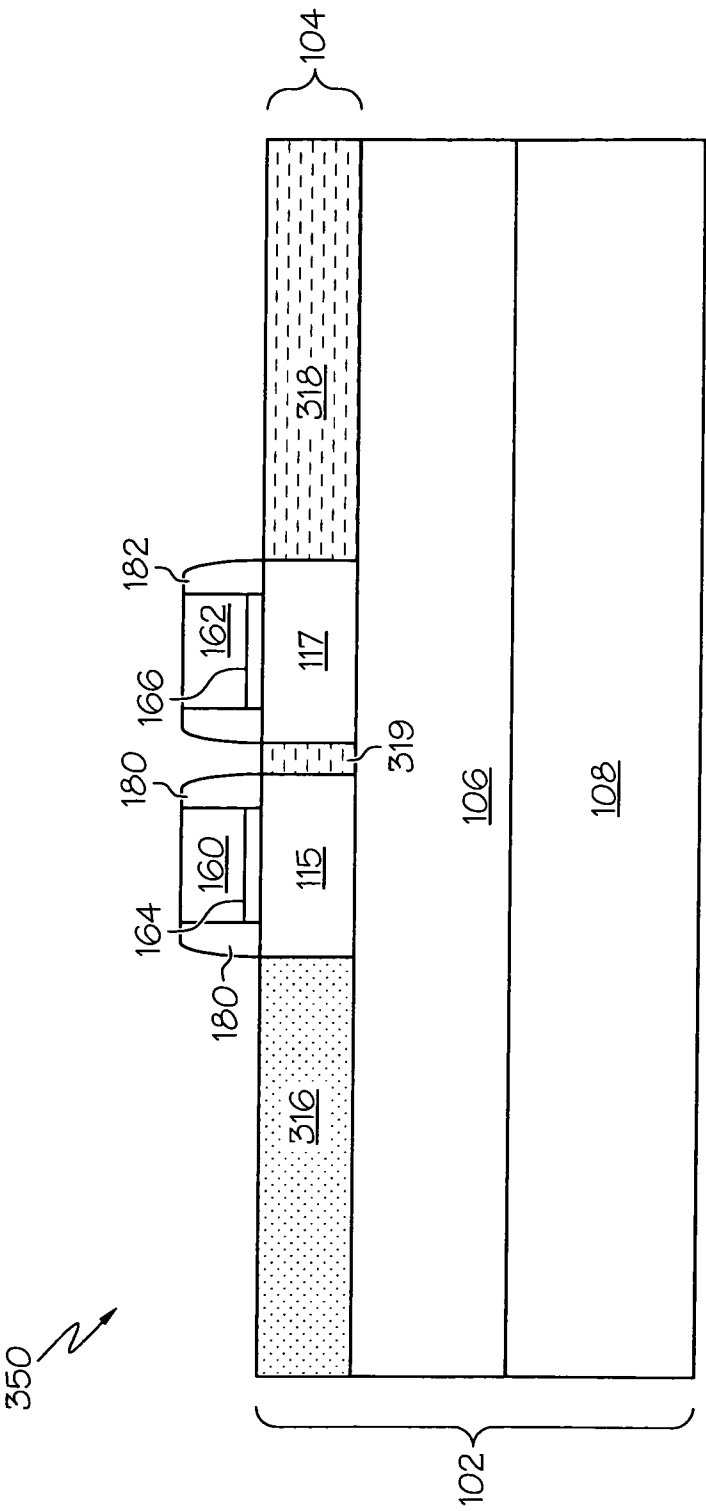


FIG. 15

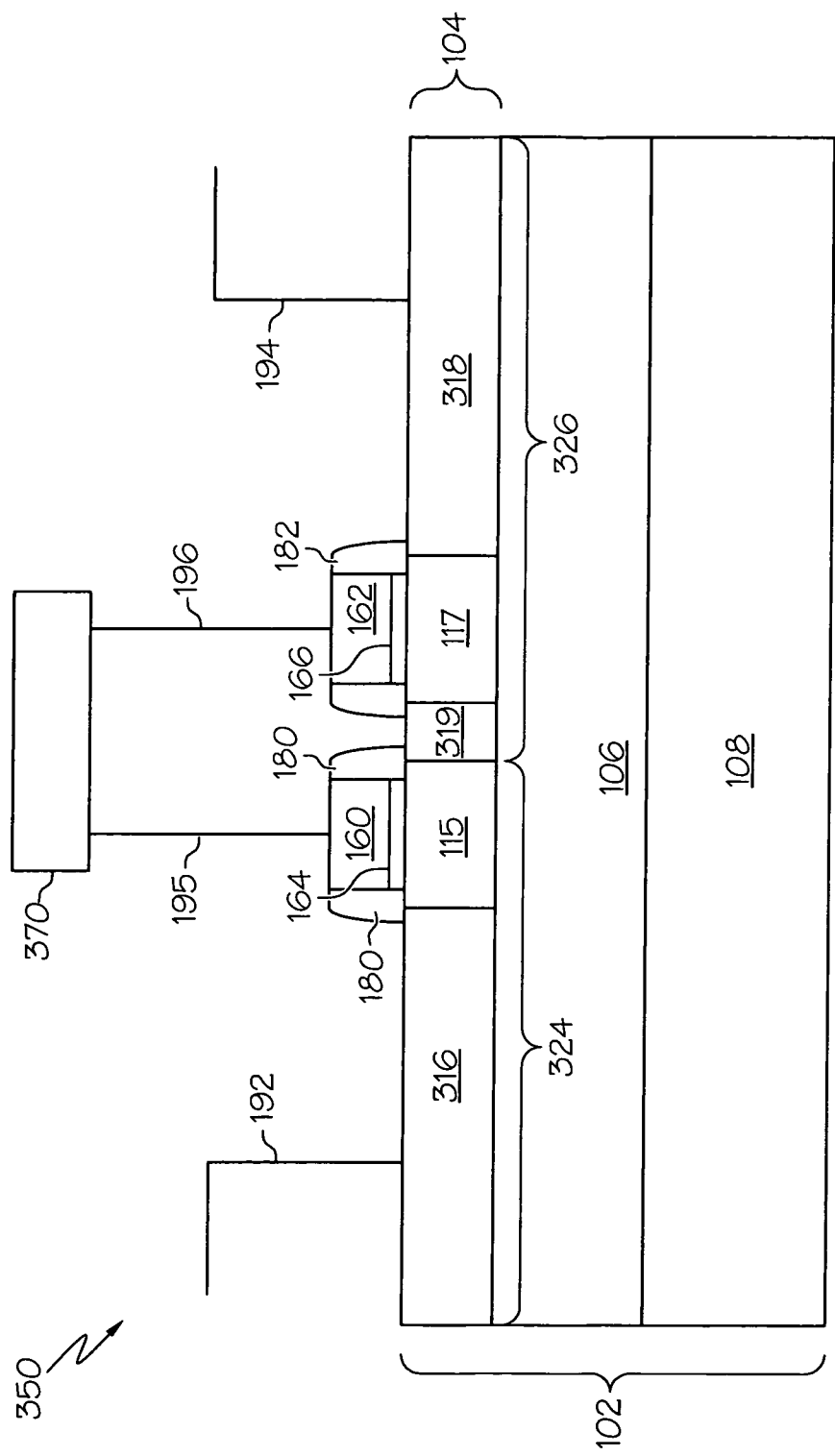


FIG. 16

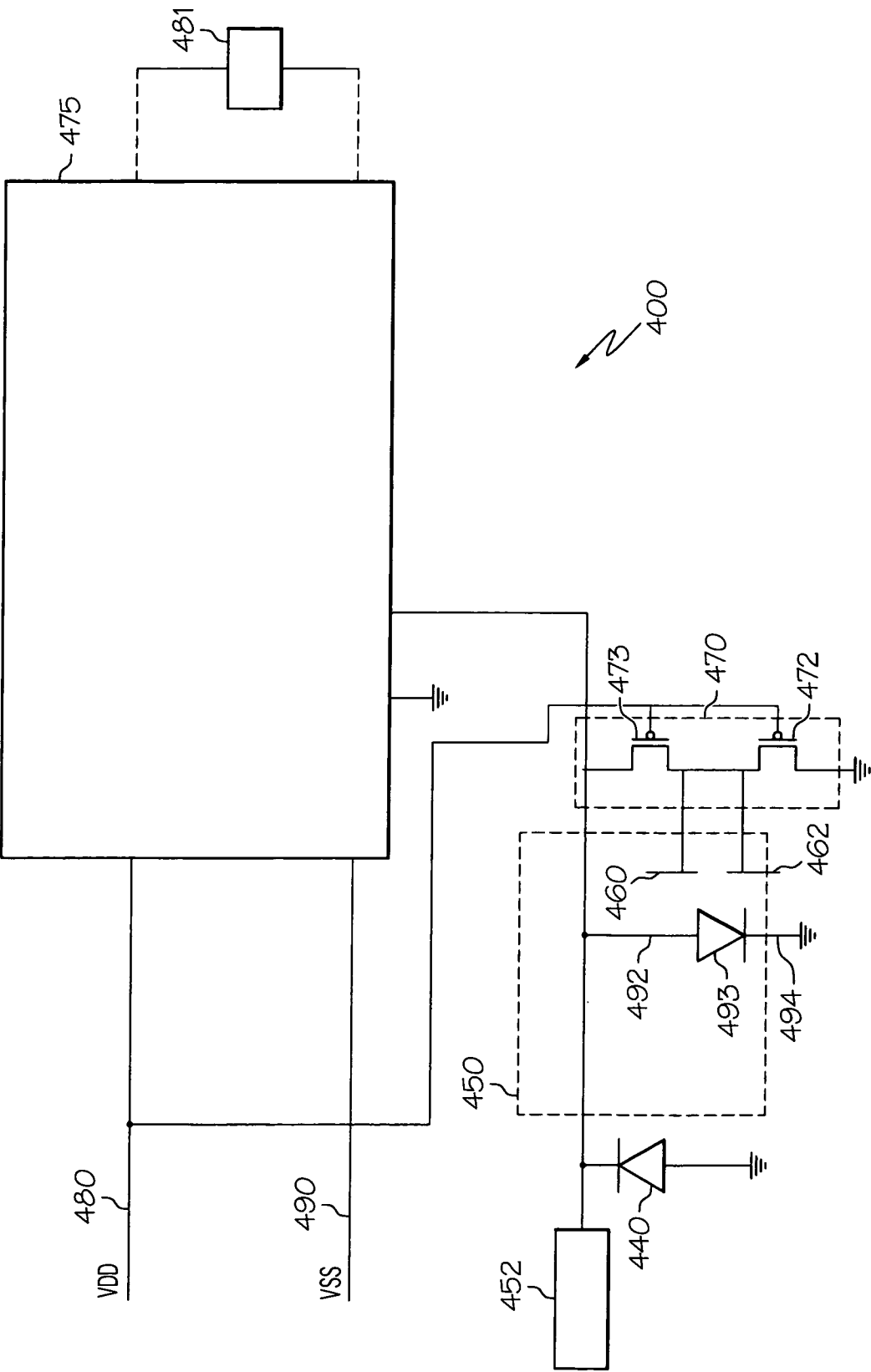


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2008/007975

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L27/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/012945 A1 (SUGIZAKI TARO [JP]) 18 January 2007 (2007-01-18) abstract paragraphs [0123] - [0126] paragraphs [0135] - [0137] paragraphs [0075] - [0078], [0080], [0083], [0085], [0087] figures 12,13	1-15
A		16-19
X	US 2007/040221 A1 (GOSSNER HARALD [DE] ET AL) 22 February 2007 (2007-02-22) abstract paragraphs [0024] - [0028], [0033] - [0036], [0140] - [0143] figures 5A,5B,5C,6A,6B,8A,8B,9A,9B	10-17
A		1-9,18, 19
	----- -/--	



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22 August 2008

Date of mailing of the international search report

01/09/2008

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2003/007301 A1 (KER MING-DOU [TW] ET AL) 9 January 2003 (2003-01-09) abstract figures 5A-9E	1-3,6,7, 10,15-17 4,5,8,9, 11-14, 18,19
X A	EP 0 852 400 A (TEXAS INSTRUMENTS INC [US]) 8 July 1998 (1998-07-08) abstract column 7, line 55 - column 9, line 14 figures 6-9	1-3,6,7, 10,15 4,5,8,9, 11-14, 16-19

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/007975

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007012945 A1	18-01-2007	JP 2007049113 A	22-02-2007
US 2007040221 A1	22-02-2007	DE 102005039365 A1	22-02-2007
		JP 2007053387 A	01-03-2007
US 2003007301 A1	09-01-2003	CN 1396662 A	12-02-2003
		US 2003122192 A1	03-07-2003
EP 0852400 A	08-07-1998	DE 69832310 D1	22-12-2005
		DE 69832310 T2	27-07-2006
		JP 10294430 A	04-11-1998