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(54) **ISOLATED STACKED DIE SEMICONDUCTOR PACKAGES**

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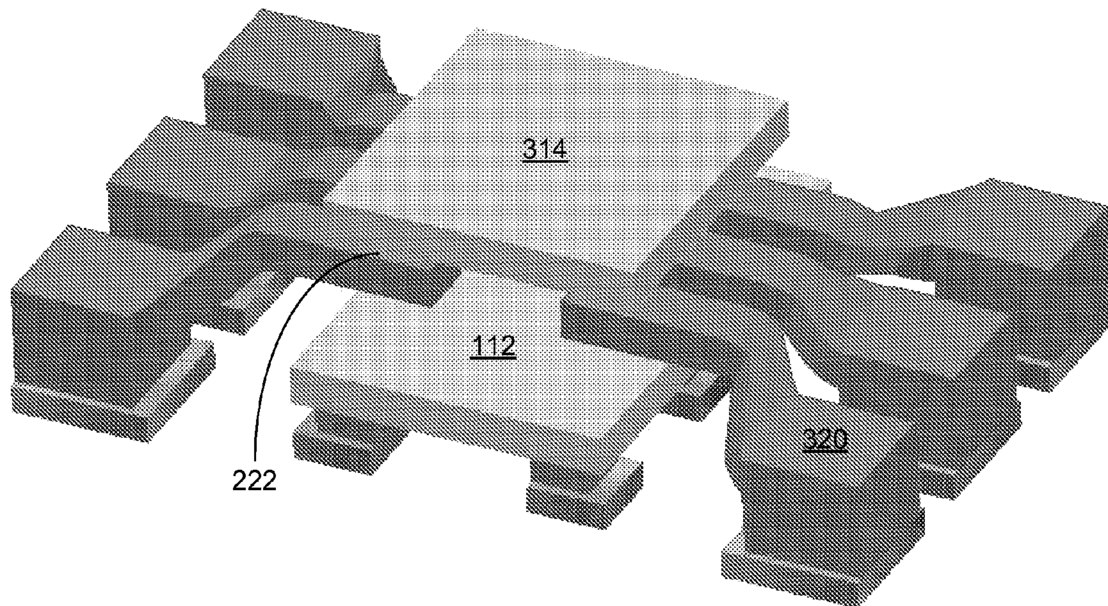
(57) **ABSTRACT**

Semiconductor packages that contain isolated stacked dies and methods for making such devices are described. The semiconductor package contains both a first die with a first integrated circuit and a second die with a second integrated circuit that is stacked onto the first die while also being isolated from the first die. The first and second dies are connected using differing arrays of metal strips that serve as interposers between the first and second dies. This configuration provides a thinner semiconductor package since wire-bonding is not used. As well, since the integrated circuit devices in the first and second dies are isolated from each other, local heating and/or hot spots are diminished or prevented in the semiconductor package. Other embodiments are also described.



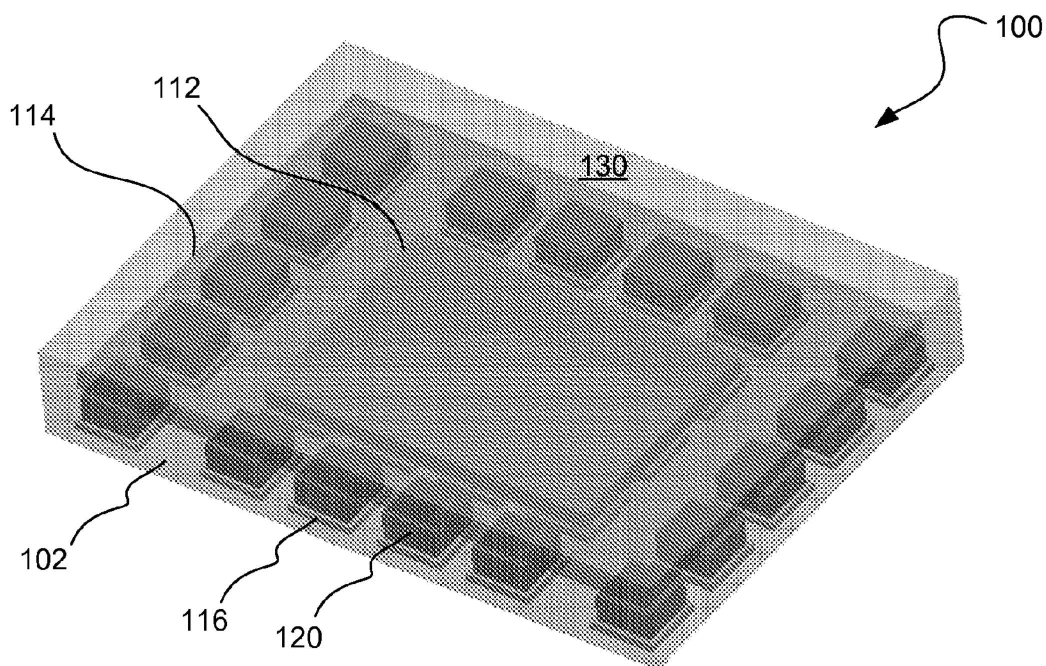


FIGURE 1

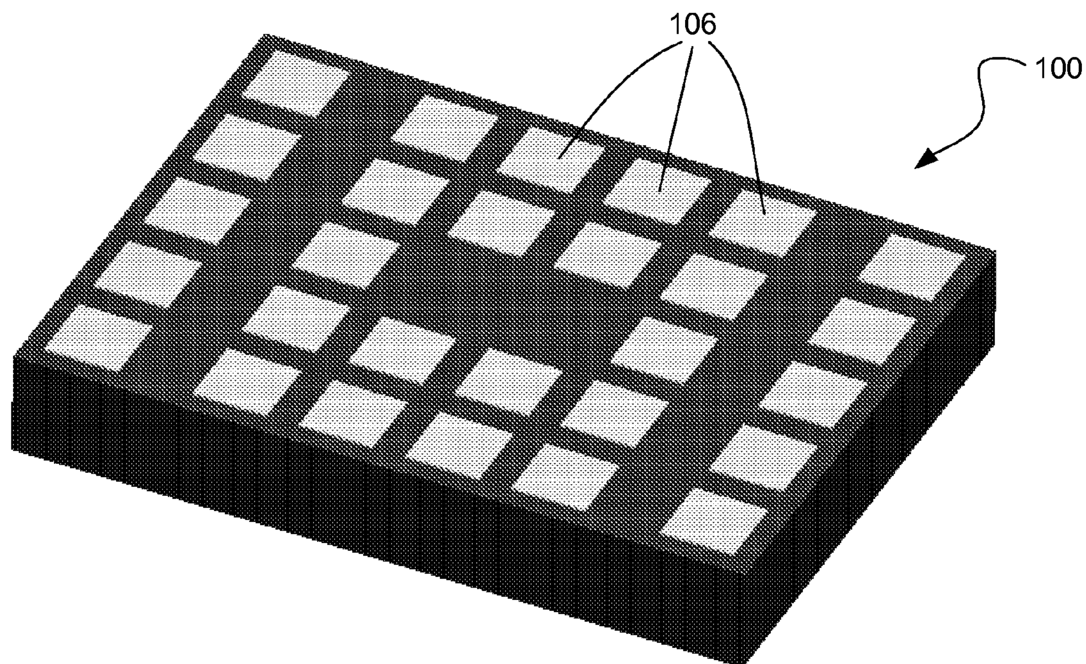


FIGURE 2

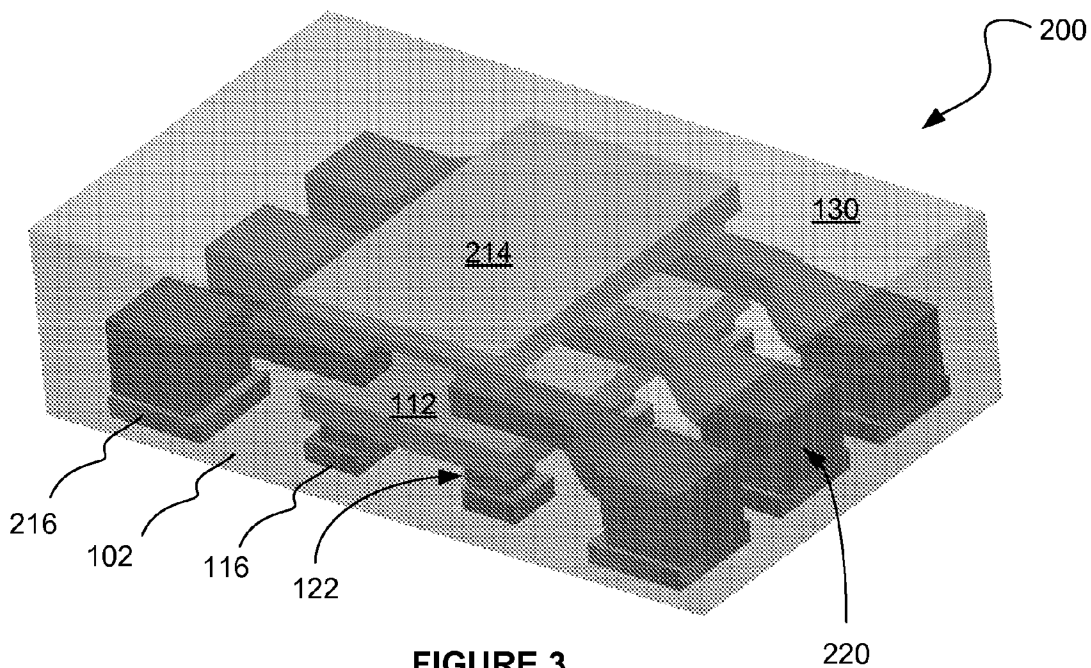


FIGURE 3

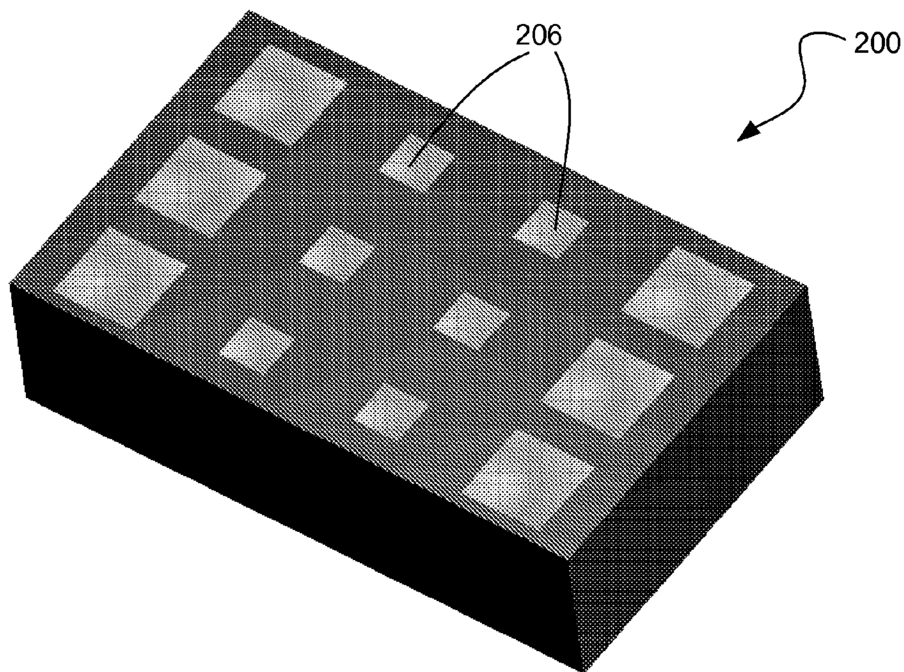


FIGURE 4

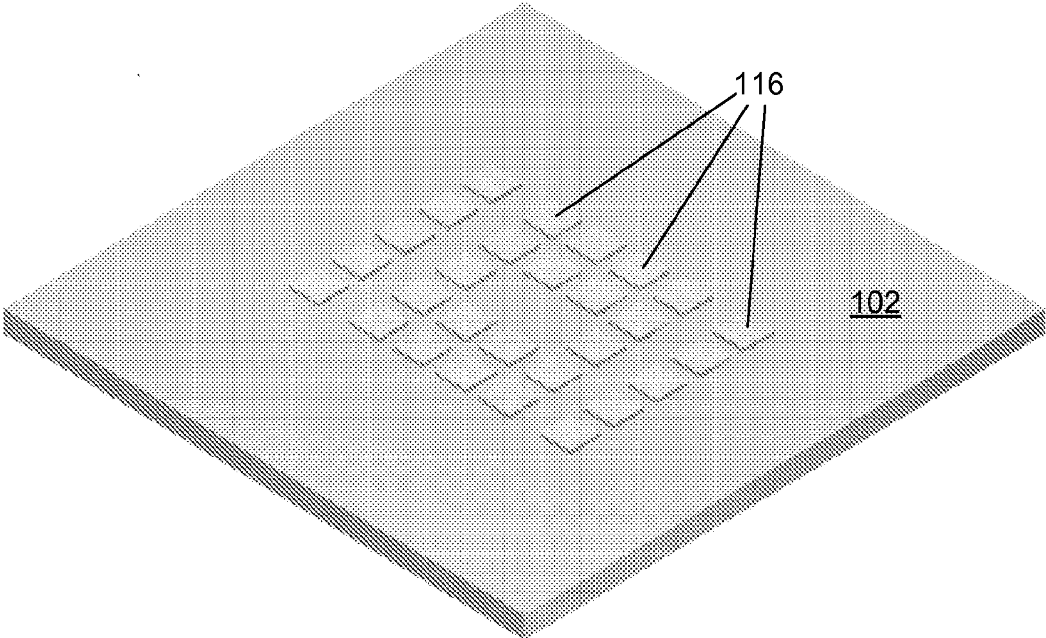


FIGURE 5

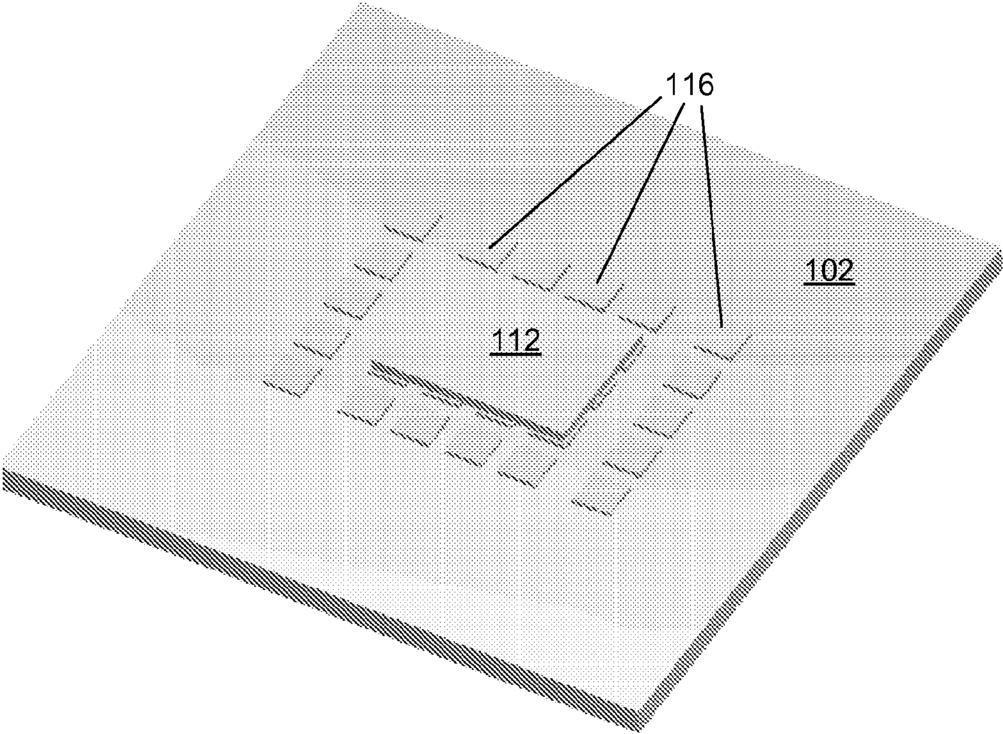


FIGURE 6

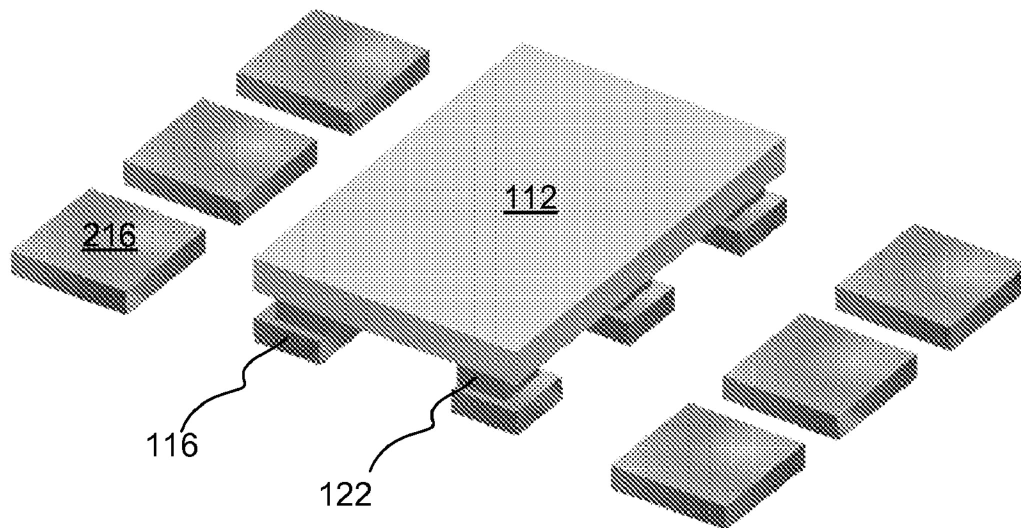


FIGURE 7

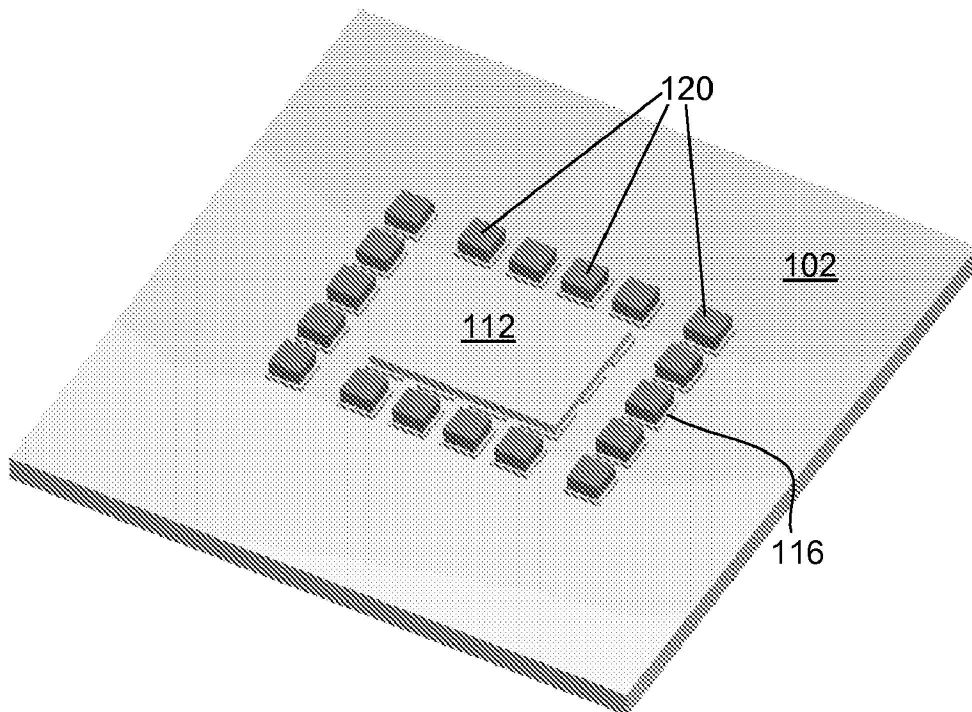


FIGURE 8

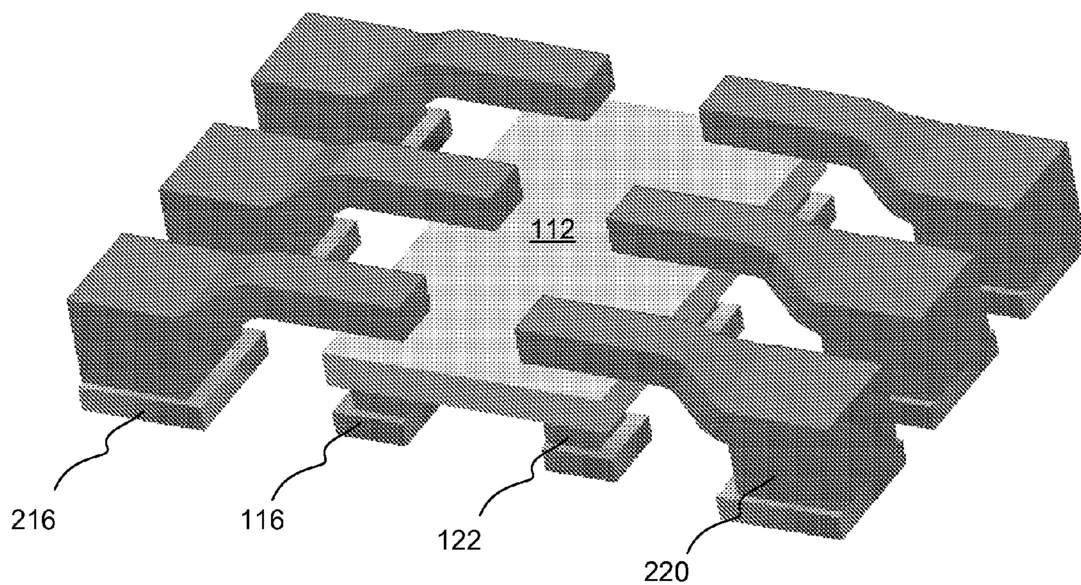


FIGURE 9

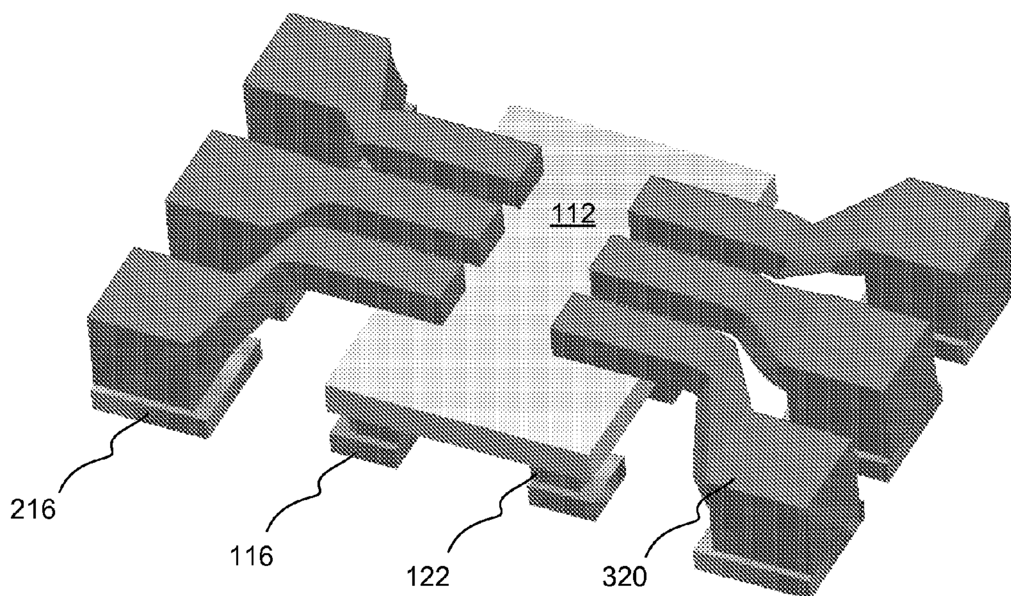


FIGURE 10

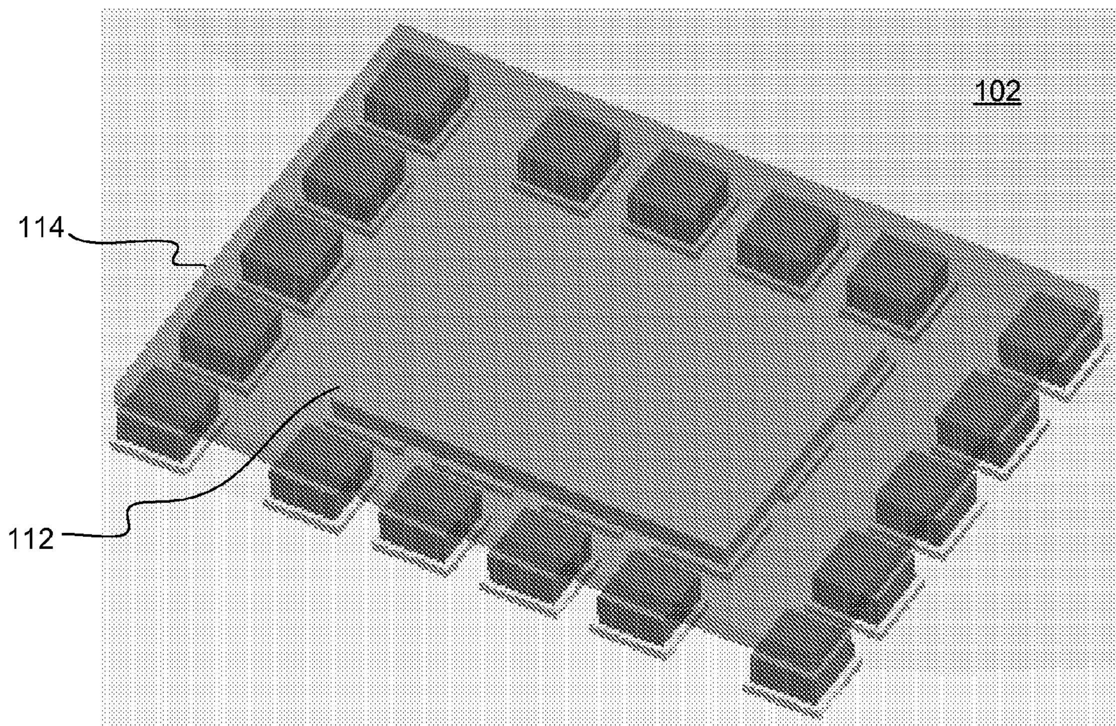


FIGURE 11

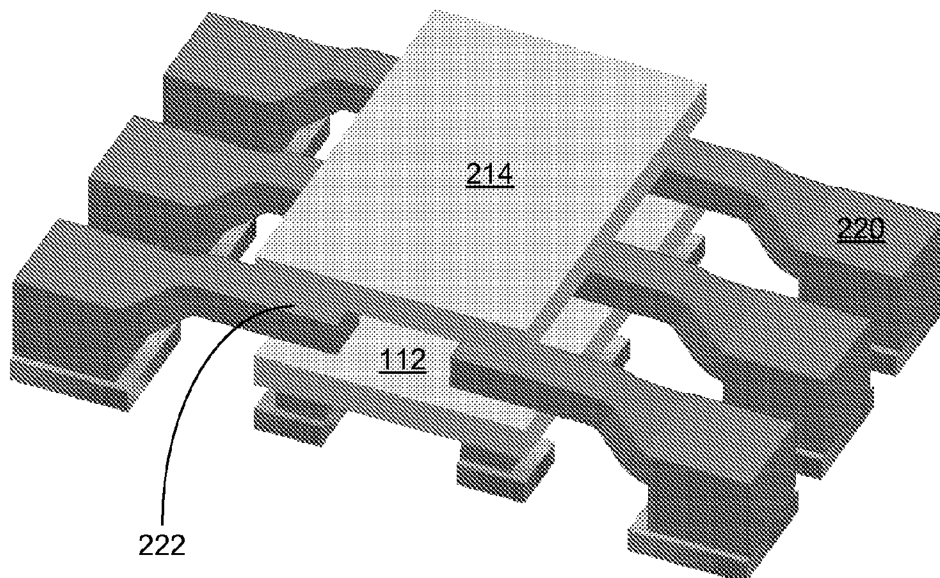


FIGURE 12

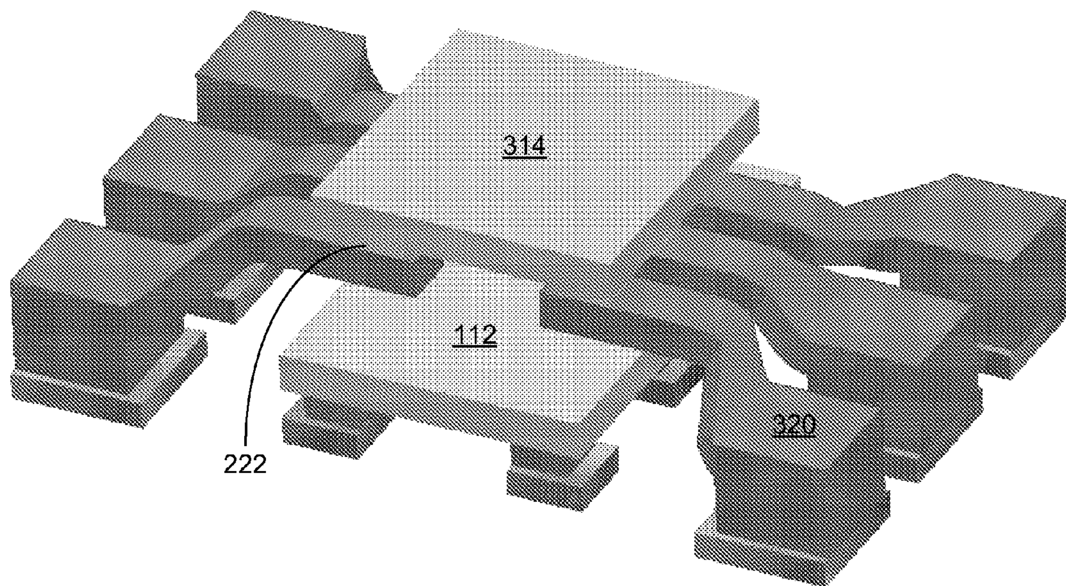


FIGURE 13

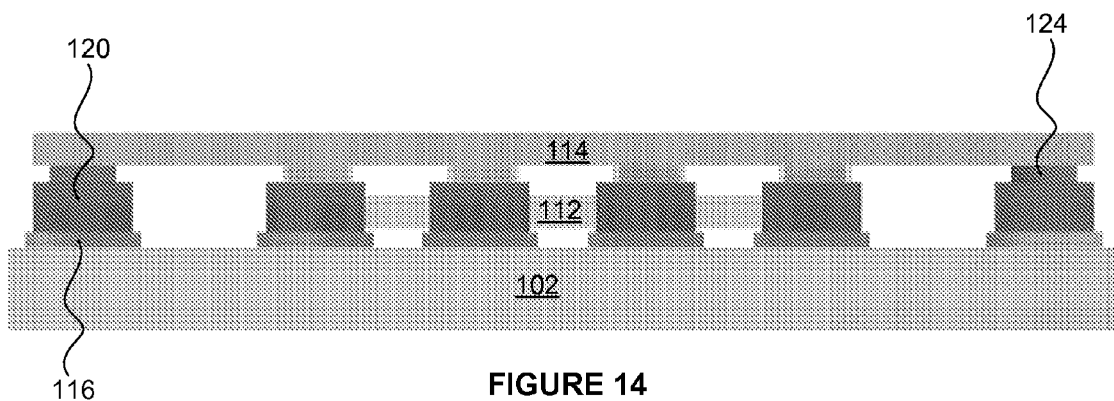


FIGURE 14

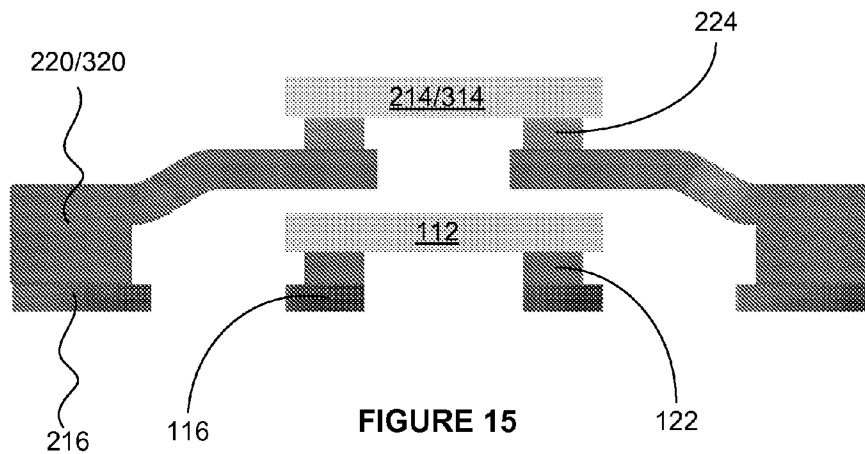


FIGURE 15

ISOLATED STACKED DIE SEMICONDUCTOR PACKAGES

FIELD

[0001] This application relates generally to semiconductor devices and methods for making such devices. More specifically, this application describes semiconductor packages that contain multiple dies containing integrated circuit devices and methods for making such devices.

BACKGROUND

[0002] Semiconductor packages are well known in the art. Often, these packages may include one or more semiconductor devices, such as an integrated circuit ("IC") die or chip, which may be connected to a die pad that is centrally formed in a lead frame. In some cases, bond wires electrically connect the IC die to a series of terminals that serve as an electrical connection to an external device, such as a printed circuit board ("PCB"). An encapsulating material can be used to cover the bond wires, the IC die, the terminals, and/or other components of the semiconductor device to form the exterior of the semiconductor package. A portion of the terminals and possibly a portion of the die pad may be externally exposed from the encapsulating material. In this manner, the die may be protected from environmental hazards—such as moisture, contaminants, corrosion, and mechanical shock—while being electrically and mechanically connected to an intended device that is external to the semiconductor package.

[0003] After it has been formed, the semiconductor package is often used in an ever growing variety of electronic applications, such as disk drives, USB controllers, portable computer devices, cellular phones, and so forth. Depending on the die and the electronic application, the semiconductor package may be highly miniaturized and may need to be as small as possible.

[0004] In most instances, each semiconductor package only contains a single die that contains the integrated circuit device, or a discrete device such as a diode or a transistor. Thus, the functionality of each semiconductor package is often limited to that discrete device or integrated circuit on the single die that it contains. To combine the functions of devices in more than a single die, two or more semiconductor packages are needed.

SUMMARY

[0005] This application relates to semiconductor packages that contain isolated stacked dies and methods for making such devices. The semiconductor package contains both a first die with a first integrated circuit and a second die with a second integrated circuit that is stacked onto the first die while also being isolated from the first die. The first and second dies are connected using differing arrays of metal strips that serve as interposers between the first and second dies. This configuration provides a thinner semiconductor package since wire-bonding is not used. As well, since the integrated circuit devices in the first and second dies are isolated from each other, local heating and/or hot spots are diminished or prevented in the semiconductor package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The following description can be better understood in light of the Figures, in which:

[0007] FIGS. **1** and **2** shows some embodiments of a semiconductor package containing multiple dies;

[0008] FIGS. **3-4** shows other embodiments of a semiconductor package containing multiple dies;

[0009] FIGS. **5-13** depict some embodiments of the methods for manufacturing a semiconductor package containing multiple dies; and

[0010] FIGS. **14-15** illustrate some embodiments of an isolated, stacked-die structure of the semiconductor packages before encapsulation.

[0011] The Figures illustrate specific aspects of the semiconductor packages that contain multiple dies with discrete devices and methods for making such devices. Together with the following description, the Figures demonstrate and explain the principles of the methods and structures produced through these methods. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer, component, or substrate is referred to as being "on" another layer, component, or substrate, it can be directly on the other layer, component, or substrate, or intervening layers may also be present. The same reference numerals in different drawings represent the same element, and thus their descriptions will not be repeated.

DETAILED DESCRIPTION

[0012] The following description supplies specific details in order to provide a thorough understanding. Nevertheless, the skilled artisan would understand that the semiconductor devices and associated methods of using the devices can be implemented and used without employing these specific details. Indeed, the devices and associated methods can be placed into practice by modifying the illustrated devices and associated methods and can be used in conjunction with any other apparatus and techniques conventionally used in the industry. For example, while the description below focuses on methods for making for semiconductor devices in the IC industry, it could be used for and applied to other electronic devices like optoelectronic devices, solar cells, MEMS structures, lighting controls, power supplies, and amplifiers. As well, while the description below describes using two dies in the same semiconductor package, it could be configured to contain more than two, including 3 or even more dies.

[0013] Some embodiments of the semiconductor packages that contain multiple dies and methods for making such devices are shown in the Figures. In the embodiments shown in FIG. **1** (top view) and FIG. **2** (bottom view), the semiconductor package **100** contains a substrate **102**, a plurality of terminals **106**, a first die **112** containing a first IC device, a second die **114** containing a second IC device, land pads **116**, connectors **120**, and encapsulation **130**.

[0014] The first IC device and the second IC device may be the same or different and may be any known integrated circuit (including any discrete device) in the art. Some non-limiting examples of these devices may include logic or digital IC, linear regulators, audio power amplifiers, LDO, driver IC, diodes, and/or transistors, including zener diodes, schottky diodes, small signal diodes, bipolar junction transistors ("BJT"), metal-oxide-semiconductor field-effect transistors ("MOSFET"), insulated-gate-bipolar transistors ("IGBT"), and insulated-gate field-effect transistors ("IGFET"). In some

embodiments, the first IC device comprises an audio amplifier and the second IC device comprises a low drop-out device (LDO).

[0015] The semiconductor package **100** contains a substrate **102** on which the other components of the semiconductor package are located. The substrate can be any low-cost, recycleable material such as steel, stainless steel, or any steel alloy known in the art. The substrate **102** can be configured with any shape and size consistent with its use in the semiconductor package **100**. The substrate **102** can have any thickness that provides the needed support for the device. In some embodiments, such as where the substrate **102** comprises stainless steel, it may have a non-limiting thickness ranging from about 0.15 millimeters to about 0.25 millimeters.

[0016] In some embodiments, the substrate **102** has the shape illustrated in the Figures since it contains an area to which multiple land pads **116** are attached. In turn, the bottom of the first die **112** is then connected to the land pads **116**. Due to the overlap of the surfaces of the die attach pad area and the first die **112**, the die attach pad area can act as both a thermal and/or an electrical conductor. Such a configuration also permits the substrate lands **116** to dissipate the heat generated by the IC devices, increasing the efficiency of the heat dissipation from the semiconductor package **100**. As described herein, the land pads **116** can also be used to bond or attach the second die **114** to the substrate **102**.

[0017] In some embodiments, the land pads **116** can also serve as leads for the semiconductor package. In these embodiments, the substrate **102** is removed or peeled-off after molding process but with the land pads **116** retained on the molded body. Thus, the ends of the land pads **116** serve as the terminals **106**. Accordingly, the lay-out of the land pads **116** and the terminals **106** are substantially similar. In other embodiments, though, the land pads **116** and the terminals **106** are formed separate from each other and a redistribution layer can be used to change the lay-out from the land pads to the terminals.

[0018] In some embodiments, the land pads **116** can comprise any bonds pads known in the semiconductor art. For example, the landing pads could comprise a metal stud and a reflowed solder material or metal deposit like Au, Ni, Ag, or combinations of these materials.

[0019] The semiconductor package **100** also contains connectors **120** that are used to connect the landing pads to the second die **114**. In some embodiments, the connectors **120** comprise an array of metal strips that can be used as interposers. The metal strips used as connectors can contain any conductive metal or metal alloy that are similar to standard leadframe known in the art, including Cu, Ni—Pd, Ni—Pd—Au, or Ni—Pd—Au/Ag. In some embodiments, the metal strips comprise Cu. The array of metal strips can be configured to substantially match the desired connection points in the second die **114**. Thus, for the semiconductor package **100** illustrated in FIGS. **1-2**, the array of Cu strips are configured to be substantially in the form of a column. While the connectors **120** are depicted in the Figures as being substantially square, other shapes can be used including substantially rectangular, circular, or any known geometrical shapes.

[0020] The first and second dies, the upper surface of the substrate **102**, and the connectors **120** can be encapsulated in any molding material **130** known in the art, as shown in FIG. **1**. In some embodiments, the molding material can comprise an epoxy molding compound, a thermoset resin, a thermoplastic material, or potting material. In other embodiments, the molding material comprises an epoxy molding compound. In FIGS. **1-2**, the molding material **130** is shown in phantom to better illustrate the internal components of semiconductor package **100**.

[0021] Other embodiments of the semiconductor packages are illustrates in FIGS. **3-4**. In these Figures, the semiconductor package **200** contains components substantially similar to those described for semiconductor package **100**, including substrate **102**, first die **112**, landing pads **116**, and molding material **130**. But in these embodiments, the semiconductor package **200** contains a different configuration of terminals (labeled as **206**) on the bottom of the package **200**. As well, the number of terminals **206** are fewer than the number of terminals **106** that are contained in the embodiments depicted in FIGS. **1-2**.

[0022] As well, the semiconductor package **200** also contains a second die **214** that is different than the second die **114**. This second die **214** is relatively smaller than the second die **114** depicted in FIG. **1** and so has been labeled **214**. In some configurations, the second die **214** can be about the same size as the first die **114**, smaller, or even slightly larger. In yet other configurations, the top die can be substantially smaller than the inner distance between the external leads **216**.

[0023] Because the second die **214** is not significantly larger than the first die, the connectors **120** depicted in FIG. **1** cannot be used for the second die **214**. Rather, connectors **220** are used in the semiconductor package **200**. As shown in FIG. **3**, connectors **220** are configured to contain a first portion that extends away from the landing pads **216**. Thus, this first portion is substantially similar in size to the landing pages **216**. The connectors **220** also contain a second portion that extends from the first potion towards the area above the first die **112**. In the embodiments depicted in FIGS. **3-4**, the second portion can be given a finger-like configuration. In some configurations, the design and size of the interposing connectors can be different since they depend on the die size.

[0024] To support the second portion, the first portion of the connectors **220** is configured to be longer in width and length than the connectors **120**. And to properly support the larger first portion of the connectors **220**, the semiconductor package **200** contains landing pads **216** which are correspondingly larger that the landing pads **116** depicted in FIG. **1**.

[0025] The semiconductor packages **100** and **200** can be made using any known process that provides the structures described above. In some embodiments, the methods described herein can be used. The method begins, as illustrated in FIG. **5**, by providing the substrate **102**. The substrate can be provided by metal stamping or etching a frame of the desired material (i.e., stainless steel) to contain multiple lands or terminals. The substrates can be peeled-off after the molding process used to form the semiconductor package.

[0026] Next, or at the same time, the first and second dies containing their IC devices are manufactured using any known processes. In some embodiments, the first and second IC devices can be manufactured separately in the first and second dies. But in other embodiments, the first and second IC devices are manufactured in their respective dies at the same time.

[0027] As shown in FIG. **5**, the landing pads **116** are formed on the substrate **102** using any process known in art. In some embodiments, the landing pads can be formed by depositing the material and then etching the undesired portions of that material, thereby forming the landing pads **116** with the desired shape. Of course, for the landing pads **216**, less mate-

rial is etched so that larger landing pads are formed, as illustrated in FIG. **3** and FIG. **7** (which does not show the substrate **102**). The terminals (**106** or **206**) are formed using any known process.

[0028] Next, as shown in FIG. **6**, the first die **112** containing the first IC device is then attached to the landing pads **116** using any known flip-chip process which does not use wirebonding. One example of these processes includes solder bumping, which may include the use of solder bumps, balls, studs, and combinations thereof along with a solder paste, followed by a cure and reflow process. Another example of these processes includes the use of a conductive adhesive between the the substrate terminals **116** substrate **102** and the first IC device. The conductive adhesive may be, for example, a conductive epoxy, a conductive film, a screen printable solder paste, or a solder material, such as a lead-containing solder or a lead-free solder. In some embodiments, this attachment is performed by a chip-on-lead (COL) with wirebonding process. For the semiconductor package **200**, the resulting structure after this attachment process (when solder bumps **122** are used) is shown in FIG. **7**.

[0029] Next, as shown in FIG. **8**, the connectors are attached to those landing pads which remain exposed after the first die **112** has been attached. This process can be performed using any known technique. In the embodiments illustrated in FIG. **8**, the connectors **120** are formed by mounting array of connectors using any known conductive adhesives in the art. In the embodiments illustrated in FIG. **9**, the connectors **220** are formed by stamping or etching or a combination of both. And in the embodiments illustrated in FIG. **10**, the connectors **320** are formed in a similar manner, but with a different configuration so that they can support a smaller second die. This configuration generally has the second portion of the connectors formed closer together than the configuration shown in FIG. **9**.

[0030] The second (or upper) die is then attached to the connectors. This process can be carried out using any known flip-chip process which does not use wirebonding. One example of these attachment processes include solder bumping, which may include the use of solder bumps, balls, studs, and combinations thereof along with a solder paste, followed by a cure and reflow process. Another example of these processes includes the use of a conductive adhesive between the connector and the second die. The conductive adhesive may be, for example, a conductive epoxy, a conductive film, a screen printable solder paste, or a solder material, such as a lead-containing solder or a lead-free solder. In some embodiments, this attachment is performed by a chip-on-lead (COL) with wirebonding process.

[0031] The resulting structure from attaching the second die is shown in FIGS. **11-13**. For the embodiments in FIG. **11** (where the second die is larger than the first die), the second die **114** has been attached to the connectors **120**. For the embodiments in FIG. **12** (where the second die is substantially the same size as the first die), the second die **214** has been attached to the connectors **220**. And for the embodiments in FIG. **13** (where the second die is smaller than the first die), the second die **314** has been attached to the connectors **320**. FIG. **14** depicts a side view of the structure illustrated in FIG. **11** with bumps **124** shown to connect the second die **114** to the connectors **120**. And FIG. **15** depicts a side view of the structures illustrated in FIGS. **12** and **13** with bumps **122** shown to connect the first die **112** to the landing pads **116** and bumps **224** shown to connect the second die **214** (or **314**) to the connectors **220** (or **320**).

[0032] After the second die has been attached to the respective connectors, the molding material **130** is then formed around the substrate **102**, first and second dies, and the connectors by any known encapsulation process, including potting, transfer molding, or injection. In some embodiments, the encapsulation process does not require any underfill. The resulting semiconductor package (such as those illustrated in FIGS. **1-4**) is then optionally marked, trimmed, formed, and singulated using processes known in the art.

[0033] The semiconductor packages formed from this process contain two dies with IC devices that are isolated from each other because the molding material is contained between them. This configuration serves to separates the dies. In this configuration, since there is no direct contact between the dies, their respective thermal stability is easier to maintain and heat is dissipated quicker.

[0034] The above semiconductor packages have a reduced size while at the same time also keeping the stacked dies isolated. In some embodiments, the thickness of the semiconductor packages can be less than about 1 mm. In other embodiments, the thickness of the semiconductor packages can range from about 0.8 mm to about 1 mm.

[0035] In some embodiments, the semiconductor packages can be configured to contain more than 2 stacked dies. The additional dies can be incorporated by including additional land pads on which additional connectors (**120**, **220**, or **320** depending on the size of the additional die) can be located. Then, the additional dies can be attached to the additional connectors by using a flip-chip process similar to those described above.

[0036] In addition to any previously indicated modification, numerous other variations and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of this description, and appended claims are intended to cover such modifications and arrangements. Thus, while the information has been described above with particularity and detail in connection with what is presently deemed to be the most practical and preferred aspects, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, form, function, manner of operation and use may be made without departing from the principles and concepts set forth herein. Also, as used herein, examples are meant to be illustrative only and should not be construed to be limiting in any manner.

1. A semiconductor package, comprising:
multiple land pads;
a first die connected to a first portion of the lands pads without wirebonding;
an array of connectors connected to a second portion of the land pads; and
a second die connected to the array of connectors without wirebonding, wherein the second die is isolated from the first die.

2. The semiconductor package of claim **1**, wherein the first die contains a first integrated circuit device and the second die contains a second integrated circuit device.

3. The semiconductor package of claim **1**, wherein the second die does not contact the first die.

4. The semiconductor package of claim **3**, wherein the semiconductor package has a thickness less than about 1 mm.

5. The semiconductor package of claim **4**, wherein the semiconductor package has a thickness ranging from about 0.8 mm to about 1 mm.

6. The semiconductor package of claim **1**, wherein the first die is smaller than the second die and the connectors are substantially columnar in shape.

7. The semiconductor package of claim **1**, wherein the first die is substantially the same size or smaller than the second die and the connectors contain a first portion extending away from the landing pads and a second portion extending towards the second die.

8. The semiconductor package of claim **1**, further comprising a molding material encapsulating the connectors and the first and second dies.

9. The semiconductor package of claim **1**, wherein the multiple land pads terminate in terminals for the package.

10. A semiconductor package, comprising:

multiple land pads;

a first die containing a first integrated circuit device and connected to a first portion of the lands pads without wirebonding;

an array of connectors connected to a second portion of the land pads; and

a second die containing a second integrated circuit device and connected to the array of connectors without wirebonding, wherein the second die is isolated from the first die and does not contact the first die.

11. The semiconductor package of claim **10**, wherein the semiconductor package has a thickness less than about 1 mm.

12. The semiconductor package of claim **11**, wherein the semiconductor package has a thickness ranging from about 0.8 mm to about 1 mm.

13. The semiconductor package of claim **10**, wherein the first die is smaller than the second die and the connectors are substantially columnar in shape.

14. The semiconductor package of claim **10**, wherein the first die is substantially the same size or smaller than the second die and the connectors contain a first portion extending away from the landing pads and a second portion extending towards the second die.

15. The semiconductor package of claim **10**, further comprising a molding material encapsulating the connectors and the first and second dies.

16. The semiconductor package of claim **10**, wherein the multiple land pads terminate in terminals for the package.

17. A method for making semiconductor package, comprising:

providing multiple land pads;

connecting a first die to a first portion of the lands pads without using wirebonding;

connecting an array of connectors to a second portion of the land pads; and

connecting a second die to the array of connectors without using wirebonding and without contacting the second die to the first die.

18. The method of claim **17**, further including providing the semiconductor package with a thickness less than about 1 mm.

19. The method of claim **18**, wherein the semiconductor package has a thickness ranging from about 0.8 mm to about 1 mm.

20. The method of claim **17**, wherein the first die is smaller than the second die and the connectors are substantially columnar in shape.

21. The method of claim **17**, wherein the first die is substantially the same size or smaller than the second die and the connectors contain a first portion extending away from the landing pads and a second portion extending towards the second die.

22. The method of claim **1**, further comprising encapsulating a molding material around the connectors and the first and second dies.

23. A method for making semiconductor package having a thickness less than about 1 mm, comprising:

providing a substrate;

forming multiple land pads on the substrate by a deposition and etch procedure;

connecting a first die to an inner portion of the lands pads by using a flip chip procedure without using wirebonding;

connecting an array of connectors to an outer portion of the land pads;

connecting a second die to the array of connectors by using a flip chip procedure without using wirebonding, wherein the second die rests on the connectors without contacting the first die;

encapsulating a molding material around the connectors and the first and second dies without underfilling; and

removing the substrate.

24. The method of claim **23**, wherein the first die is smaller than the second die and the connectors are substantially columnar in shape.

25. The method of claim **23**, wherein the first die is substantially the same size or smaller than the second die and the connectors contain a first portion extending away from the landing pads and a second portion extending towards the second die.

* * * * *