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Description

FIELD OF THE INVENTION

[0001] Various example embodiments relates to transistors including an oxide semiconductor layer.

BACKGROUND OF THE INVENTION

[0002] Oxide semiconductor devices including a transparent semiconductor material having a wide bandgap of 3.0 eV or greater have been studied for many years. The oxide semiconductor devices are mass-produced as driving devices for large-area OLED TVs.

[0003] As the degree of device integration of semiconductor devices increases, the devices are required or desired to be smaller. In the case of a transistor, as a size thereof is reduced, a channel length may decrease. A decrease in the channel length of the transistor may cause or may exacerbate a short channel effect that results in a shift of a threshold voltage. Document US10734378B2 discloses a transistor in which changes in threshold voltage caused by a reduction on the physical size of said transistor are prevented.

SUMMARY OF THE INVENTION

[0004] Provided are transistors having improved operation reliability.

[0005] However, problems to be solved are not limited to the above disclosure. Additional aspects will be set forth in part in the description which follows and, in part, will be apparent from the description, and/or may be learned by practice of various example embodiments.

[0006] According to a claimed embodiment, a transistor as defined by claim 1 includes an oxide semiconductor layer; a source electrode and a drain electrode on the oxide semiconductor layer and spaced apart from each other; a gate electrode spaced apart from the oxide semiconductor layer; a gate insulating layer between the oxide semiconductor layer and the gate electrode; and a graphene layer between the gate electrode and the gate insulating layer and doped with a metal.

[0007] The metal doped in the graphene layer may be different from a metal included in the oxide semiconductor layer.

[0008] The metal doped into the graphene layer may include at least one of ruthenium (Ru), aluminum (Al), titanium (Ti), thallium (Tl), platinum (Pt), tantalum (Ta), rhodium (Rh), iridium (Ir), cobalt (Co), and tungsten (W).

[0009] The metal may be doped in an amount of 0.2 at% or more and 5 at% or less with respect to a total amount of the graphene layer.

[0010] A work function of the graphene layer may be 4.9 eV or more and 5.1 eV or less.

[0011] A threshold voltage of the transistor may be a positive value when a current flowing from the drain electrode to the source electrode is 10^{-12}A/micron.

[0012] A thickness of the graphene layer may be less than a thickness of the gate electrode.

[0013] The thickness of the graphene layer may be 10 nm or less.

[0014] The oxide semiconductor layer may include at least one of In, Zn, Sn, Ga, and Hf.

[0015] The graphene layer may be in contact with two or more surfaces of the gate electrode.

[0016] The graphene layer may be in contact with a lower surface of the gate electrode and a side surface of the gate electrode.

[0017] The gate insulating layer may at least partially cover two or more surfaces of the gate electrode.

[0018] The gate insulating layer may at least partially cover a lower surface of the gate electrode and a side surface of the gate electrode.

[0019] The gate insulating layer may be in contact with at least one of the source electrode and the drain electrode.

[0020] At least one of the source electrode and the drain electrode may include a stepped shape.

[0021] At least one of the source electrode and the drain electrode may include a first region having a first thickness and a second region having a second thickness less than the first thickness, wherein the second region may be closer to the gate electrode than the first region.

[0022] The source electrode, the drain electrode, and the gate insulating layer may be on a same surface of the oxide semiconductor layer.

[0023] The source electrode and the drain electrode may be on a first surface of the oxide semiconductor layer, and the gate insulating layer may be on a second surface, different from the first surface of the oxide semiconductor layer.

[0024] The gate insulating layer may include a first gate insulating layer in contact with a first surface of the oxide semiconductor layer and a second gate insulating layer in contact with a second surface, different from the first surface of the oxide semiconductor layer. The gate electrode may include a first gate electrode on the first gate insulating layer and a second gate electrode on the second gate insulating layer. The graphene layer may include a first graphene layer between the first gate insulating layer and the first gate electrodes and a second graphene layer between the second gate insulating layer and the second gate electrode.

[0025] The source electrode, the oxide semiconductor layer, and the drain electrode may be sequentially arranged in one direction.

[0026] The gate insulating layer may entirely surround a side surface of the oxide semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The above and other aspects, features, and advantages of certain embodiments of the disclosure will be more apparent from the following description taken in

conjunction with the accompanying drawings, in which:

FIG. 1 is a diagram illustrating a transistor according to various example embodiments;
FIG. 2 shows results of measuring a work function of a material according to various example embodiments;
FIG. 3 shows results of measuring IV characteristics of a transistor according to various example embodiments;
FIG. 4 is a diagram illustrating a transistor having a top gate structure according to another embodiment;
FIG. 5 is a diagram illustrating a transistor having a bottom gate structure according to various example embodiments;
FIG. 6 is a diagram illustrating a transistor having a double gate structure according to various example embodiments;
FIG. 7 is a diagram illustrating a transistor having a vertical channel structure according to various example embodiments;
FIG. 8 is a diagram illustrating a transistor having a gate-all-around structure according to various example embodiments;
FIG. 9 is a diagram illustrating a transistor according to another embodiment;
FIG. 10 shows a memory device including the aforementioned transistor as a switching element and a data storage device connected to the switching element; and
FIG. 11 illustrates a memory device in which a plurality of memory devices of FIG. 10 are vertically stacked.

DETAILED DESCRIPTION

[0028] Reference will now be made in detail to various embodiments, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout. In this regard, example embodiments may have different forms and should not be construed as being limited to the descriptions set forth herein. Accordingly, example embodiments are merely described below, by referring to the figures, to explain aspects. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. Expressions such as "at least one of," when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list.

[0029] Example embodiments are described in detail with reference to the accompanying drawings. In the following drawings, like reference numerals refer to like components, and the size of each component in the drawings may be exaggerated for clarity and convenience of description. The embodiments described herein are merely examples, and various modifications may be made from these embodiments.

[0030] When it is described that a certain component is "above" or "on" another component, the certain component may be directly above another component, or a third component may be interposed therebetween. The singular expressions include plural expressions unless the context clearly dictates otherwise. When a part "includes" a component, it may indicate that the part does not exclude another component but may further include another component, unless otherwise stated. The use of the terms "a" and "an" and "the" and similar referents may cover both the singular and the plural.

[0031] FIG. 1 is a diagram illustrating a transistor 10 according to various example embodiments. Referring to FIG. 1, the transistor 10 may be disposed on or in a substrate SUB. The transistor 10 may include an oxide semiconductor layer 110, a source electrode 120 and a drain electrode 130 disposed on the oxide semiconductor layer 110 and spaced apart from each other, a gate electrode 140 disposed to be spaced apart from the oxide semiconductor layer 110, and a gate insulating layer 150 disposed between the oxide semiconductor layer 110 and the gate electrode 140.

[0032] The substrate SUB may be provided in a flat plate shape extending along one surface thereof. The substrate SUB may include a material for forming a device, and a material having good or excellent mechanical strength and/or dimensional stability may be selected. The material of the substrate SUB may include, but is not limited to, a glass plate, a metal plate, a ceramic plate, or plastic (a polycarbonate resin, a polyester resin, an epoxy resin, a silicone resin, a fluorine resin, etc.).

[0033] A first interlayer insulating layer (e.g., a first interlayer dielectric (ILD1)) may be disposed on the substrate SUB. The oxide semiconductor layer 110 may be disposed on the first interlayer insulating layer ILD1. As an example, the oxide semiconductor layer 110 may be provided in the form of an ultra-thin film. For example, a thickness of the oxide semiconductor layer 110 may be 30 nm or less. The oxide semiconductor layer 110 according to an example may include metal elements of group 12, 13 and 14 such as zinc (Zn), indium (In), gallium (Ga), tin (Sn), cadmium (Cd), germanium (Ge), or hafnium (Hf), and oxides of materials selected from one or combinations thereof. For example, the oxide semiconductor layer 110 may be formed of a Zn oxide-based material, such as one or more of Zn oxide, In-Zn oxide, Ga-In-Zn oxide, or the like. As an example, the oxide semiconductor layer 110 may be provided as a single-layer or as a multi-layer structure.

[0034] The source electrode 120 and the drain electrode 130 may be disposed on the oxide semiconductor layer 110 and spaced apart from each other. The source electrode 120 and the drain electrode 130 may be disposed on the same surface of the oxide semiconductor layer 110. The source electrode 120 and the drain electrode 130 may include an electrically conductive material. For example, the source electrode 120 and the drain electrode 130 may include a metal and/or a metal com-

pound, and may include the same, or different materials.

[0035] The gate electrode 140 may be disposed between the source electrode 120 and the drain electrode 130 on the oxide semiconductor layer 110. The gate electrode 140, the source electrode 120, and the drain electrode 130 may be disposed on the same surface of the oxide semiconductor layer 110. According to some example embodiments, the gate electrode 140 may include an electrically conductive material. For example, the gate electrode 140 may include a metal and/or a metal compound.

[0036] The gate insulating layer 150 may be disposed between the oxide semiconductor layer 110 and the gate electrode 140 to electrically disconnect the oxide semiconductor layer 110 and the gate electrode 140. For example, the gate insulating layer 150 may include a ferroelectric material. As an example, the ferroelectric material may include at least one of an oxide ferroelectric material, a polymer ferroelectric material, a fluoride ferroelectric material such as BaMgF4 (BMF), and/or a ferroelectric material semiconductor.

[0037] The transistor 10 including the oxide semiconductor layer 110 has a wide bandgap of 3.0 eV or greater. In addition, the transistor 10 including the oxide semiconductor layer 110 may reduce an OFF-current, have a low subthreshold swing (SS), and/or have a high ON/OFF ratio.

[0038] When such a transistor 10 is applied as a driving element of an electronic device, for example, a display device, a short-channel effect due to scaling down may exist or be pronounced, varying performance. Typically, a length of the transistor 10 may be reduced, so it may be difficult to control a threshold voltage. In general, in the process of forming other components of the transistor 10 after the oxide semiconductor layer 110 is formed, a conductivity of the oxide semiconductor layer 110 may increase due to the influence of a process such as plasma damage and/or an increase in the hydrogen (H) concentration. As a result, a threshold voltage of the transistor 10 may be reduced. Alternatively or additionally, when he transistor 10 is driven in a high temperature, high voltage state, the threshold voltage may be shifted to a negative value due to migration of hydrogen.

[0039] The transistor 10 according to various example embodiments includes a graphene layer 160 doped with, and/or having incorporated therein, a metal between the gate insulating layer 150 and the gate electrode 140. The metal may be interstitially within the graphene, and/or may be substitutional within the graphene; example embodiments are not limited thereto.

[0040] The metal doped in the graphene layer 160 may be different from a metal included in the oxide semiconductor layer 110. For example, the metal doped in the graphene layer 160 may include at least one of ruthenium (Ru), aluminum (Al), titanium (Ti), thallium (TI), platinum (Pt), tantalum (Ta), rhodium (Rh), iridium (Ir), cobalt (Co), and tungsten (W). The metal may be doped in an amount of about 0.2 at% or more, 0.5 at% or more, 2 at% or more, 3 at% or more, 4 at% or less, or 5 at% or less with respect to a total amount of the metal-doped graphene layer 160 A thickness of the graphene layer 160 may be less than a thickness of the gate electrode 140. The thickness of the graphene layer 160 may be about 10 nm or less.

[0041] The metal-doped graphene layer 160 may increase a work function to increase the threshold voltage of the transistor 10. An ideal threshold voltage V_T of the transistor 10 may be expressed as in Equation 1 below.

[Equation 1]

$$V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$$

[0042] Here, $\Phi ms = \Phi m - \Phi s$ represents a difference between a work function Φm of the gate electrode 140 and a work function Φs of the oxide semiconductor layer 110, Ci represents capacitance of the gate insulating layer 150, Qi represents the amount of charges in the gate insulating layer 150, Qd represents the amount of deflation charges in the gate insulating layer 150, and Φf represents a Fermi level of the oxide semiconductor layer 110.

[0043] According to Equation 1, in general, the threshold voltage V_T of the transistor 10 may increase when Ci is large, for example, when one or more of the gate insulating layer 150 is high-k, the thickness of the gate insulating layer 150 is small, or the work function of the gate electrode 140 is large.

[0044] In general, W or TiN may be used for the gate electrode 140. A work function of W or TiN may be about 4.3 to 4.65 eV. Meanwhile, an undoped graphene layer may have a work function of about 4.65 eV, which is greater than that of a metal. If the graphene layer is doped with or has incorporated therein a metal, the grapheme layer may have a higher work function. For example, a graphene layer doped with Ru has a work function of 4.9 to 5.1 eV, and thus may have a higher work function of about 0.5 eV than a gate electrode including a metal material. Therefore, when the metal-doped graphene layer 160 having a high work function is disposed between the gate insulating layer 150 and the gate electrode 140, the metal-doped graphene layer 160 may serve as the gate electrode 140, thereby increasing the threshold voltage of the transistor 10.

[0045] Alternatively or additionally, the graphene layer 160 may prevent or reduce the amount of or impact from material diffusion between the layers. Hydrogen is a dopant of an oxide semiconductor, and when the content of hydrogen in the oxide semiconductor layer 110 increases, the threshold voltage of the oxide semiconductor layer 110 decreases. During a thin film deposition and/or a heat treatment process of the transistor 10, hydrogen may be introduced into the oxide semiconductor layer 110, and during high-temperature driving of the

transistor 10, hydrogen may be introduced into the oxide semiconductor layer 110 due to bias stress. The introduced hydrogen lowers the threshold voltage of the oxide semiconductor layer 110. For example, in order to increase thermal stability and reliability of device driving, it is necessary or desirable to prevent or reduce hydrogen from diffusing into the oxide semiconductor layer 110. Because carbon atoms of graphene have a small bonding length and are bound by strong covalent bonds, the carbon atoms may act as a diffusion barrier that effectively prevents or reduces material diffusion. Accordingly, by forming the graphene layer 160 on the gate insulating layer 150, hydrogen diffusing from the gate electrode 140 may be or at least partially be properly blocked, thereby improving the reliability of the threshold voltage control.

[0046] For example, the metal-doped transistor 10 according to various example embodiments has a large work function, so that the metal-doped transistor 10 may serve as a barrier to prevent or reduce material diffusion, while serving as the gate electrode 140, thereby improving the reliability of driving of the transistor.

[0047] The metal-doped graphene layer 160 may be in contact with two or more surfaces of the gate electrode 140. For example, the metal-doped graphene layer 160 may be in contact with a lower surface and side surfaces of the gate electrode 140. The metal-doped graphene layer 160 may effectively prevent or reduce the material of the gate electrode 140 from diffusing to the outside.

[0048] The gate insulating layer 150 may also cover two or more surfaces of the gate electrode 140. For example, the gate insulating layer 150 may be disposed on the lower surface and side surfaces of the gate electrode 140. The gate insulating layer 150 may insulate the gate electrode 140 from the oxide semiconductor layer 110 as well as insulate the gate electrode 140, the source electrode 120, and the drain electrode 130. Thus, a length or a channel length of the oxide semiconductor layer 110 may be reduced.

[0049] The source electrode 120 and the drain electrode 130 may include a stepped shape. For example, the source electrode 120 may include a first source electrode 121 having a first thickness and a second source electrode 122 having a second thickness less than the first thickness, and the second source electrode 122 may be disposed closer to the gate electrode 140 than the first source electrode 121. The source electrode 120 having a stepped shape may reduce formation of parasitic capacitance between the gate electrode 140 and the source electrode 120, while securing or helping to secure a contact area with the oxide semiconductor layer 110.

[0050] The drain electrode 130 may have a symmetrical structure with the source electrode 120 with respect to the gate electrode 140. For example, the drain electrode 130 may include a first drain electrode 131 having a first thickness and a second drain electrode 132 having a second thickness less than the first thickness, and the second drain electrode 132 may be disposed closer to the gate electrode 140 than the first drain electrode 130. The drain electrode 130 having a stepped shape may reduce formation of a parasitic capacitance between the gate electrode 140 and the source electrode 120, while securing a contact area with the oxide semiconductor layer 110.

[0051] Alternatively or additionally, at least one of the source electrode 120 and the drain electrode 130 may be in contact with even the gate insulating layer 150. Thus, the transistor 10 may be integrated, while reducing the length of the oxide semiconductor layer 110.

[0052] A second interlayer insulating layer ILD2 may fill a gap between the gate insulating layer 150 and the source electrode 120 and between the gate insulating layer 150 and the drain electrode 130. The second interlayer insulating layer ILD2 may electrically disconnect the oxide semiconductor layer 110, the gate electrode 140, the source electrode 120, and the drain electrode 130 from each other. As an example, the second interlayer insulating layer ILD2 may be in contact with the first interlayer insulating layer ILD1, and bury the oxide semiconductor layer 110, the gate insulating layer 150, the gate electrode 140, the source electrode 120, and the drain electrode 130.

[0053] FIG. 2 is results of measuring a work function of each material according to various example embodiments. Referring to FIG. 2, a work function of a material including TiN and Wwas about 4.3 eV or more and 4.65 eV or less, and a work function of graphene was about 4.5 eV or more and 4.65 eV or less. A work function of the graphene layer doped with a metalloid (e.g., As) and a non-metal (e.g., P) was about 4.7 eV or more and 4.8 eV or less. A work function of a graphene layer doped with a metal, for example, Ru, was about 4.9 eV or more and 5.1 eV or less.

[0054] When a graphene layer is added to the gate electrode, it may be expected that the work function increases. In particular, when a metal-doped graphene layer is added to the gate electrode, it may be expected that a work function exceeds 4.8 eV. A work function of the metal-doped graphene layer according to various example embodiments may be 4.8 eV or more and 5.3 eV or less. Alternatively, a work function of the metal-doped graphene layer according to various example embodiments is 4.9 eV or more and 5.1 eV or less.

[0055] FIG. 3 is results of measuring current-voltage (IV) characteristics of the transistor 10 according to various example embodiments. Example is IV characteristics of a transistor including a metal-doped graphene layer, and Comparative Example is IV characteristics of a transistor not including a metal-doped graphene layer. It can be seen that, when a current IDS flowing from the drain electrode 130 to the source electrode 120 is 10^{-12} A/μm or 10^{-12} A/micron, a threshold voltage of Example is a positive voltage, whereas a threshold voltage of Comparative Example is a negative voltage. Therefore, it can be seen that the threshold voltage may be maintained at a positive value even when the drain current is 10^{-12} A/μm by adding the metal-doped

graphene layer 160 to the gate electrode 140.

[0056] The metal-doped graphene layer may be applied to various types of transistors.

[0057] FIG. 4 is a diagram illustrating a transistor 10a having a top gate structure according to various example embodiments. Comparing FIG. 4 with FIG. 1, a source electrode 120a and a drain electrode 130a of the transistor 10a of FIG. 4 disposed to be spaced apart from each other on an oxide semiconductor layer 110a. In addition, a gate insulating layer 150a, a metal-doped graphene layer 160a, and a gate electrode 140a may be sequentially stacked on the oxide semiconductor layer 110a. The metal-doped graphene layer 160a may be disposed only on a lower surface of the gate electrode 140a, and the source electrode 120a and the drain electrode 130a may be disposed to be spaced apart from the gate insulating layer 150a. A length (e.g., a channel length) of the oxide semiconductor layer 110a of the transistor 10a of FIG. 4 may be longer than that of the transistor 10 of FIG. 1.

[0058] A metal doped in the graphene layer 160a may be different from a metal included in the oxide semiconductor layer 110a. For example, the metal doped into the graphene layer 160a may include at least one of ruthenium (Ru), aluminum (Al), titanium (Ti), thallium (Tl), platinum (Pt), tantalum (Ta), rhodium (Rh), iridium (Ir), cobalt (Co), and tungsten (W), and the oxide semiconductor layer 110a may be an oxide including at least one of In, Zn, Sn, Ga, and Hf. The metal may be doped in an amount of 0.2 at% or more, 0.5 at% or more, 2 at% or more, 3 at% or more, 4 at% or less, or 5 at% or less with respect to a total amount of the graphene layer 160a, and a thickness of the doped graphene layer 160a is less than a thickness of the gate electrode 140a. For example, the thickness of the graphene layer 160a may be about 10 nm or less.

[0059] FIG. 5 is a diagram illustrating a transistor 10b having a bottom gate structure according to various example embodiments. Comparing FIG. 5 with FIG. 2, a source electrode 120b and a drain electrode 130b of the transistor 10b of FIG. 5 may be disposed to be spaced apart from each other on an upper surface of an oxide semiconductor layer 110b, and a gate electrode 140b may be disposed on a lower surface of the oxide semiconductor layer 110b. A gate insulating layer 150b may be disposed between the oxide semiconductor layer 110b and the gate electrode 140b. A metal-doped graphene layer 160b may be disposed between the gate insulating layer 150b and the gate electrode 140b. The metal-doped graphene layer 160b may also be disposed on a side surface of the gate electrode 140b, as well as between the gate insulating layer 150b and the gate electrode 140b. Characteristics of each component have been described above, and thus, a detailed description thereof is omitted.

[0060] FIG. 6 is a diagram illustrating a transistor 10c having a double gate structure according to various example embodiments. Comparing FIG. 6 with FIG. 2, a gate insulating layer 150c may include a first gate insulating layer 151 disposed on an upper surface of an oxide semiconductor layer 110c and a second gate insulating layer 152 disposed on a lower surface of the oxide semiconductor layer 110. A gate electrode 140c may include a first gate electrode 141 disposed on an upper surface of the first gate insulating layer 151 and a second gate electrode 142 disposed on a lower surface of the second gate insulating layer 152. In addition, a graphene layer 160c may include a first graphene layer 161 disposed between the first gate insulating layer 151 and the first gate electrode 142 and a second graphene layer 162 disposed between the second gate insulating layer 152 and the second gate electrode 142. The first and second graphene layers 161 and 162 may be doped with a metal.

[0061] The metal doped in the graphene layer 160c may be different from a metal included in the oxide semiconductor layer 110c. For example, the metal doped in the graphene layer 160c may include at least one of ruthenium (Ru), aluminum (Al), titanium (Ti), thallium (Ti), platinum (Pt), tantalum (Ta), rhodium (Rh), iridium (Ir), cobalt (Co), and tungsten (W), and the oxide semiconductor layer 110c may be an oxide including at least one of In, Zn, Sn, Ga, and Hf. The metal may be doped in an amount of 0.2 at% or more, 0.5 at% or more, 2 at% or more, 3 at% or more, 4 at% or less, or 5 at% or less with respect to a total amount of the graphene layer 160c, and a thickness of the metal-doped graphene layer 160c is less than a thickness of the gate electrode 140c. For example, the thickness of the graphene layer 160c may be about 10 nm or less.

[0062] FIG. 7 is a diagram illustrating a transistor 10d having a vertical channel structure according to various example embodiments. Referring to FIG. 7, an oxide semiconductor layer 110d may have a structure extending in a thickness direction of the substrate SUB. A source electrode 120d may be disposed on an upper surface of the oxide semiconductor layer 110d, and a drain electrode 130d may be disposed on a lower surface of the oxide semiconductor layer 110d. However, various example embodiments are not limited thereto. The drain electrode 130d may be disposed on the upper surface of the oxide semiconductor layer 110d and the source electrode 120d may be disposed on the lower surface of the oxide semiconductor layer 110d. A gate insulating layer 150d and a gate electrode 140d may be disposed on a side surface of the oxide semiconductor layer 110d. In addition, the metal-doped graphene layer 160d may be disposed between the gate insulating layer 150d and the gate electrode 140d. The metal-doped graphene layer 160d may cover two or more surfaces of the gate electrode 140.

[0063] FIG. 8 is a diagram illustrating a transistor 10e having a gate-all-around structure according to various example embodiments. Referring to FIG. 8, an oxide semiconductor layer 110e may have a structure extending in a thickness direction of the substrate SUB. A source electrode 120e may be disposed on an upper surface of

the oxide semiconductor layer 110e and a drain electrode 130e may be disposed on a lower surface of the oxide semiconductor layer 110e. However, various example embodiments are not limited thereto. The drain electrode 130e may be disposed on an upper surface of the oxide semiconductor layer 110e and the drain electrode 130e may be disposed on a lower surface of the oxide semiconductor layer 110e.

[0064] A gate insulating layer 150e covering the entire side surface of the oxide semiconductor layer 110e and a gate electrode 140e covering the side surface of the gate insulating layer 150 may be further disposed. Also, the metal-doped graphene layer 160e may be disposed between the gate insulating layer 150e and the gate electrode 140e. The metal-doped graphene layer 160e may be disposed not only on the side surface of the gate electrode 140e but also on the upper and lower surfaces of the gate electrode 140e.

[0065] So far, the source electrode and the drain electrode in contact with one surface of the oxide semiconductor layer have been described. However, various example embodiments are not limited thereto. The source electrode and the drain electrode may be in contact with a plurality of surfaces of the oxide semiconductor layer to integrate the transistor.

[0066] FIG. 9 is a diagram illustrating a transistor 10f according to another embodiment. Referring to FIG. 9, the transistor 10f according to an example may include a substrate SUB, an oxide semiconductor layer 110f disposed on the substrate SUB, a source electrode 120f in contact with three or more surfaces of the oxide semiconductor layer 110f, a drain region 130f in contact with three or more surfaces of the oxide semiconductor layer 110f, a gate electrode 140f apart from the oxide semiconductor layer, and a gate insulating layer 150f disposed between the oxide semiconductor layer 110f and the gate electrode 140f.

[0067] The source electrode 120f may be disposed to contact three or more surfaces of the oxide semiconductor layer 110f. As an example, the source electrode 120f may include a first contact portion 123 in contact with the oxide semiconductor layer 110f and a first conductive plug 124 in contact with the first contact portion 123 and extending in one direction.

[0068] The first contact portion 123 may be disposed between the oxide semiconductor layer 110f and the first conductive plug 124 and may be in contact with the oxide semiconductor layer 110f on three or more surfaces. As described above, as a thickness h of the oxide semiconductor layer 110f decreases to an ultra-thin film, a thickness of an effective channel formed by a gate field may substantially be equal to a thickness of the physical oxide semiconductor layer 110f. A difference in charge concentration between a lower surface and an upper surface of the oxide semiconductor layer 110f is also reduced, so that a contact area in which the entire area of the oxide semiconductor layer 110f is in contact with the source electrode 120f and the drain region 130f may be formed.

[0069] As an example, when the oxide semiconductor layer 110f is provided in the form of a thin film extending along one plane, the first contact portion 123 may include a first lower contact layer 123-1 surrounding a portion of the lower surface of the oxide semiconductor layer 110f, a first upper contact layer 123-2 surrounding a portion of the upper surface of the oxide semiconductor layer 110f, and a first side contact layer 123-3 surrounding one side surface of the oxide semiconductor layer 110f. The first lower contact layer 123-1 may be disposed to face the substrate SUB. The first upper contact layer 123-2 may be disposed to face the first lower contact layer 123-1 with the oxide semiconductor layer 110f interposed therebetween. As an example, the first upper contact layer 123-2 may be provided to contact one end of the first conductive plug 124. The first side contact layer 123-3 may be disposed between the first lower contact layer 123-1 and the first upper contact layer 123-2 to connect the first lower contact layer 123-1 to the first upper contact layer 123-2.

[0070] Like the source electrode 120f, the drain electrode 130f may also contact three or more surfaces of the oxide semiconductor layer 110f. As an example, the drain electrode 130f may include a second contact portion 133 in contact with the oxide semiconductor layer 110f and a second conductive plug 134 in contact with the second contact portion 133 and extending in one direction.

[0071] The second contact portion 133 may be disposed between the oxide semiconductor layer 110f and the second conductive plug 134 and may contact the oxide semiconductor layer 110f on three or more surfaces. As described above, as the thickness of the oxide semiconductor layer 110f decreases to an ultra-thin film, a thickness of an effective channel formed by a gate field may substantially be equal to the thickness of the physical oxide semiconductor layer 110f. A difference in charge concentration between a lower surface and an upper surface of the oxide semiconductor layer 110f is also reduced, so that a contact area in which the lower surface and the upper surface of the oxide semiconductor layer 110f are in contact with the drain electrode 130f and the drain region 130f may be formed.

[0072] As an example, when the oxide semiconductor layer 110f is provided in the form of a thin film extending along one plane, the second contact portion 133 may include a second lower contact layer 133-1 surrounding a portion of the lower surface of the oxide semiconductor layer 110f, a second upper contact layer 133-2 surrounding a portion of the upper surface of the oxide semiconductor layer 110f, and a second side contact layer 133-3 surrounding one side of the oxide semiconductor layer 110f. The second lower contact layer 133-1 may be disposed to face the substrate SUB. The second upper contact layer 133-2 may be disposed to face the second lower contact layer 133-1 with the oxide semiconductor layer 110f interposed therebetween. As an example, the second upper contact layer 133-2 may be provided to contact one end of the second conductive plug 134. The

second side contact layer 133-3 may be disposed between the second lower contact layer 133-1 and the second upper contact layer 133-2 to connect the second lower contact layer 133-1 to the second upper contact layer 133-1.

[0073] The transistor 10f includes a metal-doped graphene layer 160f between the gate electrode 140f and the gate insulating layer 150f.

[0074] A metal doped in the graphene layer 160f may be different from a metal included in the oxide semiconductor layer 110f. For example, the metal doped in the graphene layer 160f may include at least one of ruthenium (Ru), aluminum (Al), titanium (Ti), thallium (Ti), platinum (Pt), tantalum (Ta), rhodium (Rh), iridium (Ir), cobalt (Co), and tungsten (W), and the oxide semiconductor layer 110f may be an oxide including at least one of In, Zn, Sn, Ga, and Hf. The metal may be doped in an amount of 0.2 at% or more, 0.5 at% or more, 2 at% or more, 3 at% or more, 4 at% or less, or 5 at% or less with respect to a total amount of the graphene layer 160f, and a thickness of the doped graphene layer 160f is less than a thickness of the gate electrode 140f. For example, the thickness of the graphene layer 160f may be about 10 nm or less.

[0075] FIG. 10 shows a memory device 1000 using the aforementioned transistor as a switching element and including a data storage element connected to the switching element. In an example, the transistor 100 of FIG. 1, among the transistors described above, may be used as a switching element.

[0076] Referring to FIG. 10, the memory device 1000 includes a data storage element 1100 on the interlayer insulating layer ILD. The data storage element 1100 may cover the entire upper surface of the drain electrode 130 and may be in direct contact with the upper surface. The data storage element 1100 may include a capacitor, a ferroelectric capacitor, and a magnetic tunnel junction (MTJ) cell. The memory device 1000 may be a volatile memory device, such as DRAM, or a nonvolatile memory device, such as FRAM, MRAM, ReRAM, or the like, depending on the data storage element 1100.

[0077] FIG. 11 illustrates a memory device 2000 in which a plurality of memory cells MC1 of FIG. 10 are vertically stacked.

[0078] Referring to FIG. 11, a memory logic layer 2620 controlling an operation of the memory device 2000 is disposed on a substrate 2600, and a memory cell array 2640 is provided on the memory logic layer 2620. The memory cell array 2640 includes a plurality of vertically stacked memory cells MC1. In an example, the memory cell MC1 may be the memory device 1000 of FIG. 10.

[0079] In the above, the transistor including a metal-doped graphene layer has been illustrated and described, but various example embodiments are not limited to the specific exemplary embodiments described above, and may be variously modified by those skilled in the art to which the present invention pertains without departing from the scope of the present invention as claimed in the claims.

[0080] According to various example embodiments, a threshold voltage of a transistor may be increased by adding a graphene layer doped with a metal having a large work function.

[0081] The metal-doped graphene layer may serve as a barrier to improve the reliability of driving of the transistor.

[0082] However, the effect of various example embodiments are not limited to the above disclosure.

[0083] It should be understood that various example embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each embodiment should typically be considered as available for other similar features or aspects in other example embodiments, and embodiments are not necessarily mutually exclusive. While one or more embodiments have been described with reference to the figures, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the scope as defined by the following claims.

Claims

1. A transistor comprising:

   an oxide semiconductor (110) layer;
   a source electrode (120) and a drain electrode (130) spaced apart from each other on the oxide semiconductor layer;
   a gate electrode (140) spaced apart from the oxide semiconductor layer;
   a gate insulating layer (150) between the oxide semiconductor layer and the gate electrode; and
   characterised by a graphene layer (160) between the gate electrode and the gate insulating layer and doped with a metal.

2. The transistor of claim 1, wherein the metal doped in the graphene layer is different from a metal included in the oxide semiconductor layer.

3. The transistor of claim 1 or 2, wherein the metal doped into the graphene layer includes at least one of ruthenium (Ru), aluminum (Al), titanium (Ti), platinum (Pt), thallium (Tl), tantalum (Ta), rhodium (Rh), iridium (Ir), cobalt (Co), and tungsten (W).

4. The transistor of claim 1, 2 or 3, wherein the metal is doped into the graphene layer in an amount of 0.2 at% or more and 5 at% or less with respect to a total amount of the graphene layer.

5. The transistor of any preceding claim, wherein a work function of the graphene layer is greater or

equal to 4.9 eV or and less than or equal to 5.1 eV.

6. The transistor of any preceding claim, wherein a threshold voltage of the transistor is positive when a current flowing from the drain electrode to the source electrode is 10^{-12}A/micron.

7. The transistor of any preceding claim, wherein a thickness of the graphene layer is less than a thickness of the gate electrode.

8. The transistor of any preceding claim, wherein a thickness of the graphene layer is less than or equal to 10 nm.

9. The transistor of any preceding claim, wherein the graphene layer is in contact with two or more surfaces of the gate electrode, and optionally wherein the graphene layer is in contact with a lower surface of the gate electrode and a side surface of the gate electrode.

10. The transistor of any preceding claim, wherein the gate insulating layer at least partially covers two or more surfaces of the gate electrode.

11. The transistor of any preceding claim, wherein the gate insulating layer at least partially covers a lower surface of the gate electrode and a side surface of the gate electrode.

12. The transistor of any preceding claim, wherein at least one of the source electrode and the drain electrode includes a first region having a first thickness and a second region having a second thickness less than the first thickness, and the second region is closer to the gate electrode than the first region.

13. The transistor of any preceding claim, wherein the source electrode and the drain electrode are on a first surface of the oxide semiconductor layer, and the gate insulating layer is on a second surface, different from the first surface of the oxide semiconductor layer.

14. The transistor of any preceding claim, wherein

the gate insulating layer includes a first gate insulating layer in contact with a first surface of the oxide semiconductor layer and a second gate insulating layer in contact with a second surface different from the first surface of the oxide semiconductor layer,
the gate electrode includes a first gate electrode on the first gate insulating layer and a second gate electrode on the second gate insulating layer, and
the graphene layer includes a first graphene layer between the first gate insulating layer and the first gate electrodes and a second graphene layer disposed between the second gate insulating layer and the second gate electrode.

15. The transistor of any preceding claim, wherein the gate insulating layer entirely surrounds a side surface of the oxide semiconductor layer.

Patentansprüche

1. Transistor, umfassend:

eine Oxidhalbleiterschicht (110);
eine Source-Elektrode (120) und eine Drain-Elektrode (130), die auf der Oxidhalbleiterschicht voneinander beabstandet sind;
eine Gate-Elektrode (140), die von der Oxidhalbleiterschicht beabstandet ist,
eine Gate-Isolierschicht (150) zwischen der Oxidhalbleiterschicht und der Gate-Elektrode; und
gekennzeichnet durch eine Graphenschicht (160) zwischen der Gate-Elektrode und der Gate-Isolierschicht und mit einem Metall dotiert.

2. Transistor nach Anspruch 1, wobei sich das Metall, das in der Graphenschicht dotiert ist, von einem Metall unterscheidet, das in der Oxidhalbleiterschicht enthalten ist.

3. Transistor nach Anspruch 1 oder 2, wobei das Metall, das in die Graphenschicht dotiert ist, zumindest eines von Ruthenium (Ru), Aluminium (Al), Titan (Ti), Platin (Pt), Thallium (Tl), Tantal (Ta), Rhodium (Rh), Iridium (Ir), Kobalt (Co) und Wolfram (W) beinhaltet.

4. Transistor nach Anspruch 1, 2 oder 3, wobei das Metall in die Graphenschicht in einer Menge von 0,2 at% oder mehr und 5 at% oder weniger in Bezug auf eine Gesamtmenge der Graphenschicht dotiert ist.

5. Transistor nach einem vorhergehenden Anspruch, wobei eine Arbeitsfunktion der Graphenschicht größer oder gleich 4,9 eV oder und weniger als oder gleich 5,1 eV ist.

6. Transistor nach einem vorhergehenden Anspruch, wobei eine Schwellenspannung des Transistors positiv ist, wenn ein Strom, der von der Drain-Elektrode zu der Source-Elektrode fließt, 10^{-12}A/Mikrometer ist.

7. Transistor nach einem vorhergehenden Anspruch, wobei eine Dicke der Graphenschicht weniger als eine Dicke der Gate-Elektrode ist.

8. Transistor nach einem vorhergehenden Anspruch, wobei eine Dicke der Graphenschicht weniger als oder gleich 10 nm ist.

9. Transistor nach einem vorhergehenden Anspruch, wobei die Graphenschicht in Kontakt mit zwei oder mehr Oberflächen der Gate-Elektrode ist und wobei optional die Graphenschicht in Kontakt mit einer unteren Oberfläche der Gate-Elektrode und einer Seitenoberfläche der Gate-Elektrode ist.

10. Transistor nach einem vorhergehenden Anspruch, wobei die Gate-Isolierschicht zwei oder mehr Oberflächen der Gate-Elektrode zumindest teilweise bedeckt.

11. Transistor nach einem vorhergehenden Anspruch, wobei die Gate-Isolierschicht eine untere Oberfläche der Gate-Elektrode und eine Seitenoberfläche der Gate-Elektrode zumindest teilweise bedeckt.

12. Transistor nach einem vorhergehenden Anspruch, wobei zumindest eine von der Source-Elektrode und der Drain-Elektrode einen ersten Bereich mit einer ersten Dicke und einen zweiten Bereich mit einer zweiten Dicke, die weniger als die erste Dicke ist, beinhaltet und der zweite Bereich näher an der Gate-Elektrode als der erste Bereich ist.

13. Transistor nach einem vorhergehenden Anspruch, wobei die Source-Elektrode und die Drain-Elektrode auf einer ersten Oberfläche der Oxidhalbleiterschicht sind und die Gate-Isolierschicht auf einer zweiten Oberfläche ist, die sich von der ersten Oberfläche der Oxidhalbleiterschicht unterscheidet.

14. Transistor nach einem vorhergehenden Anspruch, wobei

die Gate-Isolierschicht eine erste Gate-Isolierschicht in Kontakt mit einer ersten Oberfläche der Oxidhalbleiterschicht und eine zweite Gate-Isolierschicht in Kontakt mit einer zweiten Oberfläche, die sich von der ersten Oberfläche der Oxidhalbleiterschicht unterscheidet, beinhaltet,
die Gate-Elektrode eine erste Gate-Elektrode auf der ersten Gate-Isolierschicht und eine zweite Gate-Elektrode auf der zweiten Gate-Isolierschicht beinhaltet, und
die Graphenschicht eine erste Graphenschicht zwischen der ersten Gate-Isolierschicht und den ersten Gate-Elektroden und eine zweite Graphenschicht, die zwischen der zweiten Gate-Isolierschicht und der zweiten Gate-Elektrode angeordnet ist, beinhaltet.

15. Transistor nach einem vorhergehenden Anspruch, wobei die Gate-Isolierschicht eine Seitenoberfläche der Oxidhalbleiterschicht vollständig umgibt.

Revendications

1. Un transistor comprenant :

une couche semi-conductrice d'oxyde (110) ;
une électrode de source (120) et une électrode de drain (130) espacées l'une de l'autre sur la couche semi-conductrice d'oxyde ;
une électrode de grille (140) espacée de la couche semi-conductrice d'oxyde,
une couche isolante de grille (150) entre la couche semi-conductrice d'oxyde et l'électrode de grille ; et
caractérisé par une couche de graphène (160) entre l'électrode de grille et la couche isolante de grille et dopée avec un métal.

2. Transistor de la revendication 1, dans lequel le métal dopé dans la couche de graphène est différent d'un métal compris dans la couche semi-conductrice d'oxyde.

3. Transistor de la revendication 1 ou 2, dans lequel le métal dopé dans la couche de graphène comprend au moins l'un des éléments suivants : ruthénium (Ru), aluminium (Al), titane (Ti), platine (Pt), thallium (Tl), tantale (Ta), rhodium (Rh), iridium (Ir), cobalt (Co) et tungstène (W).

4. Transistor de la revendication 1, 2 ou 3, dans lequel le métal est dopé dans la couche de graphène en une quantité de 0,2 at% ou plus et de 5 at% ou moins par rapport à une quantité totale de la couche de graphène.

5. Transistor d'une quelconque revendication précédente, dans lequel une fonction de travail de la couche de graphène est supérieure ou égale à 4,9 eV ou inférieure ou égale à 5,1 eV.

6. Transistor d'une quelconque revendication précédente, dans lequel une tension de seuil du transistor est positive lorsqu'un courant circulant de l'électrode de drain à l'électrode de source est de 10^{-12} A/micron.

7. Transistor d'une quelconque revendication précédente, dans lequel une épaisseur de la couche de graphène est inférieure à une épaisseur de l'électrode de grille.

8. Transistor d'une quelconque revendication précédente, dans lequel une épaisseur de la couche de graphène est inférieure ou égale à 10 nm.

9. Transistor d'une quelconque revendication précédente, dans lequel la couche de graphène est en contact avec deux surfaces de l'électrode de grille ou plus, et éventuellement dans lequel la couche de graphène est en contact avec une surface inférieure de l'électrode de grille et une surface latérale de l'électrode de grille.

10. Transistor d'une quelconque revendication précédente, dans lequel la couche isolante de grille recouvre au moins partiellement deux surfaces de l'électrode de grille ou plus.

11. Transistor d'une quelconque revendication précédente, dans lequel la couche isolante de grille recouvre au moins partiellement une surface inférieure de l'électrode de grille et une surface latérale de l'électrode de grille.

12. Transistor d'une quelconque revendication précédente, dans lequel au moins l'une de l'électrode de source et de l'électrode de drain comprend une première région présentant une première épaisseur et une seconde région présentant une seconde épaisseur inférieure à la première épaisseur, et la seconde région est plus proche de l'électrode de grille que la première région.

13. Transistor d'une quelconque revendication précédente, dans lequel l'électrode de source et l'électrode de drain sont sur une première surface de la couche semi-conductrice d'oxyde, et la couche isolante de grille est sur une seconde surface, différente de la première surface de la couche semi-conductrice d'oxyde.

14. Transistor d'une quelconque revendication précédente, dans lequel

la couche isolante de grille comprend une première couche isolante de grille en contact avec une première surface de la couche semi-conductrice d'oxyde et une seconde couche isolante de grille en contact avec une seconde surface différente de la première surface de la couche semi-conductrice d'oxyde,
l'électrode de grille comprend une première électrode de grille sur la première couche isolante de grille et une seconde électrode de grille sur la seconde couche isolante de grille, et
la couche de graphène comprend une première couche de graphène entre la première couche isolante de grille et les premières électrodes de grille et une seconde couche de graphène disposée entre la seconde couche isolante de grille et la seconde électrode de grille.

15. Transistor d'une quelconque revendication précédente, dans lequel la couche isolante de grille entoure entièrement une surface latérale de la couche semi-conductrice d'oxyde.

FIG. 1

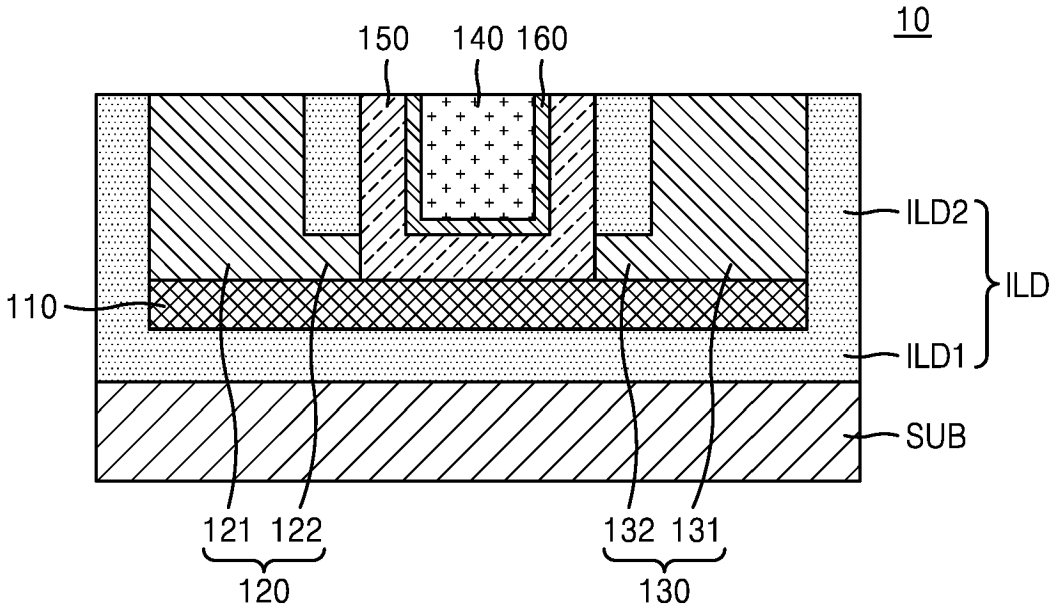


FIG. 2

Material	Work function (eV)
TiN, W	4.3~4.65
Graphene	4.5~4.65
As, P doped graphene	4.7~4.8
Ru-doped graphene	4.9~5.1

FIG. 3

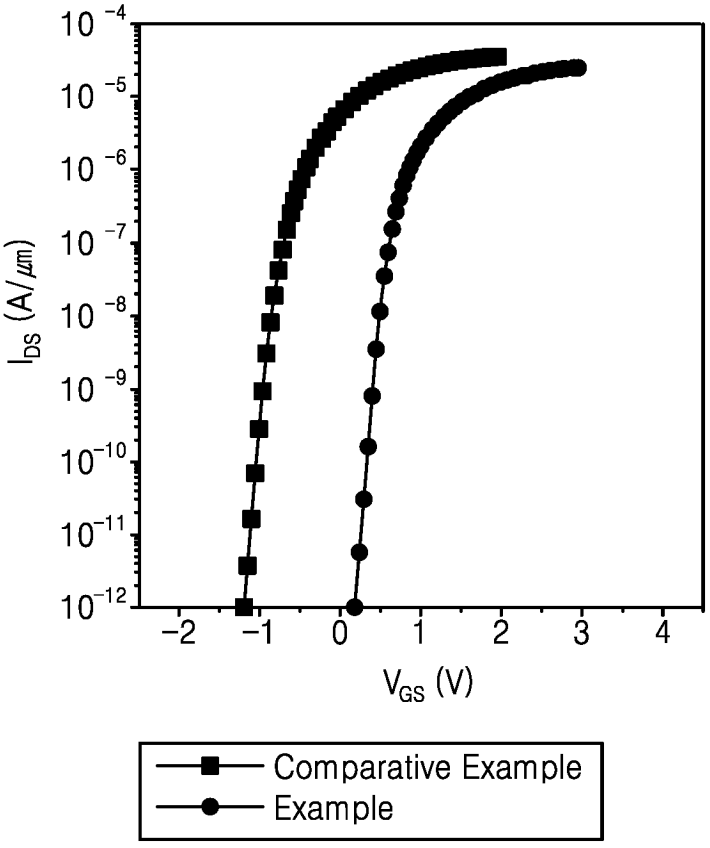

10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
I_{DS} (A/μm)
−2
−1
0
1
2
3
4
V_{GS} (V)
Comparative Example
Example

FIG. 4

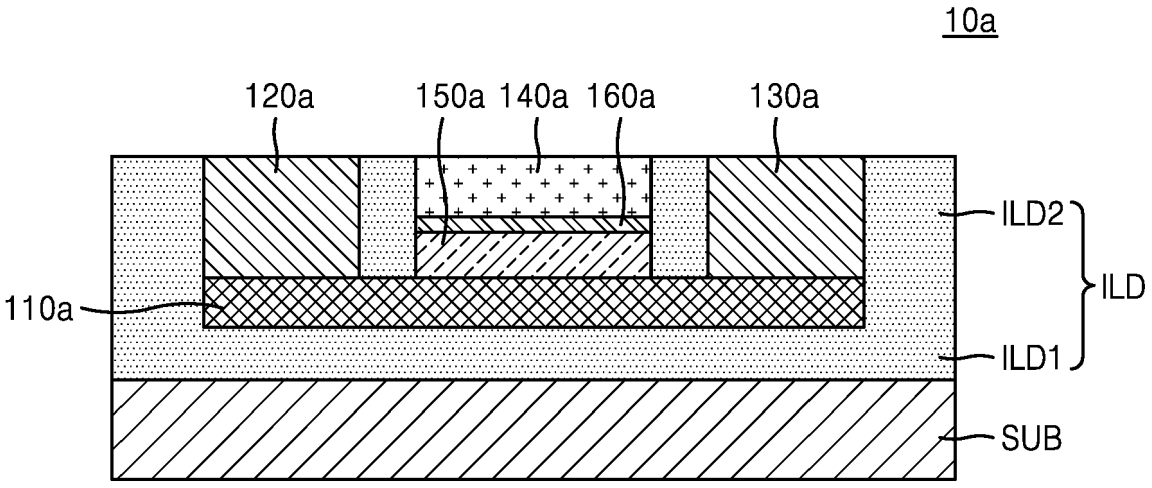


FIG. 5

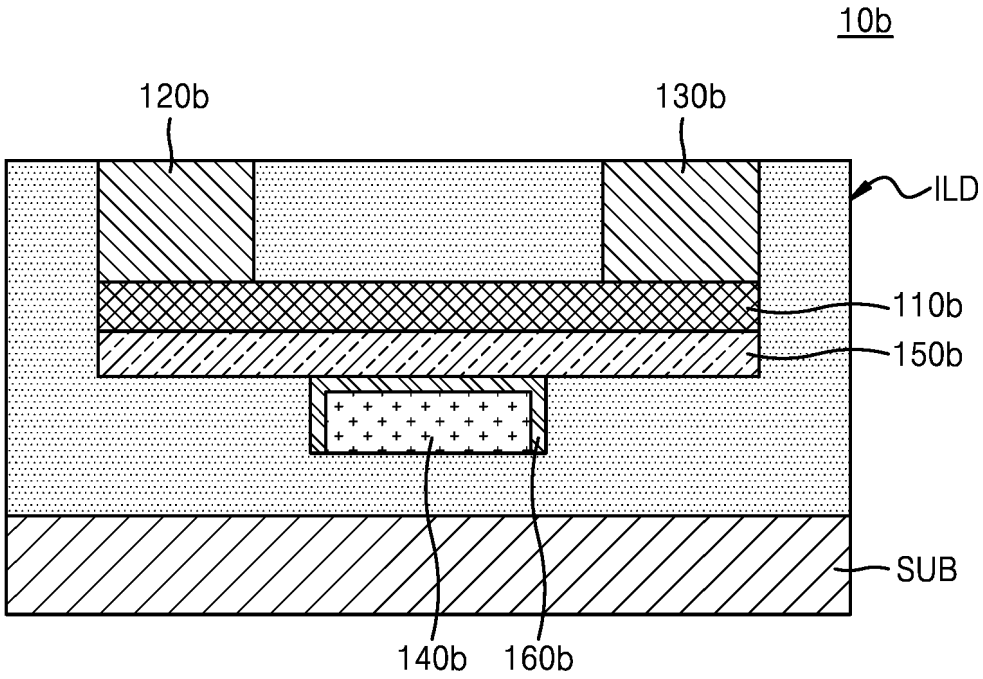


FIG. 6

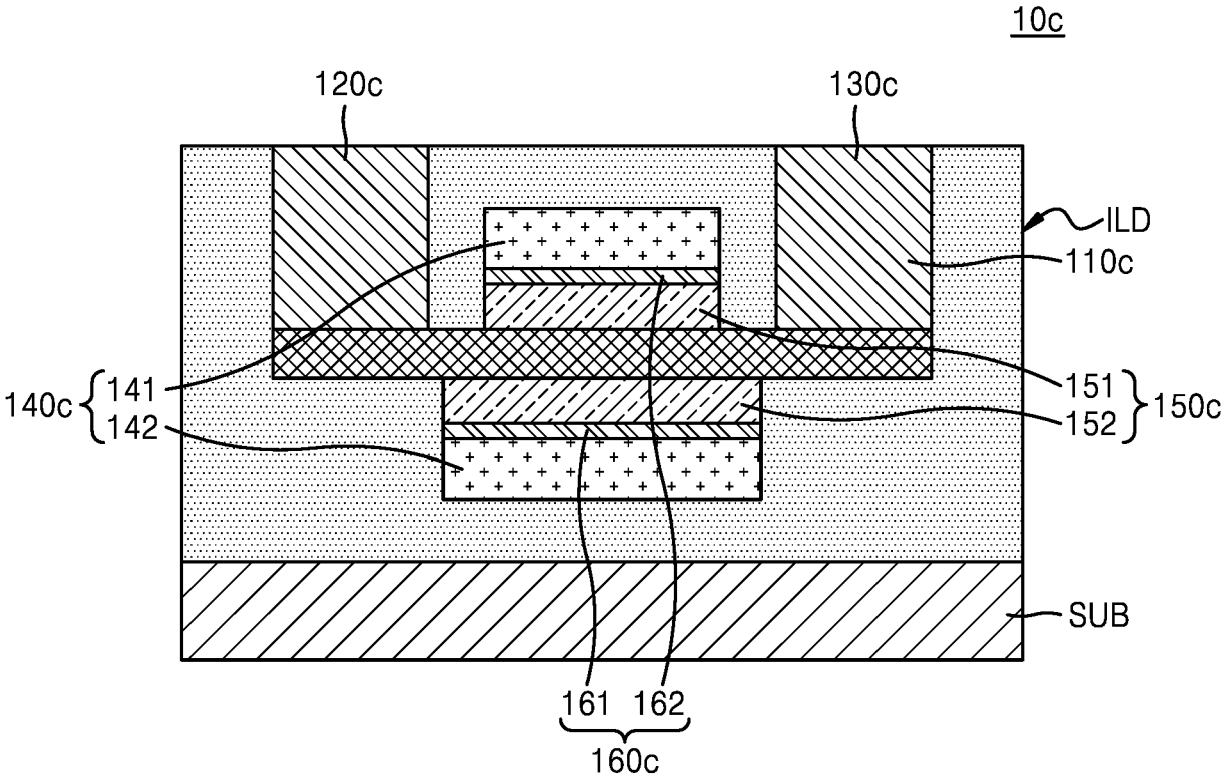

10c
120c
130c
ILD
110c
140c
141
142
151
152
150c
SUB
161
162
160c

FIG. 7

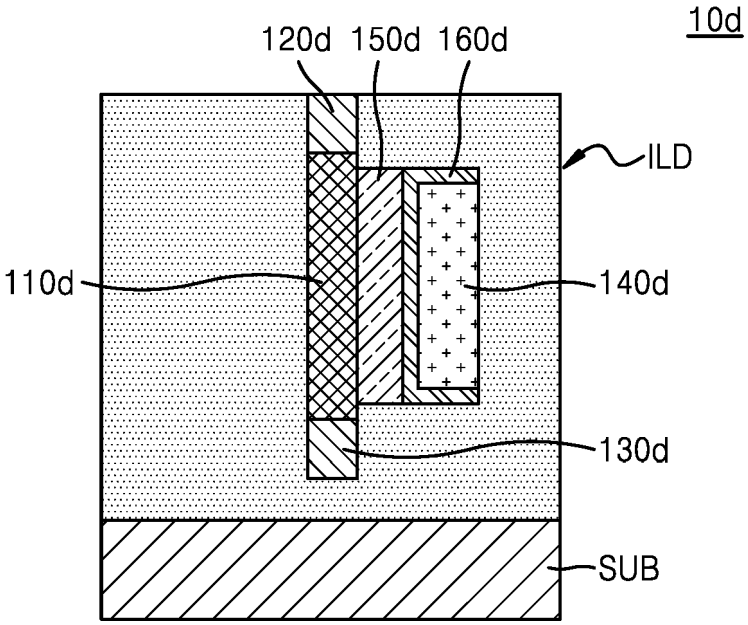


FIG. 8

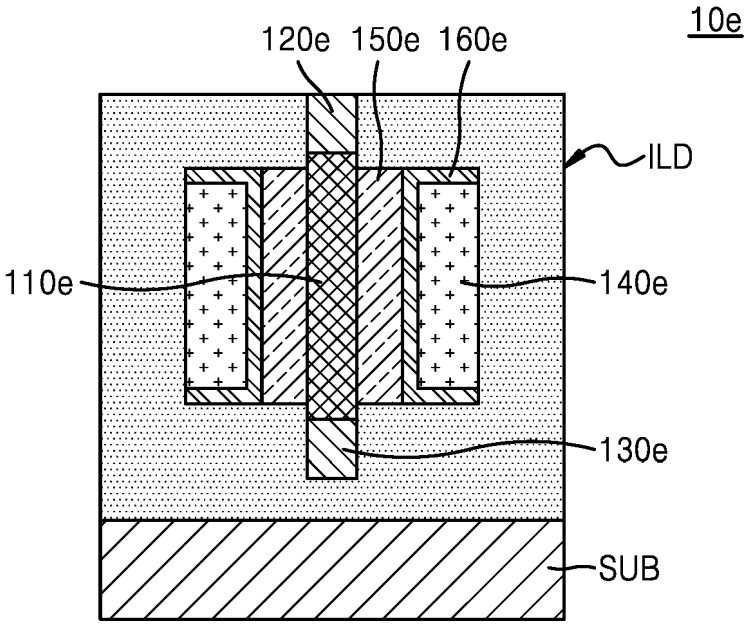


FIG. 9

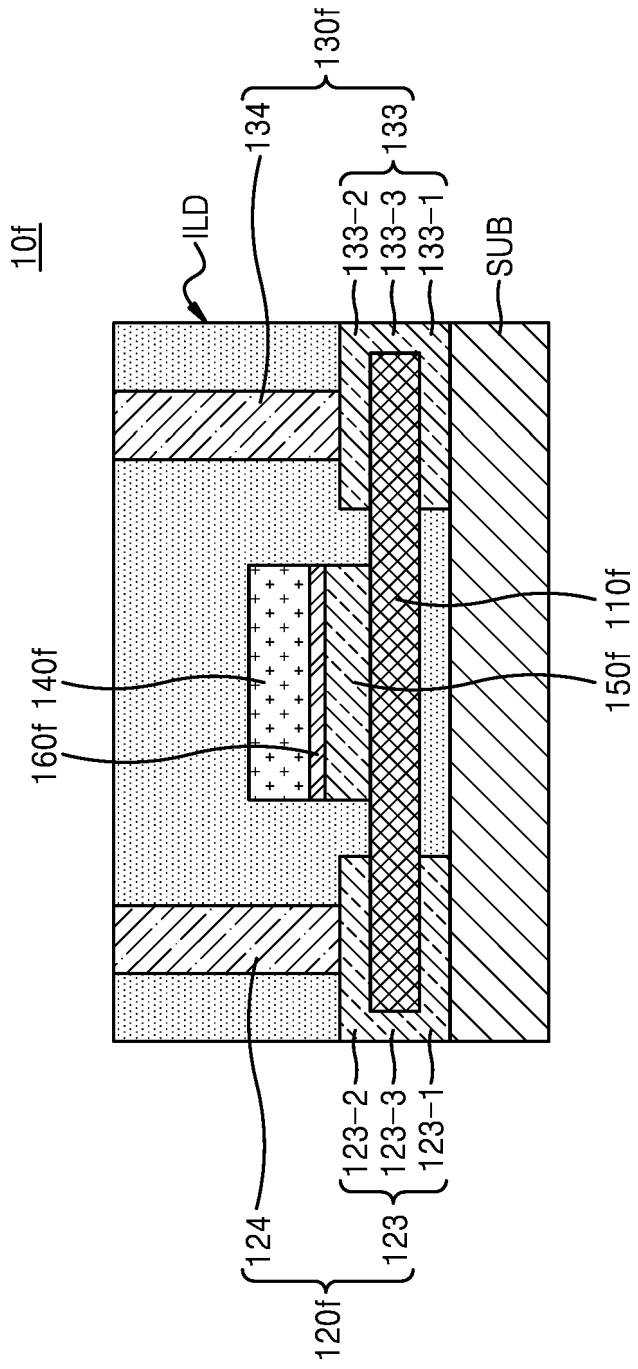

10f
ILD
134
130f
133
133-2
133-3
133-1
SUB
160f 140f
150f 110f
124
120f
123
123-2
123-3
123-1

FIG. 10

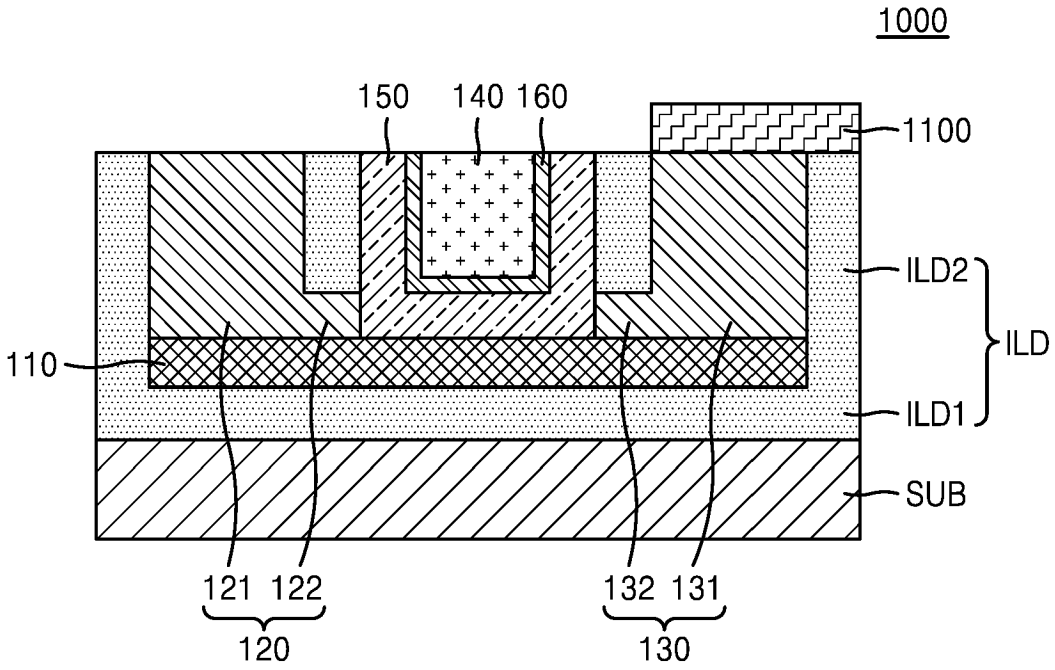
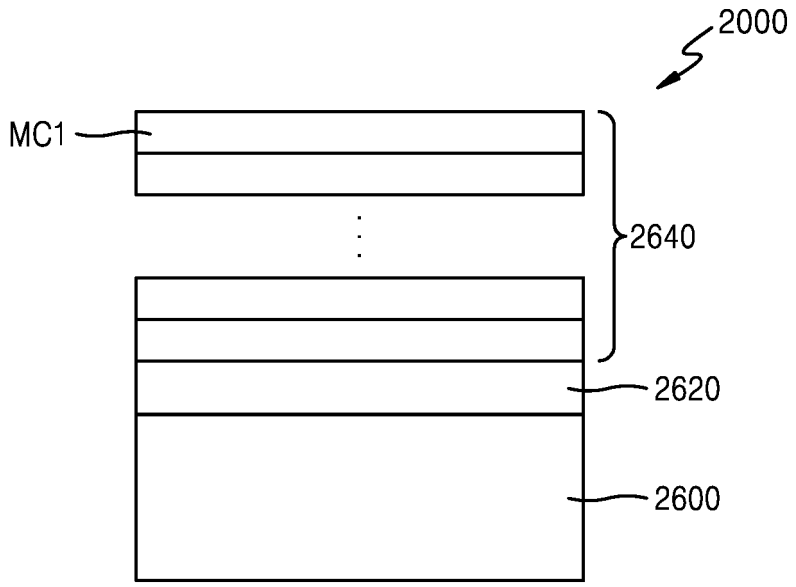

1000
150
140
160
1100
ILD2
ILD
110
ILD1
SUB
121
122
132
131
120
130

FIG. 11



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Patent documents cited in the description

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