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(54) METHOD AND COMPOSITE FOR DECREASING CHARGE LEAKAGE

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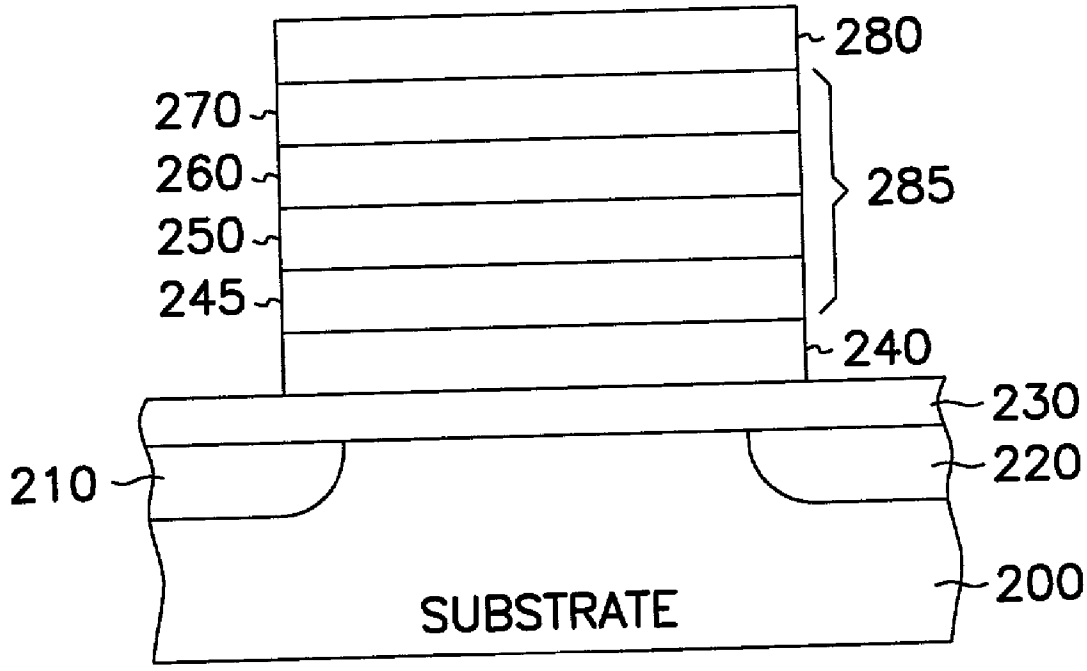
(57) ABSTRACT

A dielectric insulating composite for insulating a floating gate from a control gate in a non-volatile memory is described. A material, such as an undoped polysilicon, amorphous silicon, or amorphous polysilicon or a silicon rich nitride, is inserted in the gate structure. The oxide film that results from the oxidation of these films is relatively free from impurities. As a result, charge leakage between the floating gate and control gate is reduced.



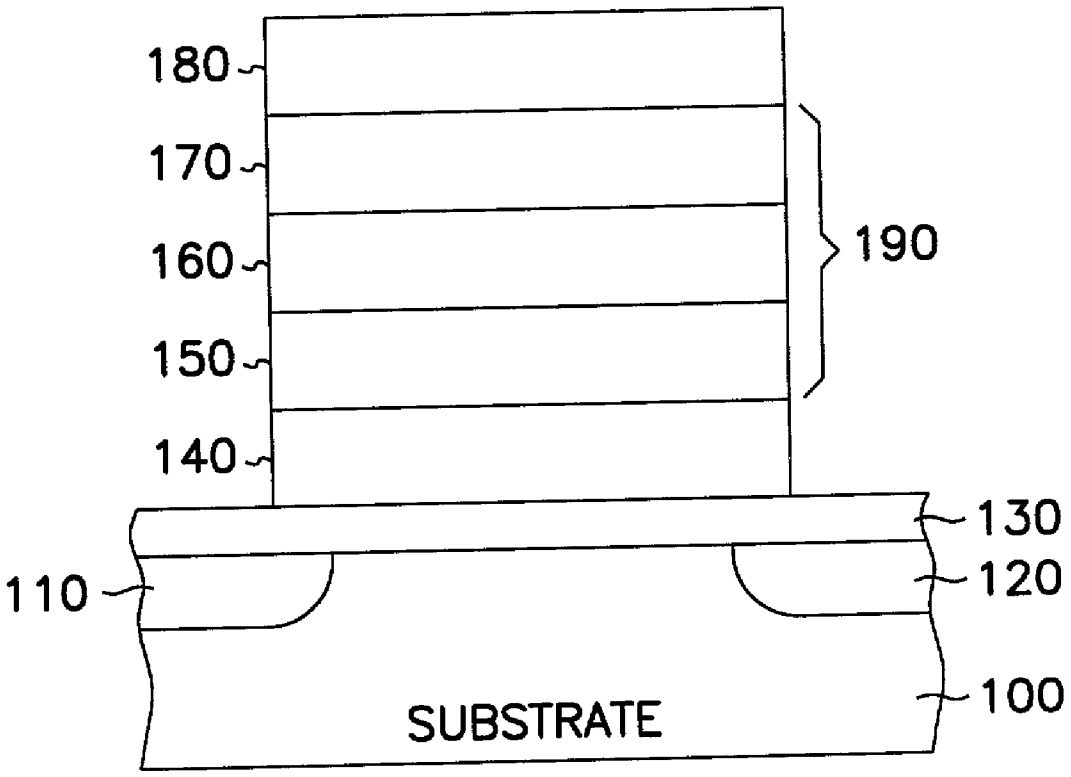


FIGURE 1 (PRIOR ART)

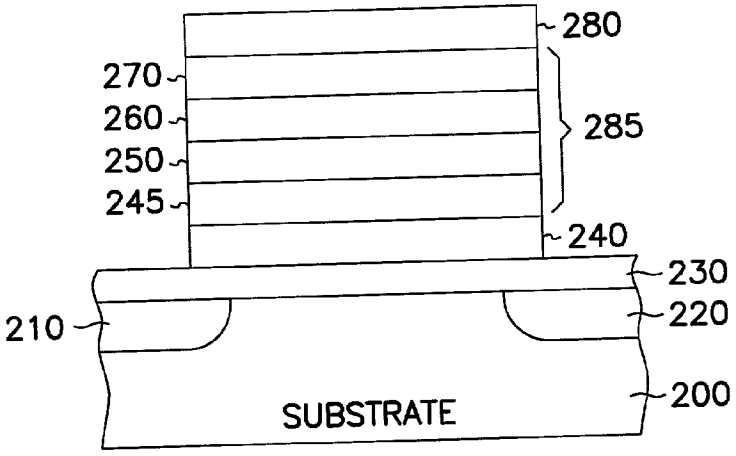


FIGURE 2

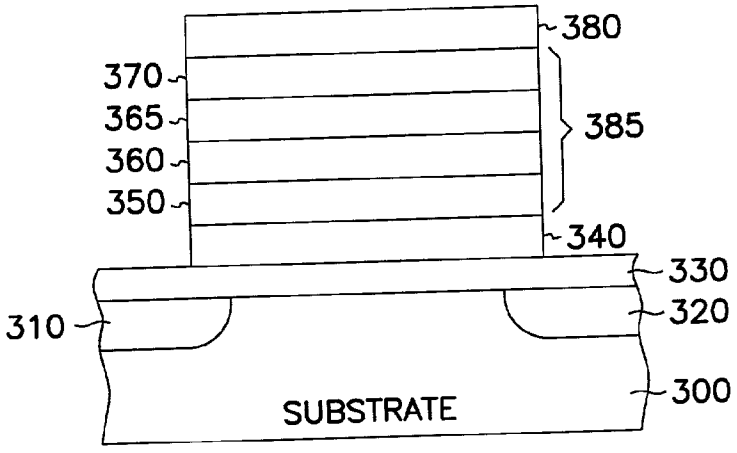


FIGURE 3

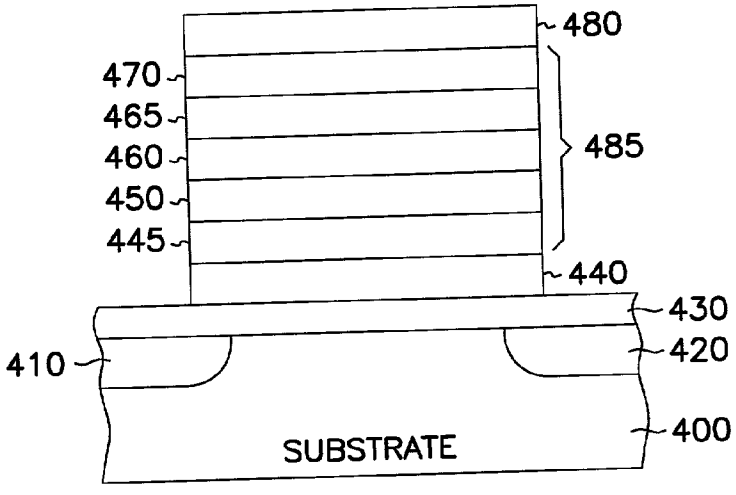


FIGURE 4

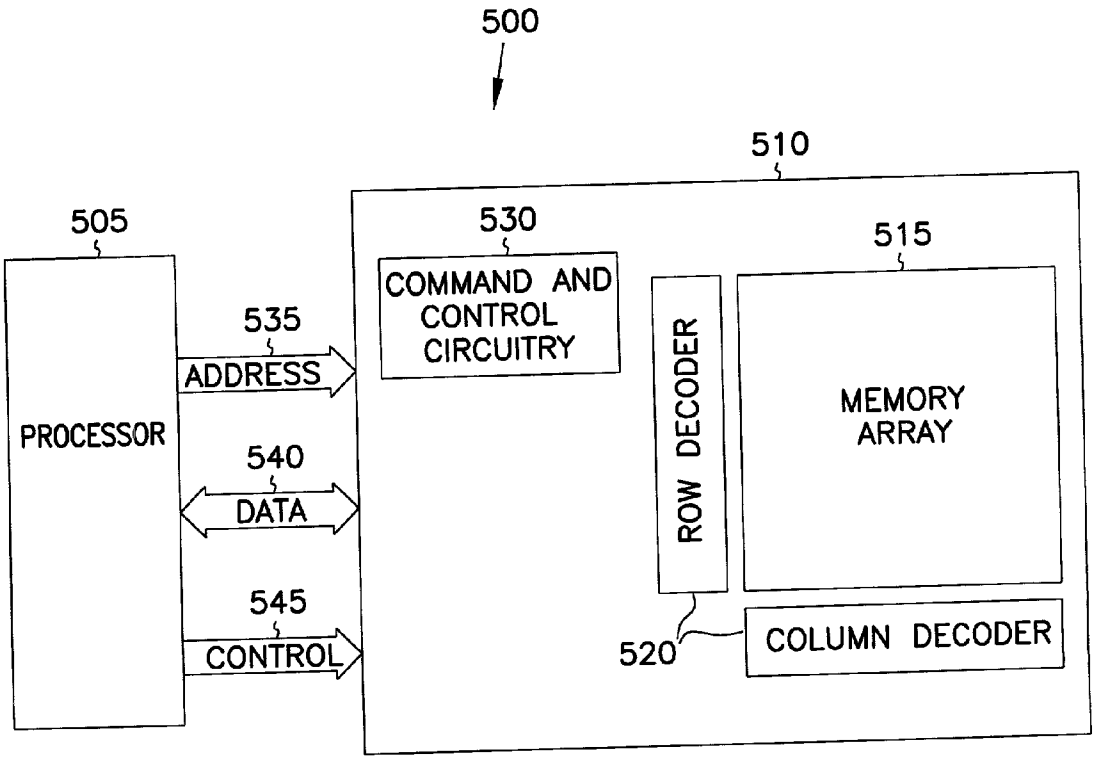

500
510
505
530
515
COMMAND AND CONTROL CIRCUITRY
535
ADDRESS
PROCESSOR
540
DATA
545
CONTROL
ROW DECODER
MEMORY ARRAY
520
COLUMN DECODER

FIGURE 5

METHOD AND COMPOSITE FOR DECREASING CHARGE LEAKAGE

FIELD OF THE INVENTION

[0001] This invention relates to the field of semiconductor memories, and more particularly to a method and manufacture for decreasing charge leakage in a non-volatile semiconductor memory.

BACKGROUND OF THE INVENTION

[0002] The demand for inexpensive, easily accessible and compact long term information storage systems continues to increase. In the past, the demand for long term information storage was met by archiving paper records. Today, however, the volume of information requiring storage makes this solution impractical. Recently, the demand for long term information storage has been met by magnetic media information storage systems and optical information storage systems. Although these systems have excellent long term information retention capability, in some applications they are not sufficiently compact. So, a current trend is to use non-volatile semiconductor memory for long term information storage.

[0003] Non-volatile semiconductor memory is compact and permits rapid access to the stored information. Information is stored in a non-volatile semiconductor memory as electronic charge. The magnitude of the electronic charge is used to represent a binary value. For instance, in some memory systems the presence of charge represents a binary one, and the absence of charge represents a binary zero. In other memory systems, a larger charge magnitude represents a binary one, and a smaller charge magnitude represents a binary zero. In either system, charge isolation is critical to successful long term information storage.

[0004] Charge isolation implies that once an electronic charge is located in a structure, the charge remains at that location indefinitely. In the art, charge is located in a structure such as a transistor having a control gate, a floating gate, a drain, a source, and a dielectric composite insulator interposed between the control gate and the floating gate. In operation, the control gate induces an electronic charge to locate at the floating gate. Once the charge is induced at the floating gate, for the transistor device to successfully operate as a long term information storage device, the charge must remain at the floating gate for a long period of time. As devices are scaled to create higher density memory, the thickness of the dielectric is reduced to maintain the same coupling. As the thickness is reduced, the ability to prevent electron migration through the insulator becomes difficult. The rate of this charge leakage defines the time that a non-volatile semiconductor memory can function as a long term information storage device.

[0005] To successfully substitute for magnetic or optical storage devices as a long term information storage device, a non-volatile semiconductor memory device, such as an EPROM, EEPROM, or a flash EPROM, must store information reliably for at least ten years, so any charge leakage from the floating gate is detrimental to the use of non-volatile semiconductor memory as a long term information storage device.

[0006] For these and other reasons there is a need for the present invention.

SUMMARY OF THE INVENTION

[0007] The above mentioned problems with charge leakage in memory cells and other problems are addressed by the present invention and will be understood by reading and studying the following specification. A method and composite for decreasing charge leakage is described.

[0008] The dielectric composite insulator of the present invention, by reducing the charge leakage from the floating gate to the control gate of a memory cell, provides for an improved non-volatile semiconductor memory cell. Reducing the charge leakage in a non-volatile semiconductor memory makes the memory a more viable long term information storage device.

[0009] A non-volatile semiconductor memory cell includes a semiconductor substrate, a source and drain formed on the semiconductor substrate, an insulator formed on the source and drain, a floating gate formed on the insulator, a composite formed on the floating gate and a control gate formed on the composite.

[0010] In one embodiment of the present invention, a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon is located between the floating gate and the layer of silicon dioxide. In an alternate embodiment of the present invention, a layer of silicon rich nitride is deposited on the layer of silicon nitride and then oxidized to form the silicon dioxide layer. In still another embodiment of the present invention, a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon is located between the floating gate and the silicon dioxide, and a layer of silicon rich nitride is located between the layer of silicon nitride and the silicon dioxide of the composite. The effect of interposing a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon, which in some designs is thin, or a layer of silicon rich nitride, which in some designs is thin, or both into the composite is to decrease the charge leakage from the floating gate to the control gate of the memory cell. A thin layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon is a layer having a thickness of less than about one-hundred angstroms, and a thin layer of silicon rich nitride is a layer having a thickness of less than about one-hundred angstroms.

[0011] Another embodiment of the present invention also includes a process for forming the dielectric insulating composite. In the art, the process for forming the composite comprises depositing a layer of silicon dioxide on the floating gate, depositing a layer of silicon nitride on the layer of silicon dioxide, and depositing a layer of silicon dioxide on the layer of silicon nitride. In the present invention, the process for forming the dielectric insulating composite comprises, in addition to the steps of the process for forming the composite, the steps of either depositing a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon or depositing a layer of silicon rich nitride, or both. In addition, in one embodiment of the process, after forming the floating gate by flowing silane and phosphine, the deposition of the layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon is accomplished by reducing the flow of phosphine. In an alternate embodiment of the process, after depositing a layer of silicon nitride formed on the layer of silicon dioxide by flowing dichlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia. And in still another

embodiment, after depositing the layer of silicon nitride formed on the layer of silicon dioxide by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] **FIG. 1** is a block diagram of a composite incorporated in a prior art memory cell.

[0013] **FIG. 2** is a block diagram of one embodiment of the composite of the present invention incorporated in a memory cell showing a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon added to the prior art memory cell.

[0014] **FIG. 3** is a block diagram of a second embodiment of the composite of the present invention incorporated in a memory cell showing a layer of silicon rich nitride added to the prior art memory cell.

[0015] **FIG. 4** is a block diagram of a third embodiment of the composite of the present invention incorporated in a memory cell showing a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon and a layer of silicon rich nitride added to the prior art memory cell.

[0016] **FIG. 5** is a block diagram of a system incorporating an embodiment of present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

[0018] In one embodiment of the present invention a composite acts as a dielectric in a memory cell of a non-volatile semiconductor memory. Referring to **FIG. 1, a** block diagram of a prior art memory cell for use in a non-volatile semiconductor memory is shown. The cell is a transistor comprising a semiconductor substrate **100**, a source **110**, a drain **120**, an insulating layer **130**, a floating gate **140**, a layer of silicon dioxide **150**, a layer of silicon nitride **160**, a second layer of silicon dioxide **170**, and a control gate **180**. Together, the layer of silicon dioxide **150**, the layer of silicon nitride **160**, and the second layer of silicon dioxide **170** make up a composite **190** that acts as a dielectric and as an insulator between the control gate **180** and the floating gate **140**. The layer of nitride **160** functions as a dielectric, and the silicon dioxide layers, the layer of silicon dioxide **150** and the second layer of silicon dioxide **170**, function as insulators.

[0019] In operation, a voltage at the control gate **180** induces a charge at the floating gate **140**. The charge represents stored information. A charge at the floating gate **140** is prevented from migrating or leaking into the semiconductor substrate **100** by the insulating layer **130**. However, as the composite **190** is reduced in thickness, it becomes a leakage path compared to insulating layer **130**, and charge leaks from the floating gate **140** to the control gate **180**. This leakage is admittedly small, but over time, as charge leaks from the floating gate **140**, the information stored at the floating gate **140** is lost. It is this leakage that limits the performance of prior art memory cells.

[0020] The process for forming the prior art composite **190** requires partially oxidizing the doped polysilicon of the floating gate **140** to form the layer of silicon dioxide **150**, depositing a layer of silicon nitride **160** by chemical vapor deposition on the layer of silicon dioxide **150**, and partially oxidizing the layer of silicon nitride **160**, under aggressive oxidation conditions, to form the second layer of silicon dioxide **170**. Oxidizing the doped polysilicon layer consumes the whole layer, while partially oxidizing the doped polysilicon layer consumes less than the whole layer. At the completion of this process, the layer of silicon dioxide **150** contains phosphorous from the doped polysilicon, and the second layer of silicon dioxide **170** contains nitrogen from the layer of silicon nitride **160**. The phosphorous and nitrogen are impurities that cause significant charge leakage through the silicon dioxide layers, when compared to the charge leakage exhibited by silicon dioxide layers free of phosphorous and nitrogen.

[0021] Referring to **FIG. 2, a** diagram of one embodiment of a memory cell for use in a non-volatile semiconductor memory is shown. The cell is a transistor comprising a semiconductor substrate **200**, a source **210**, a drain **220**, an insulating layer **230**, a floating gate **240**, a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **245**, a layer of silicon dioxide **250**, a layer of silicon nitride **260**, a second layer of silicon dioxide **270**, and a control gate **280**. Together, the layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **245**, the layer of silicon dioxide **250**, the layer of silicon nitride **260**, and the second layer of silicon dioxide **270** make up a composite **285** that acts as a dielectric and as an insulator between the control gate **280** and the floating gate **240**. The layer of nitride **260** functions as a dielectric, and the silicon dioxide layers, the layer of silicon dioxide **250** and the second layer of silicon dioxide **270**, function as insulators. Amorphous polysilicon is part silicon and part polysilicon.

[0022] A structural difference between the memory cell of **FIG. 1** and one embodiment of the present invention shown in **FIG. 2** is an inter-layer insulator that is relatively free of impurities. In the embodiment of **FIG. 2 a** layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **245** is interposed between the floating gate **240** and the layer of silicon dioxide **250**. The layer of silicon dioxide **250** is relatively free of impurities when the impurity level is at least an order of magnitude less than the impurity level of a silicon dioxide layer formed on a floating gate.

[0023] The process for forming the composite **285** requires flowing silane and phosphine to form the floating gate **240** in a chemical vapor deposition chamber. By decreasing the flow of phosphine, a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **245** is formed on the floating gate **240**. In one embodiment of the

present invention, the flow of phosphine is reduced to zero. The rest of the process for forming the composite **285** includes oxidizing or partially oxidizing the layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **245** to form the layer of silicon dioxide **250**, depositing a layer of silicon nitride **260** by chemical vapor deposition on the layer of silicon dioxide **250**, and oxidizing the layer of silicon nitride **260**, under aggressive oxidation conditions, to form the second layer of silicon dioxide **270**. At the completion of this process, the layer of silicon dioxide **250** is relatively free of phosphorous and demonstrates a decrease in charge leakage, when compared with the prior art. By decreasing the concentration of phosphorous, the allowed energy levels or traps are decreased in the layer of silicon dioxide **250**. Allowed energy levels or traps are a principal cause of charge leakage in the layer of silicon dioxide **250**. This process allows adding the new layer without removing the wafer from the chemical vapor deposition chamber or adding processing steps.

[**0024**] Referring to **FIG. 3, a** diagram of an alternate embodiment of a memory cell for use in a non-volatile semiconductor memory is shown. The cell is a transistor comprising a semiconductor substrate **300**, a source **310**, a drain **320**, an insulating layer **330**, a floating gate **340**, a layer of silicon dioxide **350**, a layer of silicon nitride **360**, a layer of silicon rich nitride **365**, a second layer of silicon dioxide **370**, and a control gate **380**. Together, the layer of silicon dioxide **350**, the layer of silicon nitride **360**, the layer of silicon rich nitride **365**, and the second layer of silicon dioxide **370** make up a composite **385** that acts as a dielectric and as an insulator between the control gate **380** and the floating gate **340**. The layer of nitride **360** functions as a dielectric, and the silicon dioxide layers, the layer of silicon dioxide **350** and the second layer of silicon dioxide **370**, function as insulators.

[**0025**] A structural difference between the memory cell of **FIG. 1** and a second embodiment of the present invention shown in **FIG. 3** is an inter-layer insulator that is relatively free of impurities. In the embodiment of **FIG. 3 a** layer of silicon rich nitride **365** is interposed between the layer of silicon nitride **360** and the layer of silicon dioxide **370**. The layer of silicon dioxide **370** is relatively free of impurities when the impurity level is at least an order of magnitude less than the impurity level of a silicon dioxide layer formed on a layer of silicon nitride.

[**0026**] The process for forming the composite **385** requires partially oxidizing the doped polysilicon of the floating gate **340** to form the layer of silicon dioxide **350** and depositing a layer of silicon nitride **360** by chemical vapor deposition on the layer of silicon dioxide **350**. As the layer of silicon nitride **360** is formed by flowing dichlorosilane and ammonia or tetrachlorosilane and ammonia, the layer of silicon rich nitride **365** is formed by reducing the flow of ammonia. In one embodiment, the flow of ammonia is reduced to zero. After forming the layer of silicon rich nitride **365**, the second layer of silicon dioxide **370** is formed by oxidizing the layer of silicon rich nitride **365**. At the completion of this process, the second layer of silicon dioxide **370** is relatively free of nitrogen and demonstrates a decrease in charge leakage, when compared with the prior art. By decreasing the concentration of nitrogen, the allowed energy levels or traps are decreased in the second layer of silicon dioxide **370**, and the less aggressive oxidizing conditions are required to achieve the same silicon dioxide thickness.

[**0027**] Referring to **FIG. 4, a** diagram of still another embodiment of a memory cell for use in a non-volatile semiconductor memory is shown. The cell is a transistor comprising a semiconductor substrate **400**, a source **410**, a drain **420**, an insulating layer **430**, a floating gate **440**, a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **445**, a layer of silicon dioxide **450**, a layer of silicon nitride **460**, a layer of silicon rich nitride **465**, a second layer of silicon dioxide **470**, and a control gate **480**. Together, the layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **445**, the layer of silicon dioxide **450**, the layer of silicon nitride **460**, the layer of silicon rich nitride **465**, and the second layer of silicon dioxide **470** make up a composite **485** that acts as a dielectric and as an insulator between the control gate **480** and the floating gate **440**. The layer of nitride **460** functions as a dielectric, and the silicon dioxide layers, the layer of silicon dioxide **450** and the second layer of silicon dioxide **470**, function as insulators.

[**0028**] Referring to **FIG. 4**, the third embodiment is a combination of the first embodiment and the second embodiment. A structural difference between the memory cell of **FIG. 1** and the memory cell of **FIG. 4** is a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **445** interposed between the floating gate **440** and the layer of silicon dioxide **450** and a layer of silicon rich nitride **465** interposed between the layer of silicon nitride **460** and the second layer of silicon dioxide **470**. The purpose of the layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **445** and the layer of silicon rich nitride **465** is to decrease the charge leakage between the floating gate **440** and the control gate **480**. As described in the first embodiment and the second embodiment, the layer of silicon dioxide **450** formed on the layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **445** contains less phosphorous than the corresponding layer in the prior art, and the layer of silicon rich nitride **465** formed on the layer of silicon nitride **460** contains less nitrogen than the corresponding layer in the prior art. So, the benefit of first embodiment, reducing charge leakage in the layer of silicon dioxide **450**, and the benefit of the second embodiment, reducing charge leakage in the second layer of silicon dioxide **470**, accrue to the third embodiment.

[**0029**] The process for forming the composite **485** combines the processes for forming the first embodiment and the second embodiment. The floating gate **440** is formed by flowing silane and phosphine. By decreasing the flow of phosphine, a layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **445** is formed on the floating gate **440**. Oxidizing or partially oxidizing the layer of undoped polysilicon, amorphous silicon, or amorphous polysilicon **445** forms the layer of silicon dioxide **450**, and the layer of silicon nitride **460** is formed by chemical vapor deposition on the layer of silicon dioxide **450**. After the layer of silicon nitride **460** is formed by flowing dichlorosilane and ammonia or tetrachlorosilane and ammonia, the layer of silicon rich nitride **465** is formed by reducing the flow of ammonia. After forming the layer of silicon rich nitride **465**, the second layer of silicon dioxide **470** is formed by oxidizing the layer of silicon rich nitride **465**. At the completion

of this process, the layer of silicon dioxide is relatively free of phosphorous and the layer of silicon rich nitride is relatively free of nitrogen, when compared with the prior art. The result is a composite that exhibits low charge leakage, when compared with the prior art.

[0030] Referring to **FIG. 5, a** block diagram of a system level embodiment of the present invention is shown. System **500** comprises processor **505** and memory device **510**, which includes memory cells of one or more of the types described above in conjunction with FIGS. **2-4**. Memory device **510** comprises memory array **515**, address circuitry **520**, and read circuitry **530**, and is coupled to processor **505** by address bus **535**, data bus **540**, and control bus **545**. Processor **505**, through address bus **535**, data bus **540**, and control bus **545** communicates with memory device **510**. In a read operation initiated by processor **505**, address information, data information, and control information are provided to memory device **510** through busses **535**, **540**, and **545**. This information is decoded by addressing circuitry **520**, including a row decoder and a column decoder, and read circuitry **530**. Successful completion of the read operation results in information from memory array **515** being communicated to processor **505** over data bus **540**.

CONCLUSION

[0031] An embodiment of a nonvolatile memory cell has been described which has a undoped polysilicon, amorphous silicon, or amorphous polysilicon layer and a silicon rich nitride layer. This embodiment exhibits low charge leakage. A system embodiment of the invention has also been described.

[0032] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed by oxidizing the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

2. The composite of claim 1, wherein the layer of silicon dioxide is formed by chemical vapor deposition and the second layer of silicon dioxide is formed by oxidation.

3. The composite of claim 1, wherein the layer of undoped polysilicon is thin.

4. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed by partially oxidizing the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

5. The composite of claim 4, wherein the layer of silicon dioxide is formed by chemical vapor deposition and the second layer of silicon dioxide is formed by oxidation.

6. The composite of claim 4, wherein the layer of undoped polysilicon is thin.

7. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of silicon dioxide formed on the floating gate;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

8. The composite of claim 7, wherein the layer of silicon dioxide formed on the floating gate is formed by oxidation and the second layer of silicon dioxide formed on the layer of silicon nitride is formed by chemical vapor deposition.

9. The composite of claim 7, wherein the layer of silicon rich nitride is thin.

10. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed by oxidizing the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

11. The composite of claim 10, wherein the layer of silicon dioxide and the second layer of silicon dioxide are formed by chemical vapor deposition.

12. The composite of claim 10, wherein the layer of undoped polysilicon and the layer of silicon rich nitride are thin.

13. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed by partially oxidizing the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

14. The composite of claim 13, wherein the layer of silicon dioxide and the second layer of silicon dioxide are formed by chemical vapor deposition.

15. The composite of claim 13, wherein the layer of undoped polysilicon and the layer of silicon rich nitride are thin.

16. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of undoped polysilicon on the floating gate;

forming a layer of silicon dioxide by oxidizing the layer of undoped polysilicon;

depositing a layer of silicon nitride on the layer of silicon dioxide; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

17. The process of claim 16, wherein depositing a layer of undoped polysilicon results in a thin layer of undoped polysilicon.

18. The process of claim 16, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of undoped polysilicon is accomplished by reducing the flow of phosphine.

19. The process of claim 18, wherein the flow of phosphine is reduced to zero.

20. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of undoped polysilicon on the floating gate;

forming a layer of silicon dioxide by partially oxidizing the layer of undoped polysilicon;

depositing a layer of silicon nitride on the layer of silicon dioxide; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

21. The process of claim 20, wherein depositing a layer of undoped polysilicon results in a thin layer of undoped polysilicon.

22. The process of claim 20, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of undoped polysilicon is accomplished by reducing the flow of phosphine.

23. The process of claim 22, wherein the flow of phosphine is reduced to zero.

24. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

forming a layer of silicon dioxide by partially oxidizing the floating gate;

depositing a layer of silicon nitride on the layer of silicon dioxide;

depositing a layer of silicon rich nitride on the layer of silicon nitride; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

25. The process of claim 24, wherein depositing a layer of silicon rich nitride results in a thin layer of silicon rich nitride.

26. The process of claim 24, wherein after depositing a layer of silicon nitride formed on the layer of silicon dioxide by flowing dichlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

27. The process of claim 26, wherein, the flow of ammonia is reduced to zero.

28. The process of claim 24, wherein after depositing a layer of silicon nitride formed on the layer of silicon dioxide by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

29. The process of claim 28, wherein the flow of ammonia is reduced to zero.

30. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of undoped polysilicon on the floating gate;

forming a layer of silicon dioxide by oxidizing the layer of undoped polysilicon;

depositing a layer of silicon nitride on the layer of silicon dioxide;

depositing a layer of silicon rich nitride on the layer of silicon nitride; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

31. The process of claim 30, wherein depositing of the layer of undoped polysilicon results in a thin layer of undoped polysilicon, and depositing a layer of silicon rich nitride results in a thin layer of silicon rich nitride.

32. The process of claim 30, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of undoped polysilicon is accomplished by reducing the flow of phosphine.

33. The process of claim 31, wherein the flow of phosphine is reduced to zero.

34. The process of claim 30, wherein after depositing a layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the layer of silicon rich nitride is accomplished by reducing the flow of ammonia.

35. The process of claim 34, wherein the flow of ammonia is reduced to zero.

36. The process of claim 30, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of undoped polysilicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

37. The process of claim 36, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

38. The process of claim 30, wherein after depositing a layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

39. The process of claim 38, wherein the flow of ammonia is reduced to zero.

40. The process of claim 30, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of undoped polysilicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

41. The process of claim 40, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

42. A nonvolatile memory cell comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite.

43. The nonvolatile memory cell of claim 42, wherein the insulator is a tunnel oxide.

44. The nonvolatile memory cell of claim 42, wherein the layer of undoped polysilicon formed on the floating gate is thin.

45. A nonvolatile memory cell comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of silicon dioxide formed on the floating gate;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite.

46. The nonvolatile memory cell of claim 45, wherein the insulator is a tunnel oxide.

47. The nonvolatile memory cell of claim 45, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

48. A nonvolatile memory cell comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite.

49. The nonvolatile memory cell of claim 48, wherein the insulator is a tunnel oxide.

50. The nonvolatile memory cell of claim 48, wherein the layer of undoped polysilicon formed on the floating gate is thin.

51. The nonvolatile memory cell of claim 48, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

52. The nonvolatile memory cell of claim 48, wherein the layer of undoped polysilicon formed on the floating gate is thin and the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

53. A memory device, comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

54. The memory device of claim 53, wherein the insulator is a tunnel oxide.

55. The memory device of claim 53, wherein the layer of undoped polysilicon formed on the floating gate is thin.

56. A memory device, comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of silicon dioxide formed on the floating gate;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon di oxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

57. The memory device of claim 56, wherein the insulator is a tunnel oxide.

58. The memory device of claim 56, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

59. A memory device, comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

60. The memory device of claim 59, wherein the insulator is a tunnel oxide.

61. The memory device of claim 59, wherein the layer of undoped polysilicon formed on the floating gate is thin.

62. The memory device of claim 59, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

63. The memory device of claim 59, wherein the layer of undoped polysilicon formed on the floating gate is thin and the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

64. A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

65. The system of claim 64, wherein the insulator is a tunnel oxide.

66. The system of claim 64, wherein the layer of undoped polysilicon formed on the floating gate is thin.

67. A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of silicon dioxide formed on the floating gate;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

68. The system of claim 67, wherein the insulator is a tunnel oxide.

69. The system of claim 67, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

70. A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of undoped polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of undoped polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

71. The system of claim 70, wherein the insulator is a tunnel oxide.

72. The system of claim 70, wherein the layer of undoped polysilicon formed on the floating gate is thin.

73. The system of claim 70, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

74. The system of claim 70, wherein the layer of undoped polysilicon formed on the floating gate is thin and the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

75. A nonvolatile memory cell comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate and having an inter-layer insulator that is relatively free of impurities; and

a control gate formed on the composite.

76. The non-volatile memory cell of claim 75, wherein the inter-layer insulator is a layer of silicon dioxide.

77. The non-volatile memory cell of claim 75, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of undoped polysilicon.

78. The non-volatile memory cell of claim 75, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of amorphous silicon.

79. The non-volatile memory cell of claim 75, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of amorphous polysilicon.

80. The non-volatile memory cell of claim 75, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of silicon rich nitride.

81. A memory device, comprising:

a nonvolatile memory cell having an inter-layer insulator that is relatively free of impurities;

an addressing circuit coupled to the memory cell for accessing the memory cell; and

a read circuit coupled to the memory cell for reading from the memory cell.

82. The memory device of claim 81, wherein the inter-layer insulator is a layer of silicon dioxide.

83. The memory device of claim 81, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of undoped polysilicon.

84. The memory device of claim 81, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of amorphous silicon.

85. The memory device of claim 81, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of amorphous poly silicon.

86. The memory device of claim 81, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of silicon rich nitride.

87. A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a nonvolatile memory cell having an inter-layer insulator that is relatively free of impurities;

an addressing circuit coupled to the memory cell for accessing the memory cell; and

a read circuit coupled to the memory cell for reading from the memory cell.

88. The memory device of claim 87, wherein the inter-layer insulator is a layer of silicon dioxide.

89. The memory device of claim 87, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of undoped polysilicon.

90. The memory device of claim 87, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of amorphous silicon.

91. The memory device of claim 87, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of amorphous polysilicon.

92. The memory device of claim 87, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of silicon rich nitride.

93. A transistor comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate and having an inter-layer insulator that is relatively free of impurities; and

a control gate formed on the composite.

94. The transistor of claim 93, wherein the inter-layer insulator is a layer of silicon dioxide.

95. The transistor of claim 93, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of undoped polysilicon.

96. The transistor of claim 93, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of amorphous silicon.

97. The transistor of claim 93, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of amorphous polysilicon.

98. The transistor of claim 93, wherein the inter-layer insulator is a layer of silicon dioxide formed on a layer of silicon rich nitride.

99. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed by oxidizing the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

100. The composite of claim 99, wherein the layer of silicon dioxide is formed by chemical vapor deposition and the second layer of silicon dioxide is formed by oxidation.

101. The composite of claim 99, wherein the layer of amorphous silicon is thin.

102. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed by partially oxidizing the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

103. The composite of claim 102, wherein the layer of silicon dioxide is formed by chemical vapor deposition and the second layer of silicon dioxide is formed by oxidation.

104. The composite of claim 102, wherein the layer of amorphous silicon is thin.

105. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed by oxidizing the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

106. The composite of claim 105, wherein the layer of silicon dioxide and the second layer of silicon dioxide are formed by chemical vapor deposition.

107. The composite of claim 105, wherein the layer of amorphous silicon and the layer of silicon rich nitride are thin.

108. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed by partially oxidizing the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

109. The composite of claim 108, wherein the layer of silicon dioxide and the second layer of silicon dioxide are formed by chemical vapor deposition.

110. The composite of claim 108, wherein the layer of amorphous silicon and the layer of silicon rich nitride are thin.

111. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of amorphous silicon on the floating gate;

forming a layer of silicon dioxide by oxidizing the layer of amorphous silicon;

depositing a layer of silicon nitride on the layer of silicon dioxide; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

112. The process of claim 111, wherein depositing a layer of amorphous silicon results in a thin layer of amorphous silicon.

113. The process of claim 111, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous silicon is accomplished by reducing the flow of phosphine.

114. The process of claim 113, wherein the flow of phosphine is reduced to zero.

115. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of amorphous silicon on the floating gate;

forming a layer of silicon dioxide by partially oxidizing the layer of amorphous silicon;

depositing a layer of silicon nitride on the layer of silicon dioxide; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

116. The process of claim 115, wherein depositing a layer of amorphous silicon results in a thin layer of amorphous silicon.

117. The process of claim 115, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous silicon is accomplished by reducing the flow of phosphine.

118. The process of claim 117, wherein the flow of phosphine is reduced to zero.

119. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of amorphous silicon on the floating gate;

forming a layer of silicon dioxide by oxidizing the layer of amorphous silicon;

depositing a layer of silicon nitride on the layer of silicon dioxide;

depositing a layer of silicon rich nitride on the layer of silicon nitride; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

120. The process of claim 119, wherein depositing of the layer of amorphous silicon results in a thin layer of amorphous silicon, and depositing a layer of silicon rich nitride results in a thin layer of silicon rich nitride.

121. The process of claim 119, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous silicon is accomplished by reducing the flow of phosphine.

122. The process of claim 120, wherein the flow of phosphine is reduced to zero.

123. The process of claim 119, wherein after depositing a layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the layer of silicon rich nitride is accomplished by reducing the flow of ammonia.

124. The process of claim 123, wherein the flow of ammonia is reduced to zero.

125. The process of claim 119, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous silicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

126. The process of claim 125, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

127. The process of claim 119, wherein after depositing a layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

128. The process of claim 127, wherein the flow of ammonia is reduced to zero.

129. The process of claim 119, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous silicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

130. The process of claim 129, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

131. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of amorphous silicon on the floating gate;

forming a layer of silicon dioxide by partially oxidizing the layer of amorphous silicon;

depositing a layer of silicon nitride on the layer of silicon dioxide;

depositing a layer of silicon rich nitride on the layer of silicon nitride; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

132. The process of claim 131, wherein depositing of the layer of amorphous silicon results in a thin layer of amor-

phous silicon, and depositing a layer of silicon rich nitride results in a thin layer of silicon rich nitride.

133. The process of claim 131, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous silicon is accomplished by reducing the flow of phosphine.

134. The process of claim 133, wherein the flow of phosphine is reduced to zero.

135. The process of claim 131, wherein after depositing a layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the layer of silicon rich nitride is accomplished by reducing the flow of ammonia.

136. The process of claim 135, wherein the flow of ammonia is reduced to zero.

137. The process of claim 131, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous silicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

138. The process of claim 137, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

139. The process of claim 131, wherein after depositing a layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

140. The process of claim 139, wherein the flow of ammonia is reduced to zero.

141. The process of claim 131, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous silicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

142. The process of claim 141, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

143. A nonvolatile memory cell comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite.

144. The nonvolatile memory cell of claim 143, wherein the insulator is a tunnel oxide.

145. The nonvolatile memory cell of claim 143, wherein the layer of amorphous silicon formed on the floating gate is thin.

146. A nonvolatile memory cell comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite.

147. The nonvolatile memory cell of claim 146, wherein the insulator is a tunnel oxide.

148. The nonvolatile memory cell of claim 146, wherein the layer of amorphous silicon formed on the floating gate is thin.

149. The nonvolatile memory cell of claim 146, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

150. The nonvolatile memory cell of claim 146, wherein the layer of amorphous silicon formed on the floating gate is thin and the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

151. A memory device, comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

152. The memory device of claim 151, wherein the insulator is a tunnel oxide.

153. The memory device of claim 151, wherein the layer of amorphous silicon formed on the floating gate is thin.

154. A memory device, comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

155. The memory device of claim 154, wherein the insulator is a tunnel oxide.

156. The memory device of claim 154, wherein the layer of amorphous silicon formed on the floating gate is thin.

157. The memory device of claim 154, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

158. The memory device of claim 154, wherein the layer of amorphous silicon formed on the floating gate is thin and the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

159. A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

160. The system of claim 159, wherein the insulator is a tunnel oxide.

161. The system of claim 159, wherein the layer of amorphous silicon formed on the floating gate is thin.

162. A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous silicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous silicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

163. The system of claim 162, wherein the insulator is a tunnel oxide.

164. The system of claim 162, wherein the layer of amorphous silicon formed on the floating gate is thin.

165. The system of claim 162, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

166. The system of claim 162, wherein the layer of amorphous silicon formed on the floating gate is thin and the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

167. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed by oxidizing the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

168. The composite of claim 167, wherein the layer of silicon dioxide is formed by chemical vapor deposition and the second layer of silicon dioxide is formed by oxidation.

169. The composite of claim 167, wherein the layer of amorphous polysilicon is thin.

170. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed by partially oxidizing the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

171. The composite of claim 170, wherein the layer of silicon dioxide is formed by chemical vapor deposition and the second layer of silicon dioxide is formed by oxidation.

172. The composite of claim 170, wherein the layer of amorphous polysilicon is thin.

173. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed by oxidizing the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

174. The composite of claim 173, wherein the layer of silicon dioxide and the second layer of silicon dioxide are formed by chemical vapor deposition.

175. The composite of claim 173, wherein the layer of amorphous polysilicon and the layer of silicon rich nitride are thin.

176. A dielectric composite for insulating a floating gate from a control gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed by partially oxidizing the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

177. The composite of claim 176, wherein the layer of silicon dioxide and the second layer of silicon dioxide are formed by chemical vapor deposition.

178. The composite of claim 176, wherein the layer of amorphous polysilicon and the layer of silicon rich nitride are thin.

179. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of amorphous polysilicon on the floating gate;

forming a layer of silicon dioxide by oxidizing the layer of amorphous polysilicon;

depositing a layer of silicon nitride on the layer of silicon dioxide; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

180. The process of claim 179, wherein depositing a layer of amorphous polysilicon results in a thin layer of amorphous polysilicon.

181. The process of claim 179, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous polysilicon is accomplished by reducing the flow of phosphine.

182. The process of claim 181, wherein the flow of phosphine is reduced to zero.

183. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of amorphous polysilicon on the floating gate;

forming a layer of silicon dioxide by partially oxidizing the layer of amorphous polysilicon;

depositing a layer of silicon nitride on the layer of silicon dioxide; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon nitride, the control gate formed on the second layer of silicon dioxide.

184. The process of claim 183, wherein depositing a layer of amorphous polysilicon results in a thin layer of amorphous polysilicon.

185. The process of claim 183, wherein after forming the floating gate by flowing silane and phosphine, the deposition

of the layer of amorphous polysilicon is accomplished by reducing the flow of phosphine.

186. The process of claim 185, wherein the flow of phosphine is reduced to zero.

187. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of amorphous polysilicon on the floating gate;

forming a layer of silicon dioxide by oxidizing the layer of amorphous polysilicon;

depositing a layer of silicon nitride on the layer of silicon dioxide;

depositing a layer of silicon rich nitride on the layer of silicon nitride; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

188. The process of claim 187, wherein depositing of the layer of amorphous polysilicon results in a thin layer of amorphous polysilicon, and depositing a layer of silicon rich nitride results in a thin layer of silicon rich nitride.

189. The process of claim 187, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous polysilicon is accomplished by reducing the flow of phosphine.

190. The process of claim 189, wherein the flow of phosphine is reduced to zero.

191. The process of claim 187, wherein after depositing a layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the layer of silicon rich nitride is accomplished by reducing the flow of ammonia.

192. The process of claim 191, wherein the flow of ammonia is reduced to zero.

193. The process of claim 187, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous polysilicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

194. The process of claim 193, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

195. The process of claim 187, wherein after depositing a layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

196. The process of claim 195, wherein the flow of ammonia is reduced to zero.

197. The process of claim 187, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous polysilicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

198. The process of claim 197, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

199. A process for forming a dielectric composite for insulating a floating gate from a control gate, the process comprising:

depositing a layer of amorphous polysilicon on the floating gate;

forming a layer of silicon dioxide by partially oxidizing the layer of amorphous polysilicon;

depositing a layer of silicon nitride on the layer of silicon dioxide;

depositing a layer of silicon rich nitride on the layer of silicon nitride; and

forming a second layer of silicon dioxide by oxidizing the layer of silicon rich nitride, the control gate formed on the second layer of silicon dioxide.

200. The process of claim 199, wherein depositing of the layer of amorphous polysilicon results in a thin layer of amorphous polysilicon, and depositing a layer of silicon rich nitride results in a thin layer of silicon rich nitride.

201. The process of claim 199, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous polysilicon is accomplished by reducing the flow of phosphine.

202. The process of claim 201, wherein the flow of phosphine is reduced to zero.

203. The process of claim 199, wherein after depositing a layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the layer of silicon rich nitride is accomplished by reducing the flow of ammonia.

204. The process of claim 203, wherein the flow of ammonia is reduced to zero.

205. The process of claim 199, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous polysilicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing dichlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

206. The process of claim 205, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

207. The process of claim 199, wherein after depositing a layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

208. The process of claim 207, wherein the flow of ammonia is reduced to zero.

209. The process of claim 199, wherein after forming the floating gate by flowing silane and phosphine, the deposition of the layer of amorphous polysilicon is accomplished by reducing the flow of phosphine, and after depositing the layer of silicon nitride by flowing tetrachlorosilane and ammonia, the deposition of the silicon rich nitride layer is accomplished by reducing the flow of ammonia.

210. The process of claim 209, wherein the flow of phosphine is reduced to zero, and the flow of ammonia is reduced to zero.

211. A nonvolatile memory cell comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite.

212. The nonvolatile memory cell of claim 211, wherein the insulator is a tunnel oxide.

213. The nonvolatile memory cell of claim 211, wherein the layer of amorphous polysilicon formed on the floating gate is thin.

214. A nonvolatile memory cell comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite.

215. The nonvolatile memory cell of claim 214, wherein the insulator is a tunnel oxide.

216. The nonvolatile memory cell of claim 214, wherein the layer of amorphous polysilicon formed on the floating gate is thin.

217. The nonvolatile memory cell of claim 214, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

218. The nonvolatile memory cell of claim 214, wherein the layer of amorphous polysilicon formed on the floating gate is thin and the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

219. A memory device, comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

220. The memory device of claim 219, wherein the insulator is a tunnel oxide.

221. The memory device of claim 219, wherein the layer of amorphous polysilicon formed on the floating gate is thin.

222. A memory device, comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

223. The memory device of claim 222, wherein the insulator is a tunnel oxide.

224. The memory device of claim 222, wherein the layer of amorphous polysilicon formed on the floating gate is thin.

225. The memory device of claim 222, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

226. The memory device of claim 222, wherein the layer of amorphous polysilicon formed on the floating gate is thin and the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

227. A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

228. The system of claim 227, wherein the insulator is a tunnel oxide.

229. The system of claim 227, wherein the layer of amorphous polysilicon formed on the floating gate is thin.

230. A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a substrate;

a source and drain formed on the substrate;

an insulator formed on the source and drain;

a floating gate formed on the insulator;

a composite formed on the floating gate, the composite comprising:

a layer of amorphous polysilicon formed on the floating gate;

a layer of silicon dioxide formed on the layer of amorphous polysilicon;

a layer of silicon nitride formed on the layer of silicon dioxide;

a layer of silicon rich nitride formed on the layer of silicon nitride; and

a second layer of silicon dioxide formed on the silicon rich nitride; and

a control gate formed on the composite;

addressing circuity coupled to the plurality of memory cells for accessing at least one of the memory cells; and

a read circuit coupled to the plurality of memory cells for reading data from at least one of the memory cells.

231. The system of claim 230, wherein the insulator is a tunnel oxide.

232. The system of claim 230, wherein the layer of amorphous polysilicon formed on the floating gate is thin.

233. The system of claim 230, wherein the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

234. The system of claim 230, wherein the layer of amorphous polysilicon formed on the floating gate is thin and the layer of silicon rich nitride formed on the layer of silicon nitride is thin.

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