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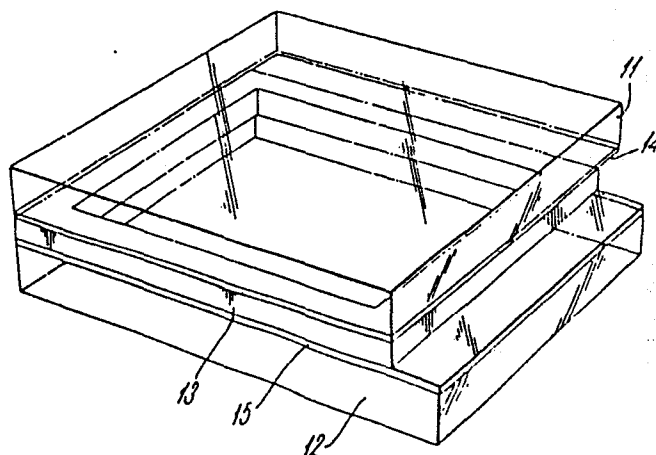
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(54) Addressing liquid crystal cells.

(57) A method of addressing a matrix addressed ferroelectric liquid crystal cell is described that uses parallel entry of balanced bipolar data pulses on one set of electrodes to co-operate with serial entry of balanced bipolar strobe pulses on the other set of electrodes. The positive- and negative-going excursions of each data pulse are asymmetric, the excursion of one polarity having 'm' times the amplitude of the other and $1/m^{\text{th}}$ the duration.

Fig.1.



ADDRESSING LIQUID CRYSTAL CELLS

This invention relates to the addressing of matrix array type ferroelectric liquid crystal cells.

Hitherto dynamic scattering mode liquid crystal cells have been operated using a d.c. drive
5 or an a.c. one, whereas field effect mode liquid crystal devices have generally been operated using an a.c. drive in order to avoid performance impairment problems associated with electrolytic degradation of the liquid crystal layer. Such
10 devices have employed liquid crystals that do not exhibit ferroelectricity, and the material interacts with an applied electric field by way of an induced dipole. As a result they are not sensitive to the polarity of the applied field, but respond to the
15 applied RMS voltage averaged over approximately one response time at that voltage. There may also be frequency dependence as in the case of so-called two-frequency materials, but this only affects the type of response produced by the applied field.

20 In contrast to this, a ferroelectric liquid crystal exhibits a permanent electric dipole, and it is this permanent dipole which will interact with an applied electric field. Ferroelectric liquid crystals are of interest in display, switching and
25 information processing applications because they are expected to show a greater coupling with an applied field than that typical of a liquid crystal that relies on coupling with an induced dipole, and hence

ferroelectric liquid crystals are expected to show a faster response. A ferroelectric liquid crystal display mode is described for instance by N.A.Clark et al in a paper entitled "Ferro-electric Liquid
5 Crystal Electro-Optics Using the Surface Stabilized Structure" appearing in Mol. Cryst. Liq.Cryst. 1983 Volume 94 pages 213 to 234. By way of example reference may also be made to an alternative mode that is described in the specification of British
10 Patent Application No. 8426976.

A particularly significant characteristic peculiar to ferroelectric smectic cells is the fact that they, unlike other types of liquid crystal cell, are responsive differently according to the
15 polarity of the applied field. This characteristic sets the choice of a suitable matrix-addressed driving system for a ferroelectric smectic into a class of its own. A further factor which can be significant is that, in the region of switching
20 times of the order of a microsecond, a ferroelectric smectic typically exhibits a relatively weak dependence of its switching time upon switching voltage. In this region the switching time of a ferroelectric may typically exhibit a response time
25 proportional to the inverse square of applied voltage or, even worse, proportional to the inverse single power of voltage. In contrast to this, a (non-ferroelectric) smectic A device, which in certain other respects is a comparable device
30 exhibiting a long-term storage capability, exhibits in a corresponding region of switching speeds a response time that is typically proportional to the inverse fifth power of voltage. The significance of this difference becomes apparent when it is
35 appreciated first that there is a voltage threshold

beneath which a signal will never produce switching however long that signal is maintained; second that for any chosen voltage level above this voltage threshold there is a minimum time t_s for which the
5 signal has to be maintained to effect switching; and third that at this chosen voltage level there is a shorter minimum time t_p beneath which the application of the signal voltage produces no persistent effect, but above which, upon removal of
10 the signal voltage, the liquid crystal does not revert fully to the state subsisting before the signal was applied. When the relationship $t_s = f(V)$ between V and t_s is known, a working guide to the relationship between V and t_p is often found
15 to be given by the curve $t_p = g(V)$ formed by plotting (V_1, t_2) where the points (V_1, t_1) and (V_2, t_2) lie on the $t_s = f(V)$ curve, and where $t_1 = 10t_2$. Now the ratio of V_2/V_1 is increased as the inverse dependence of switching
20 time upon applied voltage weakens, and hence, when the working guide is applicable, a consequence of weakened dependence is an increased intolerance of the system to the incidence of wrong polarity signals to any pixel, that is signals tending to
25 switch to the '1' state a pixel intended to be left in the '0' state, or to switch to the '0' state a pixel intended to be left in the '1' state.

Therefore, a good drive scheme for addressing a ferroelectric liquid crystal cell must
30 take account of polarity, and may also need to take particular care to minimise the incidence of wrong polarity signals to any given pixel whether it is intended as '1' state pixel or a '0' state one. Additionally, the waveforms applied to the
35 individual electrodes by which the pixels are

addressed need to be charge-balanced at least in the long term. If the electrodes are not insulated from the liquid crystal this is so as to avoid electrolytic degradation of the liquid crystal brought about by a net flow of direct current through the liquid crystal. On the other hand if the electrodes are insulated, it is to prevent a cumulative build up of charge at the interface between the liquid crystal and the insulation.

10 With these considerations in mind a number of methods for addressing matrix-array type ferroelectric liquid crystal cells are described in Patent Specification No. 2146473A to which attention is directed. In particular there is an addressing method described with reference to Figure 2 of that specification which employs balanced bipolar strobe pulses in conjunction with balanced bipolar data pulses for the addressing of the cell. In that particular addressing method the strobe pulse voltage is switched between $+V_S$ and $-V_S$ and the data pulse voltage is switched between $+V_D$ and $-V_D$. These voltages co-operate to produce a potential difference of $(V_S + V_D)$ across the thickness of the liquid crystal layer of the cell for a duration t_S , and it is arranged that this will be sufficient to effect switching of any pixel to which this signal is applied. The shape and timing of the strobe and data pulses is arranged so that at no time will a pixel see a wrong polarity signal having a magnitude exceeding $|V_S - V_D|$, or $|V_D|$, whichever is the greater. By this means is facilitated the achieving of low maximum magnitude of reverse polarity signals, but this is achieved at the expense of a line address time of 35 $4t_S$.

The present invention is concerned with modifying the waveforms with a view to reducing the minimum line address time for a given address voltage, albeit that this is achieved at the expense
5 of an exposure to larger reverse polarity signals. In this context it can be shown that certain configurations of cell with certain mixtures ferroelectric liquid crystal fillings exhibit a switching behaviour that is much more tolerant of
10 reverse polarity voltages than is implied by the above-quoted working guide, for instance producing no persistent effect when addressed with a reverse polarity pulse of the same duration but only 75% of the amplitude of a pulse that is just sufficient to
15 effect switching.

According to the present invention a method of addressing a matrix-array type liquid crystal cell with a ferroelectric liquid crystal layer whose pixels are defined by the areas of overlap between
20 the members of a first set of electrodes on one side of the liquid crystal layer and the members of a second set on the other side of the layer is characterised in that the cell is addressed on a line-by-line basis by applying strobe pulses
25 serially to the members of the first set while data pulses are applied in parallel to members of the second set, that the strobe and data pulse waveforms are balanced bipolar pulses, and that the positive- and negative-going excursions of each balanced
30 bipolar data pulse are asymmetric, the excursion of one polarity having 'm' times the amplitude of the other and $1/m^{\text{th}}$ the duration.

There follows a description of a ferroelectric liquid crystal cell and of two ways by
35 which it may be addressed. The first method has

been included for the purposes of comparison, while the second embodies the present invention in a preferred form. The first method is one of the methods described in Patent Specification No. 5 2146473A. The description refers to the accompanying drawings in which:-

Figure 1 depicts a schematic perspective view of a ferroelectric liquid crystal cell;

Figure 2 depicts the waveforms of a drive 10 scheme previously described in Patent Specification No. 2146473A, and

Figure 3 depicts the waveforms of a drive scheme embodying the invention in a preferred form.

Referring now to Figure 1, a hermetically 15 sealed envelope for a liquid crystal layer is formed by securing together two glass sheets 11 and 12 with a perimeter seal 13. The inward facing surfaces of the two sheets carry transparent electrode layers 14 and 15 of indium tin oxide, and each of these 20 electrode layers is covered within the display area defined by the perimeter seal with a polymer layer, such as polyimide (not shown), provided for molecular alignment purposes. Both polyimide layers are rubbed in a single direction so that when a 25 liquid crystal is brought into contact with them they will tend to promote planar alignment of the liquid crystal molecules in the direction of the rubbing. The cell is assembled with the rubbing directions aligned parallel with each other. Before 30 the electrode layers 14 and 15 are covered with the polymer, each one is patterned to define a set of strip electrodes (not shown) that individually extend across the display area and on out to beyond the perimeter seal to provide contact areas to which 35 terminal connection may be made. In the assembled

cell the electrode strips of layer 14 extend transversely of those of layer 15 so as to define a pixel at each elemental area where an electrode strip of layer 15 is overlapped by a strip of layer 14. The thickness of the liquid crystal layer contained within the resulting envelope is determined by the thickness of the perimeter seal, and control over the precision of this may be provided by a light scattering of short lengths of glass fibre (not shown) of uniform diameter distributed through the material of the perimeter seal. Conveniently the cell is filled by applying a vacuum to an aperture (not shown) through one of the glass sheets in one corner of the area enclosed by the perimeter seal so as to cause the liquid crystal medium to enter the cell by way of another aperture (not shown) located in the diagonally opposite corner. (Subsequent to the filling operation the two apertures are sealed.) The filling operation is carried out with the filling material heated into its isotropic phase so as to reduce its viscosity to a suitably low value. It will be noted that the basic construction of the cell is similar to that of for instance a conventional twisted nematic, except of course for the parallel alignment of the rubbing directions.

Typically the thickness of the perimeter seal 13, and hence of the liquid crystal layer, is about 10 microns, but thinner or thicker layer thicknesses may be required to suit particular applications depending for instance upon whether or not bistability of operation is required and upon whether the layer is to be operated in the S_C^* phase or in one of the more ordered phases such as S_I^* or S_F^* .

Some drive schemes for ferroelectric cells are described in Patent Specification No. 2146473A. Among these is a scheme that is described with particular reference to Figure 2 of that specification, a part of which has been reproduced herein in slightly modified form as Figure 2 of this specification. This employs balanced bipolar data pulses 21a, 21b to co-act with balanced bipolar strobe pulses 20. The strobe pulses 20 are applied serially to the electrode strips of one electrode layer, while the data pulses 21a, and 21b are applied in parallel to those of the other layer. In this particular scheme a strobe pulse 20 makes an excursion to a voltage $+V_S$ for a duration t_S , and then immediately an excursion to a voltage $-V_S$ for a further duration t_S . Both types of data pulse 21a and 21b have a total duration of $4t_S$, starting t_S before the beginning of the positive excursion of a strobe pulse, and ending t_S after the end of its negative-going excursion. A data '1' pulse 21a commences by making a positive-going excursion to a voltage $+V_D$ for a duration t_S , a negative-going excursion to a voltage $-V_D$ for a duration $2t_S$, and finally a positive-going excursion to $+V_D$ for a duration t_S . A data '0' pulse 21b is the inverse of the data '0' pulse. It starts with a negative-going excursion to $-V_D$ for a duration t_S , follows this with an excursion to $+V_D$ for a duration $2t_S$, and terminates with an excursion back to $-V_D$ for a duration t_S .

The potential difference developed across the liquid crystal layer at a pixel addressed by the coincidence of a strobe pulse 20 with a data '1' pulse 21a is given by the pulse waveform 22a, while that of 22b is that which is produced at a pixel

addressed by the coincidence of a strobe pulse 20
with a data '0' pulse 21b. In each instance the
pixel is addressed by a voltage of duration t_S and
of magnitude $|V_S + V_D|$ tending to switch the
5 pixel in the required direction, but it is also
addressed by two reverse polarity pulses of
magnitude $|V_D|$, and one of magnitude $|V_S - V_D|$,
tending to switch it in the wrong direction. The
values of V_S and V_D are chosen so that the pixel
10 is appropriately switched by the $|V_S + V_D|$
magnitude pulse without this switching being negated
by the reverse polarity pulses. In considering the
effect of reverse polarity pulses upon a given pixel
it should also be noted that the data employed to
15 address the immediately preceding and immediately
following lines may be such as to produce a pair of
reverse polarity pulses of magnitude $|V_D|$ a net
duration t_S that immediately precede and follow
the voltage waveform produced by the addressing of
20 the given pixel.

The strobe and data pulse waveforms allow
individual pixels to be switched in either
direction, that is data entry can be used to drive
into the data '1' state selected pixels that were
25 previously in the data '0' state, while at the same
time other pixels that were previously in the '1'
state are switched into the '0' state. The
waveforms are charge balanced. These features are
however attained at the expense of a line address
30 time of $4t_S$ even though the switching voltage
magnitude $|V_S + V_D|$ is capable of switching a
pixel in a quarter of this time.

Attention will now be turned to Figure 3
which depicts waveforms according to one preferred
35 embodiment of the present invention. Strobing, data

'1' and data '0' pulse waveforms are depicted respectively at 30, 31a and 31b.

As before, the data pulse waveforms are applied in parallel to the electrode strips of one of the electrode layers 14, 15 while the strobe pulses are applied serially to those of the other electrode layer.

A strobe pulse 30 is a balanced bipolar pulse having a negative-going voltage excursion to $-V_S$ following immediately after a positive-going one to $+V_S$, both excursions being of duration t_S .

The data pulses 31a and 31b are also balanced bipolar pulses. A data '1' waveform includes a negative-going voltage excursion to $-V_D$ for a duration $2t_S$, which is both immediately preceded by, and immediately followed with, voltage excursions to $+mV_D$ for durations $(1/m)t_S$, where 'm' is some factor greater than unity. A data '0' waveform is the voltage inverse of a data '1' waveform, and has a positive-going excursion to $+V_D$ for a duration $2t_S$, which is both immediately preceded by, and immediately followed with, voltage excursions to $-mV_D$ for durations $(1/m)t_S$. The factor 'm' is the same for both data significances of data pulse, and in each case it is the voltage excursion of magnitude $|V_D|$ that is synchronised with the positive- and negative-going excursions of the strobe pulse.

The potential difference developed across the liquid crystal layer at a pixel addressed by the coincidence of a strobe pulse 30 with a data '1' pulse 31a is given by pulse waveform 32a, while that of 32b is that which is produced by the coincidence of a strobe pulse 30 with a data '0' pulse 31b. A comparison of these waveforms of Figure 3 with those

of Figure 2 reveals that the minimum line address
time is reduced from $4t_S$ to $2t_S (1 + 1/m)$, but
that under the condition $|V_S - V_D| > |V_D|$ this
is achieved at the expense of raising the magnitude
5 of the peak value of wrong polarity signal from
 $|V_D|$ to $|mV_D|$, albeit for a shorter period of
time.

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CLAIM:

A method of addressing a matrix-array type liquid crystal cell with a ferroelectric liquid crystal layer whose pixels are defined by the areas
5 of overlap between the members of a first set of electrodes on one side of the liquid crystal layer and the members of a second set on the other side of the layer, characterised in that the cell is addressed on a line-by-line basis by applying strobe
10 pulses serially to the members of the first set while data pulses are applied in parallel to members of the second set, that the strobe and data pulse waveforms are balanced bipolar pulses, and that the positive- and negative-going excursions of each
15 balanced bipolar data pulse are asymmetric, the excursion of one polarity having 'm' times the amplitude of the other and $1/m^{\text{th}}$ the duration.

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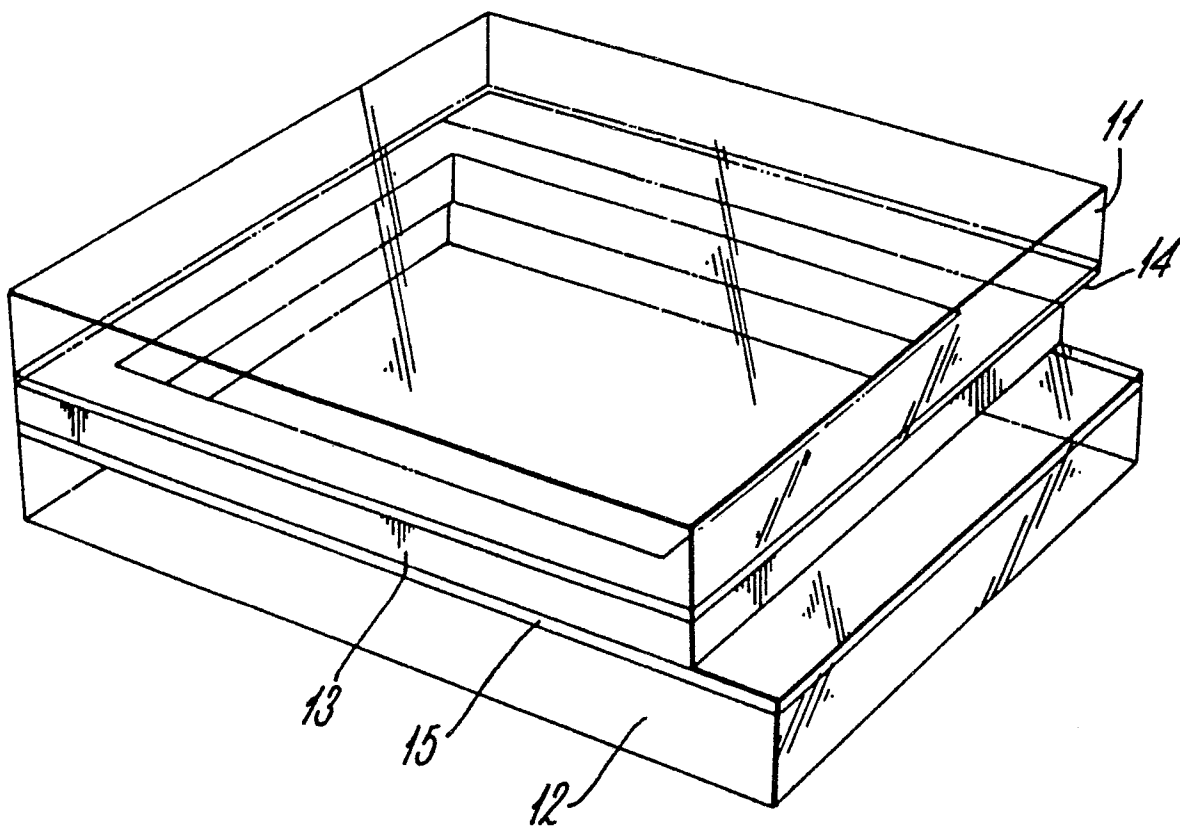
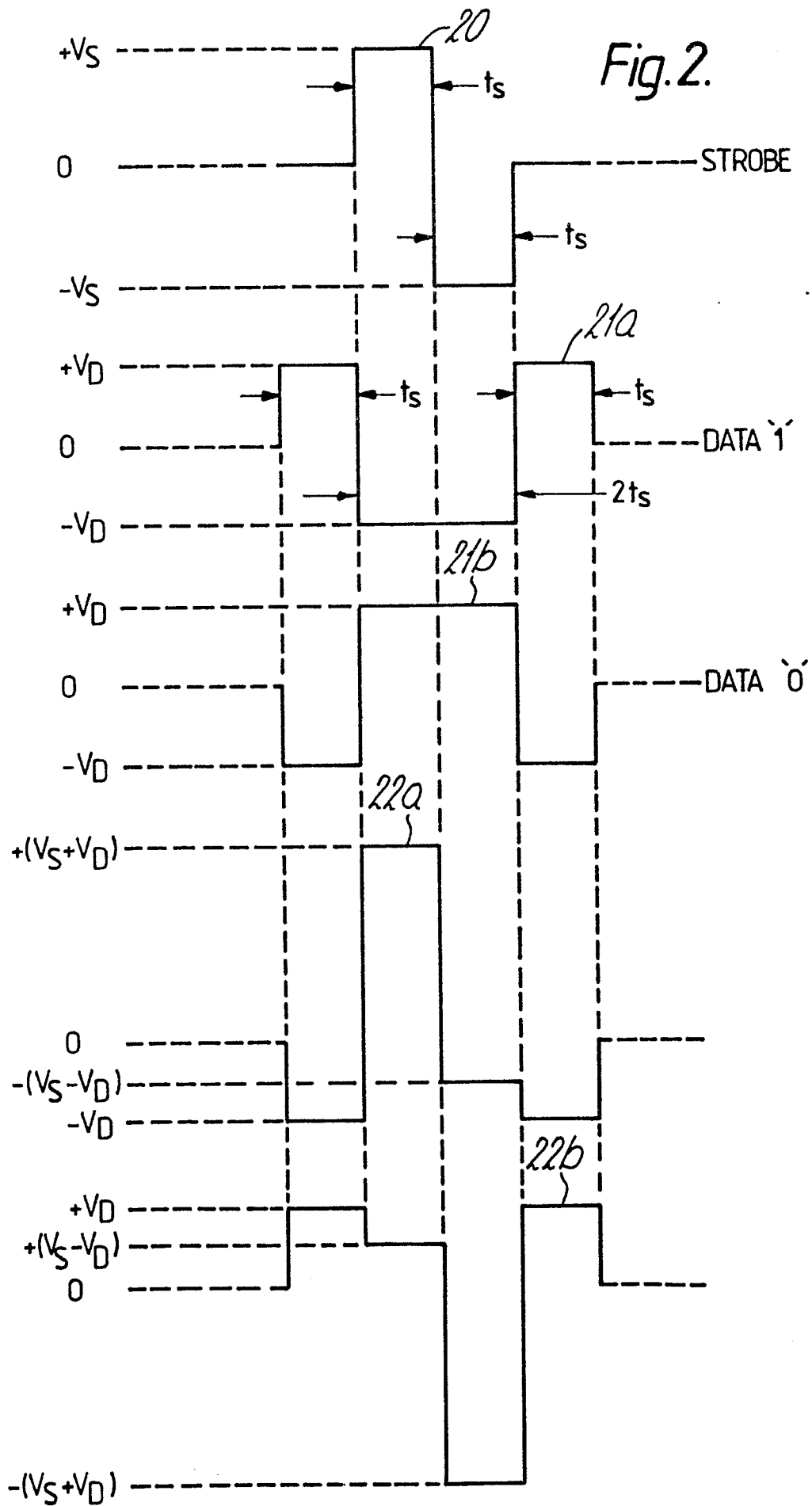
Fig.1.

Fig. 2.



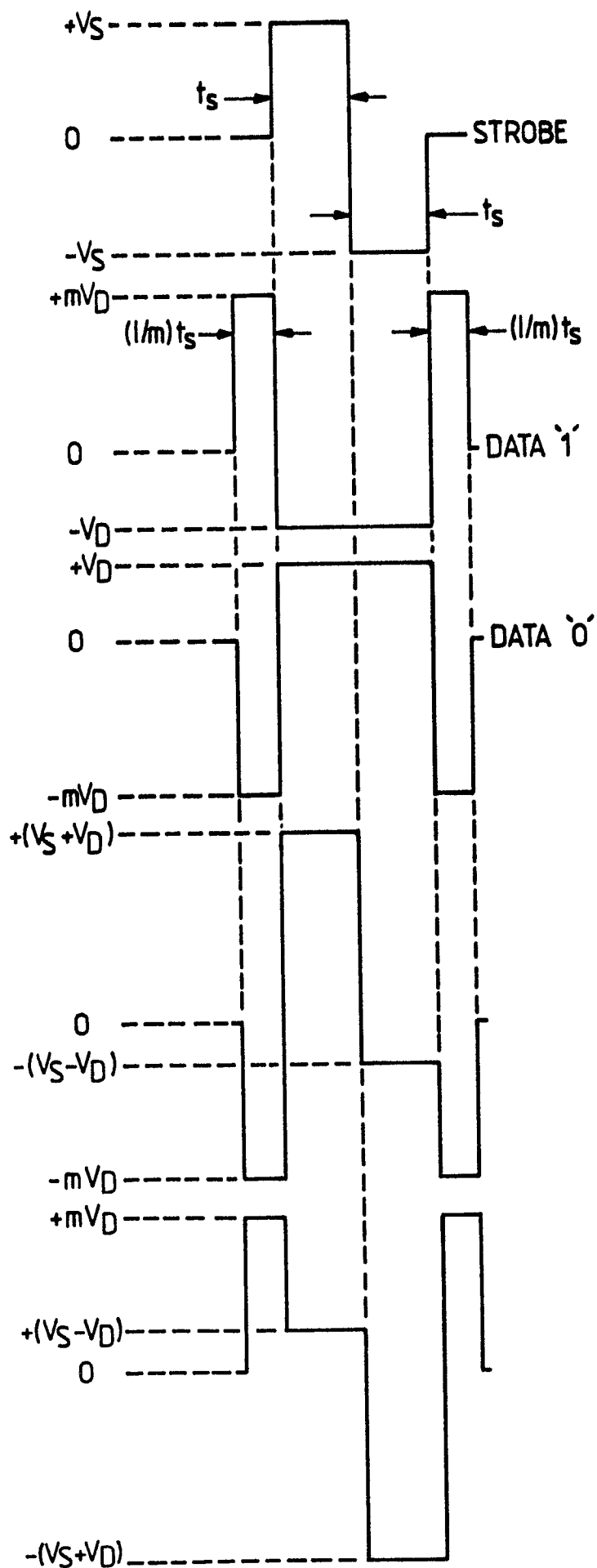


Fig.3.