



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
03.01.2018 Bulletin 2018/01

(51) Int Cl.:
G06F 3/06 (2006.01) G06F 13/40 (2006.01)

(21) Application number: **17178359.0**

(22) Date of filing: **28.06.2017**

(84) Designated Contracting States:
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO
PL PT RO RS SE SI SK SM TR**
Designated Extension States:
BA ME
Designated Validation States:
MA MD

(72) Inventors:
• **Chu, Wei-Yi**
333 Taoyuan City (TW)
• **Cheng, Chia-Feng**
333 Taoyuan City (TW)
• **Chang, Kai**
333 Taoyuan City (TW)
• **Chen, Chih-Yu**
333 Taoyuan City (TW)

(30) Priority: **30.06.2016 US 201615199504**

(71) Applicant: **Quanta Computer Inc.**
Taoyuan City 333 (TW)

(74) Representative: **Michalski Hüttermann & Partner**
Patentanwälte mbB
Speditionstraße 21
40221 Düsseldorf (DE)

(54) **RISER CARD**

(57) An apparatus having a first interface of a first type supporting a plurality of data ports, a second interface of a second type supporting at least a portion of the plurality data ports, and a third interface of the second type. The apparatus also including a switching module

coupled to a control port of the first interface and configured for selectably coupling the plurality of data ports to at least one of the second interface and the third interface based on a signal at the control port.

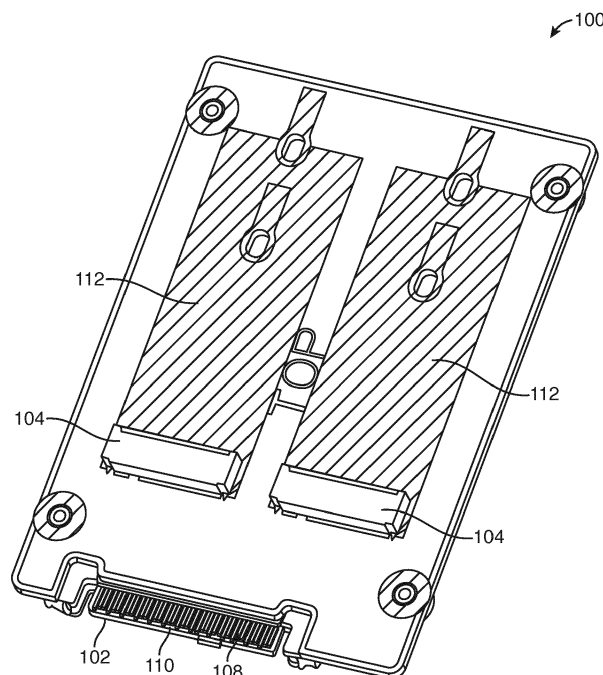


FIG. 1

Description

FIELD

[0001] The subject matter herein generally relates to a riser card. More specifically, the subject matter herein relates to a riser card configured to convert one or more M.2 (previously known as Next Generation Form Factor (NGFF)) components to work with a U.2 connector (previously known as SFF-8639).

BACKGROUND

[0002] U.2 components, such as Non-Volatile Memory Express (NVMe) peripheral component interconnect express (PCIe) solid state drives (SSD), offer high performance, but are relatively new to market and thus have significant cost. M.2 (previously known as Next Generation Form Factor (NGFF)) components provide the functionality of a U.2 component with a much smaller form factor and at a significantly reduced cost. M.2 can support PCIe with lower power consumption, cost, and maintain a high performance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Implementations of the present technology will now be described, by way of example only, with reference to the attached figures, wherein:

FIG. 1 is an isometric view of an example embodiment of a riser card with a first interface type and a second interface type in accordance with the present disclosure;

FIG. 2 is a front elevational view of an example embodiment of a riser card with a first interface type and a second interface type in accordance with the present disclosure;

FIG. 3 is a diagrammatic view of a riser card with a first interface type and a second interface type in accordance with the present disclosure;

FIG. 4 is a diagrammatic view of a riser card system in accordance with the present disclosure;

FIG. 5 is a diagrammatic view of a system in a first routing mode in accordance with the present disclosure;

FIG. 6 is a diagrammatic view of a system in a second routing mode in accordance with the present disclosure; and

FIG. 7 is a flow chart of a switching method for a riser card in accordance with the present disclosure.

DETAILED DESCRIPTION

[0004] It will be appreciated that for simplicity and clarity of illustration, where appropriate, reference numerals have been repeated among the different figures to indicate corresponding or analogous elements. In addition,

numerous specific details are set forth in order to provide a thorough understanding of the embodiments described herein. However, it will be understood by those of ordinary skill in the art that the embodiments described herein can be practiced without these specific details. In other instances, methods, procedures and components have not been described in detail so as not to obscure the related relevant feature being described. The drawings are not necessarily to scale and the proportions of certain parts may be exaggerated to better illustrate details and features. The description is not to be considered as limiting the scope of the embodiments described herein.

[0005] Several definitions that apply throughout this disclosure will now be presented.

[0006] The term "coupled" is defined as connected, whether directly or indirectly through intervening components, and is not necessarily limited to physical connections. The connection can be such that the objects are permanently connected or releasably connected. The term "substantially" is defined to be essentially conforming to the particular dimension, shape or other word that substantially modifies, such that the component need not be exact. For example, substantially cylindrical means that the object resembles a cylinder, but can have one or more deviations from a true cylinder. The term "comprising" means "including, but not necessarily limited to"; it specifically indicates open-ended inclusion or membership in a so-described combination, group, series and the like.

[0007] The present disclosure describes an apparatus having a first interface of a first type supporting a plurality of data ports, a second interface of a second type supporting at least a portion of the plurality data ports, and a third interface of the second type. A switching module coupled to a control port of the first interface and configured for selectably coupling the plurality of data ports to at least one of the second interface and the third interface based on a signal at the control port. The switching module selectably connecting the plurality of data ports to one of the second interfaces or diving the plurality of data ports between the two second interfaces.

[0008] While the present disclosure is presented with respect to a riser card capable of coupling one or more M.2 SSDs with a U.2 connector, it is within the scope of the disclosure to implement the present technology with other connectors, components, and/or switching modules.

[0009] FIGS. 1-3 illustrate a riser card 100 have a first interface 102, two second interfaces 104, and a switching module 106. The first interface 102 can have a plurality of data ports 108 capable of transmitting data between the first interface 102 and the second interface 104. The first interface 102 can have a control port 110 configured to selectably couple the plurality of data ports 108 to at least one of the second interfaces 104 based on a signal at the control port 110.

[0010] The first interface 102 and the second interfaces 104 can be of two different types, the first interface having

a first type and the second interfaces having a second type. In at least one embodiment, the first interface 102 type is an NVMe SSD interface configured to be received in a U.2 connector and the second interface 104 type 104 are M.2 interfaces.

[0011] The riser card 100 can have two receiving portions 112 corresponding to each of the two second interfaces 104. The receiving portions 112 can be configured to receive a component 114 (shown in FIG. 3), such as an M.2 PCIe SSD at least including three length types of M.2. PCIe SSD 2242, 2260, and 2280 as specified in the M.2 standard. The riser card 102 can be configured to selectively receive a component 114 in either of the two receiving portions 112, or both. As can be appreciated in FIG. 3, the first interface 102 can be receivable into a U.2 connector 200 disposed on an electronic device (not shown). The first interface 102 can electronically couple with the U.2 connector 200 allowing the two second interfaces 104 to send and receive data with the electronic device through the first interface 102.

[0012] The plurality of data ports 108 can be any number of data ports, such as two, four, six, or any other number. In the illustrated embodiment, the riser card 100 has four data ports coupling the first interface 102 with the second interfaces 104. The switching module 106 can allocate the plurality of data ports 108 between the first interface 102 and the two second interface 104. A user can control the switching module 106 to best allocate the plurality of data ports 108 according to their desired use, the installed components, and the performance required.

[0013] The riser card 100 can have a one component 114 received in a second interface 104 allowing allocation of the plurality of data ports 108 to the component 114. The riser card 100 can receive two components 114 requiring the switching module 106 to allocate the plurality of data ports 108 among the two components 114 received in the second interfaces 104.

[0014] In at least one embodiment, the riser card 100 can receive two components, and a user can allocate the plurality of ports 108 between the two received components 114 allowing utilization of one, or a combination of received components 114.

[0015] The riser card 100 can support hot-swapping of components 114 received in the second interfaces 104. Hot-swapping allows components to be removed, inserted, or replaced from the second interface 104 without removing power from the riser card 100. In at least one embodiment, the riser card 100 is received within an electronic device and hot-swapping allows one or more components 114 to be inserted or removed from the riser card 100 without powering down the electronic device.

[0016] Hot-swapping can be implemented using existing pin arrangements with the first interface 102. In the illustrated embodiment, the first interface 102 is a U.2 connector, thereby implementing P12V, P3V3_STBY, and applying the metal-oxide-semiconductor field-effect transistor (MOSFET) to achieve isolation of power hot-

swapping is achievable.

[0017] The riser card 100 can also implement Electrically Erasable Programmable Read-Only Memory (EEPROM) and hardware monitoring allowing temperature detection, voltage readings while following M.2 standard specifications. The EEPROM can include the FRU allowing a technician to maintain and repair the system.

[0018] FIGS. 4-6 illustrate a system diagram of the riser card 100 and the plurality of data ports 108. The system diagram shows mapping for the plurality of data ports coupling the first interface 102 with the two second interfaces 104. The first interface 102 and second interfaces 104 are coupled by the switching module 106. The switching module 106 allows users to select the measurement system of the riser card 100. In at least one embodiment, the riser card 100 can support PCIe 1x4 and 2x2 and allow a user to select the measurement system in order to control the switch module.

[0019] The switching module 106 can be a multiplexer (MUX) having a plurality Integrated Circuits (IC) with multiplexing capability and a routing design configured to avoid propagation delay and allow successful transition of PCIe 1x4 and PCIe 2x2. The switching module 106 can be a chip, a field-programmable gate array (FPGA), or any other controller. The switching module 106 can be any PCIe switch supporting a PCIe high speed signal.

[0020] The switching module 106 can allow the riser card 100 to operate a component 114 in a PCIe 1x4 arrangement allowing all of the plurality of data ports 108 to be utilized by one component 114. The switching module 106 can also support PCIe 2x2, allowing a portion of the plurality of data ports 108 to one of the second interfaces 104 and the remaining portion of the plurality of data ports 108 to the other second interface 104. PCIe 2x2 can allow the system to achieve maximum benefits on dual path redundancy, increased performance, and increasing the elasticity of the system structure while lowering the cost of design and overall complexity.

[0021] The switching module 106 is coupled to a control port 118 of the first interface 102 and configured for selectably coupling the plurality of data ports to at least one of the second interfaces 104 based on a control signal. When the control signal is low, the system is in PCIe 2x2 and when the control signal is high, the system is in PCIe 1x4. As can be appreciated in FIG. 4, the control port 118 is coupled with switch module_2; however, in other embodiments the control port 118 can be coupled with switch module_1, switch module_2, or a combination thereof.

[0022] The switching module 106 can couple a first interface 102 with two second interfaces 104. In the illustrated embodiment, the first interface 102 is shown as an NVMe SSD connector and the second interfaces 104 are shown as M.2 connectors, each receiving an M.2 PCIe SSD component. The switch module 106 has two switch modules switch module_1 106a and switch module_2 106b to support PCIe 1x4 and 2x2. The first interface 102

has a plurality of data ports 108, shown in FIG. 4 as [0,1] and [0,1]/[2,3], couplable with the second interfaces 104 via the switch module. Each second interface 104 can have a corresponding plurality of data ports 116, shown in FIG. 4 as [0,1] and [2,3].

[0023] As can be appreciated in FIG. 5, the switch module 106 is in a second routing mode and receives a control signal corresponding to operating the system in PCIe 1x4. The switch module_1 106a connects B1 and A1 while switching module_2 106b connects B2 and A2. Switch module_2 shifts to connect first interface 104 connector [2:3] with component 114 [2:3] allowing PCIe 1x4 for system testing. While FIG. 6 is drawn to B2 of switch module_2 106b connecting with [2,3] of component 114a, other arrangements can be implemented such as C1 of switch module_1 connecting with [2,3] of component 114b, or a combination thereof.

[0024] As can be appreciated in FIG. 6, the switch module 106 is in a first routing mode and receives a control signal corresponding to operating the system in PCIe 2x2. In PCIe 2x2, C1 (not shown) of switch module_1 106a is not routing while A1 connects to B1 and A2 of switch module_2 106b connects C2. Switch module_1 106a connects B1 with component 114a, shown as M.2 PCIe SSD_1 [0:1], and switch module_2 106b connects C2 with component 114b, shown as M.2 PCI SSD_2 [0:1]. Each component 114a, 114b receives a portion of the plurality of data ports 108.

[0025] In the illustrated embodiment, the plurality of data ports 108 is four [0,1] and [2,3] and the portion of the plurality of data ports is two, [0:1]. Each component 114 is receiving two of the available four data ports. While the illustrated embodiment is drawn to switch module_1 coupling with data ports [0,1] of the first interface 102 and switch module_2 coupling with data ports [2,3], the riser card 100 can be implemented with switch module_1 and switch module_2 reversed.

[0026] Referring to FIG. 7, a flowchart is presented in accordance with an example embodiment. The example method 700 is provided by way of example, as there are a variety of ways to carry out the method 700. The method 700 described below can be carried out using the configurations illustrated in FIGS. 1-6, for example, and various elements of these figures are referenced in explaining example method 700. Each block shown in FIG. 7 represents one or more processes, methods or subroutines, carried out in the example method 700. Furthermore, the illustrated order of blocks is illustrative only and the order of the blocks can change according to the present disclosure. Additional blocks may be added or fewer blocks may be utilized, without departing from this disclosure. The example method 700 can begin at block 702.

[0027] At block 702, an apparatus having a first interface of a first type supporting a plurality of a data ports, and a second interface and a third interface of a second type supporting at least a portion of the plurality of data portions, and a switching module, receives, at the switch-

ing module, a control signal for selectably coupling the plurality of data portions of the first interface with at least one of the second interface and the third interface.

[0028] At block 704, the switching module selects, in response to the control signal, a first routing mode or a second routing mode.

[0029] At block 706, in the first routing mode the switching module routes the signals for the plurality of data ports at a first interface to one of the second interface and the third interface.

[0030] At block 708, in the second routing mode the switching module routes at least a portion of the signals for the plurality of data ports to the second interface and the remaining portion of the data ports to the third interface.

[0031] At block 710, the switching module can monitor apparatus operating temperature, voltage, and operating statistics.

[0032] It is believed the exemplary embodiment and its advantages will be understood from the foregoing description, and it will be apparent that various changes may be made thereto without departing from the spirit and scope of the disclosure or sacrificing all of its advantages, the examples hereinbefore described merely being preferred or exemplary embodiments of the disclosure.

Claims

1. An apparatus, comprising:

- a first interface of a first type supporting a plurality of data ports;
- a second interface of a second type supporting at least a portion of the plurality data ports;
- a third interface of the second type; and
- a switching module coupled to a control port of the first interface and configured for selectably coupling the plurality of data ports to at least one of the second interface and the third interface based on a signal at the control port.

2. The apparatus of claim 1, wherein the signal indicates one of a first routing mode and a second routing mode for the switching module.

3. The apparatus of claim 2, wherein the first routing mode comprises routing the signals for the plurality of data ports at the first interface to the second interface, and wherein the second routing mode comprising routing signals for a portion of the plurality of data ports to the second interface and routing signals for a remaining portion of the plurality of data ports to the third interface.

4. The apparatus of claim 2, wherein the plurality of data ports comprises four data ports, and wherein

the portion of the plurality of data ports comprises a first two of the plurality of data ports.

5. The apparatus of claim 1, wherein the first interface comprises a U.2 interface and wherein each of the second interface and the third interface comprises a M.2 interface. 5
6. The apparatus of claim 1, wherein each of the second interface and third interface are configured to couple with a component. 10
7. The apparatus of claim 6, wherein the component is a PCIe SSD. 15
8. The apparatus of claim 6, wherein the component is hot-swappable, each second interface and third interface allowing removal from the component during operation. 20
9. The apparatus of claim 1, further comprising a hardware monitor capable of detecting device temperature and voltage usage. 25
10. A method for supporting an apparatus with two interfaces, a first interface of a first type and a second interface of a second time, the method comprising: 25
 - receiving, at a switching module, a control signal for selectably coupling a plurality of data ports of a first interface with at least one of a second interface and a third interface; 30
 - selecting, at the switching module, in response to the control signal a first routing mode or a second routing mode; 35
 - when in the first routing mode:
 - routing, at the switching module, the signals for the plurality of data ports at the first interface to one of the second interface and the third interface; and 40
 - when in the second routing mode:
 - routing, at the switching module in the second routing mode, at least a portion of the signals for the plurality of data ports at the first interface to the second interface and remaining portion of the plurality of data ports to the third interface, 45
 - wherein the first interface is of a first type and the second interface and the third interface are of a second type. 50
11. The method of claim 10, further comprising monitoring, at the switching module, apparatus operating temperature, voltage, and operating statistics. 55

12. The method of claim 10, wherein the plurality of data ports comprises four data ports, and wherein the portion of the plurality of data ports comprises a first two of the plurality of data ports.

13. The method of claim 10, wherein the first interface comprises a U.2 interface and wherein each of the second interface and the third interface comprises a M.2 interface.

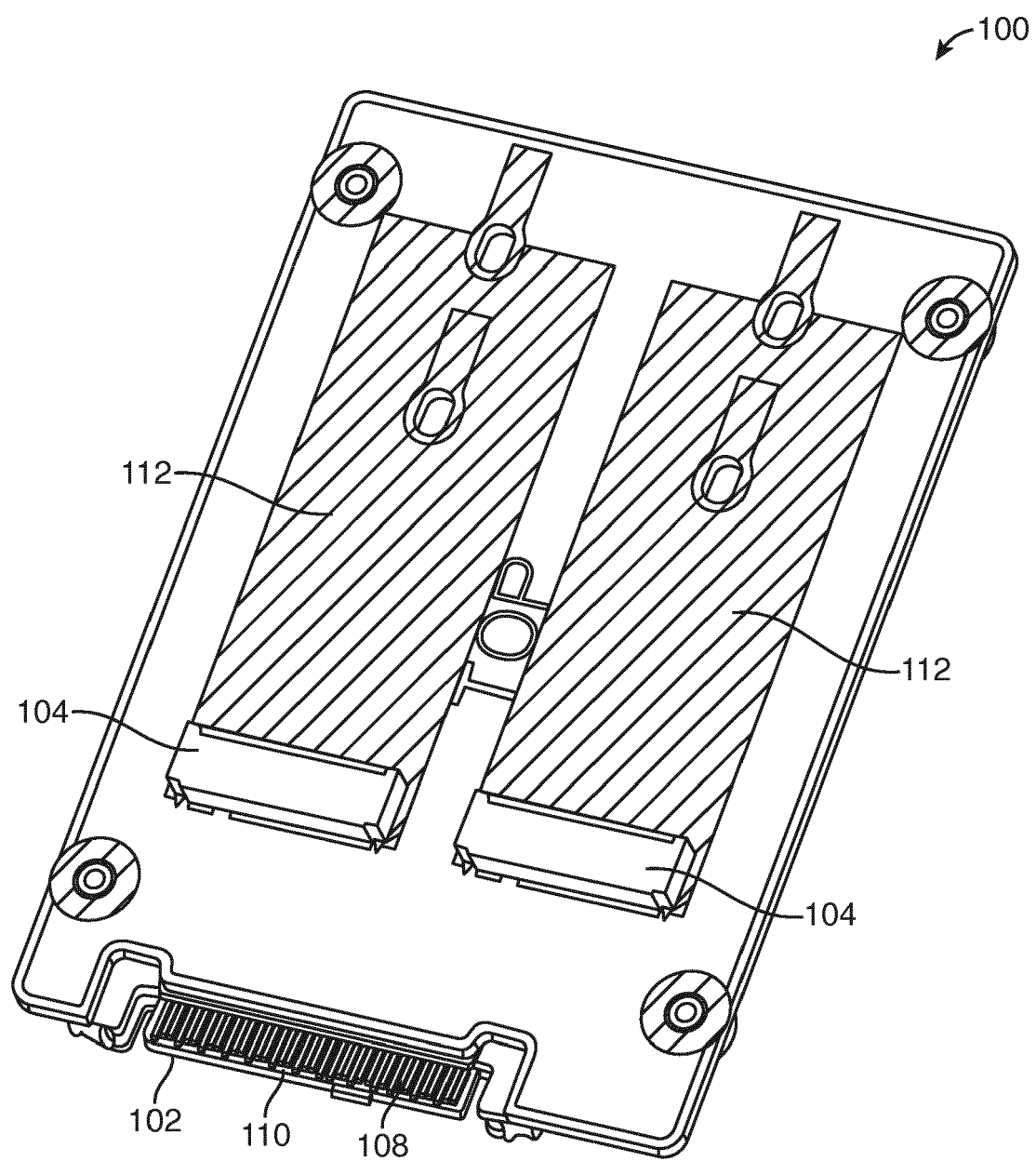


FIG. 1

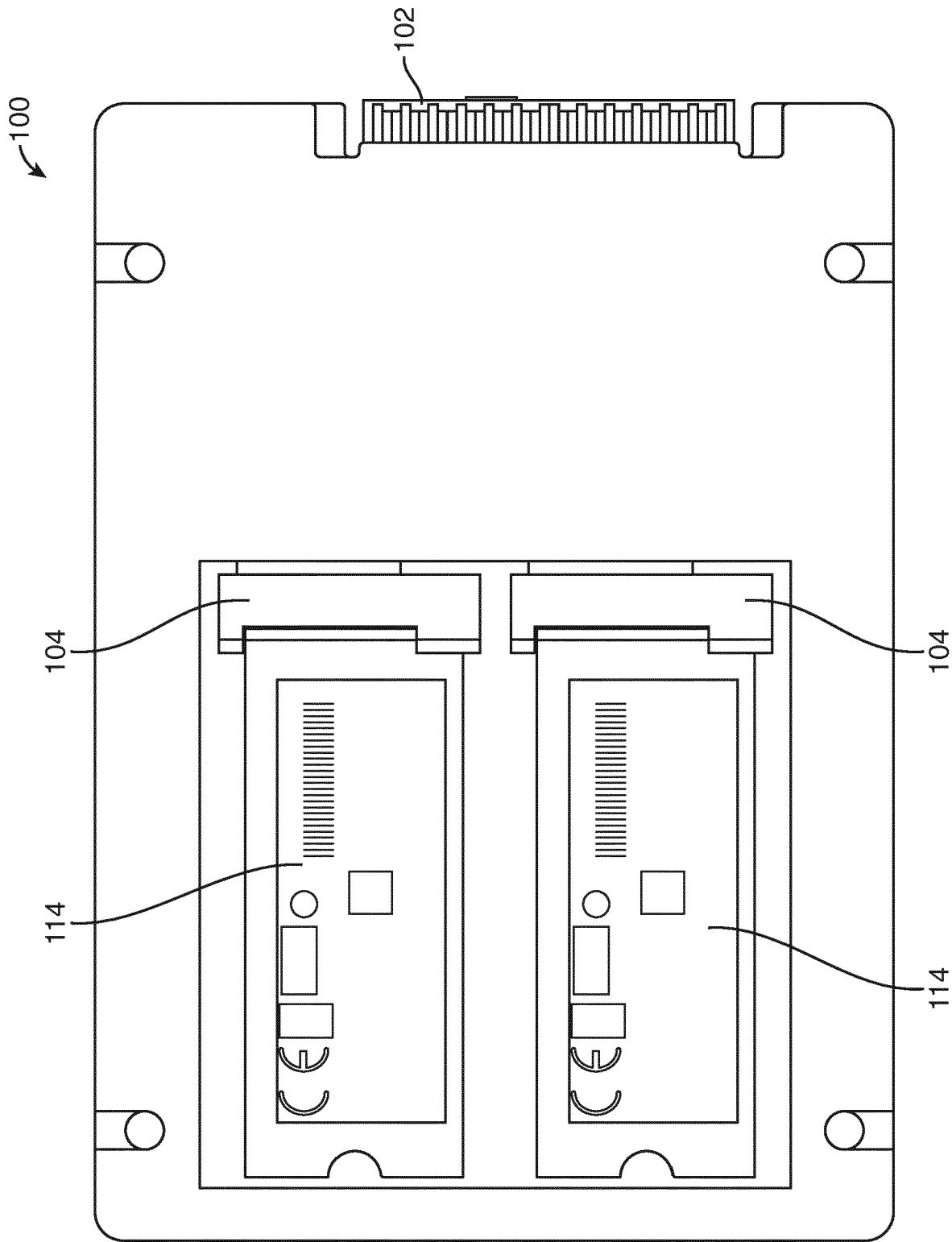


FIG. 2

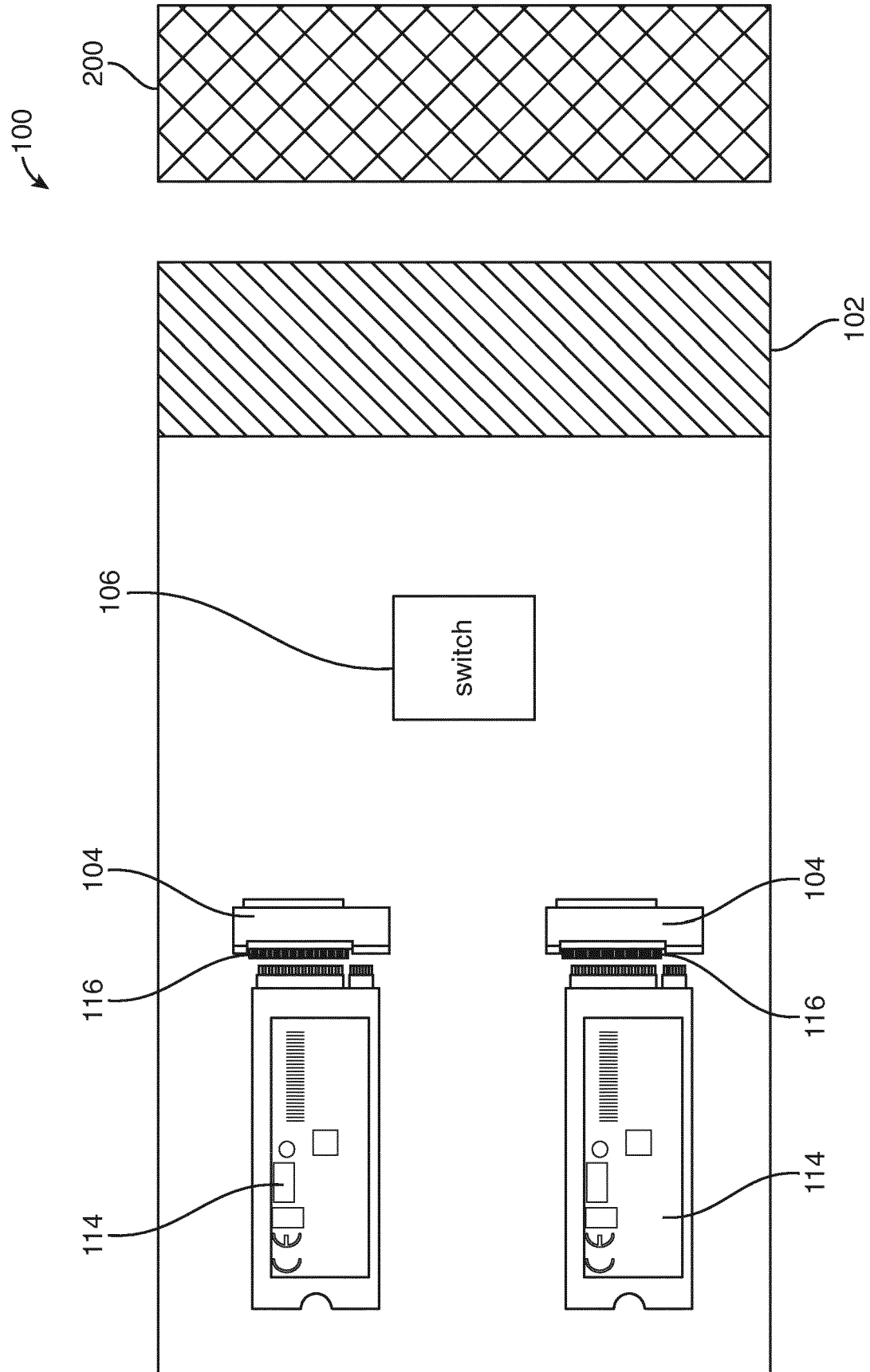


FIG. 3

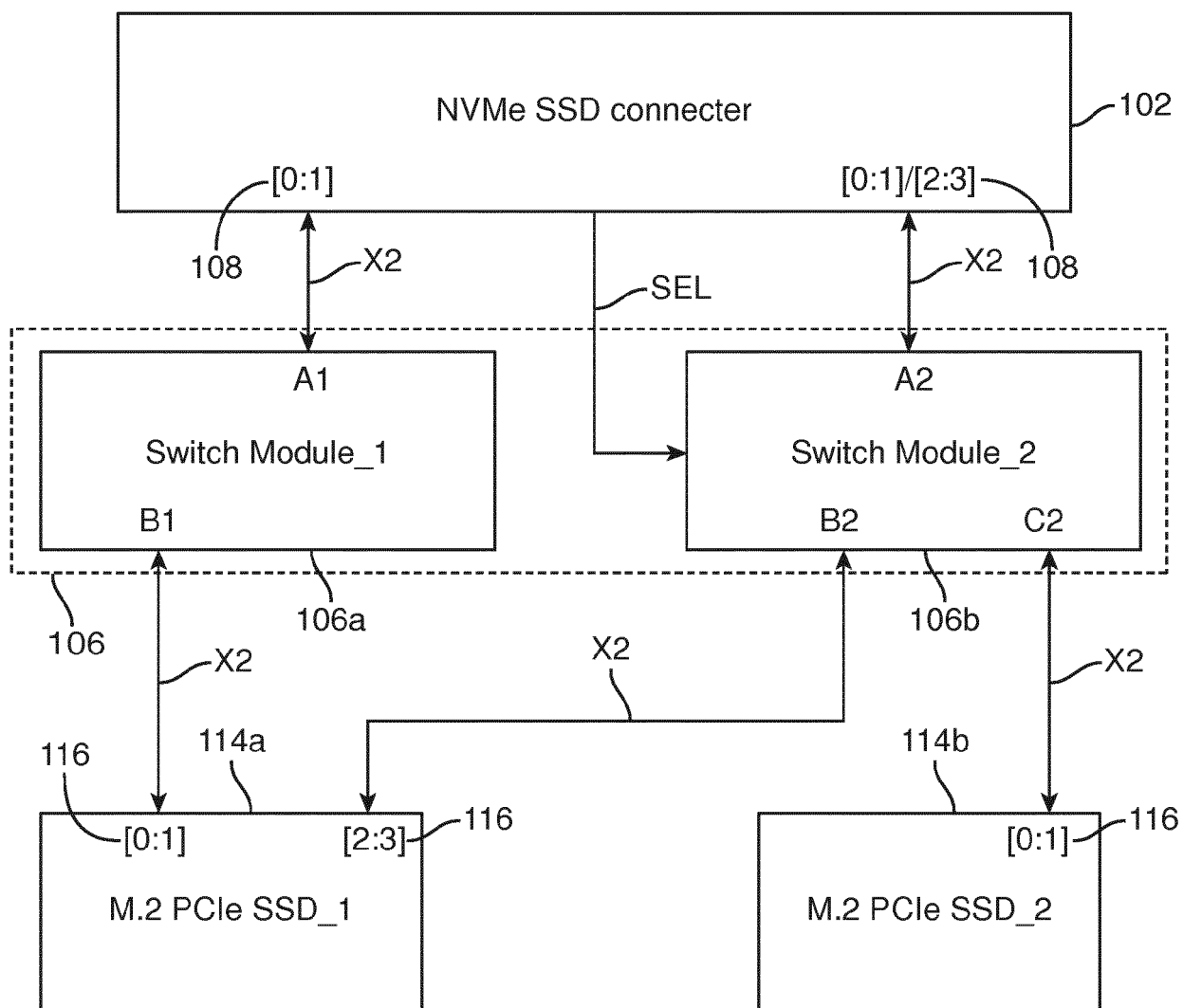


FIG. 4

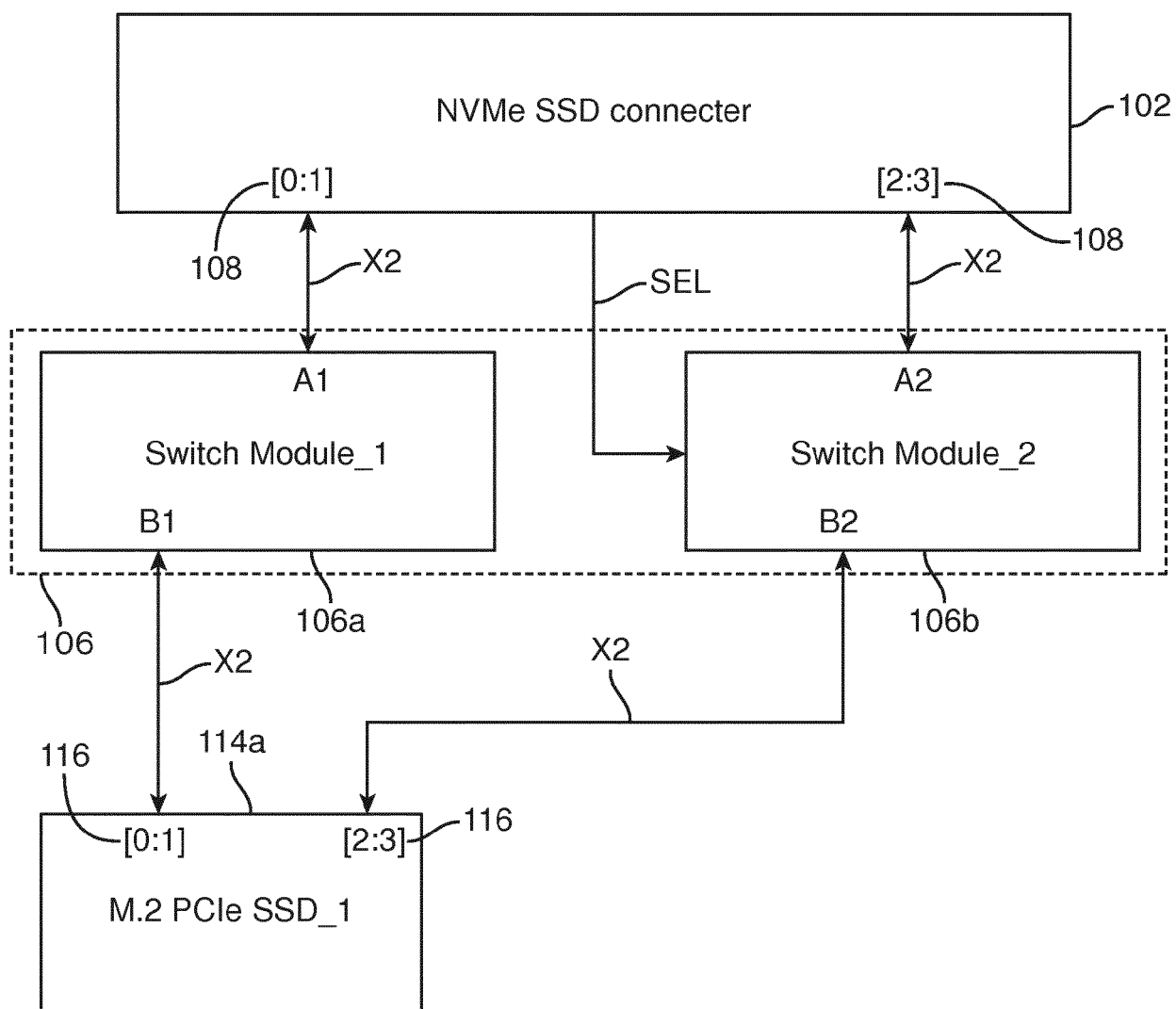


FIG. 5

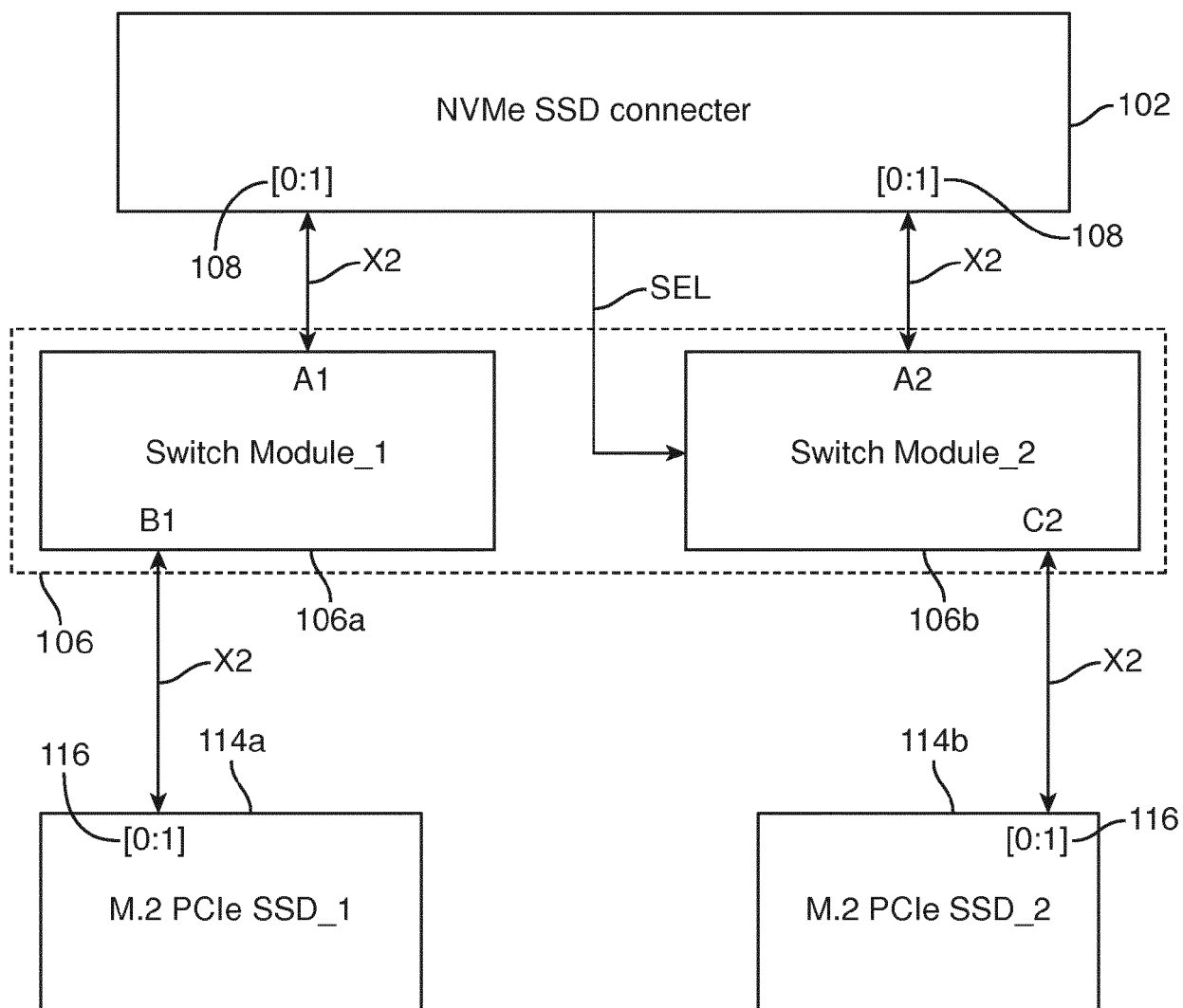


FIG. 6

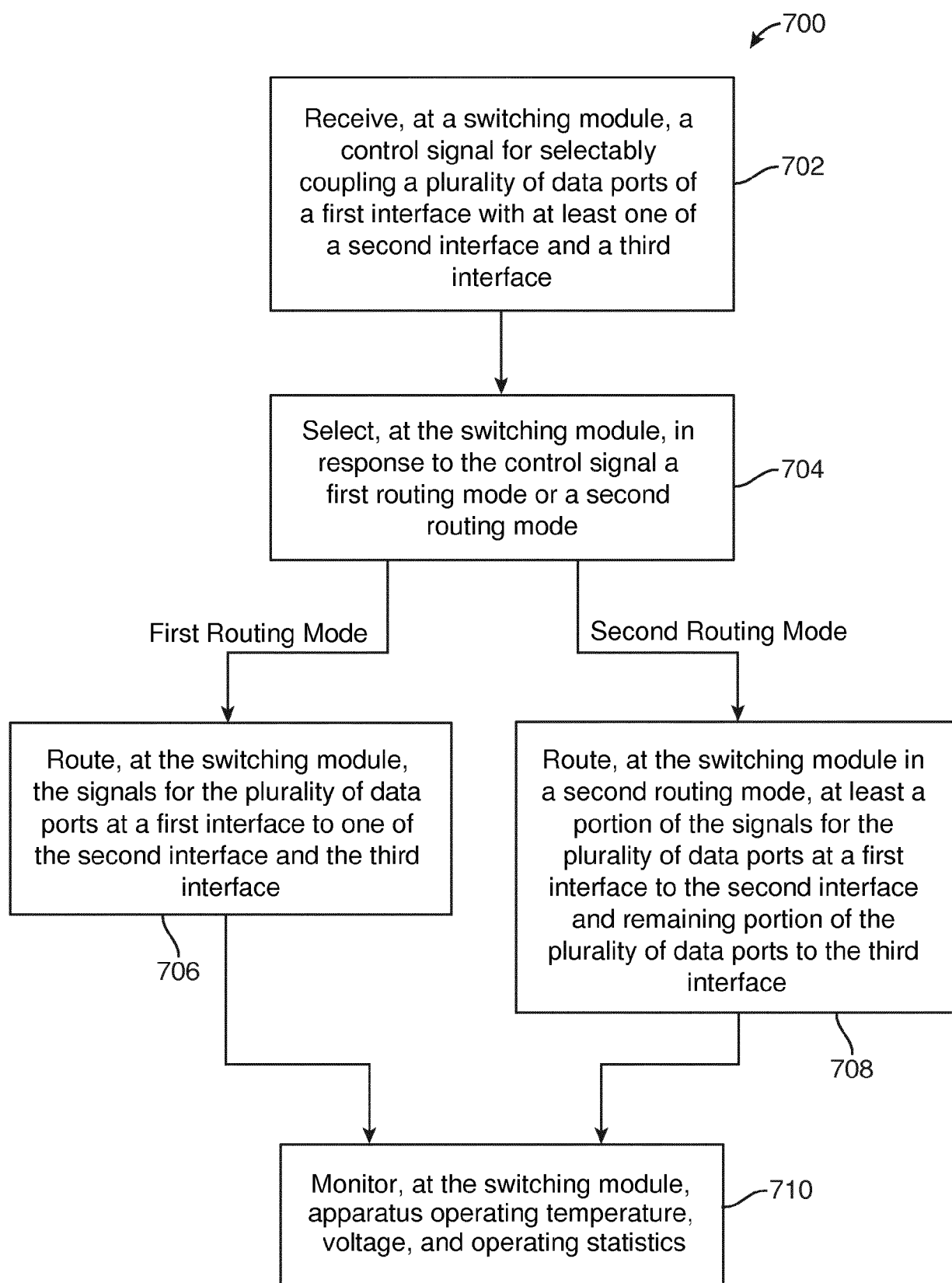


FIG. 7



EUROPEAN SEARCH REPORT

Application Number
EP 17 17 8359

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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Y	US 2011/219158 A1 (DAVIS DAVID M [GB] ET AL) 8 September 2011 (2011-09-08) * paragraphs [0034] - [0041]; figures 2-4 *	1-13	
			TECHNICAL FIELDS SEARCHED (IPC)
			G06F
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 8 November 2017	Examiner Albert, Jozsef
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03.82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 17 17 8359

5 This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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08-11-2017

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