



(51) International Patent Classification:

G06N 7/00 (2006.01) *G06N 99/00* (2010.01)
G06F 17/11 (2006.01)

(21) International Application Number:

PCT/FI2015/050580

(22) International Filing Date:

4 September 2015 (04.09.2015)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: **NOKIA TECHNOLOGIES OY** [FI/FI];
Karaportti 3, FI-02610 Espoo (FI).

(72) Inventors: **RONNOW, Troels Frimodt**; 61 Ellis Road,
Cambridge CB2 9BG (GB). **WABNIG, Joachim**; 62 Hali-
fax Road, Upper Cambourne CB23 6AX (GB).

(74) Agents: **NOKIA TECHNOLOGIES OY** et al.; Ari
Aarnio, IPR Department, Karakaari 7, FI-02610 Espoo
(FI).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD AND APPARATUS FOR OPTIMIZATION

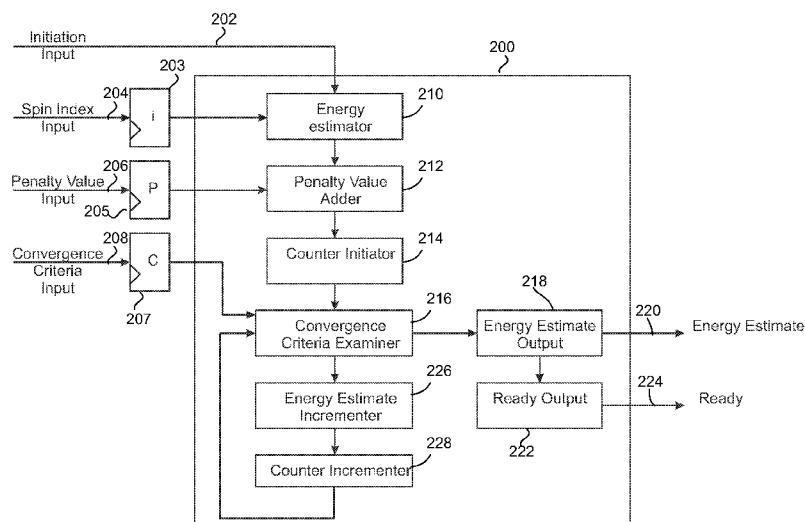


Fig. 2

(57) Abstract: An approach is provided for solving optimization problems. The present invention also relates to a method comprising receiving a spin index and receiving one or more convergence criteria. The spin index is used to estimate an energy value; wherein the convergence criteria and the estimated energy value are used to determine whether the convergence criteria was fulfilled. There are also disclosed apparatuses for implementing the method and a computer readable storage medium stored with code thereon for implementing the method.

METHOD AND APPARATUS FOR OPTIMIZATION

5 TECHNOLOGICAL FIELD

[0001] The present invention relates generally to solving optimization problems. More particularly, the present invention relates to a method for finding a solution to binary optimization problems. The present invention also relates to apparatuses and computer program products for implementing the method and circuitry relating to the binary optimization.

BACKGROUND

[0002] This section is intended to provide a background or context to the invention that is recited in the claims. The description herein may include concepts that could be pursued, but are not necessarily ones that have been previously conceived or pursued. Therefore, unless otherwise indicated herein, what is described in this section is not prior art to the description and claims in this application and is not admitted to be prior art by inclusion in this section.

[0003] Quadratic binary optimization (QUBO) is a particular type of problems. Such problems may be both extremely awkward for digital computers and important. Many cutting-edge artificial intelligence (AI) involves solving such problems. A Boltzmann machine may solve binary optimization and may accelerate sampling from a Boltzmann distribution.

[0004] An aim of the quadratic binary optimization is to minimize a quadratic function in which decision variables may only take certain discrete values, such as +1 and -1. The idea of quadratic binary optimization may be adapted to different kinds of programmable circuits. Quadratic binary optimization problems may arise in operational research such as planning, scheduling, routing, finance such as portfolio optimization, physics such as spin glass, machine learning and many more.

30

SOME EXEMPLARY EMBODIMENTS

[0005] Examples of hardware architecture for discrete optimization and a programming method are provided. Specifically, examples are provided which represent a variant of quadratic binary optimization.

5 [0006] An aim is to obtain an apparatus and method for solving optimization problems.

[0007] According to one embodiment, an apparatus comprises

a first input for receiving a spin index;

a third input for receiving one or more convergence criteria;

10 an energy estimation block adapted to use the spin index to estimate an energy value; and

a convergence estimation block adapted to use the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

[0008] According to one embodiment, a method comprises

15 receiving a spin index;

receiving one or more convergence criteria;

using the spin index to estimate an energy value; and

using the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

20 [0009] According to one embodiment, an apparatus comprises at least one processor; and at least one memory including computer program code the at least one memory and the computer program code configured to, with the at least one processor, cause the apparatus to perform at least the following:

receive a spin index;

25 receive one or more convergence criteria;

use the spin index to estimate an energy value; and

use the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

[0010] According to one embodiment there is provided a computer readable storage medium stored with code thereon for use by an apparatus, which when executed by a processor, causes the apparatus to perform:

receive a spin index;

5 receive one or more convergence criteria;

use the spin index to estimate an energy value; and

use the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

[0011] According to one embodiment, an apparatus comprises:

10 means for receiving a spin index;

means for receiving one or more convergence criteria;

means for using the spin index to estimate an energy value; and means for using the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

15 [0012] Still other aspects, features, and advantages of the invention are readily apparent from the following detailed description, simply by illustrating a number of particular embodiments and implementations.

[0013] The invention is also capable of other and different embodiments, and its several details can be modified in various obvious respects, all without departing from the spirit and scope of the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

20

[0014] There are provided examples of architectures for quantum annealing at finite temperature.

BRIEF DESCRIPTION OF THE DRAWINGS

25 [0015] The embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings:

[0016] FIG. 1a illustrates a fully connected graph for a single simulated annealing slice;

[0017] FIG. 1b illustrates a fully connected path for a quantum annealing system using time discretization;

[0018] FIG. 2 depicts a simulated annealing unit for updating spins in the Ising model based on converged criteria, in accordance with an embodiment;

5 [0019] FIG. 3 the operation of the simulated annealing unit as a flow diagram, in accordance with an embodiment;

[0020] FIG. 4a shows an embodiment as a part of a system on a chip in which one or more simulated annealing slices are used as a part of the chip, in accordance with an embodiment;

10 [0021] FIG. 4b shows an embodiment as a standalone chip, in accordance with an embodiment;

[0022] FIG. 4c shows an embodiment as a part of a system on a chip with additional observables, in accordance with an embodiment;

15 [0023] FIG. 4d shows an embodiment as a chip with custom observables, in accordance with an embodiment; and

[0024] FIG. 5 is a diagram of some components of a computing apparatus comprising the computational architecture for binary optimization according to an exemplary embodiment.

20 DESCRIPTION OF EXAMPLE EMBODIMENTS

[0025] In the following description, for the purposes of explanation, some specific details are set forth in order to provide a thorough understanding of the embodiments of the invention. It is apparent, however, to one skilled in the art that the embodiments may be practiced without these specific details or with an equivalent arrangement. In
25 other instances, well-known structures and devices are shown in block diagram form in order to avoid unnecessarily obscuring the embodiments of the invention.

[0026] Embodiments are provided to show how to implement in hardware quadratic binary optimization.

30 [0027] Binary optimization problems may occur in many fields of science and technology. Many scheduling and routing and planning tasks are binary optimization

problems. Also problems in the field of machine learning can be formulated as binary optimization problems. One type of a problem encountered in binary optimization and machine learning is that of minimizing binary quadratic functionals

$$E = \sum_i^N \sum_j^{i-1} \omega_{ij} b_i b_j + \sum_i^N a_i b_i$$

5 (1)

where b_i are binary variables and $\{\omega_{ij}\}$ and $\{a_i\}$ define a problem of interest. The minimization problem of Equation (1) is equivalent to finding the optimal configurations of an Ising spin glass with an energy functional given by

$$H = \sum_i^N \sum_j^{i-1} J_{ij} s_i s_j + \sum_i^N h_i s_i$$

10 (2)

where J_{ij} and h_i are floating points (possibly negative) and s_i are representing physical spins that can either be up or down. The variables J_{ij} represent interactions between spins s_i and s_j and h_i represents an external field affecting to the spin s_i .

[0028] Every configuration s yields a corresponding energy $E_s \equiv H(s)$ which is
15 minimal if s is an optimal solution. Often the optimal solution is not found and it is therefore instructive to use the residual energy $E_{res} = E(s) - E_{opt}$ as a measure of how a given algorithm perform.

[0029] Many different techniques may be used to obtain good solutions for Equation
20 (1) including using standard programming techniques such as divide-and-conquer, backtracking, heuristic searches, quantum optimization hardware and in particular quantum annealing.

[0030] In quantum annealing, one tries to find the optimal solution to Equation (2) through an evolution of

$$H_Q = A(t)H_D + B(t)H_P$$

25 (3)

with

$$H_D = \sum \sigma_i^x \quad \text{and} \quad H_P = \sum_{i,j} J_{ij} \sigma_i^z \sigma_j^z + \sum h_i \sigma_i^z$$

(4)

where H_P replaces the original problem in Equation (2) and σ^z and σ^x are Pauli operators. If one uses a coherent unitary evolution, it may not be possible to simulate this system much beyond 30 variables (or spins). However, simulating the thermal equilibrium distribution may be done with Monte Carlo methods for thousands of variables. In particular, if one splits the path-integrals by discretizing the imaginary time, one may arrive at a model which reads

$$H_{Qcl} = \sum_{k=1}^M \left(\sum_{i=1}^N \gamma_i s_i^{(k)} s_i^{(k+1)} + \sum_{i<j} J_{ij} s_j^{(k+1)} s_j^{(k+1)} + \sum_{i=1}^N h_i s_i^{(k+1)} \right)$$

(5)

where $\gamma = B / \Delta\tau$ with

$$B(\Delta\tau\Gamma) = -\frac{1}{2} \ln(\tanh(\Delta\tau\Gamma))$$

(6)

and $\Delta\tau = \beta / M$ for a discretization using M Trotter slices. If the original problem in Equation (2) is described in D dimensions, the corresponding Trotterised problem in Equation (5) is similar to that of Equation (2), but in D + 1 dimensions. This is illustrated in Figures 1a and 1b. Figure 1a illustrates a fully connected graph for a single simulated annealing slice and Figure 1b illustrates a fully connected path for the quantum annealing system using time discretization. Simulation of quantum annealing in this formulation may be performed, for example, as discrete time quantum Monte Carlo annealing (DTQ). If Equation (5) would only consist of the two last terms in the sum over k, this equation would just describe M independent identical problems. The additional term serves to pairwise couple identical spins between two neighboring replicas.

[0031] Implementing quantum annealing in physical hardware may be expensive and may suffer from several limitations such as limited connectivity, calibration and programming errors, and may perform worse than similar classical optimizers.

[0032] In the following a more detailed description is provided of a design using complementary metal oxide semiconductor (CMOS) technology which may be fast, may have high connectivity and may use little logic. In accordance with an embodiment, a simulated annealing apparatus may simulate certain behavioral aspects by mimicking quantum tunneling using the discretized Monte Carlo approach described above. Furthermore, for ordinary simulated annealing full connectivity may be hard to realize in hardware implementations. The following approach may solve this problem as well, although the same circuit may also be used for lower degrees of connectivity.

[0033] In simulated annealing of an Ising spin glass a spin s_i changes sign based on the criteria

$$r < \exp(-\beta \Delta E_i) \quad (7)$$

where r is a random number between 0 and 1, $\beta = T^{-1}$ is the inverse temperature and ΔE_i is given by

$$\Delta E_i = -2s_i \left(h_i + \sum_j^N J_{ij} s_j \right) \quad (8)$$

[0034] Let the couplings J_{ij} be on the interval $[-1; 1]$ and represent it using B bits of

precision as $J_{ij} = -1 + \sum_{b=0}^B J_{ij}^{(b)} 2^{-b} \approx \frac{1}{2} \sum_{b=0}^B (2J_{ij}^{(b)} - 1) 2^{-b}$

$$(9)$$

with $J_{ij}^{(b)}$ being binary variables describing the value of J_{ij} . The criteria in Equation (7), can now be recast in the form

$$T \log(r) < 2s_i \left(h_i + \frac{1}{2} \sum_j^N s_j \sum_{k=0}^B (2J_{ij}^{(k)} - 1) 2^{-k} \right) \quad (10)$$

[0035] After interchanging the sums, the criteria can be expressed in bit-wise operations

$$\begin{aligned}
T \log(r) - 2s_i h_i &< s_i \sum_{k=0}^B 2^{-k} \sum_j^N s_j (2J_{ij}^{(k)} - 1) \\
&= s_i \sum_{k=0}^B 2^{-k} \sum_j^N (2b_j - 1)(2J_{ij}^{(k)} - 1) \\
&= s_i \sum_{k=0}^B 2^{-k} \sum_j^N (1 - 2(b_j + J_{ij}^{(k)} \bmod 2)) \\
&= s_i \sum_{k=0}^B 2^{-k} [N - 2P(b \oplus J_i^{(k)})] \\
&= \sum_{k=0}^B 2^{-k} \varepsilon_i^{(k)}
\end{aligned}$$

with

$$\varepsilon_i^{(k)} = s_i [N - 2P(b \oplus J_i^{(k)})] \quad (11)$$

- 5 where b and $J_i^{(k)}$ are N -bit vectors representing the k 'th bit contribution of interaction of the i spin to all other spins in the system. The function $P(x)$ is a population count function which counts number of bits with value 1. Notably,

$$-N \leq \varepsilon_i^{(k)} \leq N \quad (12)$$

- 10 It may now be possible to compute the energy difference ΔE_i to any desired precision, and it may therefore be useful to introduce a partial estimate of $\Delta E_i^{(t)}$ as

$$-\Delta E_i^{(t)} = 2s_i h_i + \sum_{k=0}^t 2^{-k} \varepsilon_i^{(k)} \quad (13)$$

- 15 **[0036]** Then, the two possible solutions for Equation (10) may be separated at $T \log(r) + \Delta E_i = 0$. For an approximation using t bits the left-hand side is bound from above as

$$T \log(r) + \Delta E_i^{(t)} = \sum_{k=t+1}^B 2^{-k} \varepsilon_i^{(k)} \leq N \sum_{k=t+1}^B 2^{-k} < 2N2^{-t-1} \quad (14)$$

- [0037]** Likewise, the lower bound may be found as

$$T \log(r) + \Delta E_i^{(t)} = \sum_{k=t+1}^B 2^{-k} \varepsilon_i^{(k)} \geq -N \sum_{k=t+1}^B 2^{-k} > -2N2^{-t-1}$$

(15)

[0038] To determine whether the criteria of Equation (10) is fulfilled, the number of iterations t of the partial estimate $\Delta E_i^{(t)}$ may be chosen such that

$$|T \log(r) + \Delta E_i^{(t)}| > 2N2^{-t-1} = N2^{-t}$$

(16)

[0039] This criteria may be fulfilled long before exhausting all the B bits making it a much more efficient method to evaluate the flipping criteria of Equation (7). This idea may be extended to include a penalty term in the local energy difference ΔE_i which may make this approach directly applicable to the original problem in Equation (5).

[0040] Next, it will be summarized how this approach could be incorporated into a field programmable gate array (FPGA) or an application specific integrated circuit (ASIC) to accelerate the performance of the algorithm. Figure 2 depicts a simulated annealing unit 200 for updating spins in the Ising model based on converged criteria, in accordance with an embodiment, and Figure 3 illustrates the operation of the simulated annealing unit 200 as a flow diagram, in accordance with an embodiment. In Figure 2, it is shown as a block diagram how the inner most IP core would look like for an ASIC, with four incoming signals and two out-going signals. This circuit may then be deployed in parallel or alternatively sequentially. In accordance with an embodiment, all spins may be updated once or more using the described spin-update unit as a simulated annealing slice (SA slice).

[0041] The simulated annealing unit 200 may comprise an initiation input 202 for initiating the operation of the circuitry of the simulated annealing unit 200 (block 300 in the flow diagram of Figure 3). The simulated annealing unit 200 may further comprise an input 204 for a spin index, an input 206 for a penalty term, and an input 208 for convergence criteria. The spin index input 204, the penalty term input 206, and the convergence criteria input 208 may be connected to latches 203, 205, 207, respectively, to latch the input signals, wherein outputs of the latches 203, 205, 207 may be coupled to corresponding blocks of the simulated annealing unit 200.

[0042] The initiation input 202 may be coupled to an energy estimation block 210. Also the spin index input 204 may be coupled via the latch 203 to the energy estimation block 210, wherein the energy estimation block 210 may set 302 estimated energy to a local field multiplied by the i'th spin value. The value of the estimated energy may be provided to a penalty adding block 212, which also receives 304 the penalty term from the penalty term input 206 via the latch 205 and adds 306 the penalty term to the estimated energy value. A counter initialization block 214 may initiate 308 a counter b to an initialization value, which may be, for example, 0. The sum of the estimated energy and the penalty term may be provided to a convergence estimation block 216. The convergence estimation block 216 may receive a convergence criteria from the convergence criteria input 208 via the latch 207 and use the convergence criteria to determine 310 whether the sum of the estimated energy and the penalty term converges or not. If the convergence estimation block 216 determines 312 that the sum of the estimated energy and the penalty term converges, the convergence estimation block 216 may provide 314 the sum of the estimated energy and the penalty term to an energy output estimation block 218. The energy output estimation block 218 may provide 316 the energy estimate to an energy estimate output 220 and initiate 318 a ready triggering block 222 to form a ready signal at a ready signal output 224 to indicate that the simulated annealing unit 200 has obtained an energy estimate.

[0043] However, if the convergence estimation block 216 determines 320 that the sum of the estimated energy and the penalty term does not converge, an increment block 226 may increment 322 the energy estimate for every incoming spin j by $J_{ij}^{(b)} s_i s_j$. A counter incrementing block 228 may increment 324 the counter b, and the incremented energy estimate is provided 326 to the convergence estimation block 216. Hence, the convergence estimation block 216 may now again determine, whether the incremented energy estimate fulfills the convergence criteria.

[0044] If the apparatus is used as a classical simulated annealer the penalty term may be taken to zero. However, if a simulated quantum annealing unit as in Equation (5) would be implemented, many simulated annealing slices may be put together linking through the penalty term. Figures 4a to 4d illustrate some possible embodiments of the simulated annealing apparatus. Figure 4a shows an embodiment as a part of a system on a chip (SoC) 400 in which one or more simulated annealing slices 200 are used as

a part of the chip 400. The chip 400 may thus also comprise, for example, a controller 402 (CPU, central processing unit) and/or other building blocks 404, such as memory. The chip 400 may further comprise an interface 406 for transferring signals between the simulated annealing slices 200 and the controller 402 and/or other building blocks 404 of the chip 400. Figure 4b shows an embodiment as a standalone chip. In other words, the chip 400 comprises a multiple of simulated annealing slices 200. Figure 4c shows an embodiment as a part of a system on a chip with additional observables 408. Figure 4d shows an embodiment as a chip with custom observables 408. The embodiments may be performed such that a simulation unit (for instance a printed circuit board (PCB)) can be extended over several integrated chips or field programmable gate arrays (FPGA). The system on a chip implementation may include a communication interface to extend the number of simulated annealing slices, and may or may not include dedicated units to compute observables such as correlators, minimum energy found over time etc. The standalone chips may include a programming interface and may or may not include an interface to extend the number of simulated annealing slices over several chips. Likewise, the standalone chips may or may not include dedicated circuits to measure observables.

[0045] Figure 5 illustrates an example of a computing device 100 in which the computing circuitry 200 may be utilized. The computing device 100 may comprise the computing circuitry 200 implemented e.g. in a FPGA circuit or another programmable circuitry. The inputs and outputs of the computing circuitry 200 may be connected to an interface circuitry 104 which comprises means for providing information to the computing circuitry 200, e.g. to initialize some parameters and initial values for the couplings J_{ij} e.g. by setting local floating point memory into appropriate values, and for obtaining information from the computing circuitry 200. Information obtained from the computing circuitry 200 may comprise e.g. computation results.

[0046] The computing device 100 may also comprise a display 110 for displaying information to the user, and a keyboard 112 and/or another input device so that the user may control the operation of the computing device 100 and input parameters, variables etc. to be used by the computing circuitry 102. There may also be communication means 114 for communicating with a communication network such as

the internet, a mobile communication network and/or another wireless or wired network.

[0047] There may also be provided a processor 116 for controlling the operation of the computing device and the elements of the computing device. In accordance with an embodiment, the processor 116 may be implemented in the same chip than the simulated annulation units 200, as is depicted in Figures 4a and 4c, wherein the interface 104 may also be part of the chip 400, or the processor 116 and possibly also the interface 104 may be separate from the chip 400. In accordance with an embodiment, the computing unit 200 may comprise one or more controllers in addition to the processor 116.

[0048] The term computer-readable medium is used herein to refer to any medium that participates in providing information to processor 116, including instructions for execution. Such a medium may take many forms, including, but not limited to, non-volatile media, volatile media and transmission media. Non-volatile media include, for example, optical or magnetic disks, such as storage device. Volatile media include, for example, dynamic memory 118. Transmission media include, for example, coaxial cables, copper wire, fibre optic cables, and carrier waves that travel through space without wires or cables, such as acoustic waves and electromagnetic waves, including radio, optical and infrared waves. Signals include man-made transient variations in amplitude, frequency, phase, polarization or other physical properties transmitted through the transmission media. Common forms of computer-readable media include, for example, a floppy disk, a flexible disk, hard disk, magnetic tape, any other magnetic medium, a CD-ROM, CDRW, DVD, any other optical medium, punch cards, paper tape, optical mark sheets, any other physical medium with patterns of holes or other optically recognizable indicia, a RAM, a PROM, an EPROM, a FLASH-EPROM, any other memory chip or cartridge, a carrier wave, or any other medium from which a computer can read.

[0049] Embodiments of the present invention may be implemented in software, hardware, application logic or a combination of software, hardware and application logic. In an example embodiment, the application logic, software or an instruction set is maintained on any one of various conventional computer-readable media. In the context of this document, a "computer-readable medium" may be any media or means

that can contain, store, communicate, propagate or transport the instructions for use by or in connection with an instruction execution system, apparatus, or device, such as a computer, with one example of a computer described and depicted in Figures 17 and 18. A computer-readable medium may comprise a computer-readable storage medium that may be any media or means that can contain or store the instructions for use by or in connection with an instruction execution system, apparatus, or device, such as a computer.

[0050] In general, the various embodiments of the invention may be implemented in hardware or special purpose circuits or any combination thereof. While various aspects of the invention may be illustrated and described as block diagrams or using some other pictorial representation, it is well understood that these blocks, apparatus, systems, techniques or methods described herein may be implemented in, as non-limiting examples, hardware, software, firmware, special purpose circuits or logic, general purpose hardware or controller or other computing devices, or some combination thereof.

[0051] Embodiments of the inventions may be practiced in various components such as integrated circuit modules. The design of integrated circuits is by and large a highly automated process. Complex and powerful software tools are available for converting a logic level design into a semiconductor circuit design ready to be etched and formed on a semiconductor substrate.

[0052] Programs, such as those provided by Synopsys, Inc. of Mountain View, California and Cadence Design, of San Jose, California automatically route conductors and locate components on a semiconductor chip using well established rules of design as well as libraries of pre stored design modules. Once the design for a semiconductor circuit has been completed, the resultant design, in a standardized electronic format (e.g., Opus, GDSII, or the like) may be transmitted to a semiconductor fabrication facility or "fab" for fabrication.

[0053] While the invention has been described in connection with a number of embodiments and implementations, the invention is not so limited but covers various obvious modifications and equivalent arrangements, which fall within the purview of the appended claims. Although features of the invention are expressed in certain

combinations among the claims, it is contemplated that these features can be arranged in any combination and order.

CLAIMS

1. An apparatus comprising:

a first input for receiving a spin index;

5 a third input for receiving one or more convergence criteria;

an energy estimation block adapted to use the spin index to estimate an energy value; and

a convergence estimation block adapted to use the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

10

2. The apparatus of claim 1, wherein the energy estimation block is further adapted to obtain another estimate of the energy value, if the convergence criteria was not fulfilled.

3. The apparatus of claim 1 or 2 further comprising:

15 a second input for receiving a penalty term; and

an adder for adding the penalty term to the estimated energy value,

wherein convergence estimation block adapted to use the estimated energy value added with the penalty term in the convergence criteria determination.

20 4. The apparatus of claim 1, 2 or 3, wherein the energy estimation block is adapted to increment the energy estimate for every incoming spin j by $J_{ij}^{(b)} s_i s_j$ to obtain the another estimate of the energy value, where $J_{ij}^{(b)}$ is a binary variable describing the value of a coupling J_{ij} .

25 5. The apparatus of claim 1, 2, 3 or 4, wherein the energy estimation block is adapted to

find a minimum to an energy functional given by $H = \sum_i \sum_j^{i-1} J_{ij} s_i s_j + \sum_i h_i s_i$, where J_{ij} and

h_i are floating points, s_i represents a physical spin that can either be up or down, J_{ij} represents interactions between spins s_i and s_j , and h_i represents an external field affecting to the spin s_i .

30

6. The apparatus of claim 5, wherein the couplings J_{ij} are on the interval $[-1; 1]$ as

$$J_{ij} = -1 + \sum_{b=0}^B J_{ij}^{(b)} 2^{-b} \approx \frac{1}{2} \sum_{b=0}^B (2J_{ij}^{(b)} - 1) 2^{-b}, \text{ where } J_{ij}^{(b)} \text{ is a binary variable comprising } B \text{ bits}$$

describing the value of J_{ij} .

5 7. The apparatus of any of the claims 1 to 6 further comprising a counter, wherein the apparatus is adapted to change the value of the counter, if it was determined that the convergence criteria was not fulfilled.

8. A method comprising:

10 receiving a spin index;
 receiving one or more convergence criteria;
 using the spin index to estimate an energy value; and
 using the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

15

9. The method of claim 8 further comprising:

 obtaining another estimate of the energy value, if the convergence criteria was not fulfilled.

10. The method of claim 8 or 9 further comprising:

20 adding a penalty term to the estimated energy value, and
 using the estimated energy value added with the penalty term in the convergence criteria determination.

11. The method of claim 8, 9 or 10 further comprising:

25 incrementing the energy estimate for every incoming spin j by $J_{ij}^{(b)} s_i s_j$ to obtain the another estimate of the energy value, where $J_{ij}^{(b)}$ is a binary variable describing the value of a coupling J_{ij} .

12. The method of any of the claims 8 to 11 further comprising:

$$H = \sum_i^N \sum_j^{i-1} J_{ij} s_i s_j + \sum_i^N h_i s_i$$

finding a minimum to an energy functional given by J_{ij} and h_i are floating points, s_i represents a physical spin that can either be up or down, J_{ij} represents interactions between spins s_i and s_j , and h_i represents an external field affecting to the spin s_i .

13. The method of claim 12, wherein the couplings J_{ij} are on the interval $[-1; 1]$ as

$$J_{ij} = -1 + \sum_{b=0}^B J_{ij}^{(b)} 2^{-b} \approx \frac{1}{2} \sum_{b=0}^B (2J_{ij}^{(b)} - 1) 2^{-b}, \text{ where } J_{ij}^{(b)} \text{ is a binary variable comprising } B \text{ bits}$$

describing the value of J_{ij} .

14. The method of any of the claims 8 to 13 further comprising:

changing a value of a counter, if it was determined that the convergence criteria was not fulfilled.

15. An apparatus comprises at least one processor; and at least one memory including computer program code the at least one memory and the computer program code configured to, with the at least one processor, cause the apparatus to perform at least the following:

receive a spin index;

receive one or more convergence criteria;

use the spin index to estimate an energy value; and

use the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

16. A computer readable storage medium stored with code thereon for use by an apparatus, which when executed by a processor, causes the apparatus to perform:

receive a spin index;

receive one or more convergence criteria;

use the spin index a to estimate an energy value; and

use the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

17. An apparatus comprising:

- 5 means for receiving a spin index;
- means for receiving one or more convergence criteria;
- means for using the spin index to estimate an energy value; and
- means for using the convergence criteria and the estimated energy value to determine whether the convergence criteria was fulfilled.

10

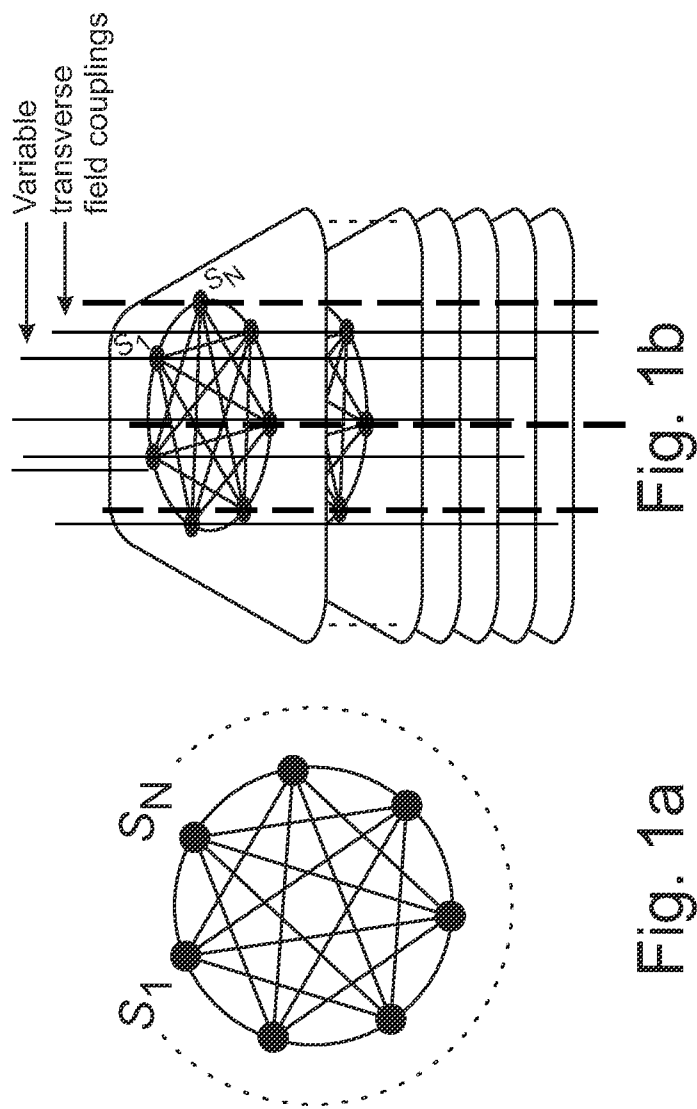


Fig. 1b

Fig. 1a

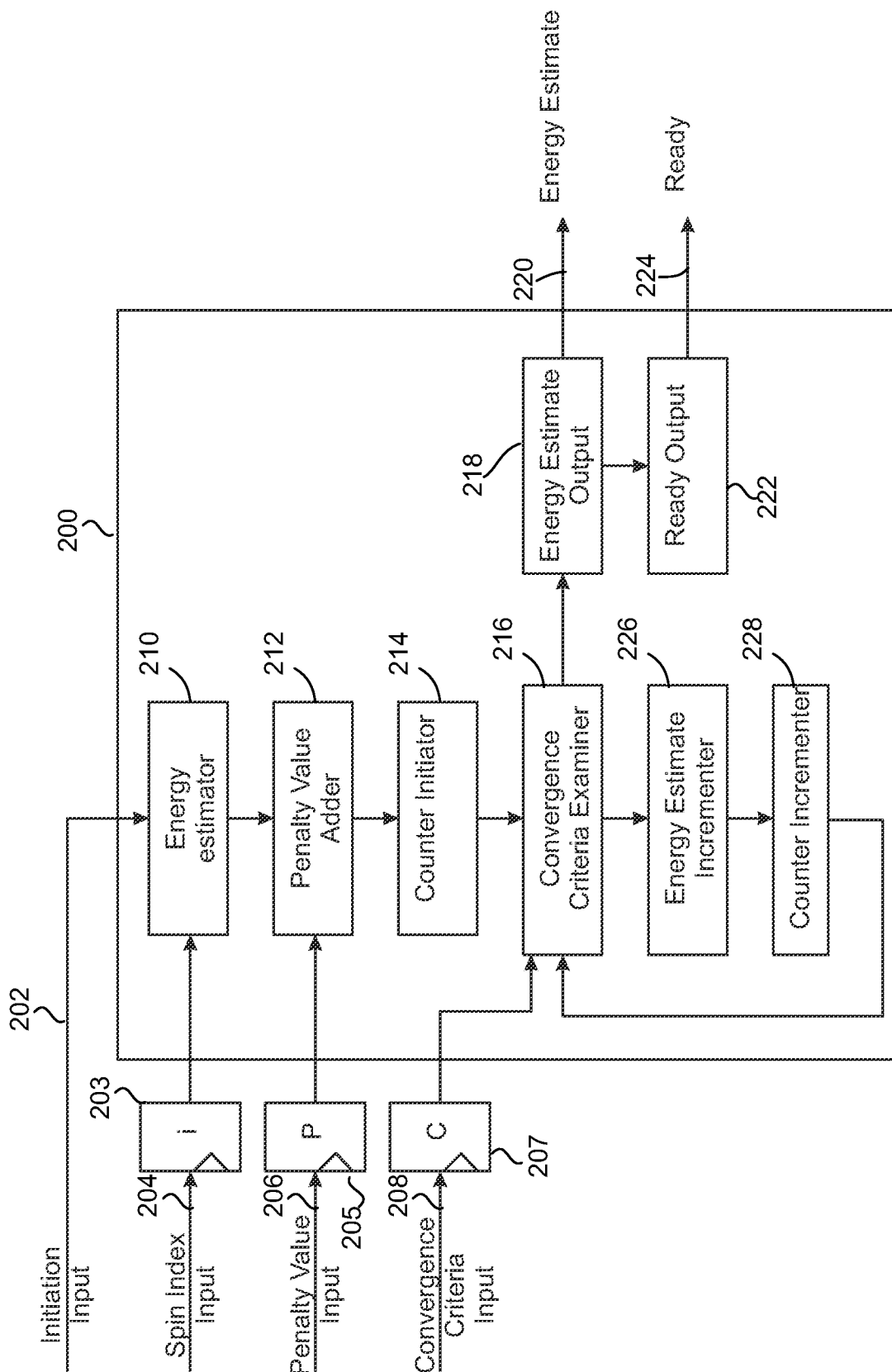


Fig. 2

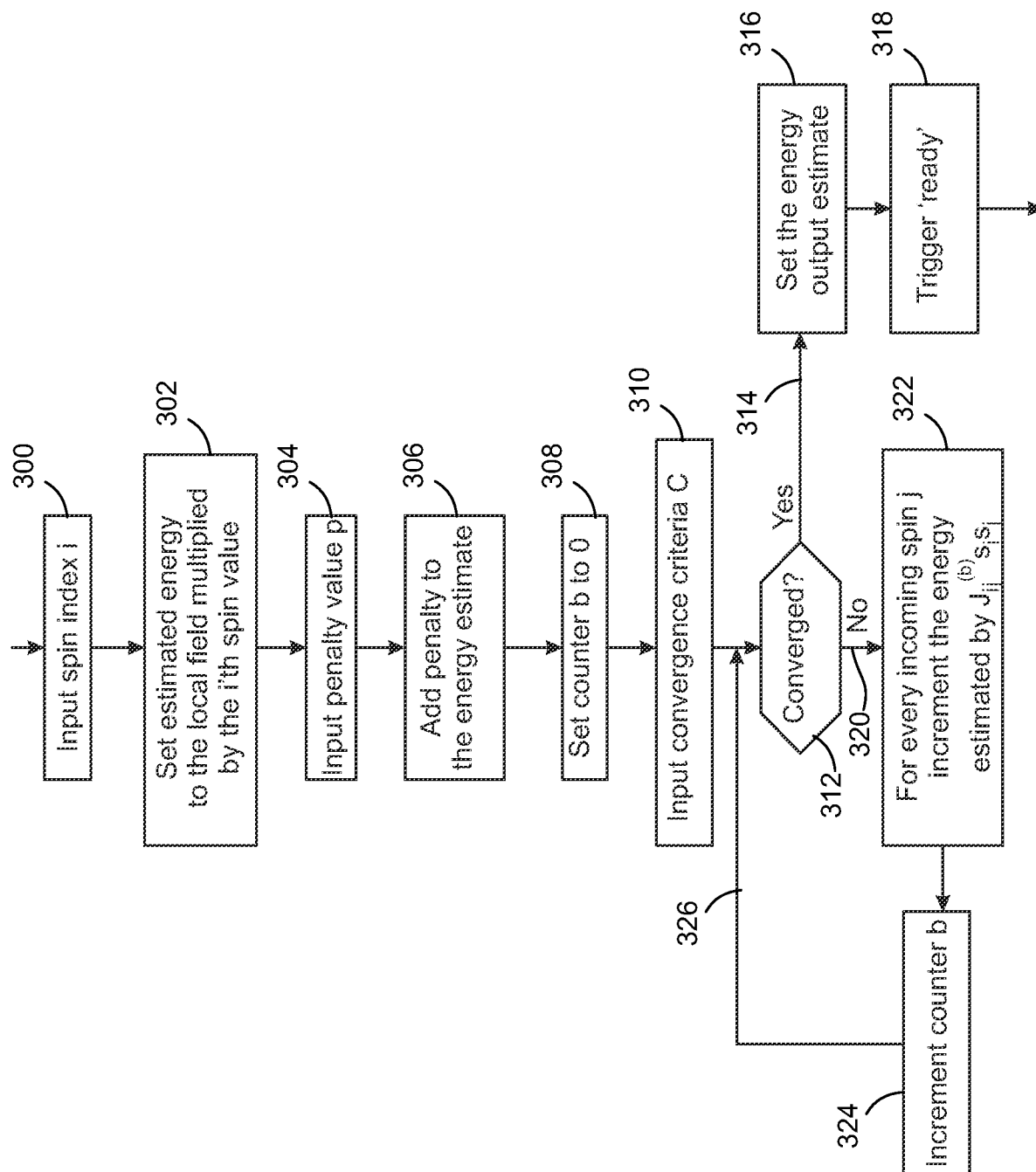


Fig. 3

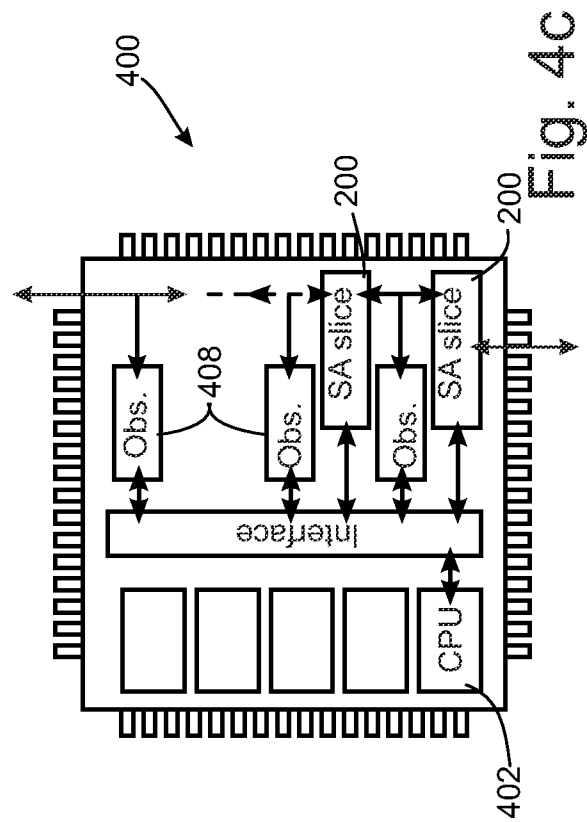


Fig. 4c

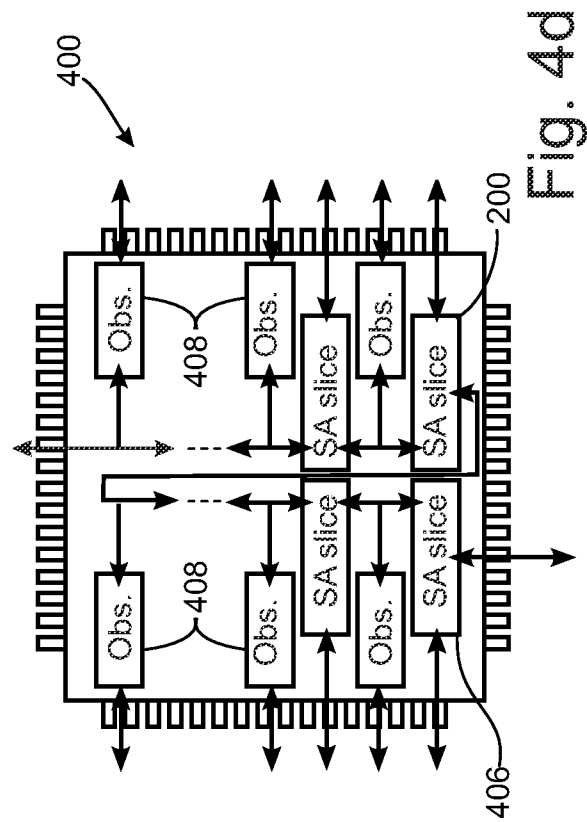


Fig. 4d

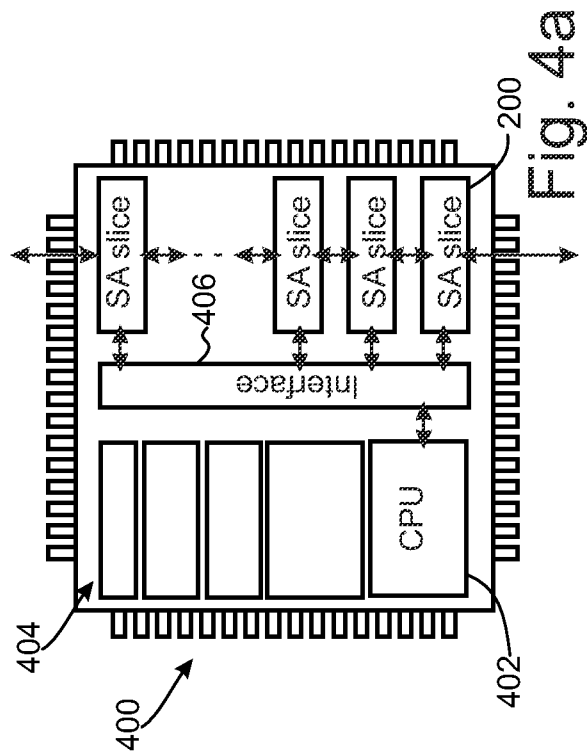


Fig. 4a

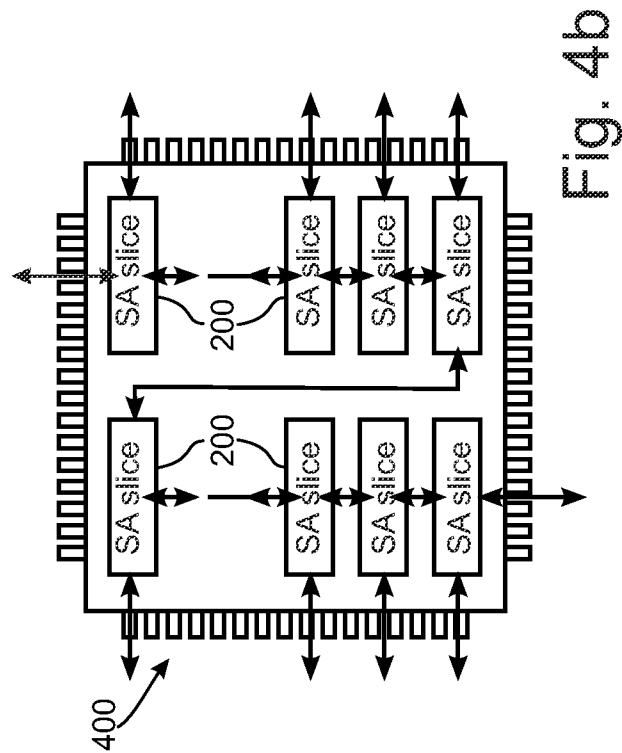


Fig. 4b

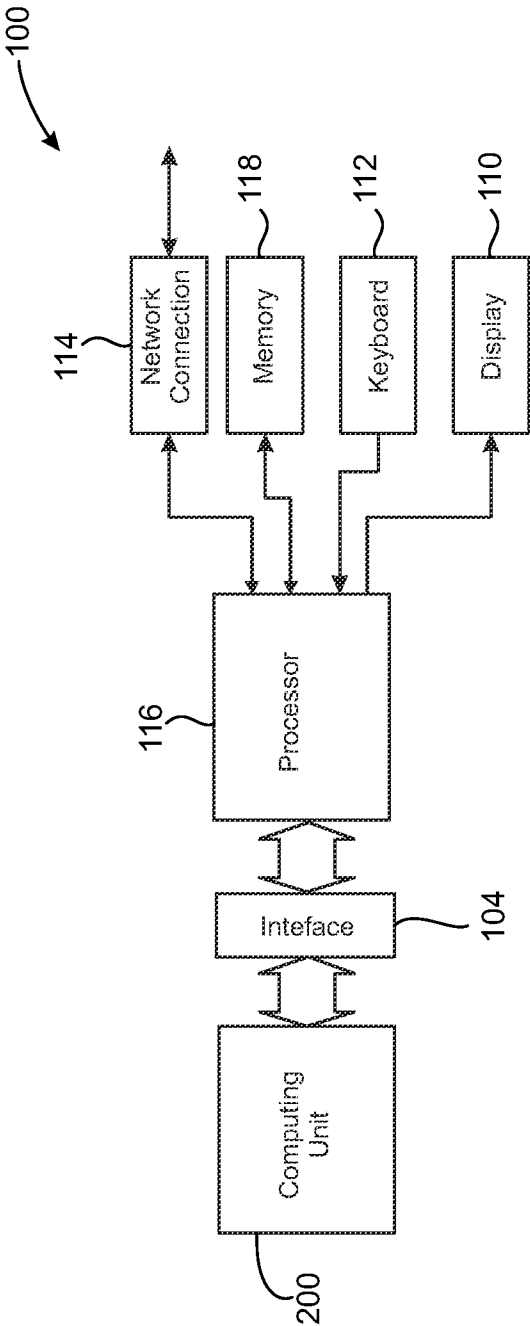


Fig. 5

INTERNATIONAL SEARCH REPORT

International application No

PCT/FI2015/050580

A. CLASSIFICATION OF SUBJECT MATTER

INV. G06N7/00 G06F17/11
ADD. G06N99/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06N G06F G06Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	F. BELLETTI ET AL: "Simulating spin systems on IANUS, an FPGA-based computer", COMPUTER PHYSICS COMMUNICATION, vol. 178, no. 3, 5 October 2007 (2007-10-05), pages 208-216, XP022424160, DOI: 10.1016/J.CPC.2007.09.006 sections 2-4 ----- -/-	1-7, 15-17



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 May 2016

Date of mailing of the international search report

30/05/2016

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Douarche, Nicolas

INTERNATIONAL SEARCH REPORT

International application No

PCT/FI2015/050580

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	M. YAMAOKA ET AL: "20k-spin Ising chip for combinational optimization problem with CMOS annealing", DIGEST OF TECHNICAL PAPERS FROM THE 2015 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE (ISSCC'15), 22 February 2015 (2015-02-22), pages 432-434, XP032748233, DOI: 10.1109/ISSCC.2015.7063111 figure 24.3.1	1-7, 15-17
X	----- S. V. Isakov et al: "Optimised simulated annealing for Ising spin glasses", arXiv:1401.1084v3, 17 June 2014 (2014-06-17), XP055237920, Retrieved from the Internet: URL:http://arxiv.org/abs/1401.1084v3 [retrieved on 2016-05-12] sections 2-4	1-7, 15-17
X	----- T. F. RØNNOW ET AL: "Defining and detecting quantum speedup", SCIENCE, vol. 345, no. 6195, 19 June 2014 (2014-06-19), pages 420-424, XP055272732, DOI: 10.1126/science.1252319 supplementary materials	1-7, 15-17
X	----- US 2015/205759 A1 (ISRAEL ROBERT [CA] ET AL) 23 July 2015 (2015-07-23) the whole document -----	1-7, 15-17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2015/050580

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☒ Claims Nos.: 8-14
because they relate to subject matter not required to be searched by this Authority, namely:
see FURTHER INFORMATION sheet PCT/ISA/210
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.1

Claims Nos.: 8-14

Independent claim 8 seeks protection any "method comprising: receiving a [...] index; receiving one [...] criteria; using the [...] index to estimate an [...] value; and using the [...] criteria and the [...] value to determine whether the [...] criteria was fulfilled." The terms "spin", "energy" and "convergence" associated with said "index", "energy" and "convergence" as such refer to scientific and mathematical models of spin glasses. The scope of protection is not limited to technical implementations of a spin glass and the claim does not define any feature that would lend a technical character to the claimed method. In particular, it is not limiting the scope of protection to specific technical interpretations for the "convergence" of a problem that would be represented by the energy of a spin glass. Dependent claims 9-14 fail to define features that would clearly contribute to a technical character of the matter for which protection is sought, as they are not limiting the indicated steps to technical activities. Therefore, insofar as claims 8-14 comply with Art. 6 PCT, their subject-matter relates as such to a matter similar to, or being analogous to, the matters listed under Rule 39.1(i),(iii)&(vi) PCT.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/FI2015/050580

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015205759	A1	23-07-2015	NONE
