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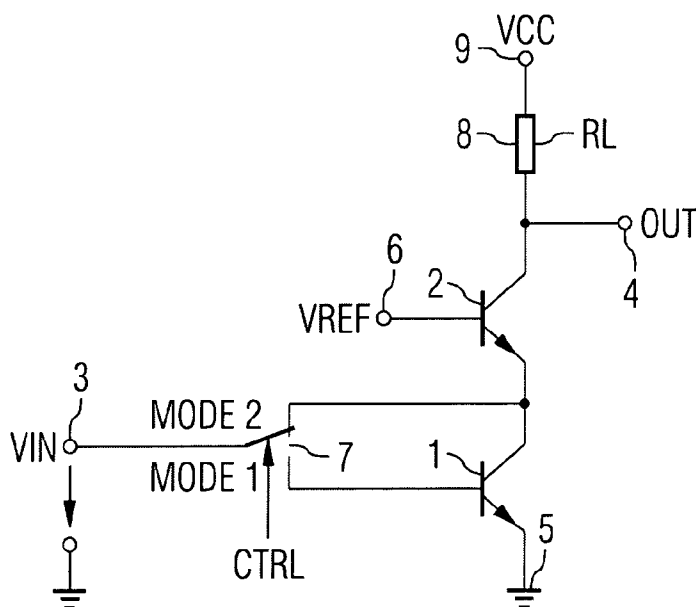
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(54) Title: **AMPLIFIER ARRANGEMENT AND METHOD**



(57) Abstract: The present invention relates to an amplifier arrangement having a transistor arrangement comprising a first transistor (1) in common-emitter configuration and a second transistor (2) in common-base configuration. A switching device (7) couples, in a first mode of operation, the first transistor (1) to an input (3) of the amplifier arrangement and while the second transistor (2) forms a cascode stage. In a second mode of operation the second transistor (2) is coupled to the input (3). While high gain is achieved during the first mode, the second mode allows for high linearity without requiring inductive degeneration.

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Amplifier arrangement and method

The present invention relates to an amplifier arrangement and to a method to amplify a signal.

5

Amplifier arrangements are widely used, for example as low-noise amplifiers in radio-frequency receiver arrangements. Depending on the power level of an incoming signal, it can be desirable to provide an amplifier with adjustable gain.

10

Usually, transistors are used for signal amplification. An amplifying transistor can be connected in common-emitter configuration. This results in relatively high gain, a low noise-figure and fairly good linearity when processing low level input signals.

15

In order to improve the linearity of an amplifier based on a common-emitter transistor configuration, it is possible to use degeneration. This is performed by connecting an inductor between the emitter terminal of the transistor and ground potential. When processing high-frequency signals, this results in a considerable improvement in linearity.

20

However, due to the fact that an inductor having a relatively large value is required, this inductor, due to its size, normally is an external component. In each case, the inductive degeneration requires either a relatively large chip area to integrate an inductor or an additional pin at an integrated circuit comprising the amplifier to connect an external, discrete inductor, resulting in higher costs.

30

It is an object of the present invention to provide an amplifier arrangement and a method which provide for improved linearity of signal amplification.

- 5 These objects are solved by an amplifier arrangement having the features of present claim 1 and by a method according to claim 16.

Preferred embodiments are presented in the dependent claims.

10

The amplifier arrangement has an input to receive a signal to be amplified and an output to provide an amplified signal derived from the input signal. A transistor arrangement couples the input to the output. The transistor arrangement
15 comprises at least a first transistor and a second transistor. While the first transistor is connected in common-emitter configuration, the second transistor is designed in common-base configuration. The second transistor is coupled to the output of the amplifier arrangement.

- 20 Further on, a switching device is provided which is coupled to the transistor arrangement such that in the first mode of operation of the amplifier arrangement, the first transistor is coupled to the input of the amplifier arrangement and the second transistor forms a cascode stage with respect to the
25 first transistor. In the second mode of operation of the amplifier arrangement, the second transistor is coupled to the input of the amplifier arrangement.

- In the first mode of operation, a common-emitter transistor
30 with cascode configuration is provided. This results in a relatively high gain, a low-noise-figure and a fair linearity in order to handle low level input signals.

In the second mode of operation, the circuit presents a common-base transistor configuration. The second transistor, which in the first mode operates as a cascode stage, is the actual input transistor in the second mode. This second
5 operation mode results in lower gain which is desirable in order to process input signals with higher input level, a higher noise-figure which is acceptable due to the higher input level signal, and a significantly higher linearity of the amplification.

10

In the second mode, the first transistor of the transistor arrangement may be part of a current source.

According to the proposed principle, no external or internal
15 inductor is needed to increase the linearity in the common-emitter structure.

Depending on the desired characteristics of an amplifier, a commutation between a common-emitter and a common-base
20 transistor configuration is provided.

Due to the fact that an inductive degeneration is no longer required with the principle suggested, a smaller low-noise amplifier, LNA, with low current consumption can be realized.
25

In a preferred embodiment of the present invention, means are provided for suppression of Direct Current, DC-components of an incoming signal which are connected between the input of the amplifier arrangement and the switching device.
30

It is preferred to design the switching device such that in the first mode of operation the input of the amplifier arrangement is coupled to the base terminal of the first

transistor and that in the second mode of operation the input of the amplifier arrangement is coupled to the emitter terminal of the second transistor.

5 By doing this, in the first mode of operation, the signal to be amplified is fed into the base terminal of the first transistor which is in a common-emitter configuration, while in the second mode of operation, the signal to be amplified is directly fed into the emitter terminal of the second
10 transistor which operates in common-base configuration.

According to another preferred embodiment, means for operating point adjustment are provided which are connected to the base terminal of the first transistor.

15

It is preferable that the switching device has a control input to receive a control signal. The switching device may be designed such that the first or second mode of operation is activated as a function of a desired value of
20 amplification of the amplifier arrangement.

The switching device may be designed such that the mode of operation is activated depending on the power level of an incoming signal.

25

The amplifier arrangement may preferably be integrated monolithically, partly or as a whole circuit. Preferably, bipolar circuit design is used.

30 In alternative embodiments, is also possible to use unipolar transistors, for example in a metal-oxide semiconductor, MOS integration technique, and/or BiCMOS.

In this case, the emitter corresponds to the source terminal, while the base terminal corresponds to the gate. Accordingly, the first transistor is in common-source configuration, while the second transistor is in common-gate configuration.

5

The amplifier arrangement is preferably used as a low-noise amplifier in a radio frequency, RF receiver. For example, the low-noise amplifier may couple an antenna to further signal processing means. The amplifier arrangement may be used on a radio frequency level as well as, after a frequency conversion for example, in an intermediate frequency or baseband frequency level.

While the different modes of operation preferably are chosen with respect to a desired amplification or gain value, it is also possible to switch between two different modes of operation depending on a modulation technique or other properties of a certain radio system, for example amplitude and/or phase modulation and/or frequency modulation, time and/or frequency duplexing, TDD, FDD, time division multiple access, TDMA, frequency division multiple access FDMA and/or code division multiple access, CDMA et cetera.

The following description of figures of exemplary embodiments may further illustrate and explain the invention.

Figure 1 shows a schematic of a first exemplary embodiment of the principle presented,

Figure 2 shows a second exemplary embodiment of a schematic of the principle presented, and

Figure 3 shows an example of a radio receiver having an amplifier according to the principle presented.

Figure 1 shows a schematic of a first embodiment of an amplifier arrangement according to the principle presented as an example. The amplifier arrangement comprises a first transistor 1 and a second transistor 2. The first transistor 1 and the second transistor 2 form a transistor arrangement. This transistor arrangement 1, 2 is coupled between an input 3 to receive a signal to be amplified and an output 4 to provide an amplified signal.

The first transistor is switched in common-emitter configuration, while the second transistor 2 is connected in common-base figuration. The emitter terminal of the first transistor 1 is directly connected to a ground potential terminal 5. The base terminal of the second transistor 2 is directly connected to a reference potential terminal 6. A switching device 7 allows for switching between a first mode of operation of the amplifier arrangement and a second mode of operation of the amplifier arrangement. In the first mode of operation, the second transistor 2 is coupled to the first transistor 1 and the signal input 3 such that the second transistor forms a cascode stage with respect to the first transistor 1. In the second mode of operation, however, the second transistor 2 is coupled, in this case with its emitter terminal, to the input 3 of the amplifier arrangement. In the second mode of operation, the first transistor 1 is part of a current source for the second transistor. The output terminal 4 is formed at a free terminal of the second transistor 2. Here, the output terminal 4 is directly connected to the collector terminal of the second transistor. In addition to

7

this, an electric load 8 is connected between a supply potential terminal 9 and the output 4.

Switch 7 connects, in a first switching position during the first mode of operation, the input 3 to the base terminal of the first transistor 1. In its second switching position during the second mode of operation, the switch 7 connects the input 3 to the emitter terminal of the second transistor 2.

In order to form a cascode configuration during the first mode of operation, the emitter terminal of the second transistor 2 is connected to the collector terminal of the first transistor 1.

In the first mode of operation, the input signal VIN is fed into the base terminal of the first transistor 1 which by means of the second transistor 2 has a cascode stage. The amplified signal is provided at the output 4. The common-emitter transistor with cascode configuration results in high gain, low noise-figure and fair linearity in order to process low-level input signals.

In the second mode of operation, the input signal VIN is fed into the emitter terminal of the second transistor 2. In this mode, the transistor arrangement represents a common-base configuration. The second transistor 2, which in the first mode represents a cascode, is the input transistor in the second mode of operation. By doing this, during the second mode of operation, a lower gain is achieved which is desirable to process higher input level signals of the input signal VIN. A higher noise figure which might occur is acceptable due to the higher input level signal. In the

second mode of operation, linearity is improved significantly. This higher linearity is achieved without the need for inductive degeneration. Especially, no external inductor is necessary.

5

In alternative embodiments, the bipolar transistors 1, 2 can be replaced by unipolar transistors, for example field effect transistors. In this case, the common-emitter configuration is realized by a common source configuration and the common
10 base configuration is realized by a common gate configuration.

Figure 2 shows a second exemplary embodiment of an amplifier arrangement according to the principle presented. As far as
15 the circuits of figures 1 and 2 correspond to each other in the parts used, their interconnection and their advantageous function, this description is not repeated here.

In addition to the switching device 7, figure 2 comprises
20 means for blocking DC components 10 of the input signal VIN, which are connected between the input 3 and switch 7. These means for suppression of DC-components 10 may for example be realized as a series capacitor.

25 The reference potential terminal 6 is, according to figure 2, directly connected to the supply potential terminal 9.

Further on, a means for operating point adjustment 11 is provided which is connected to the base terminal of the first
30 transistor 1. The means for operating point adjustment 11 comprises a third transistor 12 in common-emitter configuration, the collector terminal of which is connected, via a reference current source 13, to the supply potential

terminal 9. Further on, the means for operating point adjustment 11 comprises a fourth transistor 14 in common-collector configuration. The base terminal of transistor 14 is connected to the collector terminal of third transistor 12, the emitter terminal of the fourth transistor 14 is connected, via a first resistor 15, to the base terminal of the third transistor 12 and, via a second resistor 16, to the base terminal of the first transistor 1. The collector terminal of the fourth transistor 14 is directly connected to the supply potential terminal 9.

The ratio of the values of first and second transistor 15, 16 sets the operating point.

The switching device 7 may, for example, be realized by using two complementary switched transmission gates or single transistors.

In Figure 3, an exemplary receiver arrangement for radio frequencies is shown. The amplifier arrangement according to the present invention, for example the amplifier arrangement according to Figure 2, is coupled to an antenna 21. Means for further signal processing 22 are provided downstream of the amplifier arrangement. Switching between the first mode of operation and the second mode of operation, different gain values and linearity characteristics can be achieved for processing a received signal as already explained above.

Reference numerals

	1	transistor
	2	transistor
5	3	input
	4	output
	5	ground potential terminal
	6	reference potential terminal
	7	switching device
10	8	electrical load
	9	supply potential terminal
	10	DC-blocking means
	11	operating point adjustment means
	12	transistor
15	13	reference current source
	14	transistor
	15	resister
	16	resister
	20	amplifier arrangement
20	21	antenna
	22	signal path

Claims

1. Amplifier arrangement, having
 - an input (3) to receive a signal to be amplified,
 - 5 - an output (4) to provide an amplified signal,
 - a transistor arrangement comprising a first transistor (1) in common-emitter configuration, and a second transistor (2) in common-base configuration, which second transistor is coupled to the output (4) of the amplifier arrangement,
 - 10 - a switching device (7) coupled to the transistor arrangement such that in a first mode of operation of the amplifier arrangement the first transistor (1) is coupled to the input of the amplifier arrangement and the second transistor (2) forms a cascode with respect to the first transistor (1), and that in a second mode of operation of the amplifier arrangement the second transistor (2) is coupled to the input (3) of the amplifier arrangement, wherein
 - the switching device (7) couples the input (3) of the
 - 20 amplifier arrangement to the transistor arrangement.
2. Amplifier arrangement according to claim 1, characterized in that means for DC-component suppression (10) of a signal are
- 25 connected between the input (3) of the amplifier arrangement and the switching device (7).
3. Amplifier arrangement according to one of claims 1 to 2, characterized in that
- 30 in the second mode of operation the first transistor (1) is designed to operate as a current source.
4. Amplifier arrangement according to one of claims 1 to 3,

characterized in that

the switching device (7) is designed such that

- in the first mode of operation the input (3) of the amplifier arrangement is coupled to the base terminal of the first transistor (1) and
- in the second mode of operation the input (3) of the amplifier arrangement is coupled to the emitter terminal of the second transistor (2).

5 10 5. Amplifier arrangement according to one of claims 1 to 4, characterized in that the emitter terminal of the first transistor (1) is connected to a ground potential terminal (5).

15 6. Amplifier arrangement according to one of claims 1 to 5, characterized in that the base terminal of the second transistor (2) is connected to a reference potential terminal (6).

20 7. Amplifier arrangement according to one of claims 1 to 6, characterized in that the emitter terminal of the second transistor (2) is connected to the collector terminal of the first transistor (1).

25 8. Amplifier arrangement according to one of claims 1 to 7, characterized in that the collector terminal of the second transistor (2) is connected to a supply potential terminal (9) via an electric load (8).

30

9. Amplifier arrangement according to one of claims 1 to 8, characterized in that

13

a means for operating point adjustment (11) is provided which means is connected to the base terminal of the first transistor (1).

- 5 10. Amplifier arrangement according to claim 9, characterized in that the means for operating point adjustment (11) comprises:
- a third transistor (12) in common-emitter configuration, the collector terminal of which is connected, via a
10 reference current source (13), to a supply potential terminal (9), and
 - a fourth transistor (14) in common-collector configuration, the base terminal of which is connected to the collector terminal of the third transistor (12) and the emitter
15 terminal of which is connected, via a first resistor (15), to the base terminal of the third transistor (12) and, via a second resistor (16), to the base terminal of the first transistor (1).
- 20 11. Amplifier arrangement according to one of claims 1 to 10, characterized in that the switching device (7) has a control input to receive a control signal and is designed to activate the first or second mode of operation as a function of a desired gain
25 value of the amplifier arrangement.
12. Amplifier arrangement according to one of claims 1 to 11, characterized in that the amplifier arrangement is provided in monolithic
30 integration as a bipolar circuit.
13. Receiver arrangement having an amplifier arrangement according to one of claims 1 to 12,

characterized in that
the amplifier arrangement is provided in a receive path of
the receiver arrangement.

- 5 14. Use of an amplifier arrangement according to one of
claims 1 to 12
as a low-noise amplifier in a receive path of a receiver
arrangement.
- 10 15. Method to amplify a signal with adjustable gain,
comprising the steps of:
- receiving a signal to be amplified,
 - amplifying the signal by means of a first transistor (1) in
common-emitter configuration having a cascode stage, in a
15 first mode of operation, which cascode stage is formed by a
second transistor (2),
 - amplifying the signal by means of the second transistor
(2), which is in common-base configuration, during a second
mode of operation,
 - 20 - providing an amplified signal,
 - feeding the signal to be amplified either to the first
transistor (1) in the first mode of operation or to the
second transistor (2) in the second mode of operation.

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FIG 1

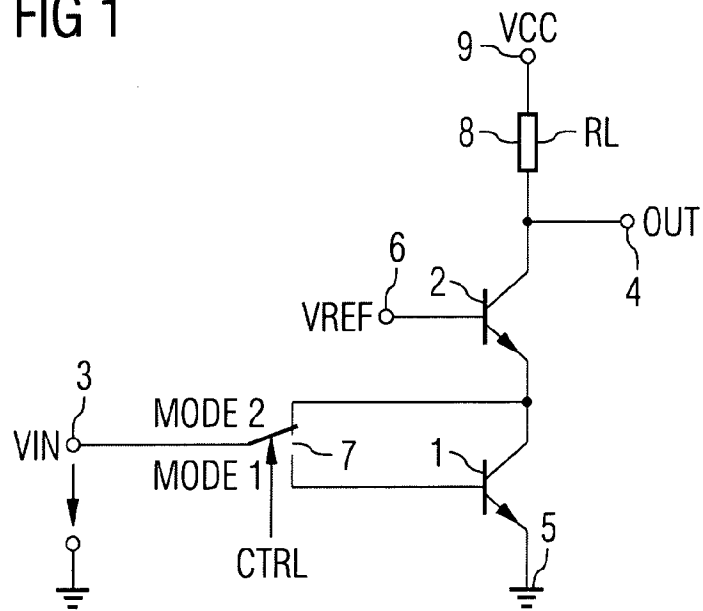


FIG 2

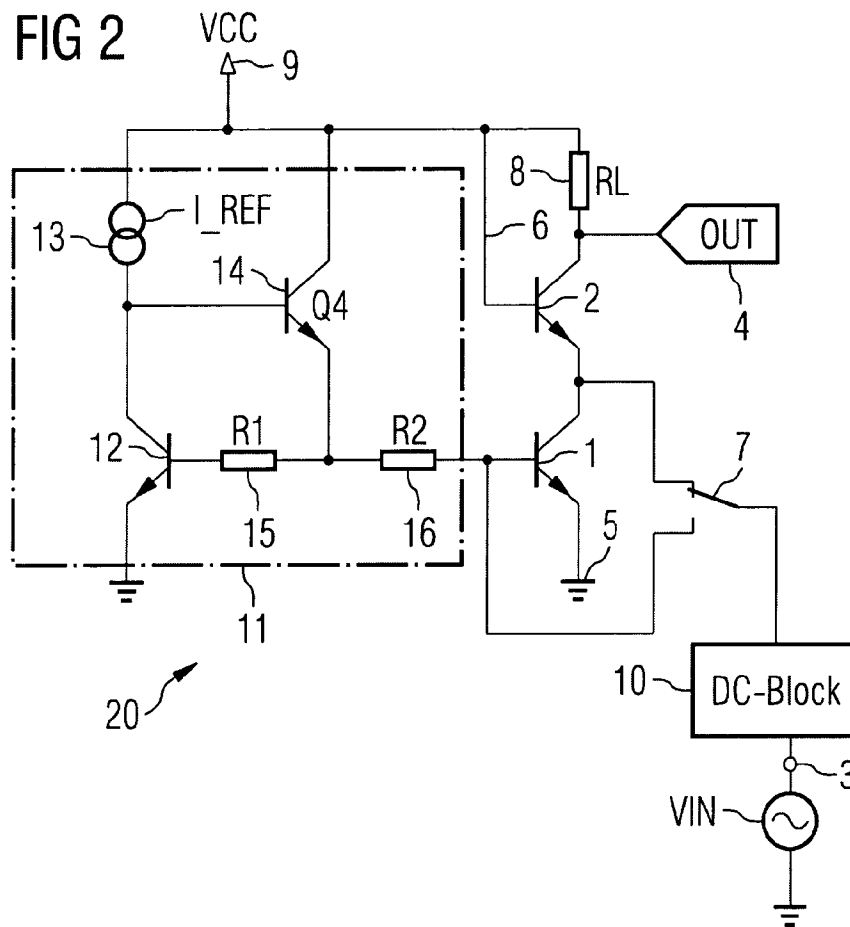
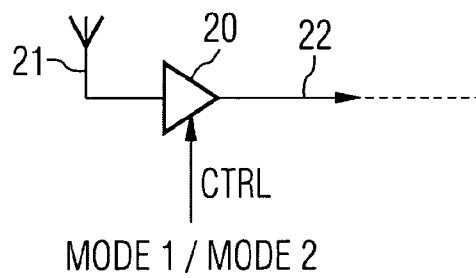


FIG 3



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/007340

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/72

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

International application No
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INTERNATIONAL SEARCH REPORT

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