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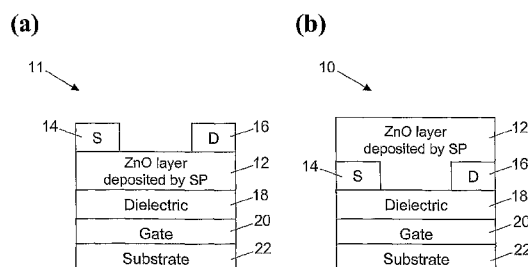


Figure 3

(57) **Abstract:** A method of forming a low-voltage thin-film field-effect transistor comprising: forming a gate; forming a dielectric layer on the surface of the gate; forming a source region and a drain region; and forming a semiconductor layer adjacent the dielectric layer; wherein the dielectric layer is formed as a native oxide layer by oxidising the surface of the gate; and wherein the semiconductor layer is deposited by spray pyrolysis. The method may further comprise functionalising the dielectric layer with a self-assembling monolayer dielectric layer. The present disclosure also discloses forming the dielectric layer as a self-assembling monolayer, without first forming a native oxide (or other) dielectric layer.

LOW-VOLTAGE THIN-FILM FIELD-EFFECT TRANSISTORS

This invention relates, in part, to thin-film field-effect transistors for low-voltage and low-power applications, and a fabrication method thereof.

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Background to the Invention

Semiconducting thin-film transistors (TFTs) comprise a substrate, a semiconducting layer, a dielectric layer, and conducting materials for the source, drain and gate electrodes. Depending on the gate potential (V_G) and the drain potential (V_D), the channel current (i.e. the current flowing from the source electrode to the drain electrode, often referred to as I_D) can be modulated.

Advances in solution-processable TFTs are sought for the realisation of high throughput yet low-cost electronic applications. Examples include integrated logic circuits [1] and backplanes for conventional as well as novel, e.g. flexible etc, optical displays [2]. Unfortunately, the vast majority of solution-processed TFTs incorporating either organic/polymeric or inorganic semiconductors require high operating voltages, typically in the range of tens of volts. Paramount to the successful implementation of TFT technology in future device applications will be low-voltage, low-power operation. Such capabilities could enable widespread adoption of the technology in numerous low-powered portable (i.e. battery powered) applications. A number of efforts have achieved this strategic goal but typically at the cost of solution-processability of the semiconductor and/or the gate dielectric layers. The primary advantage associated with solution processing is relatively simple fabrication and potentially lower manufacturing cost.

The best examples of low-voltage TFTs reported in the literature come from devices employing self-assembled monolayer (SAM) gate dielectrics using organic as well as inorganic semiconductors [3, 4]. Collet et al. [5], for example, used carboxyl terminated tetradecylenyltrichlorosilane SAMs on Si wafers for the fabrication of OFETs using evaporated α -sexithiophene. Transistor operation at 2 V was demonstrated with gate leakage currents of the order 10^{-6} A/cm². Other examples include pioneering work by Klauk et al. [6] where they demonstrated low-voltage organic TFTs based on octadecylphosphonic acid (ODPA) SAMs as the gate dielectric employing evaporated organic semiconductors. More recently, Ma et al. [7] reported the use of alkyl- and anthryl-alkyl- phosphonic acid SAMs also in combination with evaporated films of organic semiconductors. Unfortunately, organic TFTs are characterised by relatively low carrier mobilities that limit the range of potential applications. Recently alternative material systems have been explored including a number of metal oxide semiconductors. Ju et al. [8], for example, have demonstrated low operating voltage TFTs employing metal oxide semiconductors deposited by sputtering [9], as well as low voltage TFTs based on metal oxide nanowires that have been deposited/fabricated on a different substrate and transferred to the transistor array.

There is therefore a desire for TFTs that are (a) solution-processable in order to facilitate manufacture; whilst (b) operable at low voltages and thus suitable for low-power (e.g. portable, battery-powered etc.) applications; and (c) based on an inorganic (rather than organic or partly-organic) semiconductor layer in order to provide relatively high carrier mobilities.

Summary of the Invention

According to a first aspect of the present invention there is provided a method as defined in Claim 1 of the appended claims. Thus there is provided a method

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of forming a low-voltage thin-film field-effect transistor comprising: forming a gate; forming a dielectric layer on the surface of the gate; forming a source region and a drain region; and forming a semiconductor layer adjacent the dielectric layer; wherein the dielectric layer is formed as a native oxide layer by oxidising the surface of the gate; and wherein the semiconductor layer is deposited by spray pyrolysis. The order in which the various processes appear in the preceding sentence should not be interpreted as implying any particular sequence of steps in the formation of the transistor.

The native oxide dielectric layer provides multiple benefits. It is simple to form; a separate deposition step for forming the dielectric is not required, thus facilitating fabrication of the TFT. Moreover, the native oxide layer can function as an ultra-thin gate dielectric layer, thereby increasing the geometrical capacitance of the transistor channel. Since the current flowing through the semiconducting channel is directly proportional to the geometrical capacitance of the channel, this enables the operating voltage, and hence the power consumption of the transistor, to be reduced drastically. A further benefit is that the native oxide layer provides suitable surface chemistry whereby functionalisation with self-assembling monolayer (SAM) materials can be performed. Such SAM dielectric materials can provide extra insulation so that the gate leakage current is minimised.

The use of spray pyrolysis to form the semiconductor layer renders the TFT solution-processable, thereby facilitating manufacture.

Preferable, optional, features are defined in the dependent claims.

Thus, the semiconductor layer may comprise a material selected from a group comprising: oxides; oxide-based materials; mixed oxides; metallic type oxides;

group I-IV, II-VI, III-VI, IV-VI, V-VI and VIII-VI binary chalcogenides; and group I-II-VI, II-II-VI, II-III-VI, II-VI-VI and V-II-VI ternary chalcogenides. Inorganic materials which fall within this group provide relatively high carrier mobilities in comparison to organic or partly-organic semiconductor layers.

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Alternatively, the semiconductor layer may comprise one of the semiconductor materials disclosed in WO 2006/003584, i.e. a compound of any of the materials in the following group (i) together with any of the materials in the following group (ii), wherein group (i) comprises cadmium, zinc, lead, tin, bismuth, antimony, indium, copper and mercury; and group (ii) comprises sulphur, selenium and tellurium.

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The native oxide layer may be formed using an oxygen plasma asher, by annealing, or by alternative means for oxidising a metallic surface (e.g. treating with ultraviolet light in the presence of oxygen and/or water etc.) that will be apparent to those skilled in the art.

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Annealing may be performed at a temperature in the range of 100°C to 600°C, for a time in the range of 1 second to 24 hours.

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Preferably the native oxide layer is of the order of 10 nm or less in thickness. This small thickness (compared with conventional TFT dielectrics) dramatically increases the geometrical capacitance of the transistor (e.g. to around 0.4-1 $\mu\text{F}/\text{cm}^2$, compared with 15-20 nF/cm^2 for a 200 nm thick SiO_2 dielectric). This enables the magnitude of the operating voltage of the transistor to be reduced to absolute values below 2 V (i.e. values below $|2|$ V). This is roughly 20-50 times lower than the operating voltages for conventional TFTs. As a result, the power consumption of these devices during operation is also reduced by a similar factor.

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Preferably the semiconductor layer is deposited using a precursor solution. The precursor solution may be doped in order to incorporate dopant atoms in the semiconductor material once formed, which in turn may give rise to hole and/or electron transport and/or to higher charge carrier mobility in the semiconductor layer and/or induce/enhance additional physical properties. The dopant atoms may be selected from a group comprising: aluminium, indium, gallium, molybdenum, boron, nitrogen, lithium. Other dopants are also possible.

The spray pyrolysis may be performed at any suitable temperature according to the semiconductor material being deposited and the substrate used. The temperature may be in the range of 100°C to 600°C, preferably in the range of 100°C to 400°C, and more preferably in the range of 200°C to 400°C.

The semiconductor layer may be sprayed in a raster fashion, although other deposition techniques are also possible.

The semiconductor layer may be deposited in a pulsed manner. By providing a time delay between successive sprays, this enables the solution vapours to adsorb to the substrate and convert to the semiconductor material.

Alternatively the semiconductor layer may be deposited in a continuous manner.

The method may further comprise heat treating the semiconductor layer to remove residual un-reacted precursor material(s).

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In certain embodiments to be described below, the gate is formed of aluminium and thus the dielectric layer is formed of aluminium oxide. However, many alternative materials are possible.

- 5 Likewise, in the embodiments to be described below, the semiconductor layer is formed of zinc oxide. Again, many alternative materials are possible.

The method may further comprise functionalising the dielectric layer with a self-assembling monolayer dielectric layer. This improves the electrical
10 insulation of the dielectric layer and, in turn, improves the operating characteristics of the TFT.

The self-assembling monolayer may be formed from constituent molecules, each of which comprises an organic chain with a functional group at one end.
15 In the present embodiments, the self-assembling monolayer is formed from octadecylphosphonic acid, which we have demonstrated to be thermally stable and suitable for use in conjunction with spray pyrolysis for the deposition of the semiconductor layer. Other suitable self-assembling molecules may be used instead of octadecylphosphonic acid.

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According to a second aspect of the present invention there is provided a method of forming a low-voltage thin-film field-effect transistor comprising: forming a gate; forming a dielectric layer adjacent the gate; forming a source region and a drain region; and forming a semiconductor layer adjacent the
25 dielectric layer; wherein the dielectric layer is formed as a self-assembling monolayer; and wherein the semiconductor layer is deposited by spray pyrolysis. Again, the order in which the various processes appear in the preceding sentence should not be interpreted as implying any particular sequence of steps in the formation of the transistor.

By virtue of the self-assembling monolayer serving as the dielectric layer, there is no need to form an oxide (or other) dielectric layer first. This simplifies the fabrication of the TFT.

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According to a third aspect of the present invention there is provided a low-voltage thin-film field-effect transistor comprising: a source region; a drain region; a semiconductor layer disposed between the source and drain regions; a gate region; and a dielectric layer disposed between the semiconductor layer and the gate region; wherein the dielectric layer is a native oxide layer formed on the surface of the gate region.

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The term “between”, in the context of “the semiconductor layer disposed between the source and drain regions”, should be interpreted broadly, to encompass both spatially between (i.e. physically located between the source and the drain regions) and also functionally between (i.e. arranged to form a semiconducting channel from the source to the drain via the semiconductor layer).

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According to a fourth aspect of the present invention there is provided a low-voltage thin-film field-effect transistor comprising: a source region; a drain region; a semiconductor layer disposed between the source and drain regions; a gate region; and a dielectric layer disposed between the semiconductor layer and the gate region; wherein the dielectric layer is a self-assembled monolayer.

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According to a fifth aspect of the present invention there is provided an integrated circuit comprising one or more transistors in accordance with the third or fourth aspects of the invention.

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According to a sixth aspect of the present invention there is provided a two-dimensional sensor array comprising a plurality of transistors in accordance with the third or fourth aspects of the invention.

5 According to a seventh aspect of the present invention there is provided an ultraviolet detector comprising one or more transistors in accordance with the third or fourth aspects of the invention, the said transistor(s) being situated such that ambient light (i.e. the light to be detected or measured) can reach the said transistor(s).

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According to an eighth aspect of the present invention there is provided a gas sensor comprising: one or more transistors in accordance with the third or fourth aspects of the invention, wherein the transistor(s) is/are situated such that ambient gas (i.e. the gas to be detected or measured) can come into contact with the said transistor(s); means for illuminating the transistor(s) with electromagnetic radiation; and means for measuring the recovery time of the channel current of the transistor(s) following illumination by the illuminating means.

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20 Preferably the said electromagnetic radiation is ultraviolet light.

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According to a ninth aspect of the present invention there is provided a gas sensor comprising: one or more transistors situated such that an ambient gas (i.e. the gas to be detected or measured) can come into contact with the said transistor(s); means for illuminating the transistor(s) with electromagnetic radiation; and means for measuring the recovery time of the channel current of the transistor(s) following illumination by the illuminating means.

Preferably the said electromagnetic radiation is ultraviolet light, and preferably the or each transistor is a thin-film field-effect transistor.

Finally, according to a tenth aspect of the present invention there is provided an ultraviolet detector comprising one or more thin-film field-effect transistors, wherein the said transistor(s) is/are situated such that ambient light can reach the said transistor(s).

With the ninth and tenth aspects of the invention, preferably the or each transistor comprises a semiconductor layer formed of zinc oxide.

Brief Description of the Drawings

Embodiments of the invention will now be described, by way of example only, and with reference to the drawings in which:

Figure 1 illustrates a schematic representation (not to scale) of a bottom-gate bottom-contact TFT architecture according to an embodiment of the invention; Figure 2 illustrates the experimental setup of the spray pyrolysis technique employed in this work;

Figure 3 illustrates schematic representations of the ZnO TFT architectures employed, namely (a) a bottom-gate top-contact (BG-TC) TFT architecture, and (b) a bottom-gate bottom-contact (BG-BC) TFT architecture;

Figure 4 illustrates alternative TFT architectures which may be used in further embodiments of the invention, namely (a) a bottom-gate top-contact TFT, (b) a top-gate top-contact TFT, (c) a top-gate bottom-contact TFT, (d) a top-gate TFT with asymmetric source-drain contacts, and (e) a double gate TFT;

Figure 5 illustrates the chemical structure of zinc acetate di-hydrate precursor material;

Figure 6 illustrates experimentally-measured transfer curves for a ZnO TFT (channel length $L = 60 \mu\text{m}$, channel width $W = 2 \text{ mm}$) based on a native

aluminium oxide (AlO_x) gate dielectric, with the ZnO having been deposited by spray pyrolysis in ambient atmosphere at a substrate temperature of 400°C ; Figure 7 illustrates the molecular structure of the octadecylphosphonic acid used for the functionalisation of native aluminium oxide formed on the surface of an aluminium gate electrode;

Figure 8 shows water droplets on (a) Al-AlO_x and (b) $\text{Al-AlO}_x\text{-ODPA}$ surfaces;

Figure 9 shows water droplets on (a) an as-prepared $\text{Al-AlO}_x\text{-ODPA}$ surface exhibiting a contact angle (θ) of $>105^\circ$, and (b) an $\text{Al-AlO}_x\text{-ODPA}$ surface after thermal annealing of the substrate at 400°C for 10 minutes, also exhibiting a contact angle of $>105^\circ$;

Figure 10 illustrates experimentally-measured (a) transfer characteristics and (b) output characteristics, in both cases for a ZnO TFT ($L = 60\text{ }\mu\text{m}$, $W = 2\text{ mm}$) based on an AlO_x gate dielectric, with the ZnO having been deposited by spray pyrolysis in ambient atmosphere at a substrate temperature of 400°C ;

Figure 11 illustrates circuitry of a unipolar voltage inverter fabricated using two low-voltage ZnO TFTs where the ZnO was deposited via spray pyrolysis;

Figure 12 illustrates examples of alternative unipolar circuits that could be used together with low-voltage oxide TFTs to realise voltage inverters;

Figure 13 illustrates experimentally-measured transfer curves for a unipolar inverter (circuitry shown in Figure 11) employing two low-voltage TFTs based on ZnO deposited by spray pyrolysis at a substrate temperature of 400°C ;

Figure 14 illustrates experimentally-measured transfer characteristics of a low-voltage ZnO TFT ($L = 60\text{ }\mu\text{m}$, $W = 1\text{ mm}$) before and after illumination with a UV-LED; and

Figure 15 illustrates an experimental evaluation of the photoenhanced drain current (I_D) of a ZnO TFT, after brief (10 seconds) illumination with UV light ($\lambda_{\text{peak}} = 400\text{ nm}$).

In the figures, like elements are indicated by like reference numerals throughout.

Detailed Description of Preferred Embodiments

5 The present embodiments represent the best ways known to the applicants of putting the invention into practice. However, they are not the only ways in which this can be achieved.

10 By way of introduction, as illustrated in Figure 1, a conventional bottom-gate bottom-contact TFT device 10 consists of a semiconducting active layer 12 applied onto a three-terminal electrode architecture comprising a source electrode 14, a drain electrode 16 and a gate electrode 20. The gate electrode 20 is separated from the semiconductor layer 12 and the source and drain electrodes by a dielectric layer 18.

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In embodiments of the present invention, the semiconducting layer 12 is deposited using spray pyrolysis (which may be abbreviated to “SP” herein). This builds upon our earlier work on the spray pyrolysis of semiconducting layers, as described in WO 2008/129238 (for a TiO₂ semiconducting layer) and, more recently, PCT/GB2009/001635 (which claims priority from GB 0811962.0) for other semiconducting materials, in particular ZnO. However, in the presently-preferred embodiments, the dielectric 18 is formed as a native oxide layer by oxidising the surface of the gate 20, and/or as a self-assembling monolayer, prior to the deposition of the semiconducting layer 12.

25 Other fabrication sequences are, in principle, possible, though. For example, the semiconducting layer may be formed before the gate or dielectric.

As a proof of concept of embodiments of the present invention, we demonstrate the fabrication of low-voltage TFTs and inverter circuits based on zinc oxide

(ZnO) films deposited by spray pyrolysis. Spray pyrolysis is a simple low-cost deposition technique suitable for large area deposition and could potentially enable the fabrication of large area electronics at low cost. Further details of the SP process may be obtained from PCT/GB2009/001635 (which claims priority from GB 0811962.0). Importantly, ZnO can be deposited in ambient conditions without any special precautions. Freshly prepared devices exhibit air stability and are capable of operating even after exposure to atmospheric air for several months.

Experimental procedures

The spray pyrolysis technique may be used for the deposition of simple oxide films, mixed oxide films, metallic type oxides, group I-IV, II-VI, III-VI, IV-VI, V-VI and VIII-VI binary chalcogenides, and group I-II-VI, II-II-VI, II-III-VI, II-VI-VI and V-II-VI ternary chalcogenides. Films of such metal oxide and metallic spinel oxide materials prepared by SP have matching properties for a wide range of technological applications. Surprisingly, however, use of SP for the fabrication of TFTs is very limited. Recently, in PCT/GB2009/001635 (which claims priority from GB 0811962.0), we have demonstrated the fabrication of functional TFTs based on ZnO where the semiconductor was deposited by SP. The experimental setup of the spray pyrolysis technique used here is shown in Figure 2.

TFTs were fabricated in different device configurations similar to the ones shown in Figures 3(a) and (b). For the substrate 22, a number of different materials have been studied, including plastic (i.e. flexible), glass, and silicon oxide substrates. In principle any substrate material with the required physical properties could be employed. For the experimental work described here the TFTs were fabricated on glass substrates, but different type of substrates could be used, including both inorganic as well as organic (e.g. plastics) materials.

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Using conventional photolithography or simple shadow masking, gate 20, source 14 ("S") and drain 16 ("D") electrodes were defined in a bottom-gate bottom-contact (BG-BC) configuration (Figure 3(b)) or a bottom-gate top-contact configuration (Figure 3(a)).

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In principle many alternative transistor architectures could be employed, other than the bottom-gate bottom-contact architecture of Figures 1 and 3(b), or the bottom-gate top-contact architecture of Figure 3(a). Some examples are shown in Figure 4, which illustrates (a) a bottom-gate top-contact TFT, (b) a top-gate top-contact TFT, (c) a top-gate bottom-contact TFT, (d) a top-gate TFT with asymmetric source-drain contacts, and (e) a double gate TFT. These different device architectures, in combination with different metal electrodes, may be exploited for performance enhancement of the TFT depending on the particular application. Other device architectures are also envisioned and will be familiar to those skilled in the art.

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For this work, low-voltage TFTs were fabricated employing aluminium (Al) gate electrodes that were deposited using thermal vacuum sublimation to a thickness of 5 nm to 100 μm . To form a dielectric layer, the aluminium gate electrodes were then oxidised employing a plasma asher apparatus or by simple thermal annealing in ambient air or controlled oxygen atmosphere. The duration of the plasma ashing and thermal annealing varies depending on the experimental conditions. Typical treatment times were between 1 second and 24 hours. As a consequence of the plasma/thermal treatment, a native aluminium oxide (AlO_x) layer was formed in the surface of the Al gate electrode. As will be explained shortly, the native AlO_x layer plays a dual role, as well as being simple to form. Its first role is that it can function as an ultra-thin gate dielectric layer, while its second role is to provide suitable surface

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chemistry where functionalisation with self-assembling monolayer materials can be performed.

Deposition of the semiconductor was then performed. Specifically, deposition of a ZnO layer was performed using a 0.2 M methanolic precursor solution of zinc acetate di-hydrate (Figure 5) as the channel layer, onto the gate electrodes by spray pyrolysis in ambient air, at various temperatures: 100°C, 200°C, 300°C, 400°C and 500°C.

The film was grown in the following manner: The substrate was placed on the hot plate until the required substrate temperature was stabilised. The precursor solution was then sprayed with the airbrush positioned vertically above the substrate (Figure 2) in a raster fashion. A time delay of 0.1-600 seconds was given before the second spray cycle (in a similar manner) to allow the solution vapours to adsorb to the substrate and convert to ZnO (or any other oxide/semiconductor material depending on the spraying solution). The process can be repeated several times until a semiconducting layer is formed.

Semiconductor film materials, for deposition by spray pyrolysis

In spray pyrolysis a precursor solution is dispersed and transported by means of an inert carrier gas so it arrives at the surface of the targeted substrate in the form of very fine droplets. Upon arrival the material droplets react chemically and convert to the desired chemical compound in the form of a film layer. The chemical reactants are selected such that the by-products (i.e. products formed in addition to the desired compound) are volatile at the specific deposition temperature so they do not stay on the surface of the substrate.

To the best of our knowledge, to date there are no reported examples of low-voltage oxide TFTs fabricated by SP, the most relevant work being our own

patent applications WO 2008/129238, on TiO₂-based TFTs, and PCT/GB2009/001635 (which claims priority from GB 0811962.0), on TFTs based on ZnO and other materials. There are many material systems that could be suitable for the fabrication of low-voltage TFTs by spray pyrolysis. These include all precursor complexes containing cadmium (Cd), zinc (Zn), lead (Pb), tin (Sn), bismuth (Bi), antimony (Sb), indium (In), copper (Cu), mercury (Hg), sulphur (S), selenium (Se) and tellurium (Te).

Other materials that could possibly be used as inorganic semiconductors deposited by spray pyrolysis include:

1. Titanium dioxide – TiO₂ (see WO 2008/129238)
2. Magnesium oxide – MgO
3. Nickel oxide – NiO
4. Molybdenum trioxide – MoO₃
5. Tungsten oxide – WO₃
6. Iron oxide – FeO
7. Zirconium dioxide – ZrO₂
8. Or more general AMO₂ materials where A=Silver (Ag), and M=Al, Ga

9. Materials disclosed in WO 2006/003584, i.e. a compound of any of the materials in the following group (i) together with any of the materials in the following group (ii), wherein group (i) comprises cadmium, zinc, lead, tin, bismuth, antimony, indium, copper and mercury; and group (ii) comprises sulphur, selenium and tellurium.

We have proven the two important concepts of the present disclosure, namely (a) the formation of a native oxide dielectric layer, and (b) the functionalisation of the gate electrode with a self-assembled monolayer, to work with a

semiconductor layer of ZnO deposited by spray pyrolysis. Our most important findings are as follows:

Al-AlO_x-ZnO transistors – to demonstrate the formation of a native oxide dielectric layer

The first type of device that has been fabricated and studied is based on the BG-TC architecture shown in Figure 3(a). As the substrate material we employed either Si/SiO₂ or glass. Aluminium was employed as the gate electrode material, but other materials such as different metals as well as conductive metal oxides with suitable chemical properties could, in principle, be used. As the dielectric layer aluminium oxide was employed. Aluminium oxidation was performed either using an oxygen plasma asher or by annealing on a hot plate (annealing temperature 100-600°C in ambient air or in the presence of water vapour). The semiconductor precursor solution was then deposited by SP with the substrate maintained at temperatures in the range 100-600°C.

Figure 6 shows the transfer characteristics of a ZnO TFT employing an aluminium gate, a native oxide layer of AlO_x as the gate dielectric, ZnO deposited by SP as the semiconductor, and aluminium source and drain electrodes. As can be seen, clear transistor characteristics can be observed with the device exhibiting strong electron transporting (n-channel) behaviour. A current on/off ratio of 10-20 and a maximum electron mobility of ~5 cm²/Vs is obtained. The gate current (I_G) for all measurements was less than I_D by more than one order of magnitude.

Surprisingly, the native aluminium oxide in combination with the spray pyrolysis technique yields functional transistors even when the as-deposited (i.e. non oxidised) aluminium gate electrodes are annealed only for a short

period of time (e.g. 1 second to 5 minutes in the presence of ambient air or water vapour). The surprisingly easy fabrication of the low-voltage ZnO TFTs could be possibly traced to the aqueous nature of the precursor solution that provides, simultaneously, the Al gate electrode with the required oxygen for the formation of a native insulating layer of AlO_x (~1-5 nm thick), and also the required oxygen supply for the conversion of the precursor zinc acetate to ZnO. To the best of our knowledge this is the first example of spray pyrolysis combined with a solution processed metal (Zn in this specific example) acetate and ultra-thin native metal oxide (AlO_x in this specific example) for the fabrication of low-voltage TFTs. Surprisingly, performance of the transistors shown in Figure 6 is among the best reported in the literature for ZnO TFTs based on a solution-processed semiconductor layer.

Al- AlO_x -SAM-ZnO transistors – to demonstrate the functionalisation of the gate electrode with a self-assembled monolayer

Although the Al- AlO_x -ZnO based transistors shown in Figure 6 exhibit high electron mobility, the on/off ratio is relatively low while the gate leakage current (I_G , not shown here) is also relatively high and for $V_G > 1.5$ V becomes comparable with I_D (approximately ten times smaller). In order to improve the transistor characteristics we have functionalised the native aluminium oxide (AlO_x) with a self-assembled monolayer (SAM) dielectric. The specific molecule employed is the octadecylphosphonic acid (ODPA) shown in Figure 7. ODPA consists of a C-18 alkyl chain and a phosphonic acid group at one end. From the literature [6] it is known that such a SAM layer is capable of providing the necessary extra current insulation required.

Functionalisation of the ODPA layer was performed as follows: The aluminium gate electrodes were oxidised using an oxygen plasma asher or by annealing in atmospheric air using a hot plate (annealing temperature 100-

600°C in ambient air or in the presence of water vapour), thereby forming an aluminium oxide layer. The samples were then sonicated in ethanol and blown dry with nitrogen gas. The substrates were then immediately submerged in a beaker containing a 1-5 mM solution of ODPA in ethanol (other solvents may alternatively be used) and left to functionalise for several hours (although other periods of time, in the range of 1 second to 24 hours, are also possible). The modified substrates were sonicated in ethanol, dried in nitrogen gas and then placed in an oven at 140°C for a period of time.

Alternatively, the SAM layer may be functionalised via simple drop casting of the SAM solution on the Al-AlO_x surface, followed by annealing at 140°C and then washing in ethanol, drying in nitrogen gas, and placing in an oven at 140°C. In this way we avoid long time immersion of the substrate to the SAM solution and hence the entire process is very fast. Zschieschang et al. [10] have also demonstrated SAM functionalisation employing micro-contact printing of a SAM solution to an Al-AlO_x surface, and this technique may be employed in conjunction with the embodiments of the present invention.

In our present work, functionalisation of the gate electrode surfaces was confirmed using liquid contact angle measurements and current-voltage measurements. Figure 8 shows a water drop on the AlO_x surface before (Figure 8(a)) and after (Figure 8(b)) functionalisation with ODPA. A clear increase in the water drop's contact angle upon treatment of the surface is observed, confirming the presence of the ODPA SAM. It should be noted, however, that different SAM deposition procedures could be employed for the functionalisation of the ODPA, or other SAM dielectrics known from the literature (e.g. [10]), on the surface of the AlO_x (or other oxide surfaces). Such procedures and materials will be known or familiar to those skilled in the art.

Another important characteristic of the SAM dielectrics employed (ODPA in this particular case), and very relevant to the present work, is their thermally stable nature. Figure 9 shows the contact angle measurements for a water drop on a freshly prepared Al-AlO_x-ODPA dielectric immediately after functionalisation (Figure 9(a)) and after substrate annealing at 400°C for 10 minutes in nitrogen (Figure 9(b)). Clearly the ODPA monolayer is still present (as evident by the high contact angle of the water drop), even after annealing of the substrates at high temperatures for several minutes. The combination of the high insulating properties of ODPA, and possibly many other SAM materials known from the literature, and their thermal stability, make self-assembled monolayer gate dielectrics superb candidate materials for use in combination with spray pyrolysis for the fabrication of low-voltage oxide TFTs.

To prove that ODPA, and generally SAM dielectrics, could be used in combination with spray pyrolysis, and that can lead to improved device performance, we fabricated TFTs using Al-AlO_x-ODPA dielectrics and ZnO layers deposited by spray pyrolysis at substrate temperatures in the range 100-450°C. The transfer and output transistor characteristics obtained for a AlO_x-ODPA-based TFT are shown in Figures 10(a) and (b) respectively. Excellent transistor operation is observed with maximum electron mobilities in the range of 10-30 cm²/Vs, and threshold voltages of the order of $V_{TH} \sim 0$ V.

Although the functionalisation of the dielectric layer with a self-assembled monolayer is a useful technique that may be employed in conjunction with a native oxide dielectric layer, a self-assembling monolayer may be used to form a dielectric layer by itself, without needing to first form a native oxide (or other) dielectric layer. For instance, one could envision the use of conductive oxide gate electrodes, such as tin dioxide (SnO₂), doped-SnO₂ or indium tin oxide (ITO) to name a few, where the SAM dielectric is functionalised directly

onto the gate electrode followed by the deposition of the oxide semiconductor layer by SP. In principle any conductive materials (metallic, oxide, or organic) with suitable surface chemistry could be employed in combination with SAM dielectrics.

5

Low-voltage integrated circuits based on oxide TFTs fabricated using spray pyrolysis

To demonstrate the potential of the low-voltage ZnO TFTs fabricated by SP in real logic circuits, we have fabricated unipolar voltage inverters. To achieve this, two BG-TC low-voltage ZnO TFTs, employing AlO_x -ODPA as the gate dielectric, are integrated to create the circuit shown in Figure 11. The dimensions of the two transistors used here are not limited to those given in Figure 11, but could be designed to any specific size required. Similarly, the specific unipolar circuitry chosen here is not limited to the one shown in Figure 11, but could be adopted to the operating characteristics of the individual transistors used. Typical examples of other unipolar inverter circuits are shown in Figure 12. Similarly, other transistor architectures (see for example Figure 4) such as BG-BC, top-gate or dual-gate configurations could be employed. Such design procedures are standard and will be known to those skilled in the art.

20

Figure 13 shows the experimentally-measured transfer characteristics of a unipolar voltage inverter comprised of two n-channel low-voltage TFTs based on ZnO deposited by spray pyrolysis. The physical dimensions of the individual transistors are shown in Figure 11. Excellent operating characteristics are observed, with the circuits operating with a supply voltage of less than 1.8 V. This demonstrates that our transistors are capable of low-voltage low-power operation.

25

Ultraviolet light sensing ZnO transistors fabricated by spray pyrolysis

In addition to their electronic function, we have also established that ZnO TFTs (including high voltage as well as low-voltage TFTs) can be used as ultraviolet (UV) light detectors. Use of low-voltage ZnO TFTs for UV light detection, in particular, could be very attractive since the devices are operating at low voltages and hence the power consumed is also expected to be very low. An example of the effect of illuminating a low-voltage ZnO TFT with UV light (400 nm) is shown in Figure 14. The transistor structure used for this particular experiment is the one shown in Figure 3(a), but other device architectures could also be used. The UV illumination source used for this experiments was a UV light-emitting diode (UV-LED) with a peak emission (λ) at 400 nm.

The important effect observed upon illumination of the ZnO TFTs with 400 nm light is a shift on the transfer curves toward higher drain currents (I_D) and more positive gate voltages (V_G). The shift depends both on the power density (W/cm^2) of the illumination used, its wavelength (λ) and the exposure time of the TFT to the UV light. We find that when the device is illuminated with green or red light no shift in the operating curves of the transistors is observed. Photoresponse is observed only when the device is illuminated with photon energies higher than the band gap of the ZnO (for example using light wavelengths shorter than 440 nm); then a shift in the operating characteristics of the ZnO TFT is observed. In general, the shorter the light wavelength, the higher the photoresponse of the ZnO TFT observed. We have observed the same UV light induced effects with our “normal” (i.e. not low-voltage) ZnO TFTs based on thick gate dielectrics (for example SiO_2 , or fluoropolymers such as CYTOP).

Another interesting finding is that when the ZnO TFTs are illuminated while maintained in nitrogen ambient, or under vacuum, the photoinduced shift in the

22

operating curves of the transistor upon UV illumination is characterised by relatively long retention times. This means that the operating characteristics following UV illumination do not recover (i.e. back to the operating characteristics measured before UV illumination) for a long period of time that typically exceeds 1 week. When the same test is performed under ambient air, the photoresponse is faster with recovery times ranging between 30 minutes to only few minutes. The effect is shown in Figure 15. The recovery time when performed under ambient air depends on the initial illumination intensity of the UV light, its wavelength, exposure time and the presence of oxygen and relative humidity.

ZnO TFTs could therefore be used for the fabrication of discrete UV light sensors, and also two dimensional sensor arrays. One can also envision integration of such UV sensing ZnO TFTs with auxiliary driving transistors, similar but not limited to those shown in Figure 12, for the fabrication of high gain UV light sensors.

By taking advantage of the dependence of the ZnO TFT photoresponse on the ambient conditions, one can also envision fabrication of gas sensors by monitoring the recovery time of the channel current (I_D) following illumination of the device with suitable electromagnetic radiation (e.g. ultraviolet light).

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CLAIMS

1. A method of forming a low-voltage thin-film field-effect transistor comprising:

5 forming a gate;
 forming a dielectric layer on the surface of the gate;
 forming a source region and a drain region; and
 forming a semiconductor layer adjacent the dielectric layer;
 wherein the dielectric layer is formed as a native oxide layer by
10 oxidising the surface of the gate; and
 wherein the semiconductor layer is deposited by spray pyrolysis.

2. A method as claimed in Claim 1, wherein the semiconductor layer comprises a material selected from a group comprising:

15 oxides; oxide-based materials; mixed oxides; metallic type
 oxides; group I-IV, II-VI, III-VI, IV-VI, V-VI and VIII-VI binary
 chalcogenides; and group I-II-VI, II-II-VI, II-III-VI, II-VI-VI and V-II-
 VI ternary chalcogenides.

- 20 3. A method as claimed in Claim 1, wherein the semiconductor layer comprises a compound of any of the materials in the following group (i) together with any of the materials in the following group (ii), wherein

 group (i) comprises cadmium, zinc, lead, tin, bismuth, antimony,
 indium, copper and mercury; and
25 group (ii) comprises sulphur, selenium and tellurium.

4. A method as claimed in Claim 1, Claim 2 or Claim 3, wherein the native oxide layer is formed using an oxygen plasma asher.

25

5. A method as claimed in Claim 1, Claim 2 or Claim 3, wherein the native oxide layer is formed by annealing.
6. A method as claimed in Claim 5, wherein the annealing is performed at
5 a temperature in the range of 100°C to 600°C.
7. A method as claimed in Claim 5 or Claim 6, wherein the annealing is performed for a time in the range of 1 second to 24 hours.
- 10 8. A method as claimed in any preceding claim, wherein the native oxide layer is of the order of 10 nm or less in thickness.
9. A method as claimed in any preceding claim, wherein the semiconductor layer is deposited using a precursor solution.
15
10. A method as claimed in Claim 9, wherein the precursor solution is doped in order to incorporate dopant atoms in the semiconductor material once formed.
- 20 11. A method as claimed in Claim 10, wherein the dopant atoms are selected from a group comprising: aluminium, indium, gallium, molybdenum, boron, nitrogen, lithium.
12. A method as claimed in any preceding claim, wherein the spray
25 pyrolysis is performed at a temperature in the range of 100°C to 600°C.
13. A method as claimed in Claim 12, wherein the spray pyrolysis is performed at a temperature in the range of 100°C to 400°C.

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14. A method as claimed in Claim 13, wherein the spray pyrolysis is performed at a temperature in the range of 200°C to 400°C.
- 5 15. A method as claimed in any preceding claim, wherein the semiconductor layer is deposited in a raster fashion.
16. A method as claimed in any preceding claim, wherein the semiconductor layer is deposited in a pulsed manner.
- 10 17. A method as claimed in any of Claims 1 to 15, wherein the semiconductor layer is deposited in a continuous manner.
18. A method as claimed in any preceding claim, further comprising heat treating the semiconductor layer to remove residual un-reacted precursor material(s).
- 15 19. A method as claimed in any preceding claim, wherein the gate is formed of aluminium and thus the dielectric layer is formed of aluminium oxide.
- 20 20. A method as claimed in any preceding claim, wherein the semiconductor layer is formed of zinc oxide.
21. A method as claimed in any preceding claim, further comprising functionalising the dielectric layer with a self-assembling monolayer dielectric layer.
- 25 22. A method as claimed in Claim 21, wherein the self-assembling monolayer is formed from constituent molecules, each of which comprises an organic chain with a functional group at one end.

23. A method as claimed in Claim 22, wherein the self-assembling monolayer is formed from octadecylphosphonic acid.
- 5 24. A method of forming a low-voltage thin-film field-effect transistor comprising:
forming a gate;
forming a dielectric layer adjacent the gate;
forming a source region and a drain region; and
10 forming a semiconductor layer adjacent the dielectric layer;
wherein the dielectric layer is formed as a self-assembling monolayer; and
wherein the semiconductor layer is deposited by spray pyrolysis.
- 15 25. A method as claimed in Claim 24, wherein the self-assembling monolayer is formed from constituent molecules, each of which comprises an organic chain with a functional group at one end.
26. A method as claimed in Claim 25, wherein the self-assembling
20 monolayer is formed from octadecylphosphonic acid
27. A low-voltage thin-film field-effect transistor comprising:
a source region;
a drain region;
25 a semiconductor layer disposed between the source and drain regions;
a gate region; and
a dielectric layer disposed between the semiconductor layer and the gate region;

28

wherein the dielectric layer is a native oxide layer formed on the surface of the gate region.

28. A transistor as claimed in Claim 27, wherein the dielectric layer is of the order of 10 nm or less in thickness.

29. A transistor as claimed in Claim 27 or Claim 28, wherein the gate region is formed of aluminium and thus the dielectric layer is formed of aluminium oxide.

30. A transistor as claimed in any of Claims 27 to 29, wherein the semiconductor layer is formed of zinc oxide.

31. A transistor as claimed in any of Claims 27 to 30, wherein the semiconductor layer incorporates dopant atoms.

32. A transistor as claimed in Claim 31, wherein the dopant atoms are selected from a group comprising: aluminium, indium, gallium, molybdenum, boron, nitrogen, lithium.

33. A transistor as claimed in any of Claims 27 to 32, wherein the dielectric layer is functionalised with a self-assembled monolayer dielectric layer.

34. A transistor as claimed in Claim 33, wherein the self-assembled monolayer is formed from constituent molecules, each of which comprises an organic chain with a functional group at one end.

35. A transistor as claimed in Claim 34, wherein the self-assembled monolayer is formed from octadecylphosphonic acid.

36. A low-voltage thin-film field-effect transistor comprising:
a source region;
a drain region;
5 a semiconductor layer disposed between the source and drain regions;
a gate region; and
a dielectric layer disposed between the semiconductor layer and the gate region;
10 wherein the dielectric layer is a self-assembled monolayer.
37. A transistor as claimed in Claim 36, wherein the self-assembled monolayer is formed from constituent molecules, each of which comprises an organic chain with a functional group at one end.
15
38. A transistor as claimed in Claim 37, wherein the self-assembled monolayer is formed from octadecylphosphonic acid.
39. An integrated circuit comprising one or more transistors as claimed in
20 any of Claims 27 to 38.
40. A two-dimensional sensor array comprising a plurality of transistors as claimed in any of Claims 27 to 38.
- 25 41. An ultraviolet detector comprising one or more transistors as claimed in any of Claims 27 to 38, the said transistor(s) being situated such that ambient light can reach the said transistor(s).

42. A gas sensor comprising:

one or more transistors as claimed in any of Claims 27 to 38,
wherein the transistor(s) is/are situated such that ambient gas can come
into contact with the said transistor(s);

5 means for illuminating the transistor(s) with electromagnetic
radiation; and

means for measuring the recovery time of the channel current of
the transistor(s) following illumination by the illuminating means.

10 43. A gas sensor as claimed in Claim 42, wherein the said electromagnetic
radiation is ultraviolet light.

44. A gas sensor comprising:

15 one or more transistors situated such that an ambient gas can
come into contact with the said transistor(s);

means for illuminating the transistor(s) with electromagnetic
radiation; and

means for measuring the recovery time of the channel current of
the transistor(s) following illumination by the illuminating means.

20

45. A gas sensor as claimed in Claim 44, wherein the said electromagnetic
radiation is ultraviolet light.

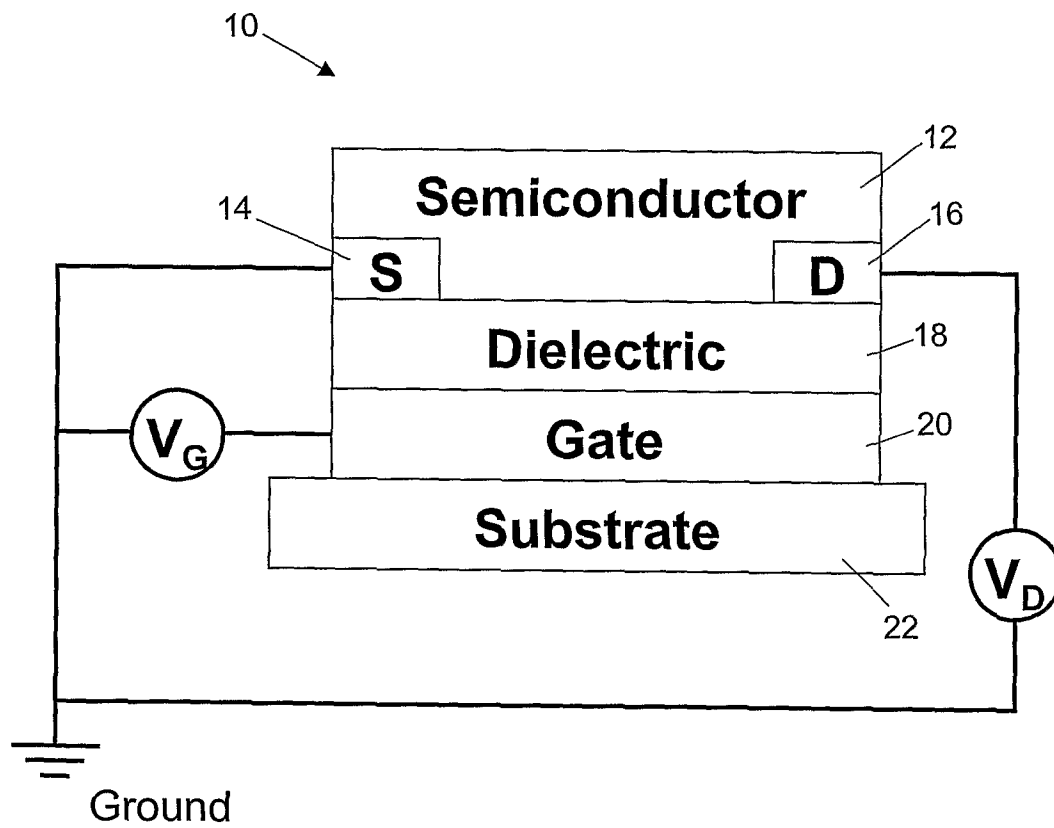
25 46. A gas sensor as claimed in Claim 44 or Claim 45, wherein the or each
transistor is a thin-film field-effect transistor.

47. An ultraviolet detector comprising one or more thin-film field-effect
transistors, wherein the said transistor(s) is/are situated such that
ambient light can reach the said transistor(s).

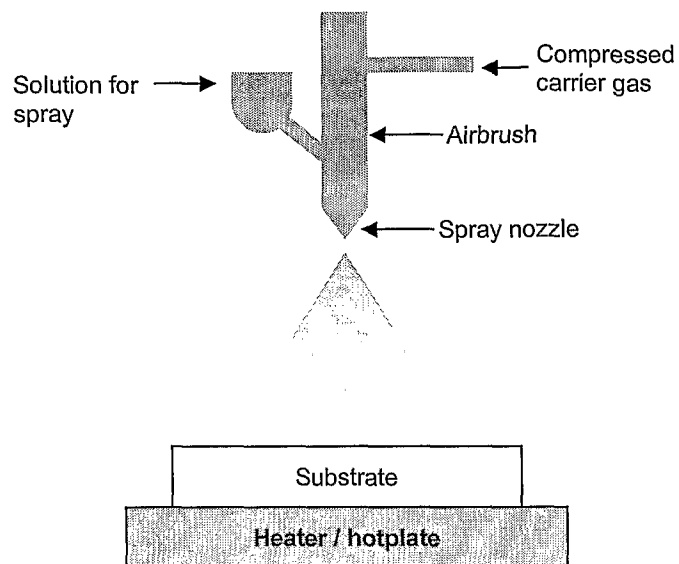
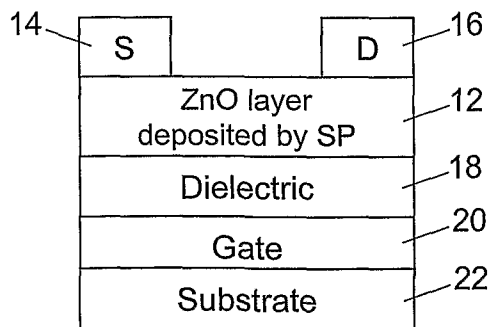
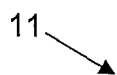
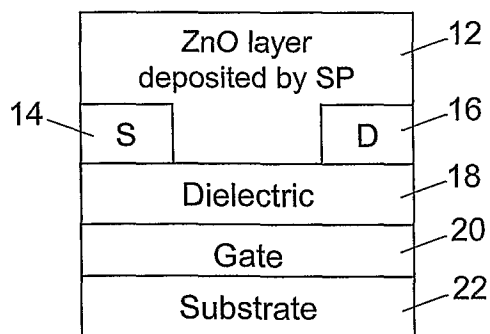
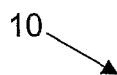
31

48. A gas sensor as claimed in any of Claims 44 to 46, or an ultraviolet detector as claimed in Claim 47, wherein the or each transistor comprises a semiconductor layer formed of zinc oxide.
- 5
49. A method of forming a low-voltage thin-film field-effect transistor substantially as herein described with reference to and as illustrated in any combination of the accompanying drawings.
- 10
50. A low-voltage thin-film field-effect transistor substantially as herein described with reference to and as illustrated in any combination of the accompanying drawings.
- 15
51. An integrated circuit substantially as herein described with reference to and as illustrated in any combination of the accompanying drawings.
52. A two-dimensional sensor array substantially as herein described with reference to and as illustrated in any combination of the accompanying drawings.
- 20
53. An ultraviolet detector substantially as herein described with reference to and as illustrated in any combination of the accompanying drawings.
- 25
54. A gas sensor substantially as herein described with reference to and as illustrated in any combination of the accompanying drawings.

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**Figure 1**

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**Figure 2****(a)****(b)****Figure 3**

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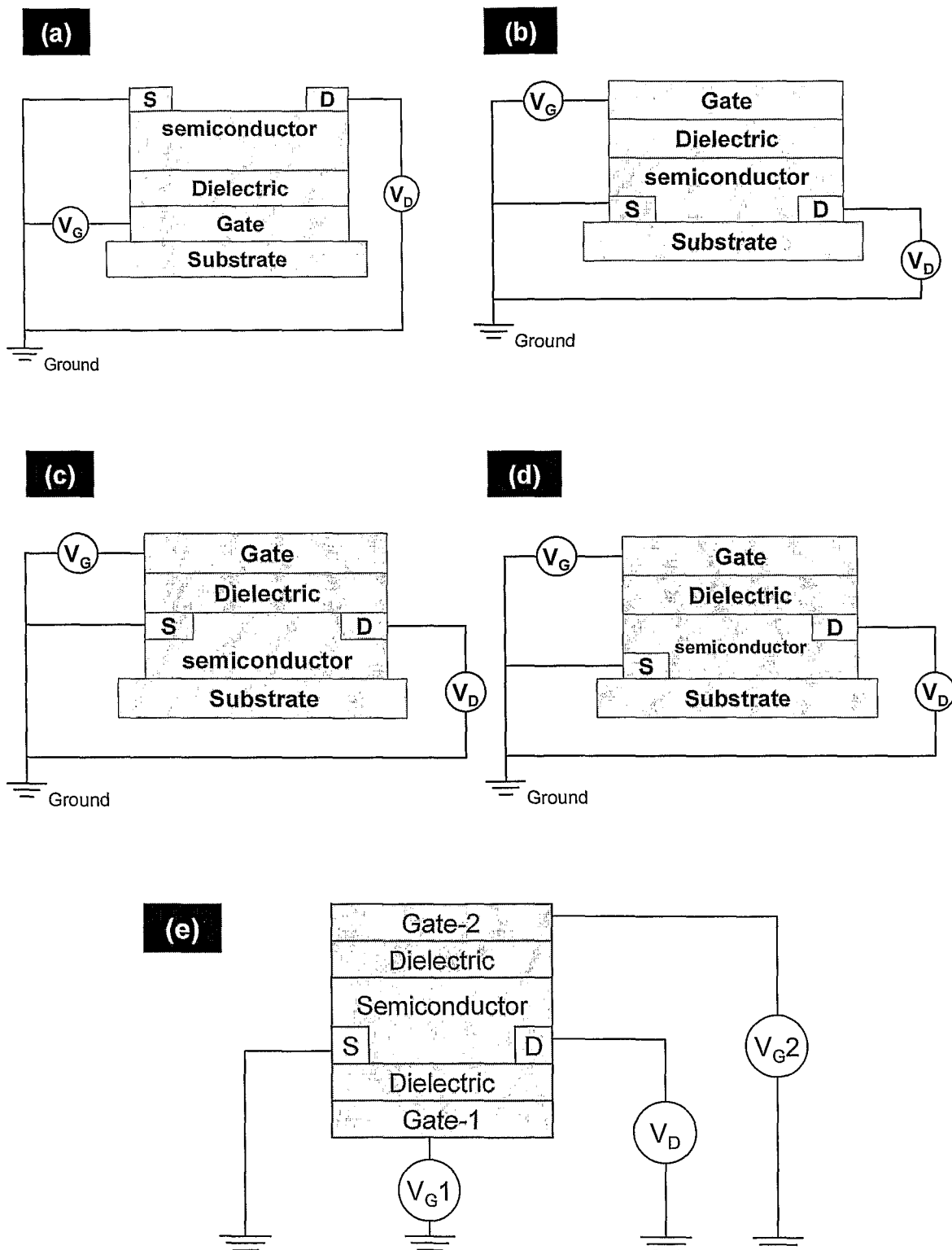
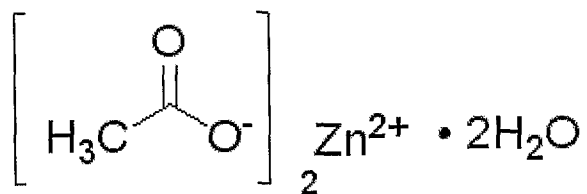
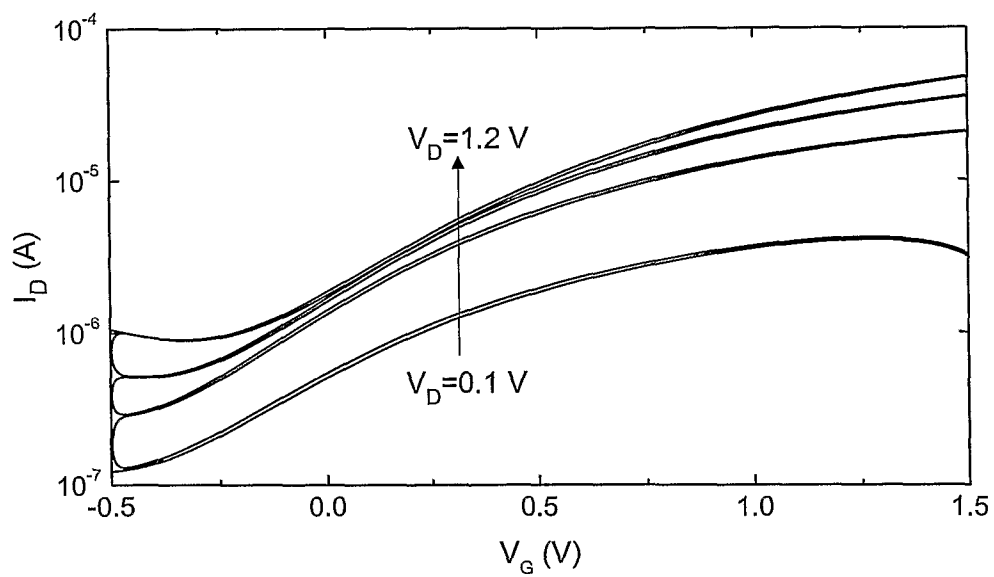
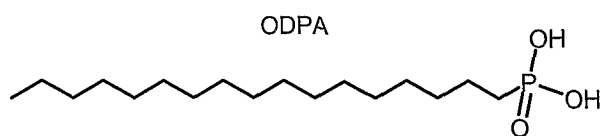


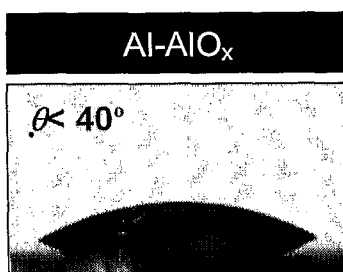
Figure 4

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**Figure 5****Figure 6****Figure 7**

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(a)

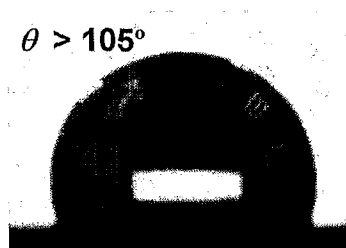


(b)



Figure 8

(a)



(b)

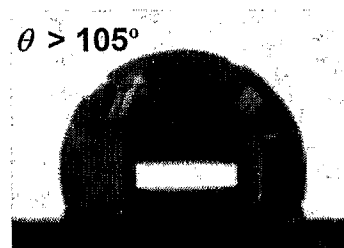


Figure 9

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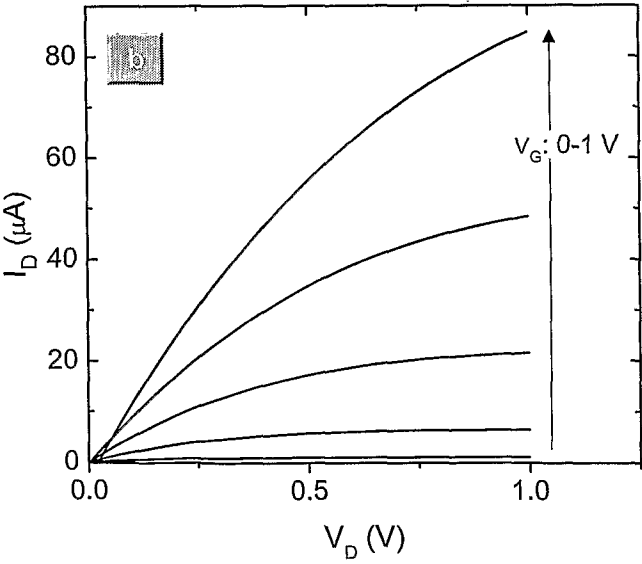
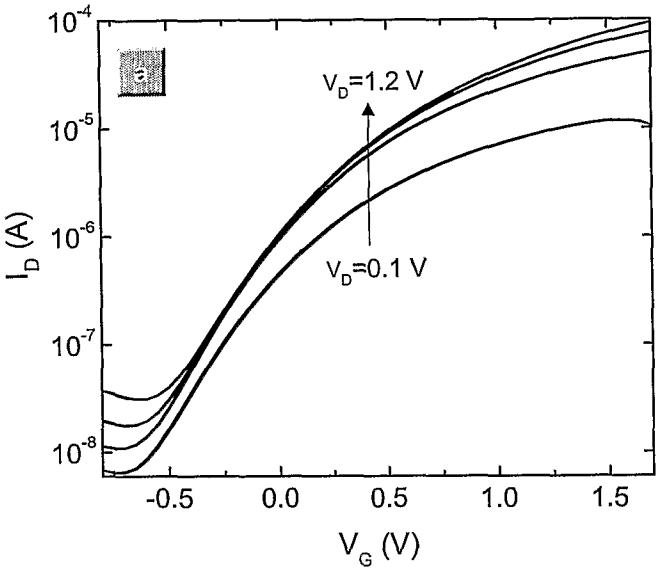
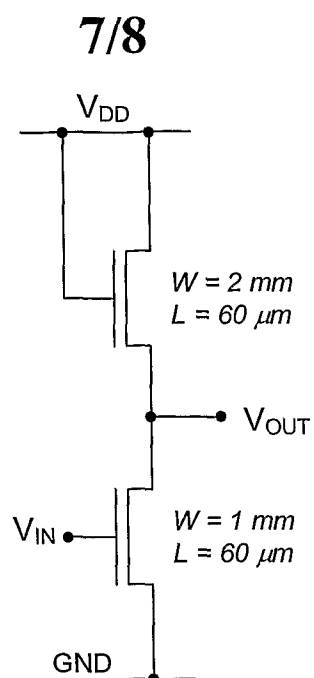
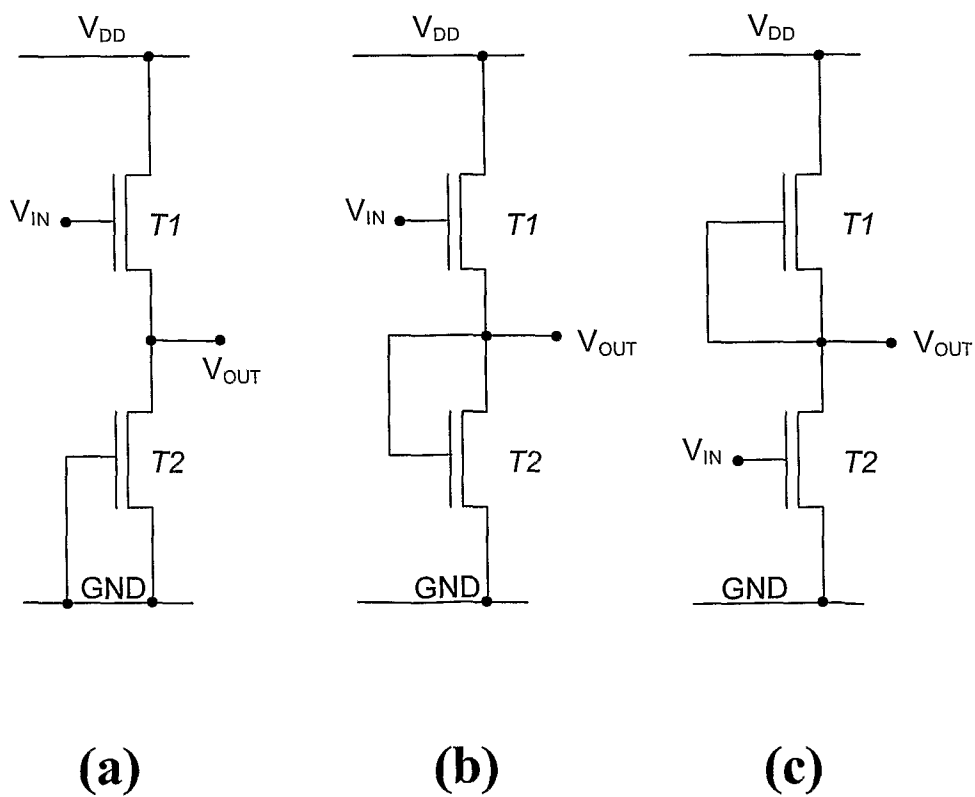


Figure 10

**Figure 11****Figure 12**

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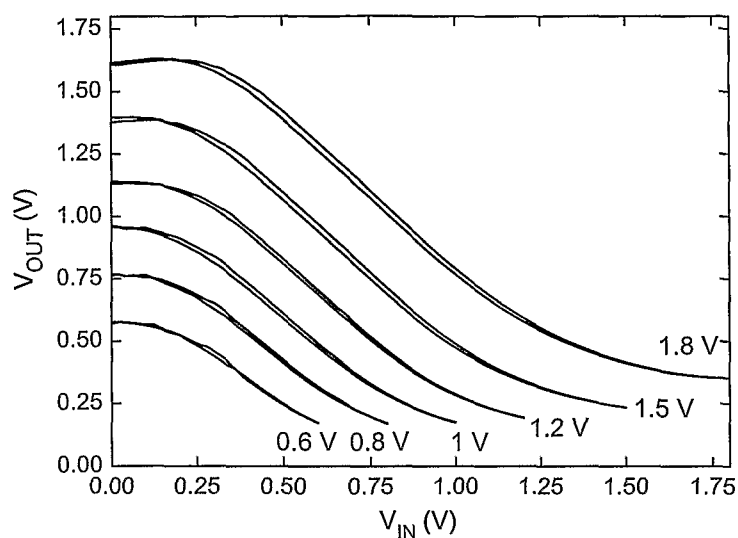


Figure 13

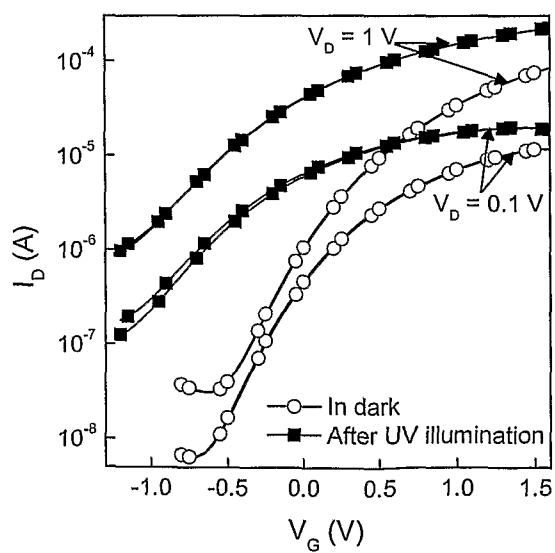


Figure 14

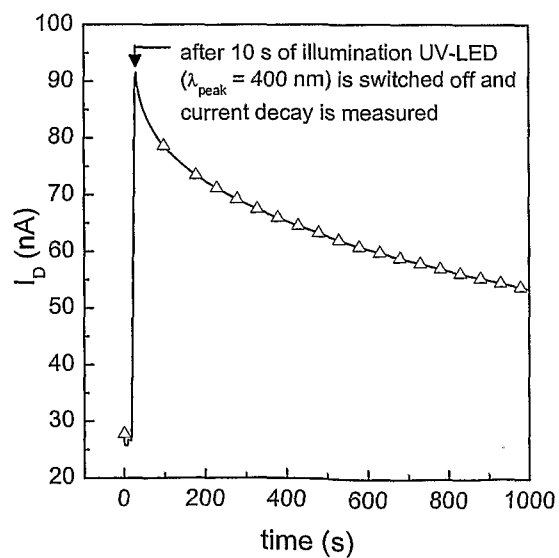


Figure 15

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2009/001687

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L29/786 H01L29/49 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	H. KLAUK ET AL.: "Ultralow-power organic complementary circuits" NATURE, vol. 445, 15 February 2007 (2007-02-15), pages 745-748, XP002544965 cited in the application	27-29, 33-35, 39,49-51
Y	the whole document	1-23, 30-32, 40-43, 52-54
Y	WO 2006/003619 A (KONINKL PHILIPS ELECTRONICS NV [NL]; VAN DAM DIRKJAN B [NL]; MARRA JOH) 12 January 2006 (2006-01-12) page 9, line 30 - page 10, line 2; figures 1,2	1-23, 30-32, 40-43, 52-54



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- * & * document member of the same patent family

Date of the actual completion of the international search

11 September 2009

Date of mailing of the international search report

02/12/2009

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Authorized officer

Juhl, Andreas

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2009/001687

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-23, 27-35, 39-43, 49-54

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International Application No. PCT/GB2009 /001687

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-23,27-35,39-43,49-54

Method of forming a TFT using as gate dielectric a native oxide and a semiconductor formed by spray pyrolysis and its related devices.

2. claims: 24-26,36-38

Method of forming a TFT with gate dielectric formed of a self-assembling monolayer and a semiconductor layer formed by spray pyrolysis and its related devices

3. claims: 44-46,48

Gas sensor having means for measuring the recovery time of the channel current following illumination.

4. claim: 47

UV detector with TFT situated such that ambient light can reach the transistor

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2009/001687

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2006003619 A	12-01-2006	NONE	