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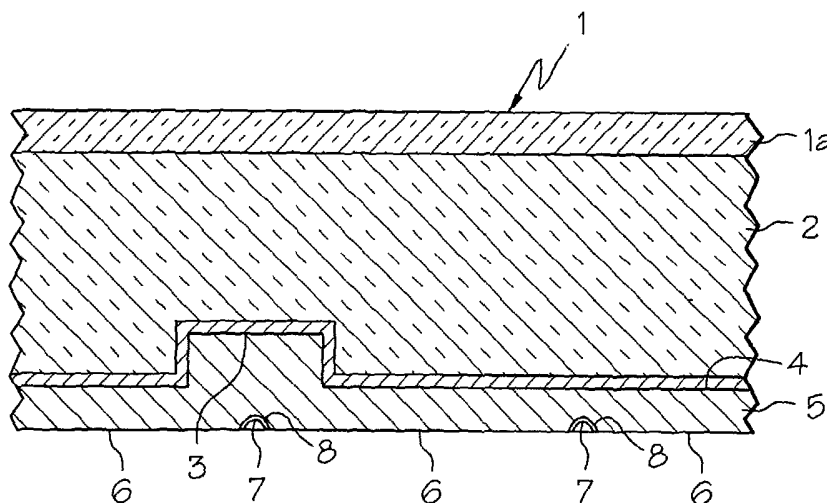
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(54) Title: METHOD OF PLANARIZING A SEMICONDUCTOR WAFER



(57) Abstract: A semiconductor wafer (1) adapted for planarization by polishing the wafer (1) with a polishing pad and a polishing fluid, the wafer (1) having a metal layer (5), and a resistant film formed selectively on low topography features of the metal layer (5) to resist the polishing fluid while high topography features of the metal layer (5) are removed by said polishing, which minimizes a time duration for attaining planarization of the wafer (1) by said polishing.

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METHOD OF PLANARIZING A SEMICONDUCTOR WAFER

The invention relates to planarization of a semiconductor wafer by polishing the wafer with a polishing pad and a polishing fluid.

An integrated circuit comprises many semiconductor transistors that are electrically connected to one another by circuit interconnects constructed as tiny metal lines. The metal lines transmit electrical signals that operate the transistors. The transistors and circuit interconnects are of miniature size, and are constructed according to semiconductor manufacturing processes that involve formation of the transistors and circuit interconnects by depositing or growing different semiconductor materials on a wafer of silicon, i.e., a semiconductor wafer.

A semiconductor wafer is adapted for manufacture thereon of many circuit interconnects arranged according to a pattern. Circuit interconnects are constructed on a semiconductor wafer, by depositing a dielectric layer on an underlying silicon wafer, followed by recessing tiny trenches in the surface of the dielectric layer, the trenches being arranged in a pattern, followed by applying a known barrier film on the dielectric layer, followed by depositing a layer of metal onto the underlying barrier film and dielectric layer to assure that the trenches are filled with metal. A process known as chemical mechanical planarization, CMP, is performed with a polishing pad and a polishing fluid to remove the layer of metal and the barrier film from the underlying dielectric layer, and to provide a polished surface that is smooth and planar. Thus, the process of CMP is often described as a method of polishing a semiconductor substrate, or as a method of planarizing a semiconductor substrate.

An aim of the process of CMP is to polish the metal in the trenches to a height that is substantially the same height as that of the smooth, planar polished surface. The polished metal in the trenches provides the circuit interconnects. The dielectric layer with the circuit interconnects provides a substrate on which successive dielectric layers are constructed. The successive dielectric layers have additional circuit interconnects to provide successive layers of circuit interconnects for integrated circuits that are constructed in large

numbers on the patterned wafer.

Planarizing a semiconductor substrate by CMP is performed with a polishing pad and a polishing fluid, which together remove material from the surface of the substrate. The polishing pad rubs against the surface to remove material by abrasion. Simultaneously, the polishing fluid is dispensed at an interface of the polishing pad and the substrate. The polishing fluid chemically reacts with the surface, and dissolves material that results from chemical reaction of the surface with the polishing fluid. Thus, material is removed from the surface by both mechanical abrasion and chemical reaction.

The surface has a surface topography with high topography features, i.e., high spots, and low topography features, i.e., low spots. The wafer is planarized, by CMP polishing of the surface with a polishing pad and a polishing fluid, which removes material from the topography features, until the topography features become substantially the same height. However, the polishing fluid reacts chemically with both the high spots and the low spots, and removes material from both of them. Thus, polishing the high spots and the low spots to the same height is counteracted by having the polishing fluid react chemically with the low spots.

The metal circuit interconnects in the trenches have corresponding low spots in the metal layer prior to a polishing operation. When such low spots on the circuit interconnects are polished by CMP, too much of the metal can be removed, as indicated by the presence of excessive concavity in the polished surfaces of the circuit interconnects. Dishing is a term that refers to the concavity in the circuit interconnects, as caused by CMP. Dishing is a structural defect of the circuit interconnects that contributes to unwanted attenuation of the signals transmitted by the circuit interconnects. Accordingly, a CMP process must be performed with care to minimize dishing.

Attempts have been undertaken to hasten the process of planarization by CMP, which would lower manufacturing costs. However, increasing the speed of a CMP process to rapidly remove material from the surface of a semiconductor wafer, causes rapid dishing, and causes an uneven polished surface, which is

indicative of deficient planarization. Thus, a need exists for an invention that minimizes dishing, while minimizing the time duration for planarizing a surface by polishing with a polishing pad and a polishing fluid.

The invention pertains to a process according to which, a resistant film is
5 selectively formed on low topography features on a semiconductor wafer.
Further, the invention pertains to a semiconductor wafer adapted for polishing with a polishing pad and a polishing fluid with which high topography features on the wafer chemically react and dissolve, and low topography features on the wafer have a resistant film that resists the polishing fluid. Further, the invention
10 pertains to apparatus for forming a resistant film selectively on low topography features on a semiconductor wafer.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings.

Fig. 1 is a fragmentary, enlarged, edgewise view of a semiconductor
15 wafer that is inverted and impinging a shield, the wafer having high topography features and low topography features.

Fig. 2 is a view similar to Fig. 1, and discloses the wafer as having a resistant film formed selectively on low topography features.

Fig. 3 is a view similar to Fig. 2, and discloses the wafer after polishing to
20 remove high topography features from the wafer.

Fig. 4 is a schematic view of apparatus for adapting a semiconductor wafer with a resistant film formed selectively on low topography features on the wafer.

The invention minimizes the time duration for planarizing a surface on a
25 semiconductor wafer by polishing the surface with a polishing pad and a polishing fluid.

The invention adapts a semiconductor wafer for removal of high topography features at a faster removal rate than for low topography features.

The invention further adapts a semiconductor wafer to minimize dishing
30 of circuit interconnects, while the high topography features are removed by polishing with a polishing pad and a polishing fluid.

The invention adapts a semiconductor wafer for minimized removal rate of the low topography features, while the high topography features are removed by polishing with a polishing pad and a polishing fluid.

Further, the invention adapts a semiconductor wafer to minimize dishing, while the high topography features are removed by polishing with a polishing pad and a polishing fluid.

Fig. 1 discloses a semiconductor wafer (1), shown inverted. The semiconductor wafer (1) includes, a thin silicon wafer (1a) on which is deposited a dielectric layer (2). Fig. 1 discloses one of a number of trenches (3) that are constructed in the dielectric layer (2), according to known photoetching, manufacturing operations. A barrier film (4) is deposited on the dielectric layer (2) that underlies the barrier film (4). A metal layer (5) is deposited on the barrier film (4) to overlie the underlying dielectric layer (2), and to assure that portions of the metal of the metal layer (5) fills the trenches (3) in the dielectric layer (2). The metal layer (5) has a surface topography, shown inverted in Fig. 1, with high topography features (6) and low topography features (7). The metal in the trenches (3) have low topography features (7), as the expected result of deposition of the metal layer (5). Low topography features (7) that occur elsewhere are due to recessed imperfections in the metal layer (5).

According to known manufacturing operations, the semiconductor wafer (1), disclosed by Fig. 1, is polished with a polishing pad and a polishing fluid, according to a known CMP operation. A first phase of CMP is performed to planarize the semiconductor wafer (1). Planarization of the semiconductor wafer (1) is attained, when the high topography features (6) and the low topography features (7) are polished to substantially the same height, with minimized dishing. After planarization is attained, a second phase of CMP is performed until a remainder of the metal layer (5) is removed from the underlying dielectric layer (2), and the dielectric layer (2) is polished to a smooth, planar polished surface. Further, the metal in the trenches (3) are polished to a height that is substantially the same height as a planar polished surface on the semiconductor wafer (1), with minimized dishing.

The invention adapts the semiconductor wafer (1) for planarization by the first phase of polishing. Further, the invention minimizes the time duration for the polishing operation to attain planarization. Further the invention minimizes dishing by the polishing operation.

5 Fig. 2 discloses a resistant film (8) selectively formed on the low topography features (7). According to an embodiment of the invention, Fig. 1 further discloses the semiconductor wafer (1) inverted, with the high topography features (6) impinging a shield (9). For example, according to an embodiment of the invention, the semiconductor wafer (1) is held in impingement with the shield
10 (9) by the mechanism of acceleration of gravity. The resistant film (8) forms on the low topography features (7) that are spaced from the shield (9). According to an embodiment of the invention, a film forming gaseous atmosphere, that has film forming, gaseous constituents, is introduced in spaces between the shield (9) and the low topography features (7). A resistant film (8) is formed by contact
15 of the gaseous atmosphere with the low topography features (7). Thus, the semiconductor wafer (1) is adapted for planarization by the first phase of polishing.

 The formation of a resistant film (8) on the high topography features (6) is minimized, such that the high topography features (6) are without substantial
20 amounts of the resistant film (8), which enables the high topography features (6) to react chemically with the polishing fluid and dissolve, while polishing the metal layer (5) with a polishing pad and a polishing fluid.

 Upon polishing the metal layer (5) with a polishing pad and with a polishing fluid, the resistant film (8) resists the polishing fluid, while the high
25 topography features (6) chemically react with the polishing fluid and dissolve, according to known CMP operations. The high topography features (6) are removed by abrasion applied by the polishing pad, and by chemical reaction and dissolution. The low topography features (7) having the resistant film (8) are
30 farther from the polishing pad than the high topography features (6), and are subject to little or no abrasion, as compared with the abrasion applied by the polishing pad on the high topography features (6). Further, the resistant film (8)

resists chemical reaction and dissolution of the low topography features (7), while the high topography features (6) are removed by chemical reaction with the polishing fluid, and then dissolution. Thus, said polishing removes the high topography features (6) at a faster removal rate than the low topography features (7), which minimizes the time duration for attaining planarization by polishing. Further, because, the resistant film (8) resists the polishing fluid, the low topography features (7), including those corresponding to metal in the trenches (3), resist chemical reaction and dissolution, while polishing the semiconductor wafer (1) by CMP. Thus, dishing of the metal in the trenches (3) is minimized.

Fig. 3 discloses the semiconductor wafer (1) with the high topography features (6) having been polished, to become substantially the same height as the low topography features (7). The low topography features (7) continue to have some of the resistant film (8) thereon. Polishing with a polishing pad and a polishing fluid continues, such that the high topography features (6) and the low topography features (7) with the resistant film (8) thereon, while at the same height, are subjected to the same abrasion, as applied by the polishing pad.

According to an embodiment of the resistant film (8), comprising a metallic compound of the metal in the metal layer (5), rubbing thereof by the pad breaks the surface tension of the polishing fluid in contact with the resistant film (8), enabling the resistant film (8) to react chemically with the polishing fluid and dissolve, which removes the resistant film (8) by chemical reaction with the polishing fluid, as well as, by abrasion applied by the polishing pad.

According to an embodiment of the resistant film (8), comprising a substance that is not a metallic compound of the metal layer (5), continued polishing will remove the resistant film (8) primarily by abrasion. The high topography features (6) and the low topography features (7) having the resistant film (8), now at the same height, are removed substantially evenly by both abrasion, and chemical reaction. They are removed substantially evenly from the underlying dielectric layer (2) by continued polishing, which further provides a smooth, planar polished surface with minimized dishing.

Fig. 4 discloses apparatus (10) for adapting the wafer (1) with a resistant film (11). The apparatus (10) includes, a chamber (11) containing the shield (9) for impingement against a corresponding wafer (1). A door (12) on the chamber (11) opens an amount sufficient for receiving the semiconductor wafer (1) edgewise as the wafer (1) is inserted into the chamber (11). The wafer (1) is positioned adjacent to the shield (9), while a film forming, gaseous atmosphere is introduced into the chamber (11). Further, the gaseous atmosphere is introduced between the wafer (1) and the shield (9). The wafer (1) is shown in broken outline, in Fig. 4. Further, the wafer (1) is inverted and impinges the shield (9), similarly as disclosed by Fig. 1. Relative movement of the wafer (1) and the shield (9) causes the wafer (1) to impinge the shield (9). The gaseous atmosphere between the wafer (1) and the shield (9) becomes trapped in the spaces between the shield (9) and the low topography features (7) on the wafer (1). The door (12) is closed, while the gaseous atmosphere is in contact with the low topography features (7). A resistant film (8) forms on the low topography features (7) by contact of the gaseous atmosphere with the low topography features (7). Subsequently, the door (12) is opened, and the semiconductor wafer (1) is removed from the chamber (11).

According to an embodiment disclosed by Fig. 4, the door (12) is opened and closed by a motor driven, door operating mechanism (13) that is operated by electrical signals transmitted between the door operating mechanism (13) and a controller (14).

Fig. 4 discloses a source (15) of gaseous atmosphere connected to the chamber (11) by a conduit (16) and a control valve (17) that controls a flow of the gaseous atmosphere from the source (15) to the chamber (11). The control valve (17) is opened and closed by a motor driven, valve control mechanism (18) that is operated by electrical signals transmitted between the valve control mechanism (18) and the controller (14). Opening the control valve (17) introduces the gaseous atmosphere into the chamber (11). According to one embodiment, the valve (17) and controller (14) comprise a mass flow control mechanism to introduce a precise mass of gaseous atmosphere of measured

chemical moles to form a resistant film (8) of desired thickness on the low topography features (7). Thereby, the gaseous atmosphere is substantially expended to form the resistant film (8). According to another embodiment, the resistant film (8) forms during a time duration sufficient to form a resistant film (8) of desired thickness on the low topography features (7), followed by removing the remainder of the gaseous atmosphere from the chamber (11), for example, by exhaust of the gaseous atmosphere through an exhaust conduit (19).

Fig. 4 discloses a motor driven, pick and place mechanism (20) that picks up the semiconductor wafer (1), for example, between reciprocating jaws (21), inserts the wafer (1) in the chamber (11), and places the wafer (1) so as to impinge the shield (9) similarly as disclosed by Fig. 1. Accordingly, the pick and place mechanism (20) imparts relative movement of the shield (9) and the corresponding semiconductor wafer (1) to impinge the shield (9) against high topography features (6) on the surface of the corresponding semiconductor wafer (1). After releasing the wafer (1), the pick and place mechanism (20) is withdrawn from the chamber (11), while the door (12) quickly closes to entrap the gaseous atmosphere in an enclosed chamber (11). The pick and place mechanism (20) is operated by electrical signals transmitted between the pick and place mechanism (20) and the controller (14). The resistant film (8) forms by contact of the gaseous atmosphere with the low topography features (7). Subsequently, after passage of sufficient time to form the resistant film (8), the door (12) is opened, and the semiconductor wafer (1) is removed from the chamber (11) by operation of the pick and place mechanism (20).

Fig. 4 discloses the controller (14) connected by signal transmitting conductors (22) to the door operating mechanism (13), the control valve (17), and the pick and place mechanism (20). Alternatively, the controller (14) may communicate with signals propagated by wireless transmission. Although the controller (14) is depicted as a single electronic unit that integrates multiple electronic devices for controlling the door (12), the control valve (17), and the pick and place mechanism (20), the controller (14) further comprises, such

multiple electronic devices as separate units. Further, the controller (14) further comprises, a machine programmable device that operates the various devices according to a desired sequence of operation.

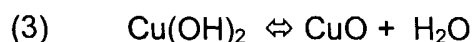
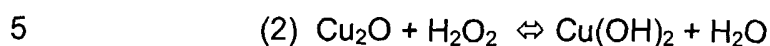
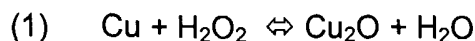
According to an embodiment of the invention, the chamber (11) is
5 provided as an annealing oven supplying heat at a controlled temperature, for example, in the range of 100 to 500 degrees C. The wafer (1) remains in the closed chamber (11) for a time duration sufficient for annealing the corresponding semiconductor wafer (1) to a desired resistivity. The metal layer (5) is annealed to lower its resistivity for compliance with industry accepted,
10 technical standards for such resistivity. Both annealing and formation of the resistant film (8) occur simultaneously in the chamber (11) of an annealing oven. Advantageously, the formation of a resistant film (8) takes place within the time duration of the annealing process.

According to an embodiment of the invention, a semiconductor wafer (1)
15 is adapted for planarization by having a resistant film (8) selectively formed on low topography features (7) on the semiconductor wafer (1). While polishing the semiconductor wafer (1) with a polishing pad and a polishing fluid, the resistant film (8) on the low topography features (7) resists the polishing fluid, which minimizes the removal rate of the low topography features (7), while the high
20 topography features (6) react chemically with the polishing fluid and dissolve, which removes the high topography features (6) at a faster removal rate than the low topography features (7).

The invention adapts a metal layer (5) for planarization by providing a resistant film (8) on low topography features (7) on the metal layer (5) to resist
25 polishing fluid while the metal layer (5) is polished by a polishing pad and the polishing fluid to remove the high topography features (6). Because the high topography features (6) are removed at a faster removal rate than the low topography features (7), the time duration for attaining planarization is minimized by the invention.

30 According to an embodiment, a semiconductor wafer (1) has a metal layer (5) of copper. A polishing fluid comprising, in part, deionized water and

hydrogen peroxide, together with a polishing pad, are used to polish the copper by CMP. Thus, the metal layer (5) of copper chemically reacts with the polishing fluid and dissolves according to the chemical reactions:



According to an embodiment of the invention, the low topography features (7) on the wafer (1) are exposed to a copper oxide forming atmosphere in an enclosed chamber (11) for a time duration sufficient to form a uniform
10 oxide film of a thickness that is sufficient to resist the polishing composition. For example, the oxide film is Cu_2O , and comprises the resistant film (8). The oxide film is formed with a sufficient thickness to resist the polishing composition by being resistant to wetting by the deionized water of the polishing fluid. Thereby, chemical reaction (2), above is precluded from reaction with the resistant film
15 (8), while the high topography features (6) of the metal layer (5) are removed by polishing with the polishing pad and the polishing fluid. Planarization is attained in a minimized time duration for polishing, because the resistant film (8) minimizes the removal rate of the low topography features (7), while the high topography features (6) are removed at a faster removal rate than the low
20 topography features (7).

Further, as disclosed by Fig. 3, once the metal layer (5) becomes substantially planar with the low topography features, polishing is continued. Thereby, the polishing pad contacts the surface of the resistant film (8), which breaks the surface tension of the polishing fluid in contact with the resistant film
25 (8), which wets the resistant film (8) with the polishing fluid. The resistant film (8) reacts chemically with the hydrogen peroxide and dissolves, according to the chemical reaction (2), above. Thereby, the resistant film (8) is removed, both by abrasion applied by the polishing pad, and by chemical reaction with the polishing fluid and dissolution. Both the metal layer (5) of Cu, and the resistant
30 film (8), are removed at substantially the same removal rate, once planarization is attained, in a manner disclosed by Fig. 3.

According to an embodiment, a patterned semiconductor wafer (1) having a metal layer (5) of copper is placed in an annealing oven, with the metal layer (5) inverted and engaged against an optically flat shield (9). The metal layer (5) has a surface topography with both high topography features (6) and low topography features (7). The high topography features (6) are known to extend in a range of 5000 Angstroms to 7000 Angstroms beyond the low topography features (7). The high topography features (6) impinge the shield (9), which holds the low topography features (7) spaced from the shield (9). A gas permeable space is present between the shield (9) and each of the low topography features (7). A gaseous atmosphere, comprised of high purity oxygen, conducive to forming a resistant film (8) of oxide of the type Cu_2O on a Cu surface is present in the oven during the time that the patterned wafer (1) undergoes a known annealing process. The known annealing process is performed by using a known annealing oven in which the patterned wafer (1) is subjected to a specified elevated temperature for a specified time duration. Industry standard annealing ovens operate at a fixed temperature in a range of 100 to 500 degrees Centigrade. According to an embodiment of the invention, the film is Cu_2O . However the invention further includes the formation of any film suitable for resisting a polishing fluid, which film forms onto a metal layer (5) by contact with a film forming gaseous atmosphere, such as, a gaseous atmosphere adapted with film forming constituents of gaseous state.

The shield (9) is a flat plate of a material capable of being machined to a flat surface that will be in intimate engagement with the high topography features (6) on the metal layer (5), and which will avoid scratching of the metal layer (5). Embodiments of the shield (9) include, and are not limited to, alumina (white sapphire), silica (quartz), polytetrafluoroethylene or steel, any of which are capable of being manufactured, such as, by machining and polishing, to a desired flatness, as, for example, a desired flatness specified by an industry standard, technical specification known as "optically flat".

The invention pertains to a process, according to which, a film suitable for repelling a polishing fluid, forms onto low topography features (7) on a metal

layer (5) of a patterned wafer (1), and adapts the wafer (1) for removal of the low topography features (7) at a slower removal rate by polishing with a polishing pad and with a polishing fluid with which the metal layer (5) chemically reacts and dissolves for removal of high topography features (6) of the metal layer (5).

The invention pertains to a process, according to which, a film, that is suitable for resisting a polishing fluid, forms onto low topography features (7) on a metal layer (5) of a patterned wafer (1), and adapts the low topography features (7) for minimized removal rate by polishing with a polishing pad and with a polishing fluid with which the metal layer (5) chemically reacts and dissolves for removal of high topography features (6) of the metal layer (5).

According to an embodiment of the invention, the low topography features (7) on the wafer (1) are exposed to a copper oxide forming atmosphere in the oven for a time duration sufficient to form a uniform oxide film of a thickness that is sufficient to resist the polishing composition. The desired oxide film forms on low topography features (7) on the metal layer (5), coextensively within the time duration of the known annealing process. As a result, when the annealed wafer (1) is finished with the annealing process, the metal layer (5) is not only annealed, but also is adapted with a film that resists a polishing fluid, and that is formed selectively on low topography features (7) on the metal layer (5).

According to an embodiment, the invention pertains to a process, according to which, a film, that is resistant to a polishing fluid, forms onto low topography features (7) on a metal layer (5) of a semiconductor wafer (1), and adapts the low topography features (7) for minimized removal rate by polishing with a polishing pad and with a polishing fluid with which the metal layer (5) chemically reacts and dissolves for removal of high topography features (6) of the metal layer (5).

Claims:

1. A semiconductor wafer adapted for planarization by polishing the wafer with a polishing pad and a polishing fluid, the wafer comprising, a metal layer having a surface topography with high topography features and low topography features, and
5 the metal layer having a resistant film on the low topography features to resist the polishing fluid, and the high topography features being chemically reactive with the polishing fluid, and dissolving while being polished with the polishing pad and the polishing fluid, which minimizes the time duration for
10 attaining planarization of the wafer by said polishing.
2. The semiconductor wafer as recited in claim 1 wherein, the resistant film is an oxide film.
3. The semiconductor wafer as recited in claim 1 wherein, the metal layer is an annealed metal layer of desired resistivity.
- 15 4. The semiconductor wafer as recited in claim 1, and further comprising: trenches in a dielectric layer underlying the metal layer, and metal of the metal layer filling the trenches, and the metal having some of the low topography features with the resistant film thereon.
5. A method of planarizing a semiconductor wafer having a metal layer
20 with a surface topography comprised of both high topography features and low topography features, comprising the steps of:
selectively forming a resistant film on the low topography features to resist polishing fluid, and
polishing the metal layer with a polishing pad and with a polishing fluid
25 with which the high topography features chemically react and dissolve, such that said polishing removes the high topography features at a faster removal rate than the low topography features, to attain planarization of the semiconductor wafer.
6. The method as recited in claim 5, further comprising the step of:
30 minimizing formation of the resistant film on the high topography features of the metal layer.

7. The method as recited in claim 5, further comprising the steps of:
annealing the metal layer, and
selectively forming the resistant film on the low topography features while
annealing the metal layer.

5 8. A method of adapting a metal layer for planarization by polishing the
metal layer with a polishing pad and a polishing fluid to remove high topography
features from the metal layer, comprising the steps of:
forming a resistant film on low topography features on the metal layer to resist
polishing fluid, and

10 minimizing formation of the resistant film on the high topography features
to adapt the high topography features for removal by polishing with a polishing
pad and a polishing fluid with which the high topography features on the metal
layer chemically react and dissolve to attain planarization of the metal layer.

15 9. The method as recited in claim 8, wherein the step of forming a
resistant film, further comprises the steps of:

impinging the high topography features with a shield to space the low
topography features away from the shield,

introducing a film forming, gaseous atmosphere between the low
topography features and the shield, and

20 contacting the film forming, gaseous atmosphere with the low topography
features to form the polishing fluid resistant film.

10. An annealing oven for selectively providing a film on low topography
features on a surface of a semiconductor wafer, comprising:

25 a chamber to enclose the wafer for a time duration and temperature to
anneal the wafer with a desired resistivity,

a shield in the chamber for impingement with the wafer,

a source of gaseous atmosphere capable of forming a film on a surface
on the wafer to resist polishing fluid,

a control valve connecting the source to the chamber,

30 a controller opening and closing the control valve to introduce the
gaseous atmosphere into the chamber to form a resistant film of desired

thickness on low topography features of the surface on the wafer, while the shield impinges high topography features on the wafer, and a mechanism controlled by the controller to impart relative movement of the shield and the wafer to insert the wafer into the chamber, and to place the wafer
5 with the high topography features impinging the shield, and to remove the wafer from the shield and from the chamber subsequent to the time duration sufficient to anneal the wafer.

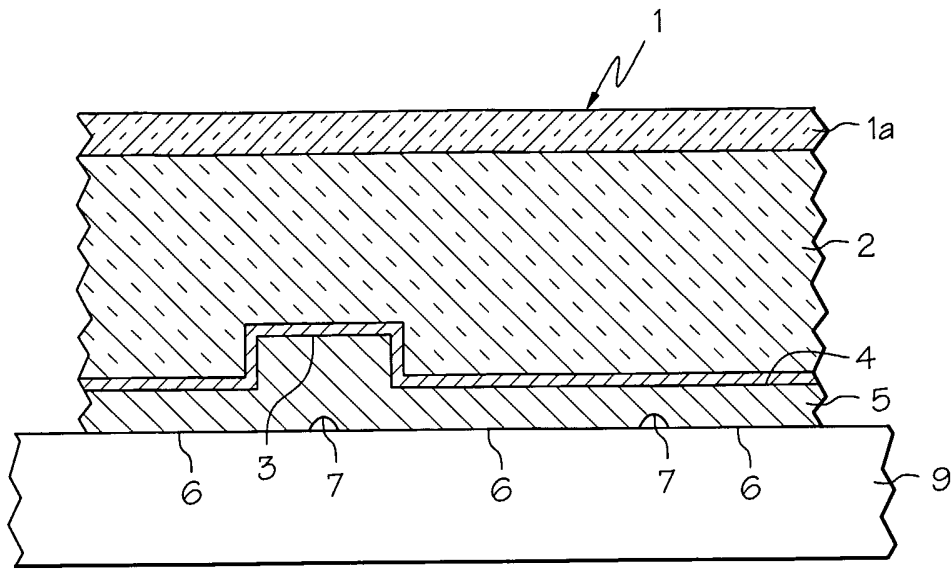


FIG. 1

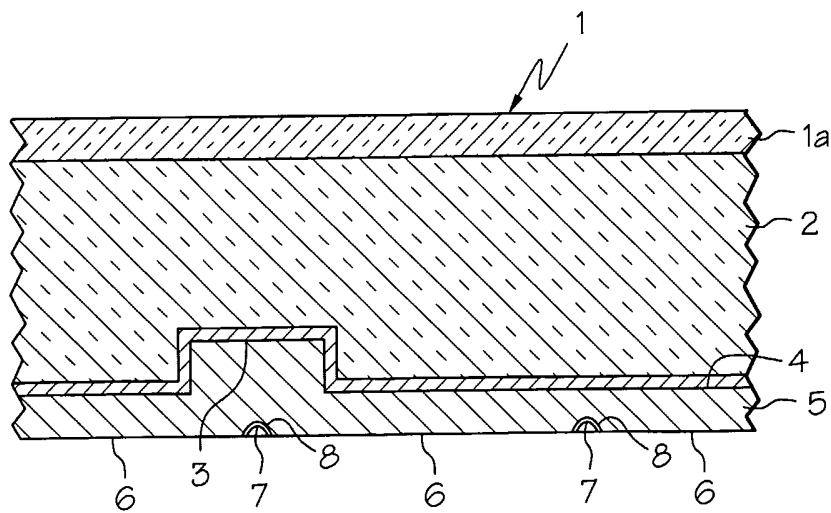


FIG. 2

INTERNATIONAL SEARCH REPORT

PCT/US 02/22335

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/321

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 051 496 A (JANG SYUN-MING) 18 April 2000 (2000-04-18) the whole document ---	1, 3-6, 8
X	US 6 069 082 A (SUDIJONO JOHN LEONARD ET AL) 30 May 2000 (2000-05-30) the whole document ---	1, 3-6, 8
X	US 6 153 523 A (CHEUNG ROBIN W ET AL) 28 November 2000 (2000-11-28) column 6; figure 2 ---	1-4
X	US 6 103 625 A (MARCYK GERALD T ET AL) 15 August 2000 (2000-08-15) column 4 --- -/--	1-4

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

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P document published prior to the international filing date but later than the priority date claimed

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