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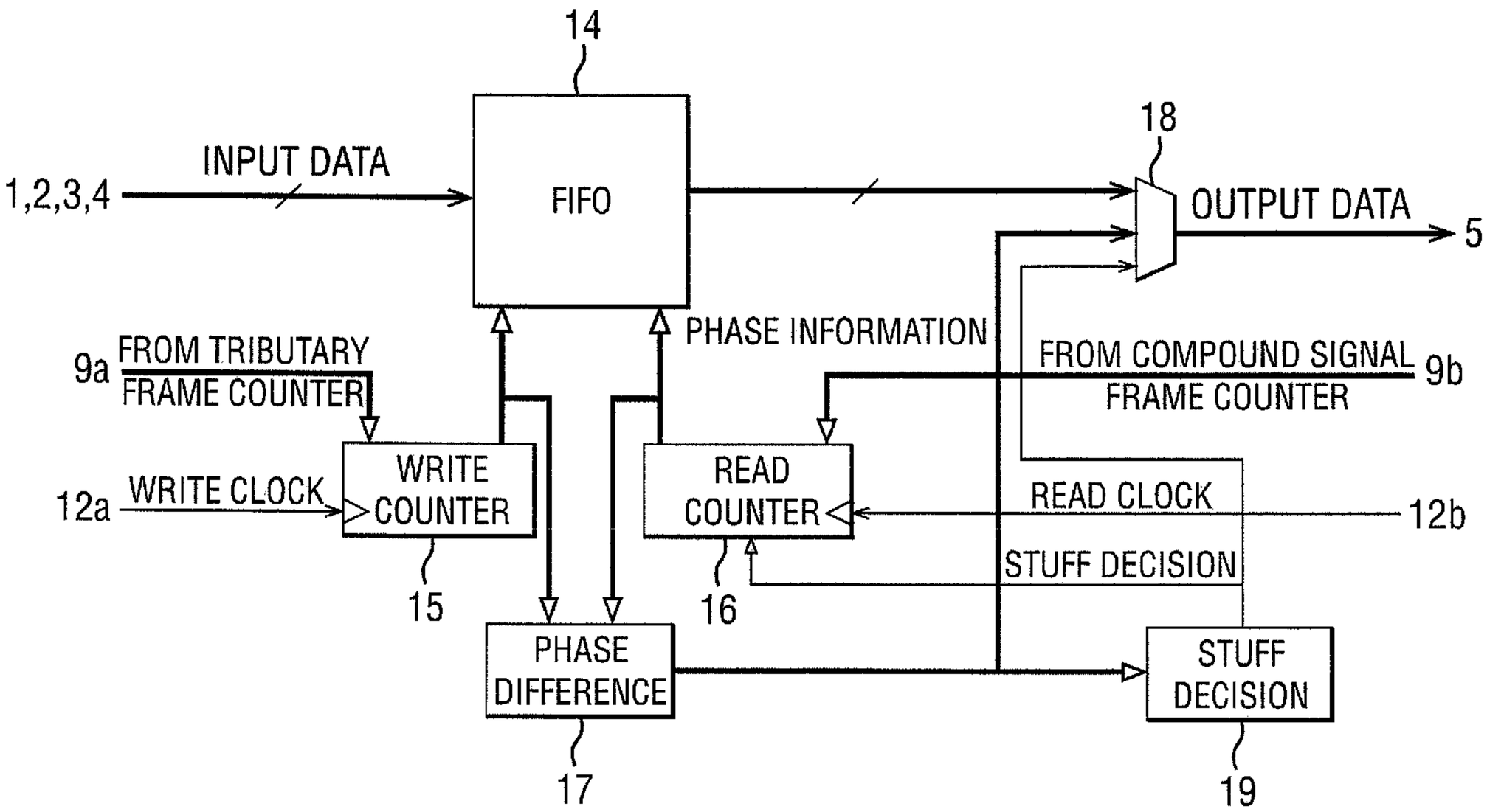
(54) Titre : METHODE ET APPAREIL POUR L'EMISSION ET LA RECEPTION DE SIGNAUX TRIBUTAIRES MULTIPLEX
(54) Title: A METHOD AND APPARATUS FOR TRANSMITTING AND RECEIVING MULTIPLEX TRIBUTARY SIGNALS



(57) Abrégé/Abstract:
Method and apparatus for transmitting and receiving a plurality of individual tributary signals in multiplex form via a common line. At the transmitting end, the tributary signals, each of which having a similar initial frequency, are converted into a compound signal having a frame structure with a common data rate. At the receiving end from the compound signal each individual tributary signal is retrieved with its initial frequency. A phase information signal portion including a respective phase difference between each tributary signal and the compound signal is formed and inserted into the compound signal in the shape of respective coded bits, and the initial frequency of each tributary signal is recovered from the phase information signal portion included in the respective coded bits belonging to the respective tributary signal.

Bleisteiner 7-7-7-22

A METHOD AND APPARATUS FOR TRANSMITTING AND RECEIVING MULTIPLEX TRIBUTARY SIGNALS

Abstract

Method and apparatus for transmitting and receiving a plurality of individual tributary signals in multiplex form via a common line. At the transmitting end, the tributary signals, each of which having a similar initial frequency, are converted into a compound signal having a frame structure with a common data rate. At the receiving end from the compound signal each individual tributary signal is retrieved with its initial frequency. A phase information signal portion including a respective phase difference between each tributary signal and the compound signal is formed and inserted into the compound signal in the shape of respective coded bits, and the initial frequency of each tributary signal is recovered from the phase information signal portion included in the respective coded bits belonging to the respective tributary signals.

A METHOD AND APPARATUS FOR TRANSMITTING AND RECEIVING MULTIPLEX TRIBUTARY SIGNALS

Field of the Invention

The invention relates to a method and an apparatus for transmitting and receiving a plurality of individual tributary signals in multiplex form via a common line.

Background of the Invention

A data line can carry a plurality of signals originating from a plurality of individual sources. In practice, a plurality of signals of nominal the same frequency termed "tributary signals" are multiplexed for being transmitted via the common line as a "compound signal". The multiplexed signals are mapped into the compound signal which has a frame structure and is of a higher data rate than the sum of the tributary frequences. The compound signal, received at the receiver, is demultiplexed. The individual tributary signals so obtained should be identical to the original tributary signals before being multiplexed at the transmitter. This means that the frequency of each demultiplexed tributary signal ("the recovered clock") should be identical to the frequency of the original signal.

In order to adapt to the common data rate of the compound signal, additional bits are used. This offers the possibility to transmit initial tributary signals of somewhat different frequencies. Some of the additional bits are used to transmit control information needed for the rate adaption of these tributary signals. Some of the additional bits can also be used to transmit some other additional information. The additional bits are put in a fixed position into the framed compound signal. Rate adaption is made by a stuffing procedure. To that end, gaps are provided in fixed frame positions, wherein information data can be inserted, or which can be left empty. When the initial tributary frequency is lower than the nominal rate, these gaps remain empty (positive stuffing). When the initial tributary frequency is higher than the nominal rate, some of the bits are inserted in the empty positions (negative stuffing). The tributary signals which are adapted in rate, are multiplexed, that

is, the bits or bytes of the signals are interleaved and transmitted to the receiver through the common line. For recovering the tributary signals at the receiver, the signals are demultiplexed. For recovering the frequency or clock, phase information transmitted with the compound signal is used, namely the phase difference between the compound signal and the tributary signal. This phase difference is transmitted in the gaps provided in the fixed frame positions and makes no big harm. However, the stuffing information means a rough quantization of the phase which causes wander and jitter of the recovered frequency or clock.

Summary of the Invention

It is an object of the invention to held wander and jitter in the compound signal as low as possible.

The invention is defined in claims 1 and 5.

In the transmitter, the phase difference between the compound signal and the tributary signal is accurately calculated. This calculated phase difference is coded preferably by a binary number and is transmitted in dedicated bytes of the compound line signal. In the receiver, the initial frequency of each tributary signal is recovered. For that purpose, the phase information transmitted is used.

The accurate calculation of the phase difference is obtained by using an auxiliary clock at the transmitter. Furthermore, the mean value of the phase difference is calculated for a fixed time interval where the mean value is obtained by an integrator.

Brief Description of the Drawings

Fig. 1 is a block diagram of a transmitter,

Fig. 2 is a block diagram of a synchronizer,

Fig. 3 is a block diagram of a receiver, and

Fig. 4 is a block diagram of a desynchronizer.

Detailed Description

Fig. 1 shows a transmitter for inputting four tributary signals 1, 2, 3, 4 and outputting a line compound signal 5 which includes all data of the tributary

signals and some control data and may have a frequency of say 10 GHz. Each tributary signal is delivered to a respective synchronizer 6 which prepares a rate adapted tributary signal 61 for being interleaved by a multiplexer 7 with the remaining rate adapted tributary signals 62, 63, and 64. The multiplexer 7 composes the data of the tributary signals 61 to 64 and delivers such composed signal to a frame constructor 8 which finally outputs the line compound signal via line 5. The frame constructor is controlled by a frame counter 9 and a system clock 10 having the frequency of the line compound signal. The system clock 10 is also delivered to the frame counter 9 and a phase-locked loop 11 which outputs an internally generated auxiliary clock. The output of the phase-locked loop 11 and a further auxiliary clock 12 are delivered to a gate 13 so that the auxiliary clock 12 can be made effective for each of the synchronizers 6.

The auxiliary clock 12 is an uncorrelated cycle to the writing cycle and the reading cycle and is used to obtain a higher resolution of the phase difference between signals.

Cycle adaption, which is aimed at, makes it necessary to use a plurality of gate functions. For this reason, cycle adaption is realized in CMOS technology which allows a relative low frequency of say 78 MHz (in relation to 10 GHz of the compound signal 5). Therefore, the serial data are transformed to parallel data and are written with this low frequency into a memory and read out with a similar low frequence from the memory.

Fig. 2 shows particulars of each synchronizer 6. Input data from one of the tributary signals 1 through 4 is delivered to a FIFO register 14 which is controlled by a write counter 15 and a read counter 16. The write counter 15 is operated by a write clock 12a and receives the numbers of the bits in the tributary signal via line 9a. The read counter 16 is operated by a read clock 12b and receives the number of the bits from the compound signal through line 9b. The register 14 is an elastic store which provides write-in positions (write address) for the data bits of the respective tributary signals 1 to 4, and read-out positions (read address) for reading out these data bits together with

bit gaps as provided by the frame structure of the compound signal. A phase difference unit 17 is provided which by the operation of the write counter 15 and the read counter 16, forms or calculates a phase difference between each tributary signal and the compound signal.

In detail, the phase difference is formed between write and read address of register 14. The resolution obtained with this measurement corresponds to the cycle time of the writing cycle or the reading cycle, that is, phase difference measurement is made syncronously with one of these cycles. However, this resolution is not sufficient to fulfil the requirements as to jitter at the output of the tributary signal. Furthermore, the phase difference between write and read address is changing continuously, and measurement is only a rough quantization of this phase difference. This is the reason why the auxiliary clock 12 is used which is uncorrelated to the writing and reading cycle and allows measurement at fine stepped times. (The auxiliary clock 12 is drifting slowly, so that, in a measuring period, the clock shifts through all possible positions during a cycle time period of the writing or reading cycle. Additionally, an average value is formed for a defined measuring period which corresponds to the distance between two stuffing positions,

i. e. the measured values are integrated across the measuring time. The average value obtained allows the decision: stuffing positively, stuffing negatively or no stuffing.

Formation of such average value allows to calculate the influence of the gaps which, due to the frame construction, occur regularly.

The phase difference unit 17 makes a binary number from the average phase difference and delivers such coded phase information to a data output gate 18. The coded phase information is also delivered to a stuff decision unit 19 which has outputs connected to the read counter 16 and the output data gate 18.

The auxiliary clock 12 with its portions write clock 12a and read clock 12b allows the accurate calculation of the phase difference between the line signal 5 and the tributary signals 1, 2, 3, and 4, respectively. The phase

difference unit 17 includes the integrator referred-to above which, for a fixed time interval, forms the mean or average value of the phase difference which is the basis for calculating, the phase difference between line signal and tributary signal.

Fig. 3 shows a receiver for four tributary data outputs 21, 22, 23, 24. These output lines 21 through 24 belong to respective desynchronizers 26 which are connected to a demultiplexer 27. The demultiplexer 27 is controlled by a frame alignment circuit 28 which is interconnected with a frame counter 29. System clock 30 is connected to frame counter 29 and a gate 25 which is also connected to the frame alignment circuit through a recovered clock line 25a. The gate 25 generates internally an auxiliary clock which is delivered to a phase-locked loop 31 which outputs to a gate 33 having a second input connected to a further auxiliary clock 32. The gated auxiliary clock is also connected to each desynchronizer 26.

Line 5 delivers the compound signal carrying the data of the tributary signals and also additional bits to the frame alignment circuit 28 which firstly outputs the data of the composed signal and secondly the recovered clock 25a of the compound signal. The recovered clock 25a is used in the frame counter 29 to decide when a frame begins and ends. The demultiplexer 27 receives the data of the composed signal 28a and is controlled by the frame counter 29 so as to deliver the appropriate rate adapted data 71 to 74 to the respective desynchronizer 26 in the adapted rate. The auxiliary clock 32 is used to reconstruct the initial frequency or rate of the respective desynchonizer 26 so that each tributary data output 21, 22, 23, or 24 has a frequency which is exactly the same as the initial frequency of the signal.

Fig. 4 shows a desynchronizer circuit 26. Data from the demultiplexer 27 on line 27a get into a FIFO register 34, to which a write counter 35 and a read counter 36 as well as a phase difference unit 37 are connected. FIFO register 34 is an elastic store having write-in positions (write address) for the compound signal received, and read-out positions (read address) for the data bits of the respective tributary signals. Input line 27a is also connected to a

phase and stuff information unit 39 which has a second input 29a from compound signal frame counter 29. Phase and stuff information unit 39 has a first output 39a for delivering stuff information to the write counter 35 and a second output 39b for delivering phase information to a summing member 40 which has a second input from the phase difference unit 37. The output of the summing member 40 is the input of the phase-locked loop 31 which includes a controller 41, a numeric controlled oscillator 42, a phase detector 43, a filter 44 and a voltage-controlled oscillator 45. The output of the voltage-controlled oscillator is the read clock 32b and is also used as the tributary clock to an output data gate 38.

The data of the composed signal reaching the demultiplexer 27 from the frame alignment circuit 28 are demultiplexed, so that signals 71 to 74 containing the additional bits in an adapted rate are obtained in succession in the several desynchronizers 26. Controlled by the frame counter 29, the additional bits in the compound signal are read out from the rate adapted data stream of the tributary signal 27a into unit 39, whereas all bits in the compound signal are written into elastic store 34. The coded phase information taken up from unit 39 is used for an accurate calculation of the phase difference between the write and read address of the elastic store 34. The whole phase difference is calculated in phase difference unit 37.

The whole phase difference has several portions:

stuffing information (which is a rough quantization of the phase course, and is only transferred when actually a stuffing operation is made),

synchronizer phase difference between write and read addresses (which has been calculated at the synchronizer and is transferred to the desynchronizer with specific bytes. This value is transferred regularly, one time per stuffing position independently from whether there is a stuffing operation, or not), and

desynchronizer phase difference between write and read addresses (calculated at the desynchronizer as a mean or average value, in the same manner as at the synchronizer).

The whole phase difference is the addition of these portion and is added to the

phase course of the system clock or cycle of the respective channel or tributary signal (when frame gaps removed) so as to yield the original phase course of the respective channel.

In detail, phase information as well as phase difference calculated is further processed for such clock recovery in the phase-locked loop 31. The loop includes a numeric controlled oscillator 42 so that the output signal thereof takes the initial frequency of the respective tributary signal 1, 2, 3, or 4. The phase-locked loop 31 is responsive for delivering the clock with the correct phase relation. When recovering the clock on line 32b, any phase deviation from the phase of an ideal clock of the same frequency is wander and jitter. With invention, wander and jitter are kept low by the procedure described above, since the tributary clock on line 32b is recovered from the clock of the demultiplexed signal from which the gaps contained in the compound signals have been removed by virtue of the phase-locked loop 31. The additional bits in the regular gaps of the frame structure of the compound signal produce only low values of phase deviation, since the phase-locked loop 31 has a low cut-off frequency. On the other hand, irregular gaps as occurring with stuffing produce irregular phase steps at the input of the phase-locked loop 31. This will produce big phase changes at the output of the phase-locked loop. However, with invention the transmitted phase difference is used when recovering the clock in the receiver so that the clock produced in the phase-locked loop 31 is a clock with the desired phase for each tributary signal. The phase at the output of summing member 40 contains no more irregular and big phase steps.

Claims

1. A method of transmitting and receiving a plurality of individual tributary signals in multiplex form via a common line, including the steps of:converting, at the transmitting end, the individual tributary signals, each of which having a similar initial frequency, into a compound signal having a frame structure with a common data rate, and retrieving, at the receiving end, from the compound signal each individual tributary signal with its initial frequency, characterized in that at the transmitting end, a phase information signal portion including a respective phase difference between each tributary signal and the compound signal is formed and inserted into the compound signal in the shape of respective coded bits, and, at the receiving end, the initial frequency of each tributary signal is recovered from the phase information signal portion included in the respective coded bits belonging to the respective tributary signals.

2. The method of claim 1 wherein the phase difference between tributary signal and compound signal is calculated by forming the difference between a write address and a read address of an elastic store (14, 34).

3. The method of claim 1 or 2 wherein a total phase is calculated which has three main portions:
   a) stuffing information,
   b) phase difference between write and read addresses at the syncrhonizer, and
   c) phase difference between write and read addresses at the desynchronizer.

4. The method of any of claims 1 through 3 wherein an auxiliary clock (12, 32) is used when calculating the phase difference between the compound signal and the tributary signal.

5. An apparatus for transmitting and receiving a plurality of individual tributary signals in multiplex form via a common line (5), comprising: a transmitter which includes

a plurality of synchronizers (6), each operating a respective individual tributary signal (1 to 4) to get tributary signals (61, 62, 63, 64) having an adapted rate,

a multiplexer (7) to interleave said adapted rate tributary signals (61 to 64) within a compound signal (5), and a receiver which includes a demultiplexer (27) to separate said compound signal (5) into respective tributary signals (71, 72, 73, 74) having an adapted rate, and a plurality of desynchronizers (26) each operating a respective adapted rate tributary signal (71 to 74) to get retrieved tributary signals (21, 22, 23, 24), characterized in that

the transmitter includes means for calculating (15, 16, 17) the phase difference between the compound signal (5) and each tributary signal (1, 2, 3, 4), means (17) for coding the phase difference in bit form, and means (18)for inserting the bits coding the phase difference into the compound signal (5), and the receiver includes means (39) for reading out the bits coding the phase difference from the compound signal (5), means (35, 36, 37, 31) for recovering the frequency of the adapted rate tributary signals, and

means (40, 41, 42) for adjusting the phase of the retrieved tributary signals (21 to 24).

6. The apparatus of claim 5 wherein transmitter and receiver each include an elastic store (14, 34) which provides write-in positions (write address) and read-out positions (read address) for writing in, at the transmitter, the data bits of the respective tributary signals, and reading out these data bits together with bit gaps as provided by the frame structure of the compound signal, and, at the receiver, for writing in the compound signal received and reading out the data bits of the respective tributary signals.

7. The apparatus of claim 6wherein the elastic store (14, 34) includes a write counter (15; 35) and a read counter (16, 36), the write counter (15; 35) being operated by a write clock (12a, 32a) derived from an auxiliary clock (12; 32) and the read counter (16; 36) being operated by a read

clock (12b , 32b) derived from a phase-locked loop (11; 31).

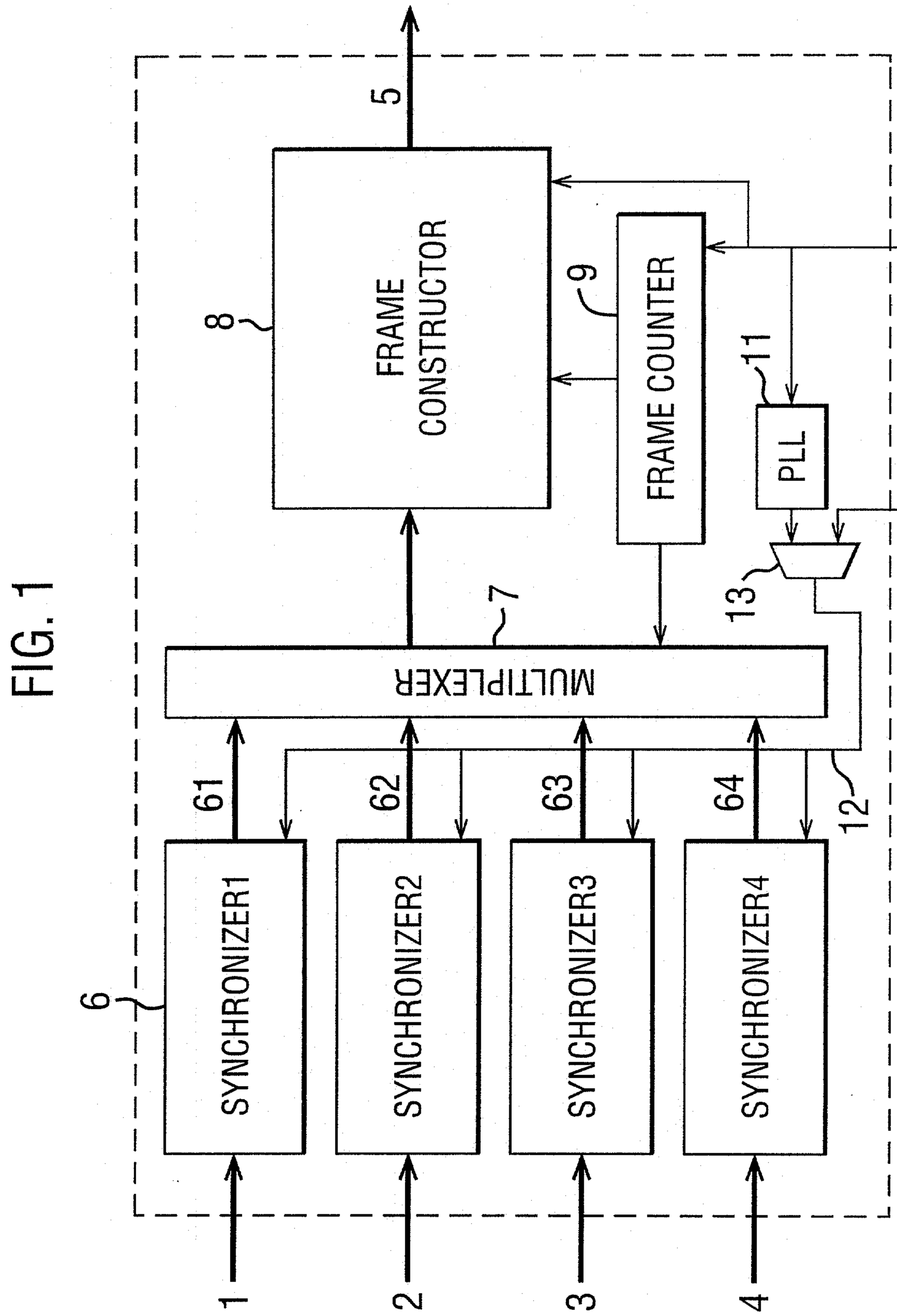

5
FRAME CONSTRUCTOR
8
FRAME COUNTER
9
10
PLL
11
12
13
7
MULTIPLEXER
12
SYNCHRONIZER1
SYNCHRONIZER2
SYNCHRONIZER3
SYNCHRONIZER4
61
62
63
64
6
1
2
3
4

FIG. 1

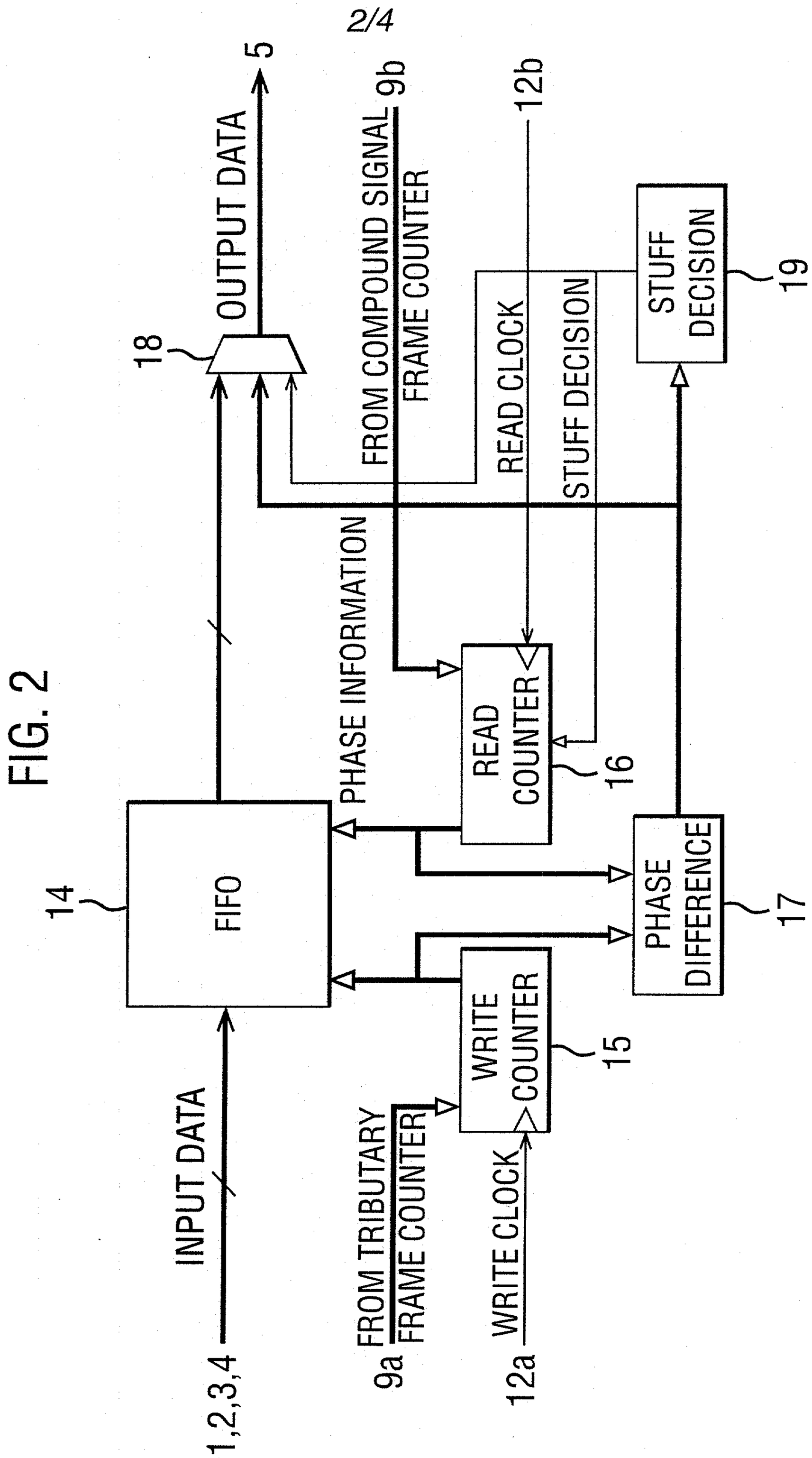

INPUT DATA
1,2,3,4
FROM TRIBUTARY FRAME COUNTER
9a
WRITE CLOCK
12a
WRITE COUNTER
15
FIFO
14
PHASE INFORMATION
READ COUNTER
16
PHASE DIFFERENCE
17
OUTPUT DATA
5
FROM COMPOUND SIGNAL
9b
FRAME COUNTER
READ CLOCK
STUFF DECISION
12b
STUFF DECISION
19
18

FIG. 2

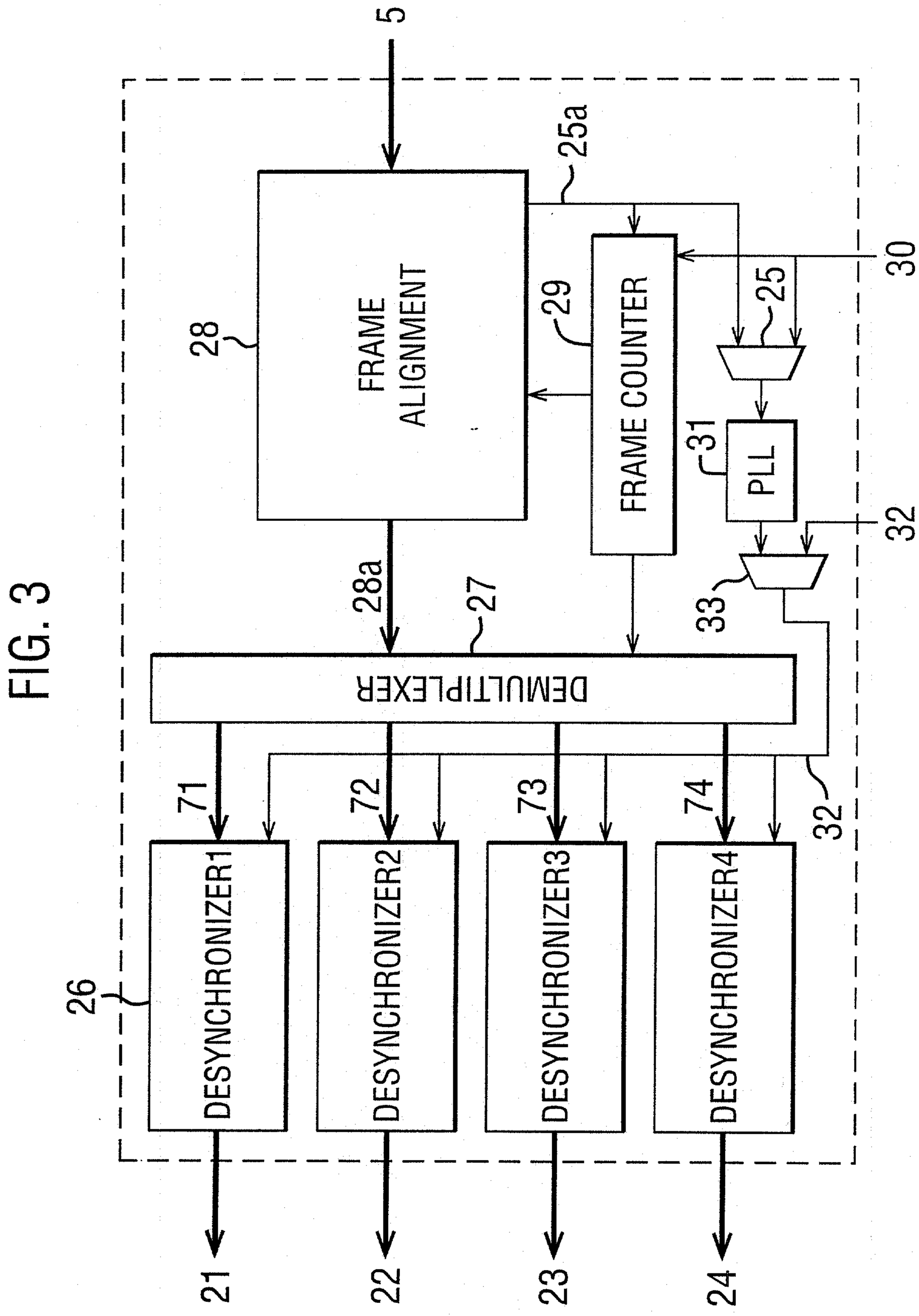

5
25a
28
FRAME ALIGNMENT
29
FRAME COUNTER
30
25
31
PLL
32
33
28a
27
DEMULTIPLEXER
71
72
73
74
32
DESYNCHRONIZER1
DESYNCHRONIZER2
DESYNCHRONIZER3
DESYNCHRONIZER4
26
21
22
23
24

FIG. 3

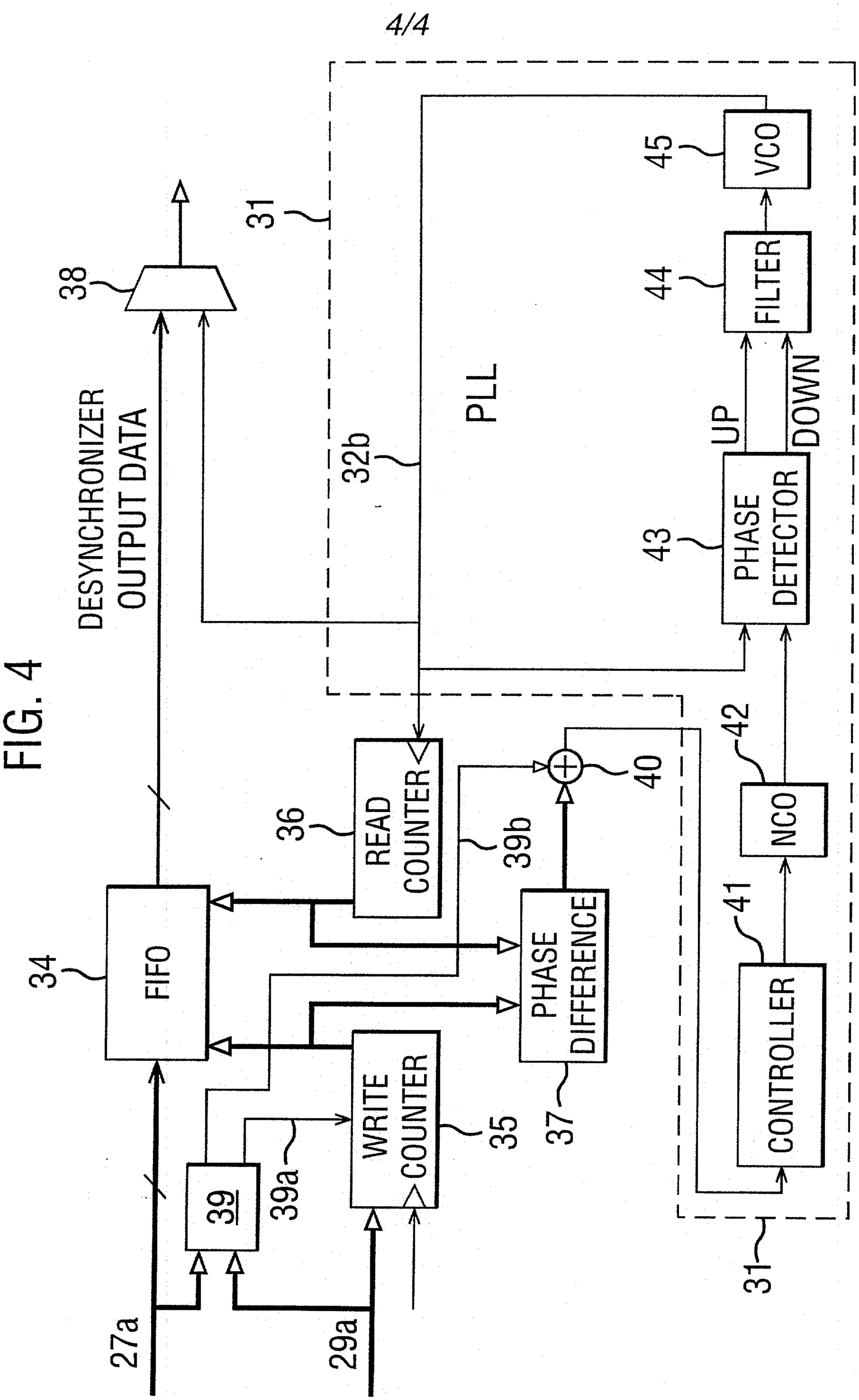
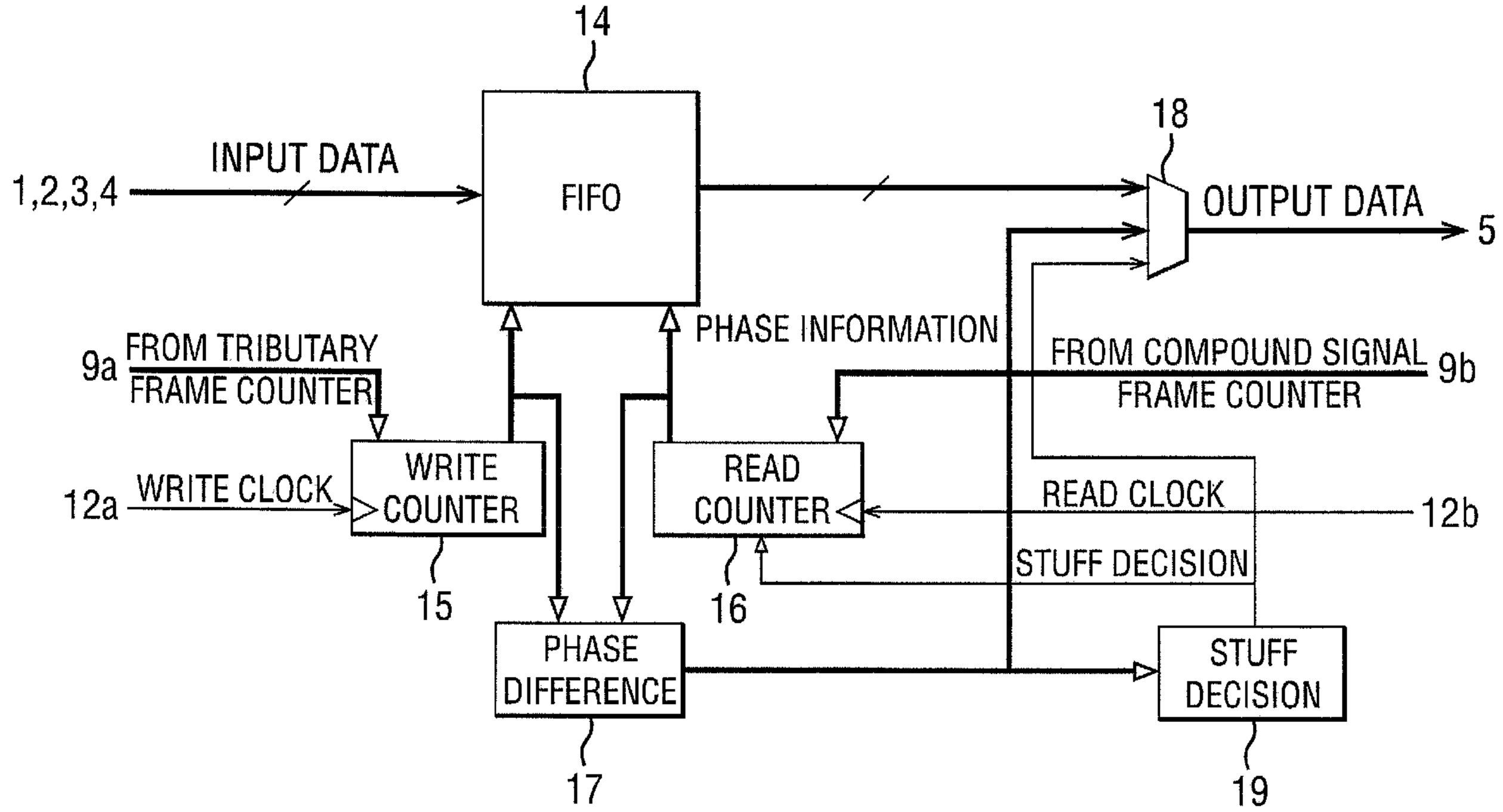

DESYNCHRONIZER OUTPUT DATA
38
31
32b
PLL
45
VCO
44
FILTER
UP
DOWN
43
PHASE DETECTOR
42
NCO
41
CONTROLLER
40
36
READ COUNTER
39b
34
FIFO
39
39a
WRITE COUNTER
35
PHASE DIFFERENCE
37
27a
29a
31

FIG. 4


14
18
INPUT DATA
1,2,3,4
FIFO
OUTPUT DATA
5
PHASE INFORMATION
9a FROM TRIBUTARY FRAME COUNTER
FROM COMPOUND SIGNAL FRAME COUNTER 9b
WRITE CLOCK 12a
WRITE COUNTER
READ COUNTER
READ CLOCK 12b
STUFF DECISION
15
16
PHASE DIFFERENCE
STUFF DECISION
17
19