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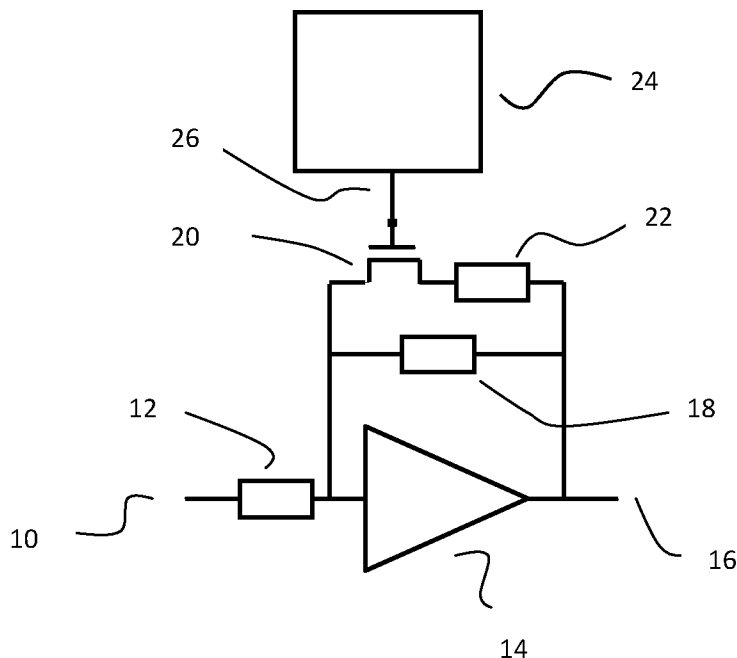
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(54) Title: VARIABLE GAIN AMPLIFIER



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FIGURE 1

(57) Abstract: A variable gain amplifier such as those used in RF circuits is operable to have a stepped gain change, which gives better signal to noise performance than a continuous gain change. However, changing between gain steps can result in disturbance to the circuitry in the signal path after the variable gain amplifier. Conventional solutions are to fix the gain after an initialization period or to implement a step-killer circuit. A variable gain amplifier (100) is described having a controller (24) which applies a ramp to the field effect transistors (20) in the gain control circuit. This results in a smoother transition between gain steps.



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VARIABLE GAIN AMPLIFIER

FIELD OF INVENTION

This invention relates to variable gain amplifiers.

5 BACKGROUND

Variable gain amplifiers (VGA) are widely used in electronic circuits such as radio frequency (RF) circuits. The variable gain amplifiers used in RF circuits typically have a discrete gain step, since this gives better performance than an amplifier having a continuous variable gain. However, a disadvantage of this approach is that
10 the gain change is abrupt which can disturb the following blocks, for example creating unlock of a reception demodulator.

To overcome this problem, for example when the VGA is incorporated into a silicon tuner for receiving TV signals, two VGA gain strategies are possible. A first possibility is that the VGA adapts its gain at the beginning of the reception during the
15 initialization phase of the silicon tuner. After the initialization phase is complete the gain is then fixed. This solution has a disadvantage that if the input signal changes, the amplifier can either saturate or alternatively the output signal will be lower than expected and consequently the SNR will be not optimized. A second possibility is to include an extra block known as a step-killer is added further in the RF signal path.
20 The step-killer compensates the abrupt VGA gain change instantaneously and afterwards recovers the wanted large gain step by very small steps during a certain amount of time. This solution has the disadvantage that the step killer is another amplifier requiring many small and accurate gain steps which requires large additional die area and results in increased power consumption.

25 There is therefore a need for an improved variable gain amplifier.

SUMMARY OF INVENTION

Various aspects of the invention are defined in the accompanying claims.

In a first aspect there is described a variable gain amplifier for an RF receiver comprising an amplifier circuit, a gain control circuit comprising a first path

comprising a series resistor arranged between the input of the variable gain amplifier and an input of the amplifier circuit, a second path comprising a feedback resistor arranged between the input and the output of the amplifier circuit, at least one further path arranged in parallel with the second path, each of the at least one further paths comprising a field effect transistor, and a controller comprising at least one output, each of the at least one outputs being coupled to the gate of each field effect transistor and configured to apply a control voltage to each field effect transistor, wherein the controller is operable to ramp the control voltage from a first voltage to a second voltage, thereby changing the gain of the variable gain amplifier.

By applying a control voltage as a ramp to switch the further resistor in parallel with the second resistor, the change between gain values is smoothed. This results in reduced disturbance to subsequent elements in the RF signal path. Hence the gain of the VGA can be continuously varied during operation without the requirement for an additional step-killer amplifier. The ramp change between the first voltage and second voltage may be a linear ramp, exponential ramp, or a programmable ramp with varying gradient.

In an embodiment, the transition time between the first voltage and second voltage is greater than 1 microsecond.

In an embodiment, the rate of transition between the first voltage and the second voltage is 1 millivolt per microsecond.

In an embodiment the slope of the gain change of the variable gain amplifier varies between 0.2dB per ms to 2.5 dB per millisecond.

In an embodiment the rate of transition between the first voltage and the second voltage is variable. This allows the profile of the ramp to be altered to optimize the performance of the variable gain amplifier.

In an embodiment each of the at least one further paths comprises a further field effect transistor coupled in parallel with the field effect transistor, wherein the control signal generator comprises at least one further output coupled to the gate of the further field effect transistor and configured to apply a further control voltage to the further field effect transistor. By having more than one field effect transistor, multiple

FETs having smaller width to length gate ratios can be used rather than one single larger FET. This results in improved linearity when switching between gain values.

In an embodiment, the variable gain amplifier controller is operable to increase the gain of the variable gain amplifier by sequentially ramping the control voltage and the
5 further control voltage from the first voltage to the second voltage.

In an embodiment, the variable gain amplifier controller is operable to decrease the gain by sequentially ramping the control voltage and the further control voltage from the second voltage to the first voltage.

In an embodiment, the gate width to length ratio of the field effect transistor is
10 different than the gate width to length ratio of the further field effect transistor. By choosing different width to length ratios for the gates of the field effect transistor and further field effect transistor, the linearity of the switching between gain values can be further optimized.

In embodiments the variable gain amplifier can be incorporated into a silicon tuner.
15 In embodiments the variable gain amplifier can be incorporated into a radio receiver.

Embodiments of the invention are now described in detail, by way of example only, illustrated by the accompanying drawings in which:

Figure 1 shows a variable gain amplifier according to a first embodiment,

Figure 2 illustrates a variable gain amplifier according to a further embodiment,

20 Figure 3 shows a graph of variation in amplifier gain during operation of the variable gain amplifier of the embodiment of figure 2,

Figure 4 illustrates a variable gain amplifier according to another embodiment,

Figure 5 shows an example of a gate voltage controller for an embodiment of a variable gain amplifier,

25 Figure 6 illustrates a flow chart for controlling the gain change according to a further embodiment of the variable gain amplifier.

DESCRIPTION

Figure 1 shows a variable gain amplifier 100. Input 10 is connected to a first terminal of a series resistor 12 having a resistance R_1 . The second terminal of the series resistor 12 is connected to an input of amplifier circuit 14 which may be an operational amplifier configured as a single-ended inverting amplifier. The output of the amplifier circuit 14 may be connected to the output of the variable gain amplifier 100. The first terminal of feedback resistor 18 having a resistance R_2 is connected to the second terminal of series resistor 12. Second terminal of feedback resistor 18 is connected to output of amplifier circuit 14. The first terminal of feedback resistor 18 may be connected to a first terminal of a field effect transistor (FET) 20 which may be a source or drain. The second terminal of FET 20 which may be a source or drain may be connected to a first terminal of further resistor 22. The combined resistance of further resistor 22 and the channel resistance of the FET when switched on is R_{2b} . The second terminal of further resistor 22 may be connected to the second terminal of feedback resistor 18. The gate of FET 20 is connected to the output 26 of controller 24. The FET 20, further resistor 22, series resistor 12, feedback resistor 18, and controller 24 may form a gain control circuit to alter the gain of the variable gain amplifier 100.

In operation, FET 20 may be initially switched off by the controller 24 applying a first voltage which may be a ground potential for an nMOS FET. When FET 20 is switched off, the gain of the variable gain amplifier 100 is determined by the ratio of the feedback resistor 18 to series resistor 12 and is approximately equal to R_2/R_1 . To reduce the gain, the controller 24 may increase the control voltage as a ramp which may be a linear ramp or some other ramp such as an exponential ramp. As the control voltage increases, FET 20 is switched on and the gain reduces since the value of the feedback resistance is now R_2 in parallel with the sum of the channel resistance of FET 20 and further resistor 22. When the voltage reaches a second voltage, the FET 20 is in saturation and the gain of the VGA 100 is approximately equal to $(R_2 \parallel R_{2b})/R_1$ i.e. $R_2 \cdot R_{2b} / (R_2 + R_{2b}) / R_1$.

By controlling the gain change with a voltage ramp, the gain change is no longer as abrupt which reduces the disturbance to circuit elements further along the signal

path. The slope of the gain during the transition can be tuned by changing the timing of the ramp voltage. For example, if the duration of the slope is doubled, the slope of the rate of change gain during the transition between the first voltage and second voltage may be divided by two.

- 5 To increase the gain, the controller 24 may ramp the voltage from a second voltage to a first voltage. As the control voltage decreases, FET 20 may switch off increasing the channel resistance and therefore increasing the value of the feedback resistance. When the control voltage is equal to the first voltage, the FET 20 is switched off and the gain of the variable gain amplifier 100 is approximately $R2/R1$.
- 10 In embodiments, the transition time to change between the first voltage and second voltage may be greater than 1 microsecond. In other embodiments the rate of transition between the first voltage and the second voltage may be 1 millivolt per microsecond. In further embodiments the slope of the gain change may vary between 0.2dB per ms to 2.5 dB per millisecond. For some embodiments where the
- 15 ramp is linear, the slope of the gain change with respect to time during switching of FET 20 may be constant during part of the transition but varies as the control voltage reaches the threshold voltage V_t of the FET.

In embodiments the further resistor 22 may be omitted and the second terminal of FET 18 may be connected to the second terminal of feedback resistor 18.

- 20 Figure 2 shows an embodiment of variable gain amplifier 200 where the input 10 is connected to a first terminal of series resistor 12 having a resistance $R1$. The second terminal of series resistor 12 is connected to an input of amplifier circuit 14 which may be an operational amplifier configured as a single-ended inverting amplifier. The output of the amplifier circuit 14 may be connected to the output of the variable gain
- 25 amplifier 200. The first terminal of feedback resistor 18 having a resistance $R2$ is connected to the second terminal of series resistor 12. Second terminal of feedback resistor 18 is connected to output of amplifier circuit 14. The first terminal of feedback resistor 18 may be connected to a first terminal of a field effect transistor (FET) 20 which may be a source or drain. The second terminal of FET 20 which may
- 30 be a source or drain may be connected to a first terminal of further resistor 22. A first terminal of a second FET 32 may be connected to a first terminal of FET 20. A second terminal of a second FET 32 may be connected to a second terminal of FET

20. A first terminal of a third FET 34 may be connected to a first terminal of FET 20. A second terminal of a third FET 34 may be connected to a second terminal of FET 20.

The combined resistance of further resistor 22 and the channel resistance of the FET 20, the second FET 32 and the third FET 34 when switched on is R_{2b} . The second terminal of further resistor 22 may be connected to the second terminal of feedback resistor 18. The gate of FET 20 is connected to the output 26 of controller 24'. The gate of second FET 32 may be connected to a second output 28 of controller 24'. The gate of third FET 34 may be connected to a third output 30 of controller 24'.

10 The FET 20, second FET 32, third FET 34, further resistor 22, series resistor 12, feedback resistor 18, and controller 24' may form a gain control circuit to alter the gain of the variable gain amplifier 200.

Figure 3 shows a graph 300 of the VGA200 in operation showing the change in gain and control voltage with respect to time when the gain of amplifier is reduced.

15 In operation, FET 20, second FET 32, and third FET 34 may be initially switched off by the controller 24' applying a first voltage which may be a ground potential for an nMOS FET. When FET 20 second FET 32 and third FET 34 are switched off, the gain of the variable gain amplifier 200 is determined by the ratio of the feedback resistor 18 to series resistor 12 and is approximately equal to R_2/R_1 . To reduce the gain, the controller 24' may increase the control voltage on first controller output 26 as a ramp which may be a linear ramp or some other ramp such as an exponential ramp. As the control voltage increases during first time period 40, FET 20 is switched on and the gain reduces since the value of the feedback resistance is now R_2 in parallel with the sum of the channel resistance of FET 20 and further resistor 22.

20 When the voltage reaches a second voltage, the FET 20 is in saturation.

Once first controller output 26 has reached a second voltage, the controller 24' may increase the control voltage on second controller output 26 as a ramp in second time period 42. As the control voltage increases, the second FET 32 is switched on which reduces the gain of VGA 200, since the value of the feedback resistance is now R_2 in parallel with the sum of further resistor 22 and the parallel channel resistances of FET 20 and second FET 32.

30

Once second controller output 28 has reached a second voltage, the controller 24' may increase the control voltage on third controller output 30 as a ramp during a third time period 44. As the control voltage increases, the third FET 34 is switched on which reduces the gain of VGA 200, since the value of the feedback resistance is now R2 in parallel with the sum of further resistor 22 and the parallel channel resistances of FET 20, second FET 32, and third FET 34. When the voltage at third controller output 30 reaches a second voltage, the third FET 34 is in saturation and the gain of the VGA 200 is approximately equal to $(R2 \parallel R2b) / R1$ i.e. $R2.R2b / (R2 + R2b) / R1$.

To increase the gain, the controller 24' may sequentially ramp the voltage from a second voltage to a first voltage on first controller output 26, second controller output 28 and third controller output 30 in reverse order compared to the decreasing gain operation. As the control voltage decreases, FET 20, second FET 32 and third FET 34 switch off increasing the channel resistance and therefore increasing the value of the feedback resistance. When the control voltage is equal to the first voltage on first control output 26, second control output 28 and third control output 30, FET 20, second FET 32 and third FET 34 are switched off and the gain of the variable gain amplifier 200 is approximately $R2/R1$.

Embodiments may have fewer or more FETs arranged in parallel. The dimensions of the gate widths and lengths may be chosen to give the same final gain as in embodiments when a single FET is used in the feedback path. In some embodiments the gate widths of FET 20, second FET 32 and third FET 34 vary. In embodiments FET 20 has the smallest gate width and is switched on first since FETs having a smaller width to length ratio have improved linearity. Since switching FET 20 first reduces the drain source voltage V_{ds} across second FET 32 and third FET 34, they can have larger gate widths without affecting the linearity as much.

Embodiments may have two FETs in parallel in the feedback path of variable gain amplifier 200 instead of three. Other embodiments may have four or more FETs arranged in parallel in the feedback path of variable gain amplifier 200. In other embodiments the further resistor 22 may be omitted and the second terminal of FET 20, the second terminal of second FET 32, and the second terminal of third FET 34 may be connected to the second terminal of feedback resistor 18.

Figure 4 shows an embodiment of variable gain amplifier 400. Input 10 is connected to a first terminal of series resistor 12 having a resistance R_1 . The second terminal of series resistor 12 is connected to an input of amplifier circuit 14 which may be an operational amplifier configured as a single-ended inverting amplifier. The output of the amplifier circuit 14 may be connected to the output of the variable gain amplifier 400. The first terminal of feedback resistor 18 having a resistance R_2 is connected to the second terminal of series resistor 12. Second terminal of feedback resistor 18 is connected to output of amplifier circuit 14. The first terminal of feedback resistor 18 may be connected to a first terminal of a field effect transistor (FET) 20 which may be a source or drain. The second terminal of FET 20 which may be a source or drain may be connected to a first terminal of further resistor 22. A first terminal of a second FET 32 may be connected to a first terminal of FET 20. A second terminal of a second FET 32 may be connected to a second terminal of FET 20. A first terminal of a third FET 52 may be connected to a first terminal of FET 20. A second terminal of a third FET 52 may be connected to a first terminal of third resistor 54. A second terminal of third resistor 54 may be connected to output of amplifier circuit 14.

The combined resistance of further resistor 22 the resistance of the FET 20, and the resistance of the second FET 32 when switched on is R_{2b} . The combined resistance of third resistor 54 and third FET 52 when switched on is R_{2c} . The second terminal of further resistor 22 may be connected to the second terminal of feedback resistor 18. The gate of FET 20 is connected to the output 26 of controller 24". The gate of second FET 32 may be connected to a second output 28 of controller 24". The gate of third FET 52 may be connected to a third output 50 of controller 24".

The FET 20, second FET 32, third FET 54, further resistor 22, series resistor 12, feedback resistor 18, third resistor 54, and controller 24" may form a gain control circuit to alter the gain of the variable gain amplifier 400.

In operation, FET 20, second FET 32, and third FET 54 may be initially switched off by the controller 24" applying a first voltage which may be a ground potential for an nMOS FET. When FET 20, second FET 32, and third FET 34 are switched off, the gain of the variable gain amplifier 400 is determined by the ratio of the feedback resistor 18 to series resistor 12 and is approximately equal to R_2/R_1 . To reduce the gain, the controller 24" may increase the control voltage on first controller output 26

as a ramp which may be a linear ramp or some other ramp such as an exponential ramp. As the control voltage increases FET 20 is switched on and the gain reduces since the value of the feedback resistance is now R2 in parallel with the sum of the channel resistance of FET 20 and further resistor 22. When the voltage reaches a second voltage, the controller 24'' may maintain the output 26 at the second voltage value.

Once first controller output 26 has reached a second voltage, the controller 24'' may increase the control voltage on second controller output 28 as a ramp in second time period 42. As the control voltage increases, the second FET 32 is switched on which reduces the gain of VGA 400, since the value of the feedback resistance is now R2 in parallel with the sum of further resistor 22 and the parallel channel resistances of FET 20 and second FET 32. Once second controller output 28 has reached a second voltage the gain of the VGA 400 is approximately equal to $(R2 \parallel R2b) / R1$ i.e. $R2.R2b / (R2 + R2b) / R1$.

Alternatively by switching FET 20 and second FET 32 off by ramping down the gate voltage and switching on third FET 52, the gain of the VGA is approximately equal to $(R2 \parallel R2c) / R1$ i.e. $R2.R2c / (R2 + R2c) / R1$.

To increase the gain, the controller 24'' may ramp the voltage from a second voltage to a first voltage on first controller output 26, second controller output 28. As the control voltage decreases, FET 20 and second FET 32 switch off increasing the channel resistance and therefore increasing the value of the feedback resistance. When the control voltage is equal to the first voltage on first control output 26, second control output, FET 20, second FET 32 are switched off. The controller may also switch off third FET 52. In the case where FET 20, second FET 32 and third FET 52 are switched off, the gain of VGA 400 increases to approximately $R2/R1$.

Figure 5 shows an example of a controller 24''. Signal generator 62 generates a ramp voltage between a first voltage which may be a supply voltage VDD and a second voltage which may be a ground potential. Signal generator 62 may generate a ramp from a first voltage to a second voltage or from a second voltage to a first voltage. The signal generator 62 may generate a linear ramp using a capacitor loaded or unloaded by a constant programmable current or other known circuit. In other embodiments signal generator 62 may generate a programmable ramp of

exponential or other shape using a D to A converter and other known circuit techniques. Signal generator 62 is connected to a first terminal of first analog multiplexer 64, a first terminal of second analog multiplexer 66, and a first terminal of third analog multiplexer 68.

- 5 Digital control 60 has a first output connected to a second terminal of first analog multiplexer 64, a second output connected to a second terminal of second analog multiplexer 66, and a third output connected to a second terminal of a third analog multiplexer 68.

10 Digital state machine 70 has control input bus 72, an output connected to signal generator 62, a further output connected to digital control 60 and further outputs connected respectively to a control terminal of first analog multiplexer 64, second analog multiplexer 66, and third analog multiplexer 68.

An example of the operation of the digital state machine 70 to change a single gain step is shown in figure 6. In step 80, a check is made as to whether a change in gain
15 is required. If no change is required, the state machine 70 remains at step 80. If a change is required, the state machine 70 progresses to step 82.

If a gain increase is required, in step 84 the state machine configures the signal generator to ramp down and connects it to output 28 by controlling second analog multiplexer 68. The output on controller output 28 ramps down from the second
20 voltage to the first voltage in step 86. In step 88, the state machine couples the second controller output 28 to the output of digital control 60 which is set to the first voltage which may be a ground. In step 90, the state machine connects the signal generator 62 to the first controller output 26. In step 92 the first controller output 26 ramps down from the second voltage to the first voltage. In step 94 the state
25 machine couples the first controller output 26 to the output of digital control 60 which is set to the first voltage which may be a ground. In step 96 the transition ends and returns to step 80.

If a gain decrease is required, in step 98 the state machine configures the signal generator to ramp up and connects it to output 26 by controlling first analog
30 multiplexer 68. The output on controller output 26 ramps up from the first voltage to the second voltage in step 110. In step 112, the state machine couples the first

controller output 26 to the output of digital control 60 which is set to the second voltage which may be a supply voltage. In step 114, the state machine connects the signal generator 62 to the second controller output 28. In step 116 the second controller output 28 ramps up from the first voltage to the second voltage. In step 118 the state machine couples the second controller output 28 to the output of digital control 60 which is set to the second voltage which may be a supply voltage. In step 96 the transition ends and returns to step 80.

In embodiments the variable gain amplifier VGA1 is a single-ended inverting amplifier with resistive feedback which provides -8dB input return loss across 50MHz-1GHz. Embodiments of the invention may provide a noise figure of less than 3.0 dB and linearity performance as determined by the ratio of composite triple beat and composite second order of greater than 60 dB. Embodiments may have a programmable gain derivative from 0.1dB/ms to 2dB/ms.

Embodiments of the variable gain amplifier may be implemented on a CMOS integrated circuit using known design techniques. Embodiments of the variable gain amplifier may be incorporated into receivers for TV, Satellite and cable such as a full spectrum receiver or transceiver. However, the variable gain amplifier is not restricted to use in RF circuits and further embodiments of the variable gain amplifier may be included into other devices.

In further embodiments, the amplifier may be a low noise amplifier (LNA). An LNA is an amplifier used to amplify very weak signals such as those captured by an antenna or satellite dish. LNAs can adapt the gain to give the largest output level without saturation while maintaining the signal-to-noise ratio (SNR) at an acceptable level. A typical LNA will have a low noise figure, for example less than 5 dB and a suitable maximum gain which may be, for example, 20 dB.

From reading the present disclosure, other variations and modifications will be apparent to the skilled person. Such variations and modifications may involve equivalent and other features which are already known in the art of variable gain amplifiers and which may be used instead of, or in addition to, features already described herein.

Although the appended claims are directed to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to
5 the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention.

Features which are described in the context of separate embodiments may also be provided in combination in a single embodiment. Conversely, various features which are, for brevity, described in the context of a single embodiment, may also be
10 provided separately or in any suitable sub combination.

The applicant hereby gives notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

For the sake of completeness it is also stated that the term "comprising" does not
15 exclude other elements or steps, the term "a" or "an" does not exclude a plurality, a single processor or other unit may fulfil the functions of several means recited in the claims and reference signs in the claims shall not be construed as limiting the scope of the claims.

CLAIMS

1. A variable gain amplifier comprising:
 - an amplifier circuit (14),
 - a gain control circuit comprising
 - 5 a first path comprising a series resistor (12) arranged between an input of the variable gain amplifier and an input of the amplifier circuit,
 - a second path comprising a feedback resistor (18) arranged between the input and the output of the amplifier circuit (14),
 - 10 at least one further path arranged in parallel with the second path, each of the at least one further paths comprising a field effect transistor (20), and
 - a controller (24) comprising at least one output (26), each of the at least one outputs being coupled to a gate of each field effect transistor and configured to apply a control voltage to each field effect
 - 15 transistor, wherein the controller is operable to ramp the control voltage from a first voltage to a second voltage, thereby changing the gain of the variable gain amplifier.
- 20 2. The variable gain amplifier according to claim 1 wherein the each of the at least one further paths comprises a further resistor (22) coupled to the field effect transistor.
3. The variable gain amplifier according to claim 1 or 2 wherein a transition time
- 25 between the first voltage and second voltage is greater than 1 microsecond.
4. The variable gain amplifier of claim 1 or 2 wherein a rate of transition between the first voltage and the second voltage is 1 millivolt per microsecond.
5. The variable gain amplifier according to claim 1 or 2 wherein the slope of the
- 30 gain change varies between 0.2dB per ms to 2.5 dB per millisecond.
6. The variable gain amplifier of claim 1 or 2 wherein a rate of transition between the first voltage and the second voltage is variable.

7. The variable gain amplifier according to any preceding claim, wherein each of the at least one further paths comprises a further field effect transistor (32) coupled in parallel with the field effect transistor, wherein

5 the controller (24') comprises at least one further output (28) coupled to the gate of the further field effect transistor and configured to apply a further control voltage to the further field effect transistor.

10 8. The variable gain amplifier of claim 7 wherein the controller is operable to increase the gain of the variable gain amplifier by sequentially ramping the control voltage and the further control voltage from the first voltage to the second voltage.

15 9. The variable gain amplifier of claim 7 wherein the controller is operable to decrease the gain by sequentially ramping the control voltage and the further control voltage from the second voltage to the first voltage.

20 10. The variable gain amplifier of any of claims 7 to 9, wherein the gate width to length ratio of the field effect transistor is different than the gate width to length ratio of the further field effect transistor.

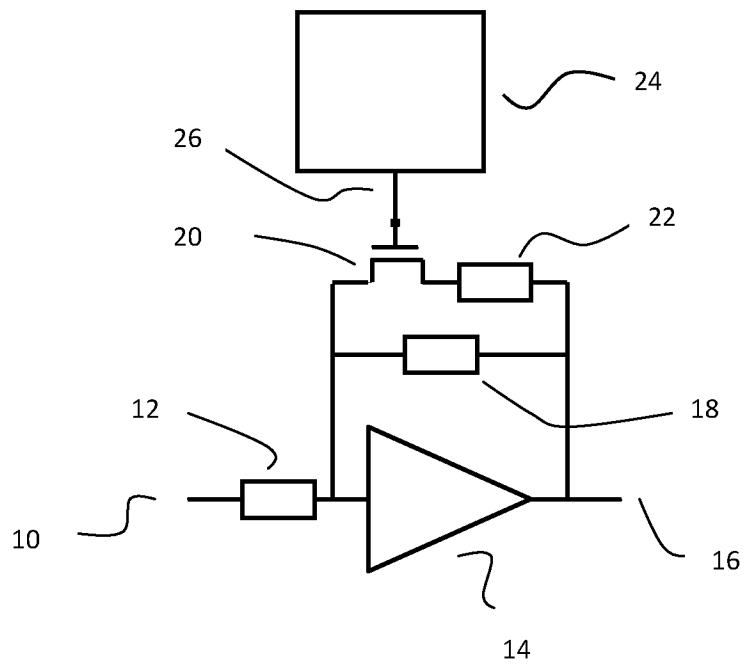
25 11. The variable gain amplifier of any preceding claim configured as a low noise amplifier.

30 12. A CMOS integrated circuit comprising the variable gain amplifier of any preceding claim.

13. A silicon tuner comprising the variable gain amplifier of any preceding claim.

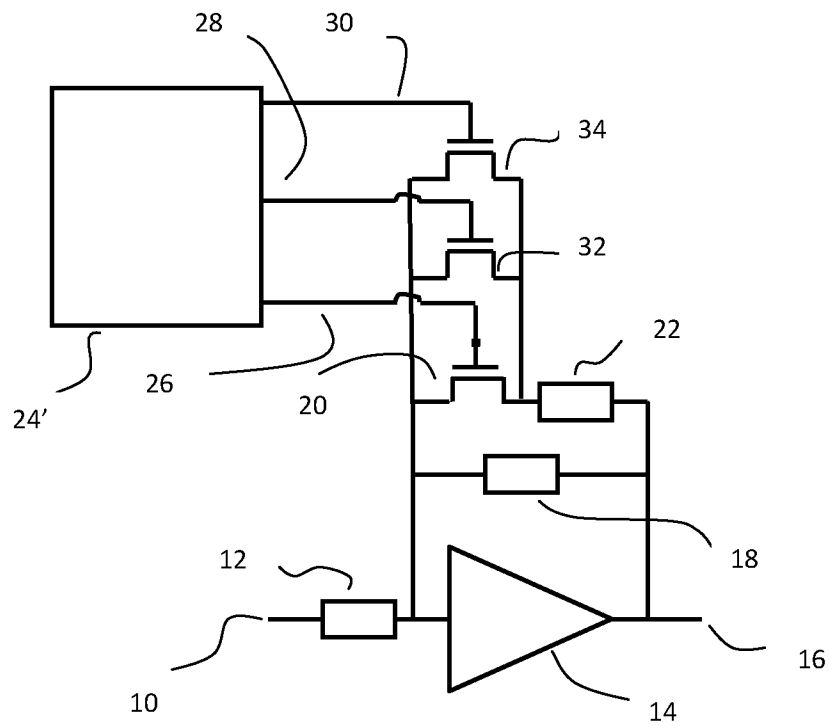
14. A radio receiver comprising the variable gain amplifier of any of claims 1 to 10.

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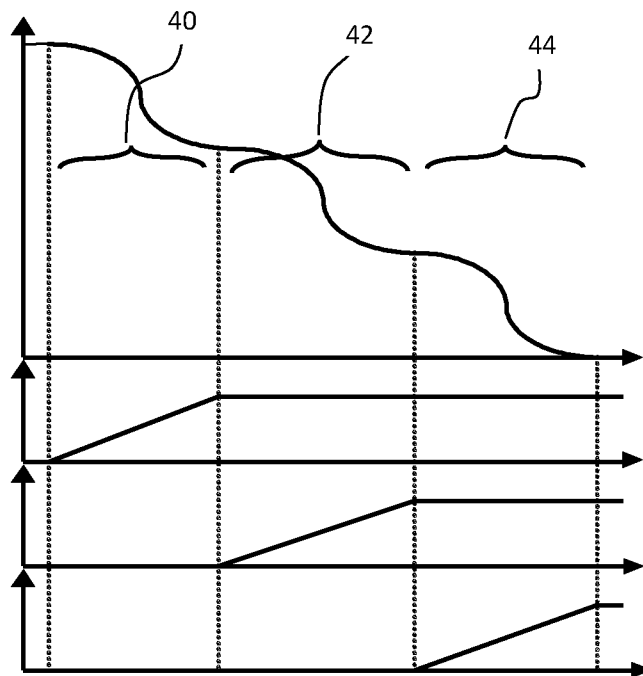
FIGURE 1



200

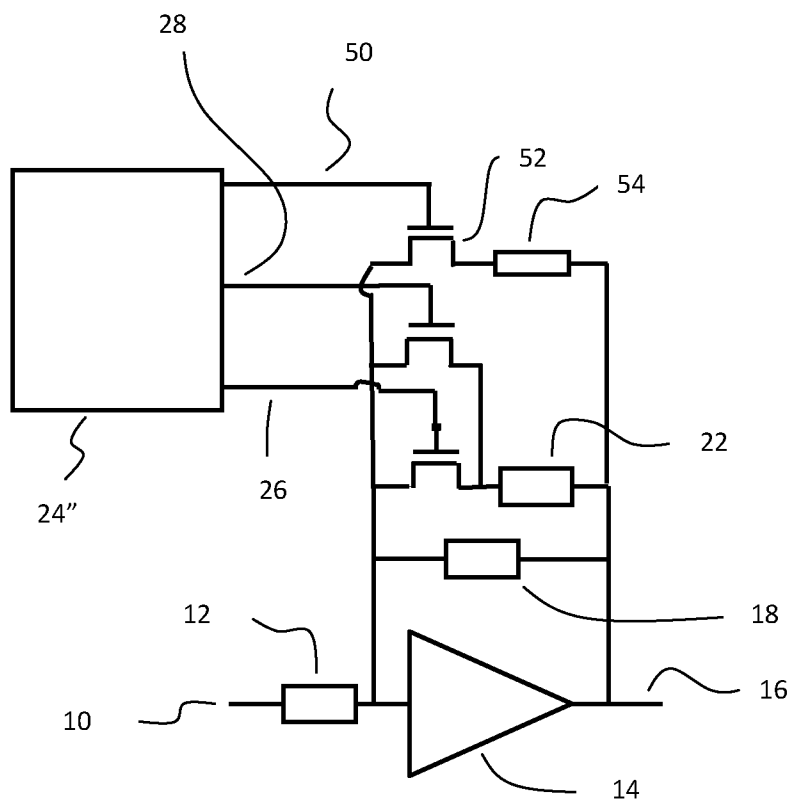
FIGURE 2

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300

FIGURE 3



400

FIGURE 4

3/3

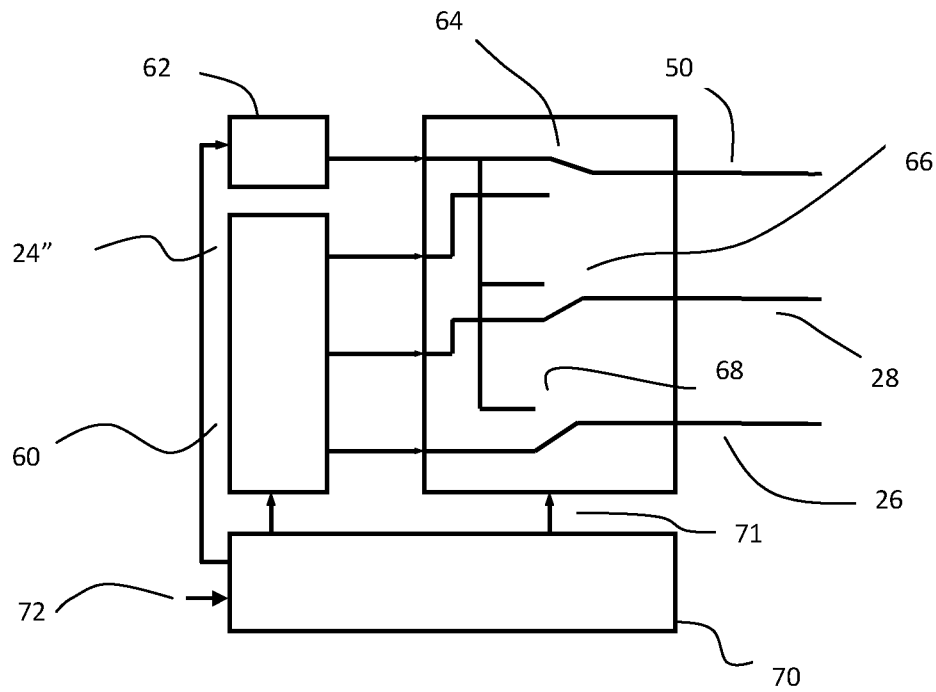


FIGURE 5

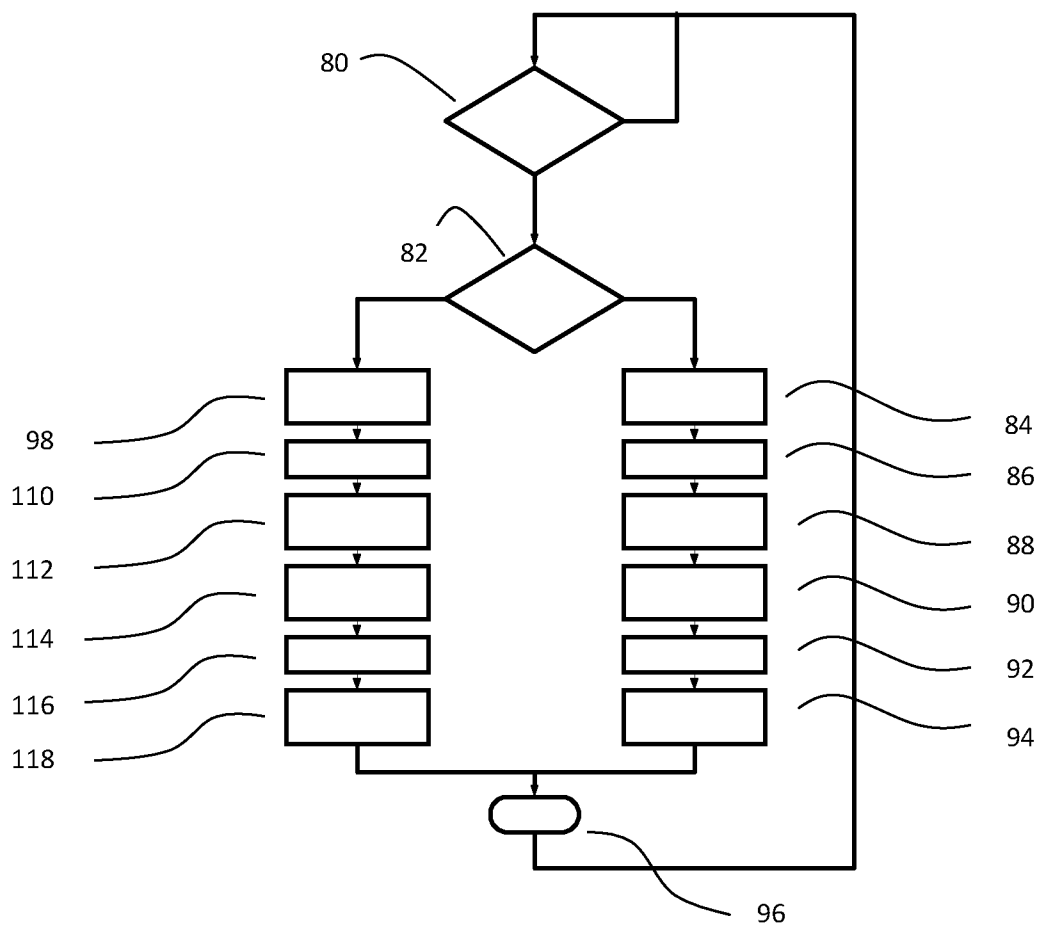


FIGURE 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/071745

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03G1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03G H03F H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7 423 482 B2 (BLON THOMAS [DE]) 9 September 2008 (2008-09-09)	1-6, 11-14
Y	abstract; figures 1, 2 column 2, line 3 - column 4, line 6 column 4, line 26 - column 5, line 63 column 6, lines 48-67	7-10
X	WO 2007/149632 A2 (NEWPORT MEDIA INC [US]) 27 December 2007 (2007-12-27)	1-6, 11-14
Y	abstract; figures 4-6 paragraphs [0034] - [0043], [0060], [0062], [0064]	7-10
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☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search

21 March 2012

Date of mailing of the international search report

28/03/2012

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Authorized officer

Wichert, Beate

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2011/071745

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	abstract; figures 1,2 page 1, line 21 - page 3, line 2 page 3, line 28 - page 6, line 4 -----	7-10
Y	US 2009/179688 A1 (IGARASHI MASAHIRO [JP] ET AL) 16 July 2009 (2009-07-16) abstract; figures 7-9 paragraphs [0096] - [0114] -----	7-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2011/071745

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			US 2007075768 A1	05-04-2007

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