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(54) **NONVOLATILE SEMICONDUCTOR MEMORY DEVICE**

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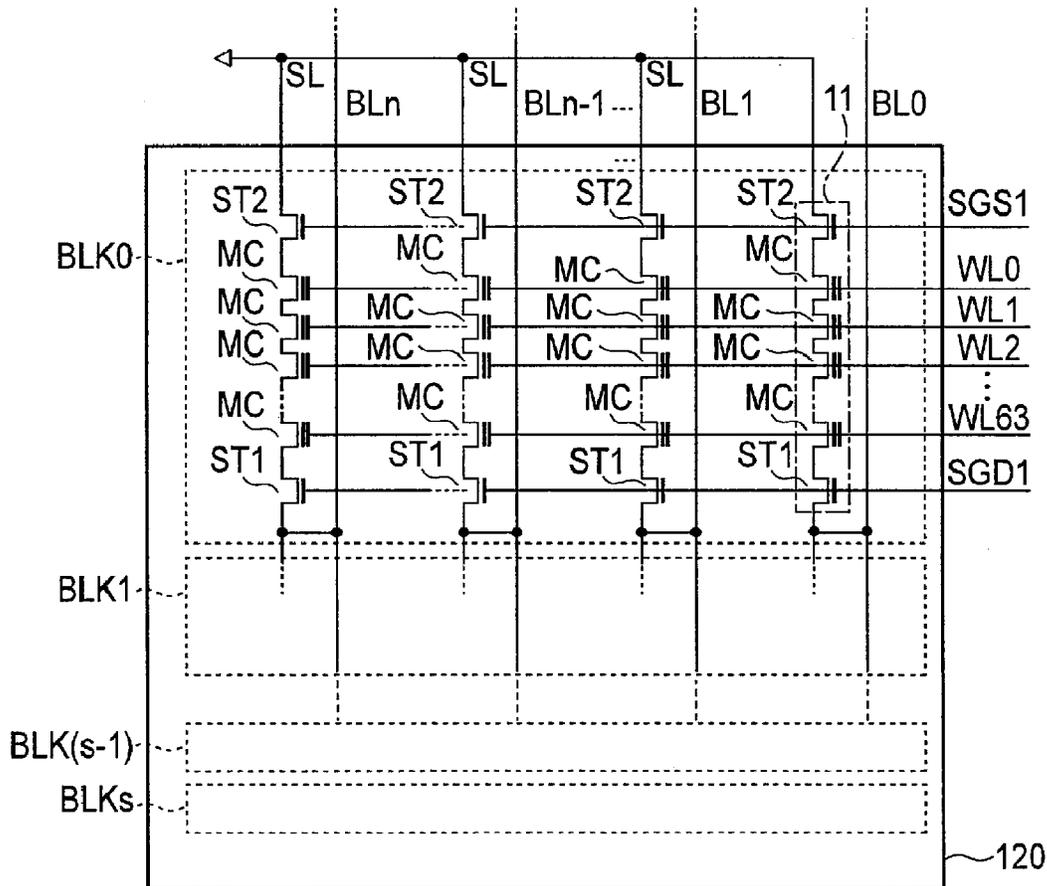
(57)   **ABSTRACT**

A semiconductor memory device includes a memory cell array, a sense amplifier, a register, a controller. The memory cell array includes a memory cell. The sense amplifier connects to the bit line. The register holds write data, and a write voltage. The controller outputs a busy signal. The controller causes the register to hold the write data and the write voltage upon receiving the first command, and resumes the write operation based on the write data and the write voltage held in the register upon receiving the resumption command.

F I G. 1

F I G. 2

F I G. 3

START

Perform write operation ⟋S0

S1

Break command received? — NO

↓YES

Switch busy signal to="H" ⟋S2

Receive read command ⟋S3

Change busy signal to "L" and perform read operation ⟋S4

Data out via SDL ⟋S5

Receive resumption command ⟋S6

Resume write operation ⟋S7

END

F I G. 4A

V5

V4

V3

V2

V1

Read

Break write
(stored in register 170)

Write from V5

"H" Busyn: "H"
Busyn:"L"   "L"

F I G. 4B

Program
command
8x A1 D 1X

Busyn="L"
Break
command

Read command
00   30

Data out   YY

XDL:Upper
LDL:Lower
SDL:Free

Busyn="H"

XX

Program

Program

XDL:Upper
LDL:Lower
SDL:Free

Read

XDL:Upper
LDL:Lower
SDL:Read data

t0   t1   t2   t3   t4   t5   t6t7   t8   t9

F I G. 5A

Memory
cell
array

Sense
unit

(1)

SDL   41

(3)

(2)

UDL   42

(4)

LDL   43

Program
data

XDL   44

To I/O line
data out

Data out

DBUS

F I G. 5B

Program
command

Busyn="L"
Break
command

Read command

8x A1 D 1X

Busyn="H"

XX

00 | 30

Data out

YY

XDL:Upper
LDL:Lower
SDL:Free

Program

Program

Read

XDL:Upper
LDL:Lower
UDL:QPW
SEN:Free

XDL:Read data
LDL:Lower
UDL:QPW
SEN:Upper

t0   t1   t2   t3   t4   t5 t6t7   t8 t9

F I G. 6A

Sense unit   Read data (1)   41

Memory
cell
array

SEN

(4)

SDL

45

(3)

42

UDL

QPW

43

LDL

Program
data

44

(2)

XDL

To I/O line
data out

DBUS

F I G. 6B

Break command   Resumption command

| Program | | Read | | Program verify | Program |

Break   Data out

XDL:Lower data   XDL:Lower data   XDL:Lower data   XDL:Lower data
LDL:Upper data   LDL:Upper data   LDL:Upper data   LDL:Upper data
UDL:QPW Data   UDL:Read data   UDL:QPW Data   UDL:QPW Data

Busyn="H"(Ready)   Busyn="H"(Ready)

Busy="L"

t0   t1   t2   t3

Overwrite on   Reconstruct
read data   QPW data

F I G. 7A

Sense
unit   Read data (1)   SDL   ~41

Memory
cell
array

(2)   42   (5)

UDL   } QPW=>Read data

43

LDL

(3)   (4)   44   } Program
                            data
XDL

To I/O line
data out

DBUS

F I G. 7B

F I G. 8

F I G. 9

35 ⟋ ⊣⊢

DDC ⟍54

34 ⟋ ⊣⊢

BDC ⟍53

33 ⟍ ⊣⊢

CDG ⟍52

(1)

500 ⟍ 50

(3-1)

30 ⟍ ⊣⊢ →TDC ⟍ N2   31 ⟍

55 ⟍ ⟊   (3-3)   N3   (3-2)   501 ⟍   PDC

510 ⟍ 51

(2)   32 ⟍ ⊣⊢   (5)

N4   511 ⟍   SDC   36 ⟍ ⊣⊢ —IO

(4)

Sense amplifier140

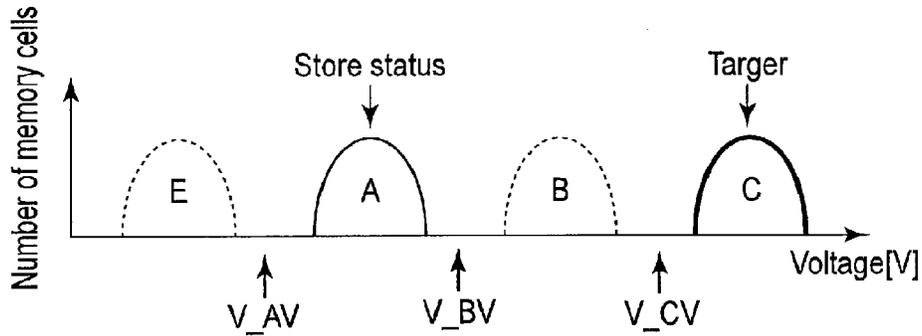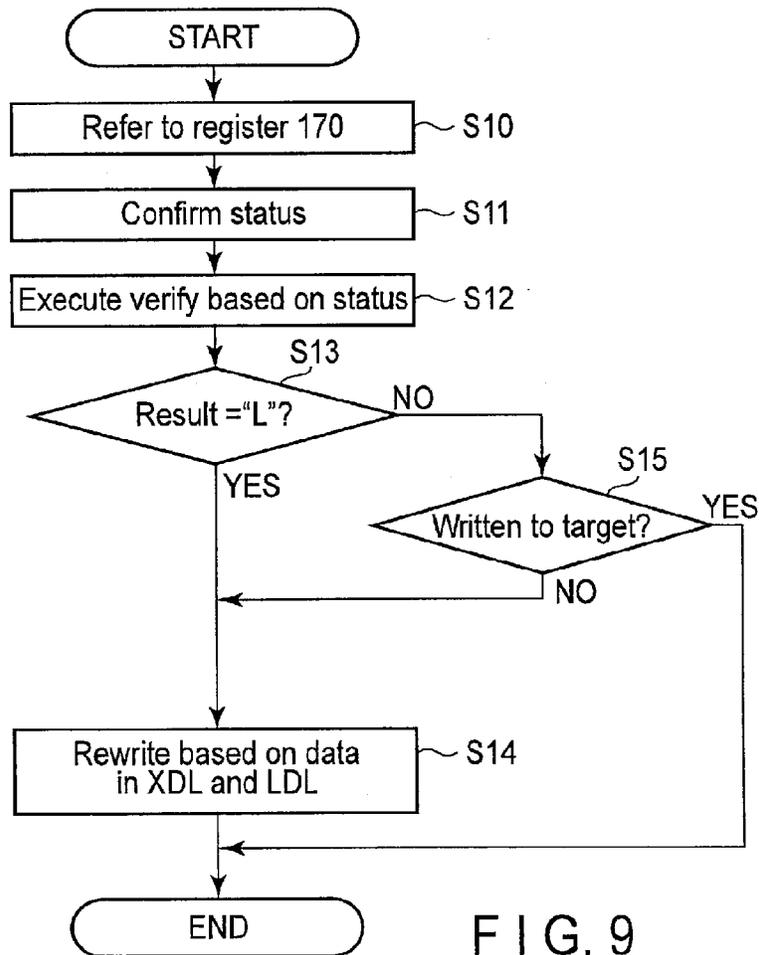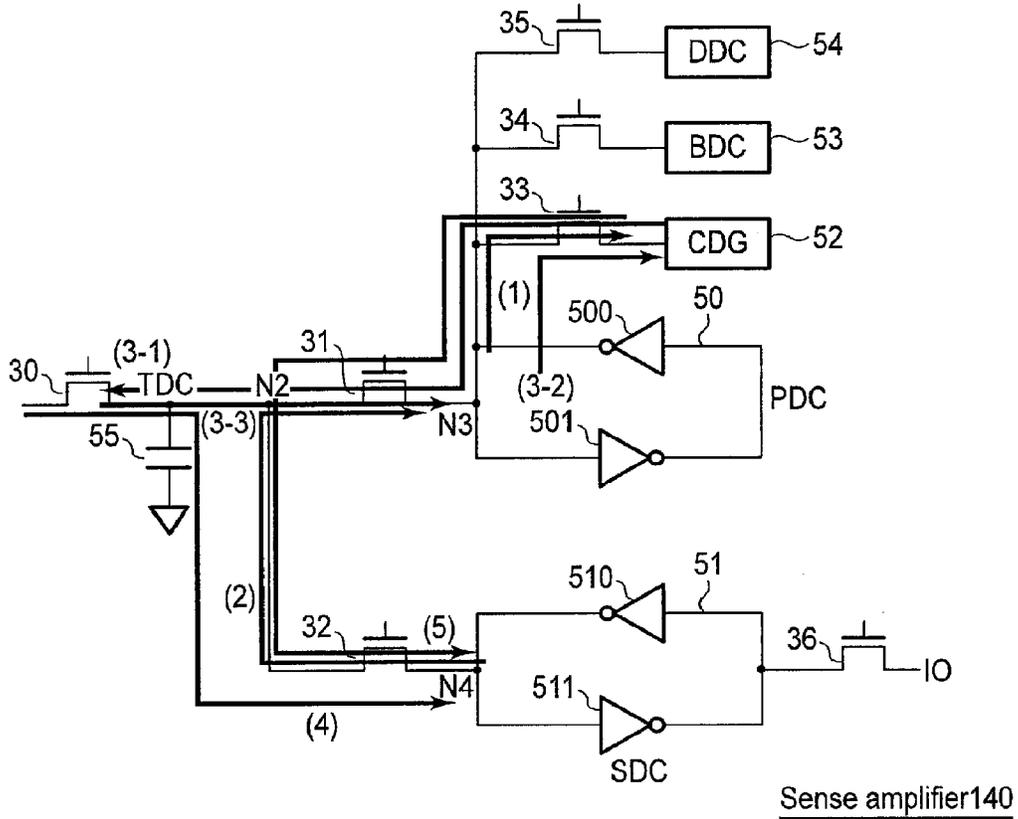## F I G. 10A

Step1:PDC=>CDG

Step2:SDC=>PDC

Step3:CDG=>TDC PDC=>CDG TDC=>PDC

Step4:Read=>SDC

Step5:CDG=>SDC

F I G. 10B

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of and claims the benefit of priority under 35 U.S.C. §120 from U.S. Ser. No. 14/862,412 filed Sep. 23, 2015, the entire contents of which is incorporated herein by reference. U.S. Ser. No. 14/862, 412 is a National Stage of PCT/JP2013/075382 filed Sep. 12, 2013 which was not published under PCT Article 21(2) in English and claims the benefit of priority from Japanese Patent Application No. 2013-062125 filed Mar. 25, 2013, the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments relate to a nonvolatile semiconductor memory device, memory controller, and memory system.

BACKGROUND

[0003] A NAND flash memory includes a plurality of memory cells arranged in a matrix, and a sense amplifier capable of holding write data to these memory cells.

BRIEF DESCRIPTION OF THE DRAWING

[0004] FIG. 1 is an overall arrangement of a nonvolatile semiconductor memory device according to the first embodiment;

[0005] FIG. 2 is a conceptual view of a memory cell array according to the first embodiment;

[0006] FIG. 3 is an example of the circuit arrangement of a sense amplifier according to the first embodiment;

[0007] FIGS. 4A and 4B show an operation according to the first embodiment in which FIG. 4A is a flowchart when an interrupt command and a resumption command have been received, and FIG. 4B is a conceptual view of a write voltage when an interrupt command and a resumption command have been received;

[0008] FIGS. 5A and 5B show the operation of a memory system according to the first embodiment in which FIG. 5A is a sequence of commands issued by a memory controller, and FIG. 5B is a conceptual view showing data saving;

[0009] FIGS. 6A and 6B show the operation of a memory system according to a modification of the first embodiment in which FIG. 6A is a sequence of commands issued by a memory controller, and FIG. 6B is a conceptual view showing data saving;

[0010] FIGS. 7A and 7B show the operation of a memory system according to the second embodiment in which FIG. 7A is a sequence of commands issued by a memory controller, and FIG. 7B is a conceptual view showing data saving;

[0011] FIG. 8 is a conceptual view of information held in a register according to the second embodiment;

[0012] FIG. 9 is a flowchart showing the operation of a nonvolatile semiconductor memory device according to the third embodiment; and

[0013] FIGS. 10A and 10B show the nonvolatile semiconductor memory device according to the third embodiment in which FIG. 10A is a circuit diagram showing an example of the arrangement of a sense amplifier, and FIG. 10B is a conceptual view showing data saving.

DETAILED DESCRIPTION

First Embodiment

[0014] In general, according to one embodiment, a semiconductor memory device includes a memory cell array, a sense amplifier, a register, a controller. The memory cell array includes a memory cell. The memory cell electrically connects to a bit line. The sense amplifier electrically connects to the bit line. When a write operation is interrupted, the register configured to be capable of holding a write data and a write voltage at the time of interrupt. The controller configured to output a first signal representing that the write operation is progressing, and to receive a first command to interrupt the write operation and a second command to request a read operation during program operation, and when the read operation has ended, to receive a third command to request resumption of the write operation. The controller causes the register to hold the write data and the write voltage upon receiving the first command, and resumes the write operation based on the write data and the write voltage held in the register upon receiving the resumption command.

[0015] In the first embodiment, upon receiving an interrupt command from the outside during busy (Busyn="L", for example, write operation), the write operation is interrupted, and an externally received read operation is performed. After that, upon receiving a resumption command, the write operation is executed again from the point of interrupt. Note that "n" of Busyn indicates negative logic.

[0016] At this time, the read operation is executed even if the cache in the sense amplifier is not released.

[0017] 1. Example of Overall Arrangement

[0018] FIG. 1 is a block diagram showing the arrangement of a memory system according to the first embodiment. The memory system includes a semiconductor device 1 and a host device 2. The semiconductor device 1 is connectable to the host device 2, and operates under the control of the host device 2.

[0019] The semiconductor device 1 also includes a nonvolatile semiconductor memory device 10, and a memory controller 20 (controller) that controls the nonvolatile semiconductor memory device 10. Examples of the semiconductor device 1 are an SD™ card and an SSD.

[0020] In this embodiment, a NAND flash memory will be exemplified below as the nonvolatile semiconductor memory device 10.

[0021] 1. <Semiconductor Apparatus 1>

[0022] 1.1<Nonvolatile Semiconductor Memory Device 10>

[0023] The nonvolatile semiconductor memory device 10 includes a memory cell array 120 (memory cell array in FIG. 1), a row decoder 130 (R/D in FIG. 1), a sense amplifier 140 (sense amp in FIG. 1), a controller 150 (controller in FIG. 1), a voltage generator 160 (voltage generator in FIG. 1), and a register 170 (resister in FIG. 1).

[0024] 1.1<Example of Arrangement of Memory Cell Array 120>

[0025] As shown in FIG. 2, the memory cell array 120 includes blocks BLK0 to BLKs (s is a natural number) each including a plurality of nonvolatile memory cells MC. Each of the blocks BLK0 to BLKs includes a plurality of NAND strings 11 in which the nonvolatile memory cells MC are

connected in series. Each of the NAND strings **11** includes, for example, 64 memory cells MC, and select transistors ST**1** and ST**2**.

[0026] Each memory cell MC may hold data of two or more values. The memory cell MC has an FG structure including a floating gate (charge conductive layer) formed on a gate insulating film on a p-type semiconductor substrate, and a control gate formed on an inter-gate insulating film on the floating gate. Note that the memory cell MC may have a MONOS structure. The MONOS structure includes a charge accumulation layer (for example, insulating film) formed on a gate insulating film on a semiconductor substrate, an insulating film (to be referred to as a block layer hereinafter) formed on the charge accumulation layer and having a dielectric constant higher than that of the charge accumulation layer, and a control gate formed on the block layer.

[0027] The control gate of the memory cell MC is electrically connected to a word line, the drain is electrically connected to a bit line, and the source is electrically connected to a source line. The memory cell is an n-channel MOS transistor. The number of memory cells MC is not limited to 64 and may be 128, 256, or 512, and the number is not limited. The memory cells MC adjacent to each other share the source and the drain. The memory cells MC are arranged so that the current path is connected in series between the select transistors ST**1** and ST**2**. The drain region on one end side of the memory cells MC connected in series is connected to the source region of the select transistor ST**1**. The source region on the other end side is connected to the drain region of the select transistor ST**2**.

[0028] The control gates of the memory cells MC on the same row are commonly connected to one of word lines WL**0** to WL**63**. The gate electrodes of the select transistors ST**1** and ST**2** on the same row are commonly connected select gate lines SGD**1** and SGS**1**, respectively. Note that for the sake of simplicity, if the word lines WL**0** to WL**63** need not be discriminated, they will sometimes simply be referred to as the word lines WL hereinafter. The drains of the select transistors ST**1** on the same column in the memory cell array **120** are commonly connected to one of bit lines BL**0** to BLn (n is a natural number). As for the bit lines BL**0** to BLn as well, they will altogether be referred to as the bit lines BL hereinafter if they need not be discriminated. The sources of the select transistors ST**2** are commonly connected to an source line SL.

[0029] Data are written at once in the plurality of memory cells MC connected to the same word line WL. This unit will be referred to as a page. The data of the plurality of memory cells MC are erased at once in each block BLK.

[0030] Note that each memory cell MC may hold any one of the data of, for example, four values. The four values are "E" level, "A" level, "B" level, and "C" level in ascending order of voltage. The "E" level is called an erase state and indicates a state in which no charges exist in the charge accumulation layer. As the charges are accumulated in the charge accumulation layer, the voltage rises from "A" level to "B" level and then to "C" level.

[0031] The memory cell MC in the erase state corresponds to "11" data. The memory cell MC whose threshold distribution is "A" level corresponds to "10" data. The memory cell MC whose threshold distribution is "B" level corresponds to "00" data. The memory cell MC whose threshold distribution is "C" level corresponds to "01" data.

[0032] When the held data is represented by "□Δ", "□" is called an upper bit that is stored in the fourth latch to be described later at the time of data write, and "Δ" is called a lower bit that is stored in the third latch to be described later at the time of write.

[0033] The memory cell array **120** need not always have the above-described arrangement, and may have an arrangement described in, for example, U.S. patent application Ser. No. 12/407,403 "Three Dimensional Stacked Nonvolatile Semiconductor Memory" filed Mar. 19, 2009. Alternatively, the memory cell array **120** may have an arrangement described in U.S. patent application Ser. No. 12/406,524 "Three Dimensional Stacked Nonvolatile Semiconductor Memory" filed Mar. 18, 2009, U.S. patent application Ser. No. 12/679,991 "Non-Volatile Semiconductor Storage Device And Method of Manufacturing The Same" filed Mar. 25, 2010, or U.S. patent application Ser. No. 12/532,030 "Semiconductor Memory And Method for Manufacturing Same" filed Mar. 23, 2009. These patent applications are incorporated in this specification by reference in their entirety.

[0034] 1.2<Arrangement of Peripheral Circuits>

[0035] The row decoder **130** is connected to the plurality of word lines WL, and selects and drives the word lines WL at the time of data read, write, and erase.

[0036] The sense amplifier **140** is connected to the plurality of bit lines BL, and controls the BL voltage of the bit lines at the time of data read, write, and erase. The sense amplifier **140** also senses, for example, the potential of the bit line BL at the time of data read. Note that the sense amplifier **140** need not always sense the potential and may sense, for example, a cell current.

[0037] The sense amplifier **140** also applies a voltage corresponding to write data to the bit line BL at the time of data write. Note that the detailed arrangement of the sense amplifier **140** will be described later.

[0038] The controller **150** generates a control signal to control the sequence of data write, read, and erase based on a command CMD (interrupt command, resumption command, or the like to be described later) and an external control signal supplied from the memory controller **20** in accordance with the operation mode. This control signal is sent to the row decoder **130**, the sense amplifier **140**, the voltage guarantor **160**, and the like.

[0039] In this embodiment, upon receiving an interrupt command from the memory controller **20**, the controller **150** interrupts the write operation even if the operation is progressing, and then handles an interrupt of an externally received read operation. After that, upon receiving a resumption command from the memory controller **20**, the controller **150** executes the write operation from the point of interrupt.

[0040] More specifically, when resuming the write operation, the controller **150** refers to the register **170** to be described later, and causes the voltage guarantor **160** to generate the next write voltage to be transferred to the word line WL in accordance with the data held in the register **170**.

[0041] Note that the interrupt command in the first embodiment is, for example, an FF command. That is, the command is a special command that enables reception of the interrupt command even when the nonvolatile semiconductor memory device **10** is outputting a busy signal of "L" level.

[0042] The voltage guarantor **160** generates a read voltage (Vread, VCGR), a write voltage (VPGM), a verify voltage

(V_AR, V_BR, or V_CR), and voltages necessary for various kinds of operations of the memory cell array **120**, the row decoder **130**, and the sense amplifier **140** in accordance with various kinds of control signals sent from the controller **150**.

[0043] The register **170** exchanges various data with the memory controller **20** or the sense amplifier **140** (more specifically, via the fourth latch). More specifically, read data, write data, and the like are exchanged.

[0044] In addition, the register **170** holds information of the write voltage to be transferred to the word line WL next, the write count to the same memory cell MC, write data at the time of interrupt of the write operation, and the status (threshold distribution) to which the memory cell MC has transited at the time of interrupt of the write operation. The write voltage, write count, write data, and status are information to be referred to by the controller **150** or the memory controller **20**. In the following embodiment, the controller **150** refers to the information.

[0045] 2. <Example of Arrangement of Sense Amplifier **140**>

[0046] The arrangement of the sense amplifier will be described next with reference to FIG. **3**. The sense amplifier **140** includes a sense unit SU, a first latch circuit **41** (to be referred to as an SDL hereinafter), a second latch circuit **42** (to be referred to as a UDL hereinafter), a third latch circuit **43** (to be referred to as an LDL hereinafter), and a fourth latch circuit **44** (to be referred to as an XDL hereinafter). The sense unit SU includes a fifth latch circuit **45** (to be referred to as an SEN hereinafter).

[0047] The sense unit SU reads out data from the memory cell MC and transfers it to the SDL. The sense unit SU also transfers a write enable voltage (for example, 0 V) or a non-write voltage (for example, VDD) to the bit line BL in accordance with data stored in the XDL and the LDL.

[0048] The SDL holds the data read by the sense unit SU. The controller **150** transfers this data from the SDL to the XDL and then transfers it to the register **170** via an I/O (not shown).

[0049] The UDL holds data for quick path write (to be referred to as QPW hereinafter). That is, the UDL holds information representing whether the threshold voltage of the memory cell MC has exceeded a certain verify voltage.

[0050] Note that QPW is a data write method used to obtain a fine threshold distribution of the memory cell MC. QPW is described in, for example, U.S. patent application Ser. No. 10/051,372 "Non-Volatile Semiconductor Memory Device" filed Jan. 22, 2002. This patent application is incorporated in this specification by reference in its entirety.

[0051] A threshold distribution is obtained by performing verify using a voltage lower than the target threshold voltage and selectively performing write to the memory cell MC with a threshold transition smaller than normal.

[0052] The threshold voltage is lower than the verify voltage, the UDL holds, for example, "0" data. At the time of write, the bit line BL is clamped to a predetermined voltage (>0 V).

[0053] Note that in the first embodiment, since the write method using QPW is not performed, the UDL may be eliminated. Note that the write using QPW will be explained in a modification.

[0054] As described above, the LDL holds lower data out of write data formed from 2 bits. More specifically, the LDL holds one of "0" and "1" data.

[0055] As described above, the XDL holds upper data out of write data formed from 2 bits. More specifically, the XDL holds one of "0" and "1" data.

[0056] The data in the LDL and the XDL are combined, thereby writing desired data ("11", "10", "00", or "01") in the memory cell MC.

[0057] The SEN temporarily holds read data and transfers it to the SDL. The SEN is usable not only for the read data but also for the operation among the data latches.

[0058] 2. <Memory Controller **20**>

[0059] Referring back to FIG. **1**, the memory controller **20** will be described. The memory controller **20** receives an instruction from the host device **2**, and controls the nonvolatile semiconductor memory device **10** based on the instruction.

[0060] In the first embodiment, for example, if a data read request is received from the host device **2** during the write operation, the memory controller **20** issues an interrupt command to the nonvolatile semiconductor memory device **10** during the data write and then issues a read command.

[0061] When the read operation has ended, the memory controller **20** issues a resumption command to resume the interrupted write.

[0062] When the memory controller **20** issues the interrupt command to the nonvolatile semiconductor memory device **10**, the nonvolatile semiconductor memory device **10** executes the following operation.

[0063] 3. <Operation of Nonvolatile Semiconductor Memory Apparatus **10**>

[0064] The operation of the nonvolatile semiconductor memory device **10** according to the first embodiment will be described next with reference to FIGS. **4A** and **4B**. FIG. **4A** is a flowchart showing the operation of the nonvolatile semiconductor memory device **10**. FIG. **4B** shows the write voltage and the busy signal (Busyn in FIG. **4**) transferred to the word line WL and is a conceptual view showing a state in which write is interrupted based on the interrupt command and resumed.

[0065] 3.1<Flowchart>

[0066] As shown in FIG. **4A**, first, the write operation to the memory cell MC is executed (step S0). The write operation is executed by transferring a write voltage to the word line WL while transferring a write enable voltage or a non-write voltage to the bit line BL.

[0067] As shown in FIG. **4B**, the write voltage transferred to the word line WL rises stepwise as the write count increases. This aims at raising the threshold voltage of the memory cell MC up to the target voltage.

[0068] When the memory controller **20** issues the interrupt command in the middle of step S0 (YES in step S1), the controller **150** interrupts the write operation and issues a busy signal (indicating the Ready state) of "H" level to the memory controller **20** (step S2, FIG. **4B**).

[0069] This will be described in detail. After the write operation has been ended up to a predetermined step as shown in FIG. **4B**, the controller **150** switches the busy signal to the Ready state (Busyn="H" level). In FIG. **4B**, for example, a voltage V4 is transferred to the selected word line WL, and after that, the write operation is interrupted.

[0070] Additionally, since the state is the Ready state, as shown in FIG. **4B**, a read command is received from the memory controller **20** after that (step S3).

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[0071] Upon receiving the read command, the controller **150** issues the busy signal of "L" level to the memory controller **20** and starts the read operation (step S**4**, FIG. **4**B).

[0072] In the read operation, the read data is temporarily stored in the SDL and then transferred to the register **170** via the fourth latch circuit **44**, as described above (step S**5**).

[0073] After that, upon receiving the resumption command from the memory controller **20** (step S**6**), the controller **150** refers to the register **170** and resumes the write operation from a predetermined voltage, as shown in FIG. **4**B (step S**7**).

[0074] 4. <Command Sequence and Data Transfer of Sense Amplifier **140**>

[0075] FIGS. **5**A and **5**B are conceptual time-serially showing the sequence of commands transferred from the memory controller **20** and the data stored state in the sense amplifier **140** at the time of the read operation.

[0076] As shown in FIG. **5**A, when a write command ("8x A1 D 1x") is issued at time t**0**, the nonvolatile semiconductor memory device **10** executes the write operation based on this command (times t**1** to t**2** in FIG. **5**A). At this time, the controller **150** issues the busy signal of "L" level to the memory controller **20**. Note that "8x 1x" indicates the write command, "A1" indicates the address of the memory cell MC of the write target, and "D" indicates the write data.

[0077] After that, at time t**2**, when the memory controller **20** issues the interrupt command ("XX" in FIG. **5**A), the controller **150** interrupts the write operation up to that time and changes the busy signal to "H" level at time t**3**.

[0078] At time t**4**, the read command ("00 30" in FIG. **5**A) is issued. Then, the controller **150** outputs the busy signal of "L" level to the memory controller **20** and executes the read operation during the period of times t**5** to t**6**.

[0079] In the read operation, inter-latch data transfer to be described below is executed to output the read data to the register **170**.

[0080] As shown in FIG. **5**B, after the read data is temporarily stored in the SDL (represented by (1) in FIG. **5**B), the read data is transferred from the SDL to the UDL.

[0081] After that, since the SDL is a free space, the upper bit stored in the XDL is transferred to the SDL. Then, the read data stored in the UDL is output to the register **170** via the XDL. The read data is sequentially transferred to the register **170** via the I/O.

[0082] Data transfer to the sense amplifier **140** has been described above. However, the step of data transfer is not limited to this. In brief, focusing on the fact that the UDL has a free space, a step of transferring (1) write data from the XDL to the UDL and then transferring the read data from the SDL to the XDL may be employed. Hence, the step of data transfer is not limited to that described above.

[0083] Note that at this time, the data (lower bit) necessary for the write is stored in the LDL without being moved, as shown in FIGS. **5**A and **5**B.

[0084] The data transfer is controlled by the controller **150**.

[0085] After that, when the memory controller **20** issues the resumption command ("YY" in FIG. **5**A) at time t**8**, the controller **150** that has received it issues the busy signal of "L" level and resumes the write operation.

<Effect According to First Embodiment>

[0086] The memory system according to the first embodiment may obtain an effect (1).

[0087] (1) Throughput of Read Operation May be Improved

[0088] That is, in this embodiment, the memory controller **20** issues the interrupt command and the resumption command. Upon receiving the interrupt command, the nonvolatile semiconductor memory device **10** may interrupt the write operation and handle an interrupt of, for example, the read operation.

[0089] In general, data write requires a time of several ms. That is, when executing the read operation, the data is read after waiting for several ms. In this case, the operation speed of the memory system cannot be increased as a whole.

[0090] If the memory controller **20** simply issues the read command during the write operation, the write to the memory cell MC cannot be completed, and data written in the page direction (described with reference to FIG. **2**) at once may be destroyed.

[0091] This phenomenon will be described in detail. If the read operation intervenes in the middle of the rise of the voltage V**4** as shown in, for example, FIG. **4**B in accordance with the data in the XDL and the LDL, the read data is stored in the XDL via the I/O line. That is, the read data is overwritten on the write data up to that time. The data may be destroyed in this way.

[0092] In this case, it is necessary to switch the page and execute the write operation anew. However, the memory controller **20** does not necessarily issue the resumption command to the nonvolatile semiconductor memory device **10**. That is, from the viewpoint of the memory controller **20**, the request of the memory controller **20** is met when the data is read. Hence, the interrupted write command is not always issued by the memory controller **20**.

[0093] However, the memory system according to this embodiment includes both the interrupt command and the resumption command.

[0094] The interrupt command according to this embodiment has a function of causing the nonvolatile semiconductor memory device **10** to end the write operation up to certain step and output the read data to the register **170** without destroying the write data. It is therefore possible to obviate the necessity of waiting until the end of the write operation, as described above, and issue the interrupt command any time.

[0095] For this reason, the wait time from issuance of the read request by the memory controller **20** to the start of the read operation may be as short as several hundred μs. This increases the read throughput as compared to the above-described arrangement.

[0096] In addition, the register **170** in the nonvolatile semiconductor memory device **10** holds information immediately before the interrupt. Hence, even when the resumption command is received, the write voltage may be transferred to the word line WL from the point of interrupt.

[0097] As described above, in the memory system according to the first embodiment, data may be read without waiting for the completion of the write operation even in the middle of the write operation.

<Modification>

[0098] A memory system according to a modification (to be referred to as a first modification hereinafter) of the first embodiment will be described next.

[0099] In the first modification, a technique of the read operation in a state in which the QPW information is held in the UDL will be explained. In this case, data are stored in all of the latch circuits, that is, the SDL, UDL, LDL, and XDL. Hence, the SEN in the sense unit SU needs to be used for the operation among the data latches.

[0100] FIGS. 6A and 6B are conceptual views showing the command sequence and data transfer in the sense amplifier 140. Note that a description of the same operation as in the first embodiment will be omitted.

[0101] As shown in FIG. 6A, when the memory controller 20 issues the interrupt command, the upper bit, lower bit, and QPW information have been stored in the XDL, LDL, and UDL in the sense amplifier 140.

[0102] After that, when the read operation from time t7 is executed, the read data is stored in the SDL and finally transferred to the register 170 via the XDL. Data transferring to the sense amplifier 140 will be described with reference to FIG. 6B.

[0103] Note that the write data and QPW data stored in the UDL and the LDL are not stored in the sense amplifier 140. This is because there is no need to stored the data in the UDL and the LDL to one of the latch portions from the viewpoint of transferring the read data to the register 170 via the XDL. That is, the data that needs to be stored is the upper bit stored in the XDL.

[0104] As shown in FIG. 6B, the read data is transferred from the sense unit SU to the SDL (1). The data in the SDL needs to be transferred to the register 170 via the XDL. To do this, the data in the XDL is transferred to the SEN (2).

[0105] Since the XDL is a free space, the data is transferred from the SDL to the XDL (3).

[0106] Since the SDL is a free space, the upper data stored in the SEN in (2) is transferred to the SDL (5). After the read data stored in the XDL is transferred to the register 170, the upper data is returned from the SDL to the XDL.

<Effect According to First Modification>

[0107] Even the memory system according to the first modification may obtain the effect (1). That is, even if the necessary data are stored in all latch circuits, the read data may be transferred to the register 170 using the SEN for the operation among the data latches. For this reason, even when the write command is issued by the memory controller 20, the operation may quickly transit to the read operation.

Second Embodiment

[0108] A memory system according to the second embodiment will be described with reference to FIGS. 7A and 7B. The second embodiment is different from the above-described embodiment in that read data is overwritten on QPW data stored in a UDL. That is, the UDL is used in the second embodiment, although the SEN is used in the modification. Instead, QPW data stored in the UDL till then needs to be restored after the read operation. This will also be explained.

[0109] 1. <Sequence and Data Transfer>

[0110] FIGS. 7A and 7B are conceptual views showing the command sequence and data transfer to a sense amplifier 140. Note that a description of the same sequence as in the first embodiment will be omitted.

[0111] When the read operation is performed at time t1, a controller 150 transfers read data to the UDL in which the QPW data is stored. More specifically, the read data is temporarily stored in an SDL and then transferred to the UDL. Note that in this case as well, an XDL and an LDL keep holding the upper bit and the lower bit, respectively.

[0112] After that, the read data stored in the UDL by the controller 150 is transferred to a register 170 via the XDL.

[0113] This process will be described with reference to FIG. 7B. As shown in FIG. 7B, the data read by a sense unit SU is stored in the SDL by the controller 150 (1) and then transferred to the UDL (2). The verify result for the interrupted write operation disappears here.

[0114] Next, the controller 150 transfers the data in the XDL to the SDL having a free space (3). Since this makes it possible to store the read data in the XDL, the controller 150 transfers the data in the UDL to the XDL (4) and further transfers it to the register 170 (represented by Data Out in FIG. 7B).

[0115] After the end of the read, the controller 150 transfers the data in the SDL to the XDL so that the upper bit is stored in the XDL (5).

[0116] The controller 150 stores the QPW data in the UDL. A QPW data restore method will be described with reference to FIG. 8.

[0117] 2. <QPW Data Reconstruction Method>

[0118] Information held in the register 170 will be described first.

[0119] 2.1<Information Held in Register 170>

[0120] FIG. 8 shows information held in the register 170. FIG. 8 shows the threshold distribution of a memory cell MC and information stored in the register 170. That is, when the write operation is interrupted, the register 170 stores the status written in the memory cell MC.

[0121] FIG. 8 indicates that, for example, a status A is written in the memory cell MC. Note that the target threshold is "C" level.

[0122] 2.2<Flowchart (Restore Method)>

[0123] The operation of the QPW restore method will be described with reference to the flowchart of FIG. 9.

[0124] When the write operation is resumed, the controller 150 refers to the register 170 (step S10). The controller 150 then confirms the status of the memory cell MC stored in the register 170 (step S11).

[0125] The controller 150 executes a verify operation based on the status (step S12). More specifically, as shown in FIG. 8, the verify point is raised from a voltage V_AV to a voltage V_BV and to voltage V_CV, and it is checked whether a NAND string 11 flows current.

[0126] If the verify result is "L" level (YES in step S13), it is determined that transition up to the desired threshold distribution is not completed yet. The controller 150 executes rewrite based on the data stored in the XDL and the LDL (step S14). That is, the QPW data in the UDL is restored at this point of time.

[0127] If the verify result is "H" level in step S13 (NO in step S13), the controller 150 confirms whether transition up to the target threshold distribution is completed. That is, if the XDL and the LDL hold a data combination other than "1" and "1" (NO in step S15), the controller 150 determines that the target threshold distribution has not been reached yet, and executes the operation in step S14.

<Effect According to Second Embodiment>

[0128] As described above, when the register 170 is caused to hold, as information, the threshold distribution of the memory cell MC before the interrupt, the QPW data that has been erased may be restored. This is because the register 170 grasps the threshold distribution (status) of the memory cell MC immediately before the interrupt. That is, when the status information and write data are held, as in the second embodiment, the QPW data may be restored.

[0129] In addition, even the memory system according to the second embodiment may obtain the effect (1).

Third Embodiment

[0130] A memory system according to the third embodiment will be described next with reference to FIGS. 10A and 10B. The third embodiment is different from the above-described embodiments in that a sense amplifier 140 alternately reads data of odd- and even-numbered bit lines BL or alternately executes data write. The arrangement of the sense amplifier 140 will be described below. Nota that the same reference numerals denote the same components.

[0131] 1. <Example of Arrangement of Sense Amplifier 140>

[0132] FIG. 10A is a conceptual view showing the arrangement of the sense amplifier 140 and the step of data transferring. The arrangement of the sense amplifier 140 will be described here.

[0133] As shown in FIG. 10A, the sense amplifier 140 according to the third embodiment includes n-channel MOS transistors 30 to 36, latch circuits 50 to 54, and a capacitor element 55. Note that a latch circuit 50 (to be referred to as a PDC hereinafter) is formed from inverters 500 and 501, and a latch circuit 51 (to be referred to as an SDC hereinafter) is formed from inverters 510 and 511.

[0134] The arrangement of the sense amplifier 140 will be described below. Note that signals supplied to the gate of the MOS transistors are not illustrated.

[0135] One end of the current path of the MOS transistor 30 is connected to a bit line BL, and the other end is connected to a node N2. The node N2 will be referred to as a TDC hereinafter.

[0136] One electrode of the capacitor element 55 is connected to a node N2, and the other electrode is grounded.

[0137] One end of the current path of the MOS transistor 31 is connected to the node N2, and the other end is connected to a node N3. The PDC is connected to the node N3. More specifically, both the output terminal of the inverter 501 and the input terminal of the inverter 500 are connected to the node N3.

[0138] One end of the current path of the MOS transistor 32 is connected to the node N2, and the other end is connected to the SDC at a node N4. More specifically, the other terminal of the MOS transistor 32 is connected to the output terminal of the inverter 510 and the input terminal of the inverter 511 at the node N4.

[0139] The output terminal of the inverter 510 and the input terminal of the inverter 511 are connected to one end of the current path of the MOS transistor 36 via a node N4. Note that the other end of the current path of the MOS transistor 36 is connected to a register 170 via an I/O line.

[0140] One-end sides of the current paths of the MOS transistors 33 to 35 are connected to the node N3, and the other terminal sides of the MOS transistors are connected to

the latch circuit 52 (to be referred to as a CDG hereinafter), the latch circuit 53 (to be referred to as a BDC hereinafter), and the latch circuit 54 (to be referred to as a DDC hereinafter), respectively.

[0141] In the above-described arrangement, the upper bit of write data is stored in the SDC, and the lower bit is stored in the PDC.

[0142] Data transferring among the latch circuits at the time of data read will be described below with reference to FIGS. 10A and 10B.

[0143] 2. <Read Operation>

[0144] As described above, FIG. 10A is a conceptual view showing the arrangement of the sense amplifier 140 and the step of data transferring. FIG. 10B is a conceptual view showing the order of transfer of data stored in the latch circuits in FIG. 10A.

[0145] As shown in FIGS. 10A, and 10B, first, the lower bit stored in the PDC is transferred to the CDG (1). Since the PDC is a free space, the upper bit stored in the SDC is transferred to the PDC (2). The PDC is a latch circuit configured to exchange data with the register 170, and therefore needs to be temporarily released in this way.

[0146] After that, the lower bit stored in the CDG is transferred to the TDC, the upper bit stored in the PDC is transferred to the CDG, and the lower bit transferred to the TDC is stored in the original PDC (3).

[0147] Next, since the SDC is released, the read operation is executed. That is, read data is transferred to the SDC and then output to the register 170 via the SDC (4).

[0148] Finally, the upper bit saved in the CDG is stored in the original SDC (5).

[0149] The above-described steps (1) to (5) are performed, thereby executing the read operation while interrupting the write operation.

[0150] <Effect According to Third Embodiment>

[0151] Even the memory system according to the third embodiment may obtain the effect (1). That is, even if the data read method is different, when the interrupt command is issued, the write operation is interrupted, and the operation may immediately transit to the read operation. Note that although in the above description, the memory controller issues the interrupt command and the resumption command, this function may be imparted to the host device 2.

[0152] The area where the register 170 is arranged is not limited to the area in the nonvolatile semiconductor memory device 10. That is, the register 170 may be arranged in the memory controller 20 or the host device 2.

[0153] In, for example, FIG. 5A, the nonvolatile semiconductor memory device 10 meets the request of the read command from the memory controller 20 a plurality of number of times until the resumption command (YY) is received from the memory controller 20. That is, the nonvolatile semiconductor memory device 10 may perform the read operation any number of times.

[0154] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompa-

nying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a word line connected to a memory cell array; and

a controller configured to be capable of applying a voltage to the word line, perform a write operation upon reception of a write command, and output a busy signal representing that the write operation is progressing,

wherein the write operation includes a first phase, a second phase, and a third phase that are executed in the order given,

the controller performs a first verify operation after applying a first program voltage to the word line during the first phase; applies a second program voltage to the word line during the second phase; interrupts the write operation if an interruption command is received during the second phase; resumes the write operation if a resumption command is received after the interruption; applies a third program voltage to the word line during the third phase after the resumption; and the second program voltage is higher than the first program voltage, and the third program voltage is higher than the second program voltage.

2. The device of claim 1, wherein the controller outputs a ready signal after the interruption, and outputs a busy signal after resumption of the write signal.

3. The device of claim 2, wherein the controller performs a read operation if a read command is received after the interruption, and is capable of receiving the resumption command after completion of the read operation.

4. The device of claim 3, wherein the controller outputs a busy signal during the read operation.

5. The device of claim 1, wherein the controller performs a second verify operation before applying the third program voltage to the word line during the third phase if the resumption command is received.

6. The device of claim 1, wherein the controller applies the third program voltage to the word line during the third phase in response to the resumption command.

7. The device of claim 1, wherein the controller performs operations based on commands from an external memory controller.

8. A nonvolatile semiconductor memory device comprising:

a word line connected to a memory cell array; and

a controller configured to be capable of applying a voltage to the word line, perform a write operation upon reception of a write command, and output a busy signal representing that the write operation is progressing,

wherein the write operation includes a first phase and a second phase that are executed in the order given,

the controller performs applies a first program voltage to the word line during the first phase; interrupts the write operation if an interruption command is received during the first phase; resumes the write operation if a resumption command is received after the interruption; applies a second program voltage to the word line during the second phase after the resumption; and the second program voltage is higher than the first program voltage.

9. The device of claim 8, wherein the controller outputs a ready signal after the interruption, and outputs a busy signal after resumption of the write signal.

10. The device of claim 9, wherein the controller performs a read operation if a read command is received after the interruption, and is capable of receiving the resumption command after completion of the read operation.

11. The device of claim 10, wherein the controller outputs a busy signal during the read operation.

12. The device of claim 8, wherein the controller performs a first verify operation before applying the second program voltage to the word line during the second phase if the resumption command is received.

13. The device of claim 8, wherein the controller applies the second program voltage to the word line during the second phase in response to the resumption command.

14. The device of claim 8, wherein the controller performs operations based on commands from an external memory controller.

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