

March 23, 1965

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3,175,184

STATIC LOGIC POWER CONTROL

Filed Aug. 28, 1961

3 Sheets-Sheet 1

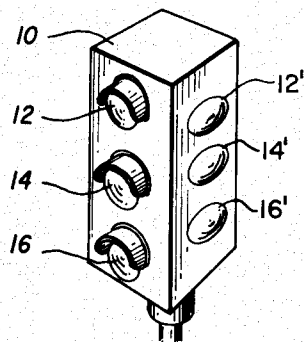


FIG. 1

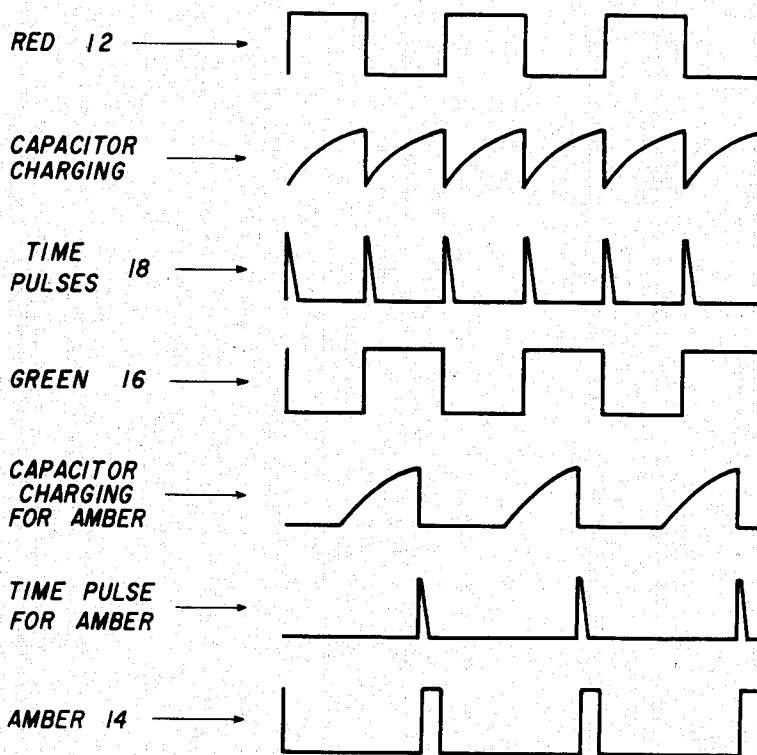


FIG. 2

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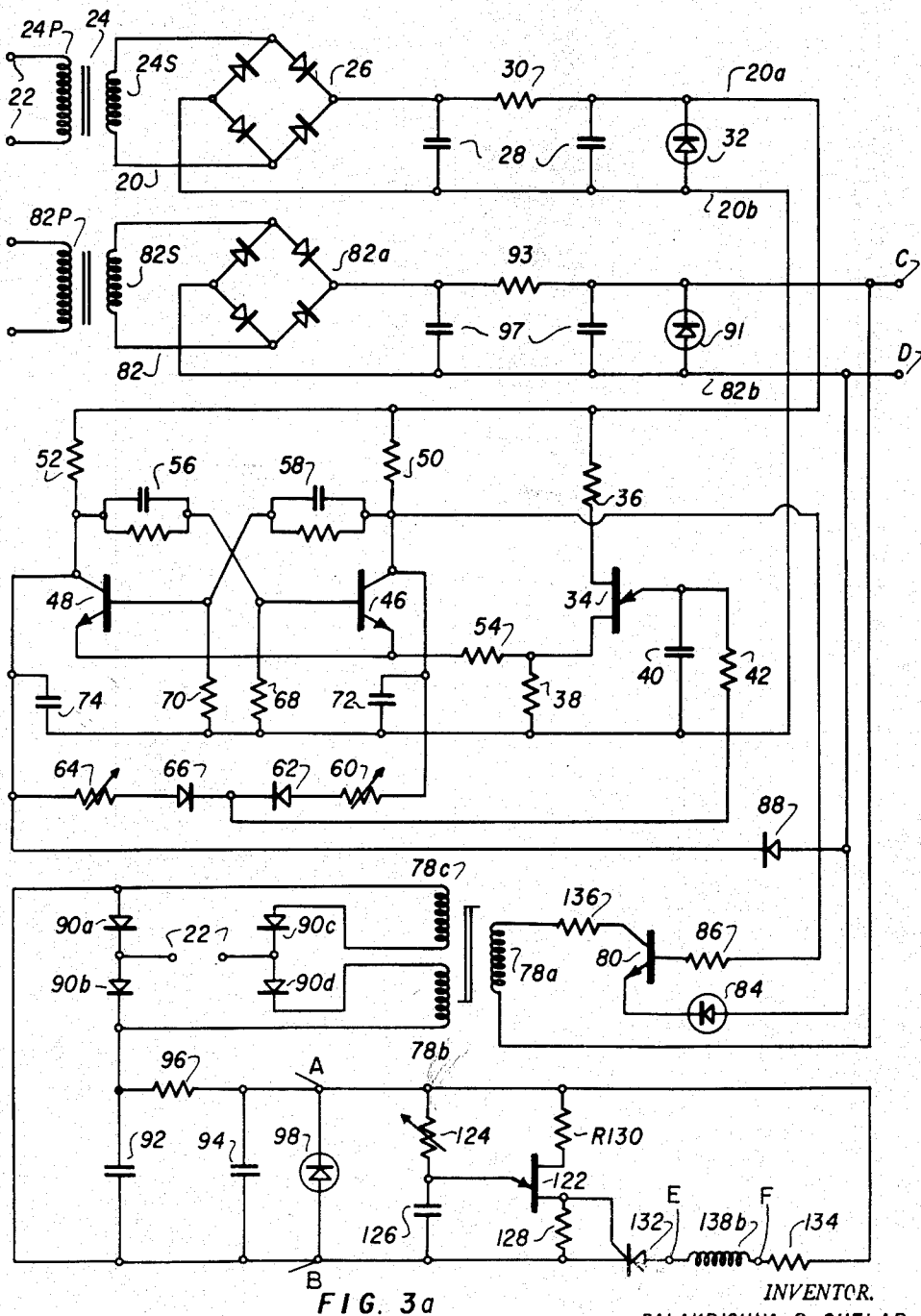
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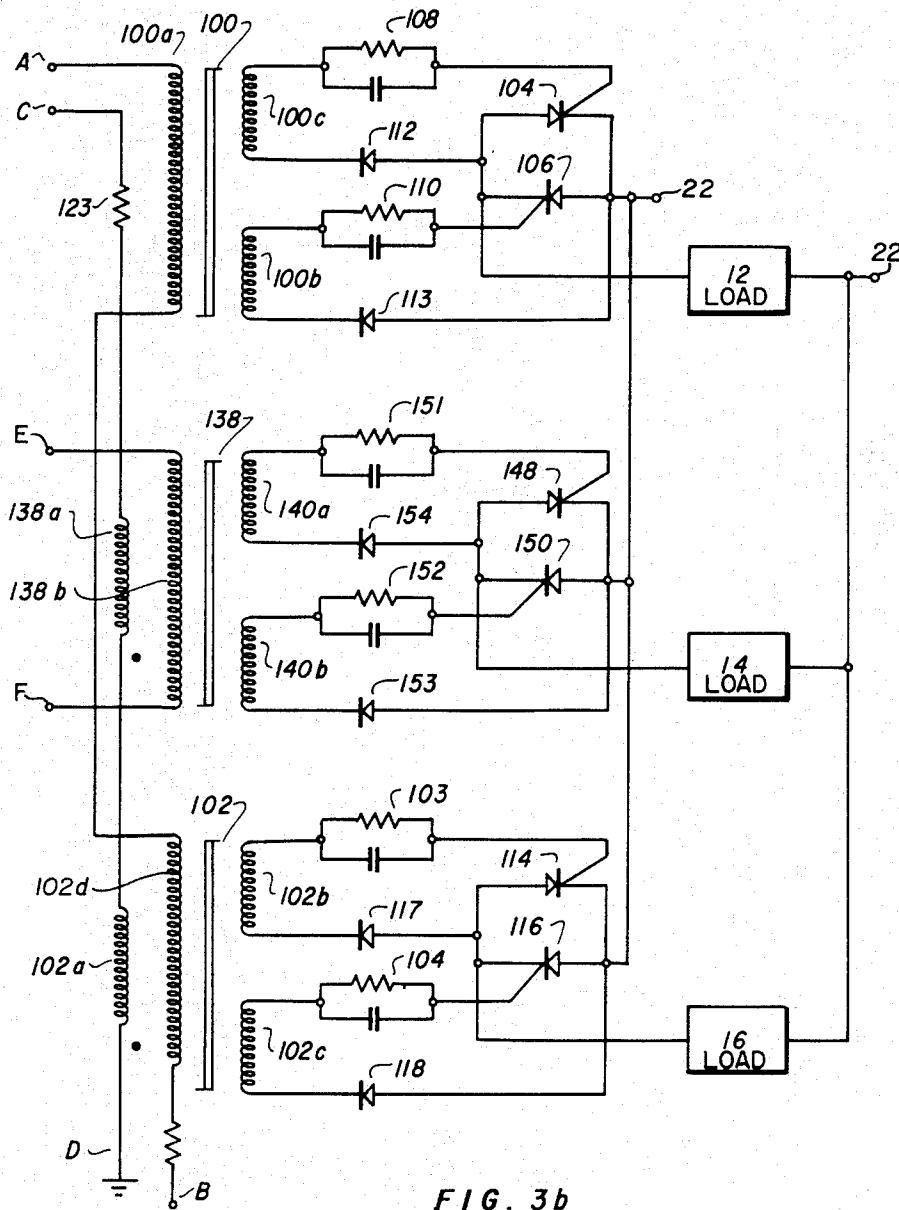
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STATIC LOGIC POWER CONTROL
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11 Claims. (Cl. 340—41)

The present invention relates to an improved control system for controlling two or more electrical loads alternately, simultaneously, and cyclically, at pre-determined time or pulse intervals. The apparatus herein described and claimed is especially useful as an entirely static apparatus for controlling numerous electrical loads in a logical system. This system can be specially adapted to vehicle control lights.

Vehicle control lights at street intersections—so-called “stop and go” lights—are in common use for the automatic control of cross traffic from the intersecting streets. Such lights must be controlled by an appropriate timing mechanism that assures that the traffic from the respective streets is allowed to pass for the time desired, that the appropriate stop signals are energized to arrest traffic in the direction to be stopped, and that an appropriate warning signal is energized to caution going traffic on the imminent stop signal to follow. Such timing mechanisms must be flexible to accommodate varying go and stop periods for the respective traffic—enabling the user to adjust the time period for each direction for the most favorable traffic control (including, if necessary, a longer “go” period in one direction than in the other).

Heretofore, control mechanisms for vehicle control lights have been largely of the mechanically operated type. That is, a cam switch is provided for each light, an appropriate cam-carrying shaft is provided in co-action with the switches, and a drive motor is used to rotate the shaft. Despite the availability of clever devices permitting variation in the respective light-energizing periods, apparatus of this type presents problems as to setting the time periods, is subject to frequent failures, and is often adversely affected by weather conditions. Additionally, optimum operation can be obtained only through recourse to frequent and thorough inspections and adjustments.

The apparatus of the present invention overcomes these difficulties by providing an entirely static control system for vehicle control lights. In brief, timed pulses are generated by a suitable main control pulse generator at the intervals when the change from red to green and from green to red are desired. These pulses serve, through the use of appropriate responsive apparatus to apply A.-C. current to the respective red and green lamps to provide the desired red and green alternate indications on the vehicle control lights. In addition, alternate pulses are rendered effective in delayed action to energize the amber light for a terminal part of each green and, or red, lamp energizing period. Further in accordance with the present invention all of these energizing periods are adjustable through the use of appropriate adjusting devices, thereby enabling the user to set the go and stop and caution times as desired. All of these operations are achieved with logic circuits using only semiconductor and other control devices having no filaments and no moving parts.

It is therefore a general object of the present invention to provide an improved control system apparatus for vehicle control lights that utilizes only static components.

A further object of the present invention is to provide such an apparatus wherein the respective stop, go, and caution periods are adjusted readily and over a range sufficient for normal applications.

Another and more particular object of the present invention is to provide a stop and go light control device wherein semi-conductor elements produce periodic main control pulses having controllable spacings, from which

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are derived all the necessary control signals to energize the respective green, amber, and red producing lights in a highly efficient, reliable, readily adjusted, and commercially effective manner, the whole being effective to energize the signal lamps from an alternating voltage source.

The novel features which I believe to be characteristic of my invention are set forth with particularity in the appended claims. My invention itself, however, together with further objects and advantages thereof, will best be understood by reference to the following description taken in connection with the accompanying drawings, in which:

FIGURE 1 is a perspective view of a conventional traffic signal light with which the present invention is concerned,

FIGURE 2 is a graphic representation of the time, voltage, and pulse relationships of the signalling system of the present invention, and,

FIGURES 3a and 3b are separate portions of a schematic diagram of a preferred embodiment of the present invention.

Referring now to FIGURE 1, there is shown a somewhat diagrammatic perspective view of a vehicle control light of the type to which the present invention may be applied. The light includes a housing 10 having vertically spaced groups of windows with appropriate colored lenses 12, 14, and 16, and 12', 14', and 16'. Lenses 12 and 12' are colored red to produce the red signal; lenses 14 and 14' are colored amber to produce the amber signal; and lenses 16 and 16' are colored green to produce the green signal. Incandescent lamp bulbs 12'', 14'', and 16'', not shown, are located behind the lenses 12, 14, and 16, respectively to produce—when energized—the correspondingly colored control signals. Similar incandescent lamp bulbs (not shown) are provided for the lenses 12', 14' and 16' and energized as hereinafter described.

In use, the red lens 12 and the green lens 16' are illuminated to indicate that traffic in one direction should stop and in the other direction may go. A predetermined period after this illumination starts, the amber lens 14' is illuminated to provide a caution indication for the terminal portion of this period for traffic in the “go” direction. Thereafter, the illumination on all these lenses is turned off in unison and the red lens 12' and the green lens 16 are illuminated to indicate that the traffic in the first direction must stop and in the other direction may go. A predetermined period thereafter, the amber lens 14 is illuminated for the terminal portion of this period to provide a caution indication for traffic in the direction that is now the “go” direction. Finally, at the conclusion of each complete cycle, illumination on the lenses 12', 16, and 14 is turned off in unison. The cycle is repeated indefinitely.

The above cycle, insofar as it involves illumination of lenses 12, 14, and 16, is shown diagrammatically in FIGURE 2. As shown in the bottom curve of this chart, the green illumination 16 takes place periodically—in this instance with the green occupying more than half of the total time. As shown in the next superior curve, the red illumination 12 occurs when the green illumination 16 is off. The next higher curve shows the amber illumination 14, which for illustrative purposes is shown as commencing at the last one third of each green illumination period and continuing in each instance to the terminous of the green illumination period. As is further discussed hereafter, this sequence of operations is controlled by the main control pulses 18 (top curve) which occur at the beginnings of the respective red and green illumination periods.

Referring now to the apparatus as shown in FIGURES 3a and 3b, the main D.-C. control power is derived from the power supply indicated generally at 20. The alternating voltage source 22 (preferably the conventional

110 volt, 60 cycle source) energizes the primary winding 24p of the transformer 24 and thereby produces voltage in the secondary winding 24s. This voltage may for example, be about 25 volts R.M.S. The secondary winding 24s is connected to the A.-C. terminals of the bridge rectifier 26. The D.-C. terminals of this rectifier are connected to the filter defined by the capacitors 28 and the resistance 30. The voltage is further smoothed and controlled by the zener or breakdown diode 32, which may, for example, be a type IN3029, to produce a well smoothed and regulated voltage of about 30 volts across the D.-C. output terminals 20a and 20b.

The control pulses 18, FIGURE 2, are generated by the time pulse trigger generator defined by the unijunction transistor 34 (which may, for example, be a type 2N491) and the associated circuitry. The main conducting circuit of the time pulse trigger generator may be traced from the positive terminal 20a of power supply 20 through resistor 36 to one base electrode of transistor 34 and thence to the other base electrode thereof. The circuit further extends through resistor 38 to the negative terminal 20b of power supply 20. Current flow through this circuit is controlled by the voltage of the emitter of the transistor 34, which voltage at any time is determined by the charge on the capacitor 40. This capacitor charges through resistance 42 and the other current elements hereinafter described in detail. As the voltage applied to the emitter of the transistor 34 reaches a predetermined positive conducting value (as capacitor 40 charges), the transistor 34 becomes highly conducting, relatively large current momentarily travels through the main conducting circuit (producing a voltage drop in resistance 38), and the emitter current flow discharges capacitor 40 to arrest the main current flow through the transistor after a very short time interval. Conduction of transistor 34 is not restored until the capacitor 40 is again charged through the resistor 42 as hereafter described. In consequence, the resistor 38 carries a short current pulse of the wave shape and timing of 18, FIGURE 2, to produce a voltage pulse that operates the flip flop circuit indicated generally at 44.

The multivibrator of flip-flop 44 is defined by the two NPN transistors indicated at 46 and 48, respectively, which may, for example be type 2N167 transistors. The collectors of these transistors are connected, respectively, to the positive terminal 20a of the power supply through the resistors 50 and 52, the latter serving as an output voltage resistor. The emitters are connected together and through resistors 54 and 38 to the negative power supply terminal 20b. The base of transistor 46 is connected to the collector of transistor 48 through the R.C. circuit 58, and the base of transistor 48 is connected to the collector of transistor 46 through the R.C. circuit 56. The resulting circuit is effective, if the flip flop is free running, to give rise to current flow in transistor 46 with essentially cutoff condition of transistor 48, subsequent discharge of the capacitor of R.C. circuit 58 until transistor 48 conducts, and then discharge of the capacitor of the R.C. circuit 56 until transistor 46 conducts to complete the cycle.

The resistors 50 and 52 thus carry alternate current pulses corresponding to the current flows through the respective transistors. They accordingly produce alternate negative and positive voltage pulses at the collectors in relation to the average collector voltages. The positive voltage pulse across resistor 50 and on the collector of transistor 46 is applied through variable resistor 60 and rectifier 62 to resistance 42, thus causing the capacitor 40 to charge when there is a positive voltage pulse across resistance 50. Similarly, when the positive voltage pulse appears across resistance 52, current flows through variable resistance 64 and rectifier 66 to resistance 42 to charge the capacitor 40. In each instance, the capacitor 40 is ultimately charged to the voltage giving rise to conduction in the transistor 34. Transistor 34 thereupon

executes a relaxation oscillation to produce current giving use to a voltage pulse 18 (FIGURE 2) across resistance 38. The emitters of the transistors 46 and 48 are driven in unison the positive direction through the action of resistance 54 and the related circuitry. The magnitude of the resultant voltage applied to the emitters is sufficient (in relation to the time when the pulse 18 is applied) to cause the nonconducting transistor 46 or 48, as the case may be, to become conducting and to flip the multivibrator 44 essentially in unison with the instant the transistor 34 becomes conducting.

Since the above action takes place at a time determined by the charging of capacitor 40 through the variable resistance 60 in one instance and variable resistance 64 in the other instance, the adjustments of these resistances determine the lengths of time between the successive flips. Since the resistances may have different adjustments, the duration of each condition of the multivibrator 44 is independently adjustable.

Resistance 68 and 70 and capacitors 72 and 74 stabilize the action of the flip flop or multivibrator 44.

The resultant voltage across resistance 52 (and hence the current value therethrough) is depicted as curve 52, FIGURE 2. It will be noted that this voltage goes from zero to essentially a fixed value on each alternate pulse 18 and drops from that value to essentially zero on each of the other pulses 18. As hereinafter described, this control pulse is fed to a "OR" gate logic circuit.

This "OR" gate logic circuit consists of transistor 80 which may be a type 2N335A as in FIGURE 3a. The power to this logic circuit is provided by regulated power supply 82 which consists of rectifier bridge, filter network and a zener reference. The output of this regulated supply is about 25 volts. This output appears at terminals 82a and 82b.

The emitter of the transistor 80 (2N335A) has been biased by a zener reference 84, in the emitter circuit to ground (82b). The pulses derived from flip-flop circuit across R52 are impressed on the base of the transistor 80 through R36. The height of the positive pulses appearing at the "OR" gate are the order of 15 volts, only the positive pulses of such heights are allowed to pass through "OR" gate as the emitter of the transistor 80 has been biased to this level—in other words, the transistor 80 will conduct only when it receives a pulse of a predetermined height and thus act as an "OR" gate. The collector of transistor 80 is connected to terminal 82a in series with a control winding 78a diode 88 has been used as a blocking diode between flip flop circuit and "OR" gate.

In FIGURE 3a magnetic core memory 78 consists of gate windings 78b and 78c, these windings are connected to full wave rectifier bridge which is composed of 90a, 90b, 90c, 90d. A.C. voltage source is applied at 22. Output of this magnetic core memory is fed to a filter circuit which consists of condenser 92, 94 and resistance 96, the filtered D.C. is regulated through zener 98. The regulated D.C. output appears at terminals A and B.

Normally the magnetic core memory has maximum output as it is not biased. When transistor 80 conducts upon the application of time pulse between the base of transistor 80 and ground a current flow is established from point 82a through control winding 78a and collect or through emitter to ground. This flow of current through control winding 78a of magnetic core memory cuts the output of the magnetic core memory to almost zero. This means that there will be no time pulse appearing at terminals A and B of FIGURE 3a. When the current flow through 78a ceases at the termination of time pulse from flip flop circuit, a full output pulse of shape 52, FIGURE 2, appears at terminals A and B, FIGURE 3a.

The output time pulses from magnetic core memory at terminals A and B are directly applied to phase shifter magnetic memory core 100 and 102 as shown in FIGURE

3b. The phase shifter magnetic memory core consists of gate windings 100c, 100b and a control winding 100a (this is for phase shifter magnetic memory core 100) similarly 102 consists of two gate windings 102b, 102c and control winding 102a. 102 also has an additional winding called bias winding which is connected to terminals C and D to provide necessary bias current for 102.

The main function of these phase shifter magnetic memory core is to provide necessary firing pulses to the silicon controlled rectifier gates at proper time intervals and perform logic function in controlling different loads through silicon controlled rectifiers.

The gate windings of phase shifter magnetic memory core consists of R.C. network 108, diode 112, R.C. network 110 and diode 113 in series with each gate winding. Respectively the phase shifter magnetic memory core 102 also consists of R.C. networks and diodes as shown in FIGURE 3b. One end of each phase shifter magnetic memory core gate winding is connected to the anode of silicon controlled rectifiers which are connected into a back to back fashion to give full wave A.C. output to the load, upon conduction, other end of the phase shifter magnetic memory core gate winding is connected through pulse differentiating R.C. network to the gate of respective silicon controlled rectifiers 104, 106, 114, and 116 as indicated in FIGURE 3b. Normally when the phase shifter magnetic memory core is saturated, a maximum A.C. voltage appears at the gate windings. This action takes place only when a respective controlled rectifier anode has a positive half cycle of the A.C. This positive part of A.C. appearing at the gate windings of the phase shifter memory core is rectified and differentiated in a form of narrow sharp pulse and is applied to the gate of respective controlled rectifiers as shown in FIGURE 3b. This will allow the controlled rectifiers to conduct fully and maximum A.C. voltage will appear at the load. When we apply a D.C. current to the control winding of phase shifter magnetic memory core to desaturate, the gate windings become highly unsaturated and no voltage appears at the terminals of the gate windings—therefore, no pulses appear at the gate of the silicon controlled rectifier; therefore the conduction of the silicon controlled rectifier is ceased and no A.C. voltage will appear at the load.

Phase shifter magnetic memory core 100 controls red light 12 and 102 controls green light 16. The control windings 100a and 102a are connected in series at the terminals A and B where the pulses of form 52, FIGURE 2, appear. At the start of the system if we assume that there is no pulse appearing at terminals A and B, therefore no current will flow in the control windings 100a and 102a phase shifter. Magnetic memory core 100 is highly saturated and provides the pulses to fire the silicon controlled rectifiers 104 and 106. This will apply full A.C. voltage at (load) red light 12 and the red light will be illuminated.

Phase shifter magnetic memory core 102 is highly unsaturated due to the application of bias through the winding 104 at terminals C and D, and therefore, no firing pulses appear at the gates of the silicon controlled rectifiers 114 and 116. This means that the controlled rectifiers 114 and 116 will not conduct—therefore no A.C. voltage will appear at (load) green light 16.

When the time pulse 52 in FIGURE 2 appears at terminals A and B a current starts to flow through the control windings 100a and 102a. The current flow in winding 100a desaturates the phase shifter magnetic memory core as the application of the current through 100a is in the direction to cancel the saturating M.M.F. and make the phase shifter magnetic memory core 100 unsaturated. This will mean that no firing pulses will appear at the gates of the silicon controlled rectifiers 104, 106. Therefore the conduction of silicon controlled rectifiers 104 and 106 will be ceased and no voltage

will appear at (load) red light 12, and the red light will be completely cut off.

The flow of current through winding 102a of 102 phase shifter magnetic memory core is in such a direction that it will cancel the M.M.F. produced due to the flow of current through bias windings 104; the current through bias winding 104 normally unsaturates the phase shifter magnetic memory core. The application of current through control winding 102a cancels the M.M.F. produced by the bias winding 104 and make the phase shifter magnetic memory core highly saturated. This produces the firing pulses which are applied to the gates of silicon controlled rectifiers 114, 116. These firing pulses allow the silicon controlled rectifiers to conduct—therefore A.C. voltage will appear at (load) green light 16 and illuminate the green light for the duration of the time pulse current flow through control winding 102a. An A.C. voltage source for loads is derived from terminal 22, FIGURE 3b.

The amber light (load) 14 is energized during a predetermined terminal part of the energized period of the green light 16.

The amber light control circuit consists of phase shifter magnetic memory core 138 which is similar to other phase shifter magnetic memory cores 100 and 102 and is biased to desaturation through winding 138b. Associated control circuit consists of time pulse trigger generator which is composed of unijunction transistor 122. This transistor has two bases and an emitter, base one of this transistor is connected to terminal B through R128 and base two is connected to terminal A through R130. Emitter of this transistor is connected to a junction of R124 and capacitor 126—the other end of the R124 is connected to terminal A, and the other end of the capacitor 126 is connected to terminal B. This circuit forms a time pulse trigger generator. In this circuit capacitor 126 is charged through R124. The rate of charge of capacitor 126 determines the delay of the time pulses trigger. Normally the unijunction transistor 122 is in a non-conducting state when capacitor 126 is charged to a firing voltage the capacitor 126 is discharged through the emitter, the current flow in the emitter causes the transistor 122 to conduct very heavily for a short duration. This conduction gives a rise to a pulse in base one resistance 128.

These time pulses are then fed to an "and" gate logic circuit which uses a silicon controlled rectifier as an "and" gate. The anode of this silicon controlled rectifier is connected to terminal A in series with control winding 138a and R134. The cathode is connected to terminal B, gate of the silicon controlled rectifier is connected to base one of the unijunction transistor 122 as shown in FIGURE 3b.

It is necessary to satisfy two conditions to operate the "and" gate circuit. The first condition is that A pulse shape 52, FIGURE 2, must appear at terminals A and B. The second condition is that time pulse trigger generator must provide a trigger pulse to the gate of silicon controlled rectifier 132. Once the trigger pulse is applied to the gate of silicon controlled rectifier 132, a current flow is established from point A through R134 and control winding 138a through silicon controlled rectifier 132 to terminal B "and" gate remains in conduction as long as there is a pulse at terminals A and B. The on period of "and" gate is predetermined as a portion of pulse 52, FIGURE 2, and this is variable as a function of the charging rate of the capacitor 126. As soon as the "and" gate is on a current will start to flow in the control winding 138a of 138 phase shifter magnetic memory core. The flow of the current in control winding 138a is in such a direction that it cancels the M.M.F. produced by the flow of current in bias winding 138b. This cancellation of M.M.F. saturates the phase shifter magnetic core memory 138. This saturation will produce necessary firing pulses to fire silicon controlled rectifier 148 and 150

in the same manner as described in relation to phase shifter magnetic memory core 100 and 102. Once the silicon controlled rectifiers 150 and 148 start conduction, a full wave A.C. voltage will appear at (load) amber light and illuminate the amber light. Amber light 16 will be on for the remaining portion of the pulse 52 appearing at terminals A and B. As soon as the pulse 52 at terminals A and B disappears the amber light will be cut off. At this instance a new cycle of operation starts that is a red light 12 will illuminate and the rest of the lights will be cut off.

In a device constructed in accordance with the circuits of FIGURES 3a and 3b, the following component parts were used:

Capacitors 40 and 126	50 microfarads.
Resistances 60, 64, and 124	.25M-2 ohms, variable.
Resistances 50 and 52	2,000 ohms.
R.C. networks 56 and 58	.001 microfarad, 47,000 ohms.
C28-C92, 94, 97, 98	16 microfarads.
R-136-134, 123	800.
Resistance 38	47 ohms.
Resistance 54	677 ohms.
Resistances 36 and 130	300 ohms.
Resistance 42	4,000 ohms.
Resistance 96+30	3,000 ohms.
R93	1,000 ohms.
Transistors 34 and 122	2N491 type.
Transistors 46 and 48	2N167 type.

While I have shown and described a specific embodiment of the present invention it will be understood that various modifications and alternative constructions may be made without departing from the true spirit and scope of the invention. I therefore intend by the appended claims to cover all such modifications and alternative constructions as fall within their true spirit and scope.

What I claim as new and desire to secure by Letters Patent of the United States is:

1. A static commutator for sequentially energizing a load circuit comprising: a first saturable core transformer having an input connection and an output connection, a source of pulses having an output coupled to the input of said saturable core transformer to unsaturate said core for the duration of said pulses, an alternating current source, rectifier means coupled to said alternating current source and to the output circuit of said saturable core transformer, said rectifier means supplying a direct current output during the saturated periods of said transformer, a second saturable core transformer having an input connection and an output connection, said input connection coupled to said direct current output to unsaturate said second core for the duration of said current, alternating current gating means connected to said second transformer output connections, said gating means being operated to a conductive state by the saturation of said second transformer, and load means connected to said gating means and said alternating current source to be controlled in response to the changes in the states of conduction thereof.

2. A device as claimed in claim 1 including: a delay circuit having an input and an output, said delay circuit input connected to said direct current output terminals and providing an output after a predetermined delay period after the occurrence of a direct current at said pair of output terminals, and saturable core transformer having an input connection, an output connection and a bias connection, said third transformer input connection connected to said delay circuit output terminals, said third transformer bias connection connected to said bias source to maintain it in a desaturated condition, second alternating current gating means connected to said third transformer output connection, said second gating means being operated to a conductive state for the saturated period of said third transformer and second load means

connected to said second gating means and said alternating current source to be controlled in response to the changes in the states of conduction thereof.

3. A device as claimed in claim 1 including: a direct current bias source, a third saturable core transformer having an input connection, an output connection and a bias connection, said bias connection connected to said bias source to desaturate said third core, said input connection coupled to said direct current output to overcome said bias desaturation for the duration of said rectifier means direct current output, second alternating current gating means connected to said third transformer output connection operated to a conductive state for the saturated period of said third transformer, and second load means connected to said second gating means and said alternating current source to be controlled in response to the changes in the states of conduction thereof.

4. A device as claimed in claim 3 including: a delay circuit having an input and an output, said delay circuit input connected to said direct current output terminals and providing an output after a predetermined delay period after the occurrence of a direct current at said pair of output terminals, and a fourth saturable core transformer having an input connection, an output connection and a bias connection, said fourth transformer input connected to said delay circuit output terminals, said fourth transformer bias connection connected to said bias source to maintain it in a desaturated condition, third alternating current gating means connected to said fourth transformer output connection, said third gating means being operated to a conductive state for the saturated period of said fourth transformer and a third load means connected to said third gating means and said alternating current source to be controlled in response to the changes in the states of conduction thereof.

5. A static commutator for sequentially energizing a load circuit comprising: a first saturable core transformer having an input connection and an output connection, a source of pulses having an output coupled to the input of said saturable core transformer to unsaturate said saturable core transformer for the duration of said pulses, an alternating current source, rectifier means coupled to said alternating current source and to the output circuit of said saturable core transformer, said rectifier means supplying a direct current output during the saturated periods of said saturable core transformer, a direct current bias source, a second saturable core transformer having a control winding connection, a gate winding connection and a bias connection, said bias connection connected to said bias source to desaturate said second saturable core transformer, said control winding connection coupled to said direct current output to overcome said bias desaturation for the duration of said rectifier means direct current output, alternating current gating means connected to said second saturable core transformer gate winding connection, said gating means being operated to a conductive state for the saturated period of said second saturable core transformer, and load means connected to said gating means and said alternating current source to be controlled in response to the changes in the states of conduction thereof.

6. An electric control system for alternately energizing a first and then a second load, comprising: an alternating current source, a first rectifier means and a direct current source, a first magnetic core means including a first and a second winding means, first circuit means comprising the connections of said first rectifier means, said alternating current source, said first magnetic core second winding means and a pair of output terminals, said first circuit means operated to supply a direct current at said pair of output terminals, a time pulse generator means operated to supply a periodic input signal to said first magnetic core first winding means sufficient to unsaturate said magnetic core means for the duration of said input pulse, said first magnetic core means operated in response

to said input signal to shut off said first circuit means direct current output, a second magnetic core means including a first and a second winding means, a third magnetic core means including a first, a second and a third winding means, said first winding means of said second and third magnetic core means connected in series to said pair of output terminals, said third winding means connected to said direct current source, a first and a second pair of controlled solid state rectifier devices each having means for controlling the conductivity of the device, each said pair of devices having their opposite terminal regions connected together, first and second terminal circuit means for connecting said first and second pair of devices in series with said alternating current source and said first and second load respectively, first and second control circuit means for connecting said controlling means of said first and said second pair of devices in series with said second and third magnetic core second winding means and a terminal of said devices, said first pair of devices operated upon the absence of current in said second magnetic core first winding means and shut off during the flow therethrough of a current from said pair of output terminals, said second pair of devices operated during the presence of current in said third magnetic core first winding means and shut off during the absence of a current flow therethrough.

7. An electric control system for alternately energizing a first, a second and then a third load, comprising: an alternating current source, a direct current bias source, a first rectifier means and a direct current source, a first magnetic core means including a first and a second winding means, first circuit means comprising the connections of said first rectifier means, said alternating current source, said first magnetic core second winding means and a pair of output terminals, said first circuit means operated to supply a direct current at said pair of output terminals, a timing pulse generator means operated to supply a periodic input signal to said first magnetic core first winding means sufficient to unsaturate said magnetic core means for the duration of said input pulse, said first magnetic core means operated in response to said input signal to shut off said first circuit means direct current output, a delay circuit means having input and output connections, said input connections connected to said direct current output terminals and providing an output a predetermined period of time after the occurrence of a direct current at said pair of output terminals, a second magnetic core means including a first and a second winding means, a third and a fourth magnetic core means including a first, a second and a third winding means, said first winding means of said second and third magnetic core means connected in series to said pair of output terminals, said first winding means of said fourth magnetic core means connected to said delay circuit output terminals, said third winding means of said third and fourth magnetic core means connected to said bias current source, a first, a second, and a third pair of controlled solid state rectifier devices each having means for controlling the conductivity of the device, each said pair of devices having their opposite terminal regions connected together, first, second, and third terminal circuit means for connecting said first, second and third pair of devices in series with said alternating current source and said first, second, and third loads respectively, first, second, and third control circuit means for connecting said controlling means of said first, second and third pair of devices in series with said second, third, and fourth magnetic core second winding means and a terminal of said devices, said first pair of devices operated upon the absence of current in said second magnetic core first winding means and shut off during the flow therethrough of a current from said pair of output terminals, said second pair of devices operated during the presence of current in said third magnetic core first winding means and shut off during the absence of a current flow therethrough,

said third pair of devices operated during a portion of the periods of said first and said second pair of devices.

8. A device as claimed in claim 7 wherein said delay circuit comprises: a charging circuit including a resistor and a capacitor in series and connected across said direct current output terminals, an input sensing transistor having an input base electrode, a collector electrode and an emitter electrode, with the base electrode connected to the junction of said resistor and capacitor to respond to the voltage across the capacitor, an output transistor for connecting said direct current output to said delay circuit output terminals, means coupling the collector electrode of the first transistor to the input base electrode of said output transistor to cause said output transistor to operate when the input transistor senses a predetermined voltage accumulated across the capacitor.

9. A device as claimed in claim 7 wherein said delay circuit comprises: a charging circuit including a resistor and a capacitor in series and connected across said direct current output terminals, an input sensing transistor having an input base electrode, a collector electrode and an emitter electrode, with the base electrode connected to the junction of said resistor and capacitor to respond to the voltage across the capacitor, a silicon controlled rectifier for connecting said direct current output to said delay circuit output terminals, means coupling the collector electrode of the first transistor to the input base electrode of said silicon controlled rectifier to cause said silicon controlled rectifier to conduct when the input transistor senses a predetermined voltage accumulated across the capacitor.

10. A device as claimed in claim 9 wherein the second winding means of said first magnetic core means comprises a pair of output windings and said first circuit means comprises a bridge rectifier configuration including said pair of windings in two of said bridge arms.

11. In a traffic control apparatus for a two-way vehicle control light having red stop, yellow caution and green go indicating lights for each direction, comprising in combination: an alternating current source, a direct current bias source, a first rectifier means and a direct current source, a first magnetic core means including a first and a second winding means, first circuit means comprising the connections of said first rectifier means, said alternating current source, said first magnetic core second winding means and a pair of output terminals, said first circuit means operated to supply a direct current at said pair of output terminals, a timing pulse generator means operated to supply a periodic input signal to said first magnetic core first winding means sufficient to desaturate said magnetic circuit for the duration of said input pulse, said first magnetic core means operated in response to said input signal to shut off said first circuit means direct current output, a delay circuit means having input and output connections, said input connections connected to said direct current output terminals and providing an output a predetermined period of time after the occurrence of a direct current at said pair of output terminals, a second magnetic core means including a first and a second winding means, a third and a fourth magnetic core means including a first, a second and a third winding means, said first winding means of said second and third magnetic core means connected in series to said pair of output terminals, said first winding means of said fourth magnetic core means connected to said delay circuit output terminals, said third winding means of said third and fourth magnetic core means connected to said bias current source, a first, a second and a third pair of silicon controlled rectifier devices each having means for controlling the conductivity of the device, each said pair of devices having their opposite terminal regions connected together, first second and third terminal circuit means for connecting said first, second and third pair of devices in series with said alternating current source and said red, green and yellow traffic lights, first, second and third control circuit means for connecting said controlling means of said first,

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second and third pair of devices in series with said second and third and fourth magnetic core, second winding means and a terminal of said devices, said first pair of devices operated upon the absence of current in said second magnetic core first winding means and shut off during the flow therethrough of a current from said pair of output terminals, said second pair of devices operated during the presence of current in said third magnetic core first winding means and shut off during the absence of a current flow therethrough, said third pair of devices operated

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during a portion of the periods of said first and said second pair of devices.

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