(12) UK Patent (19) GB (11) 2 133 622 B

(54) Title of invention

An integrated injection logic semiconductor integrated circuit device

(51) INT CL⁴; H01L 27/04 29/40 29/70

(21) Application No
8403188

(22) Date of filing
21 Jan 1983
Date lodged
8 Feb 1984

(30) Priority data

(31) 57/006932

(32) 25 Jan 1982

(33) Japan (JP)

(60) Derived from Application No. 8301731 under Section 15(4) of the Patents Act 1977

(43) Application published
25 Jul 1984

(45) Patent published
20 Nov 1985

(52) Domestic classification
H1K 11A3A 11B3 11C1A 11C4 11D1 11D3 11D 1AA1 1AA2 1FJ 4C11 4C1U 4C2B 9B3 9B4A 9E 9P2 9R2 GAH

(56) Documents cited
None

(58) Field of search
H1K

(73) Proprietors
Hitachi Ltd
(Japan)
6 Kanda Surugadai 4-chome
Chiyoda-ku
Tokyo
Japan

(72) Inventors
Setsuo Ogura
Shizuo Kondoh

(74) Agent and/or
Address for Service
Mewburn Ellis & Co.,
2/3 Cursitor Street,
London EC4A 1BQ

GB 2 133 622 B

FIG. 1

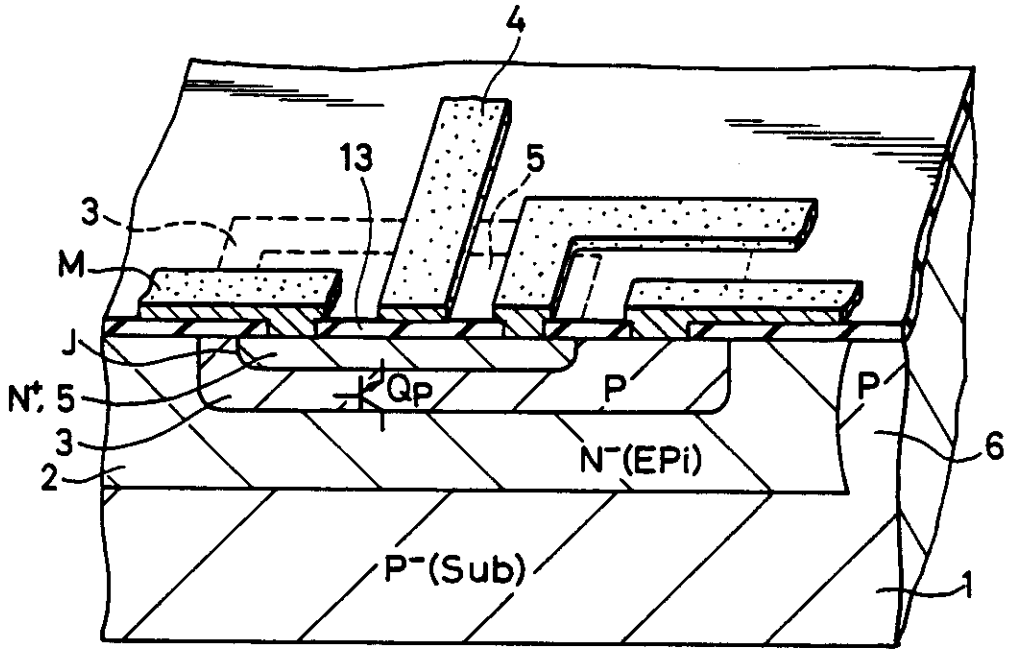

4
13
5
3
M
J
N+ 5
3
2
Qp
P
P
N⁻(EPi)
P⁻(Sub)
6
1

FIG. 2

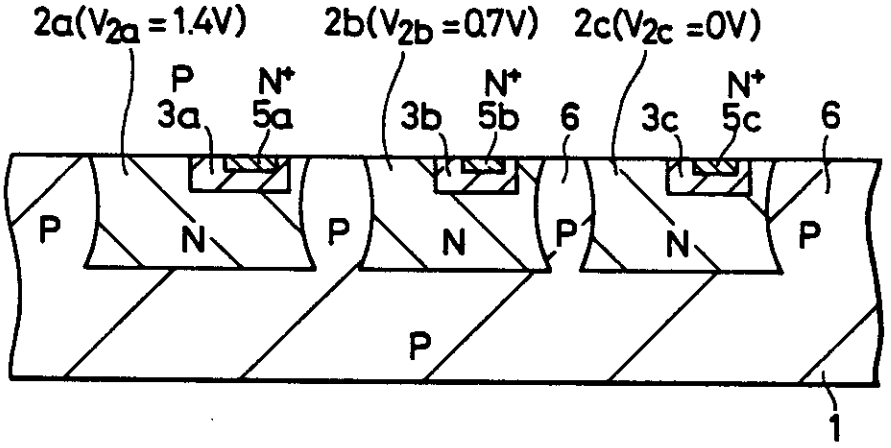

2a(V2a = 1.4V)
2b(V2b = 0.7V)
2c(V2c = 0V)
P
N+
3a
5a
3b
5b
6
3c
5c
6
P
N
P
N
P
N
P
P
1

FIG. 3

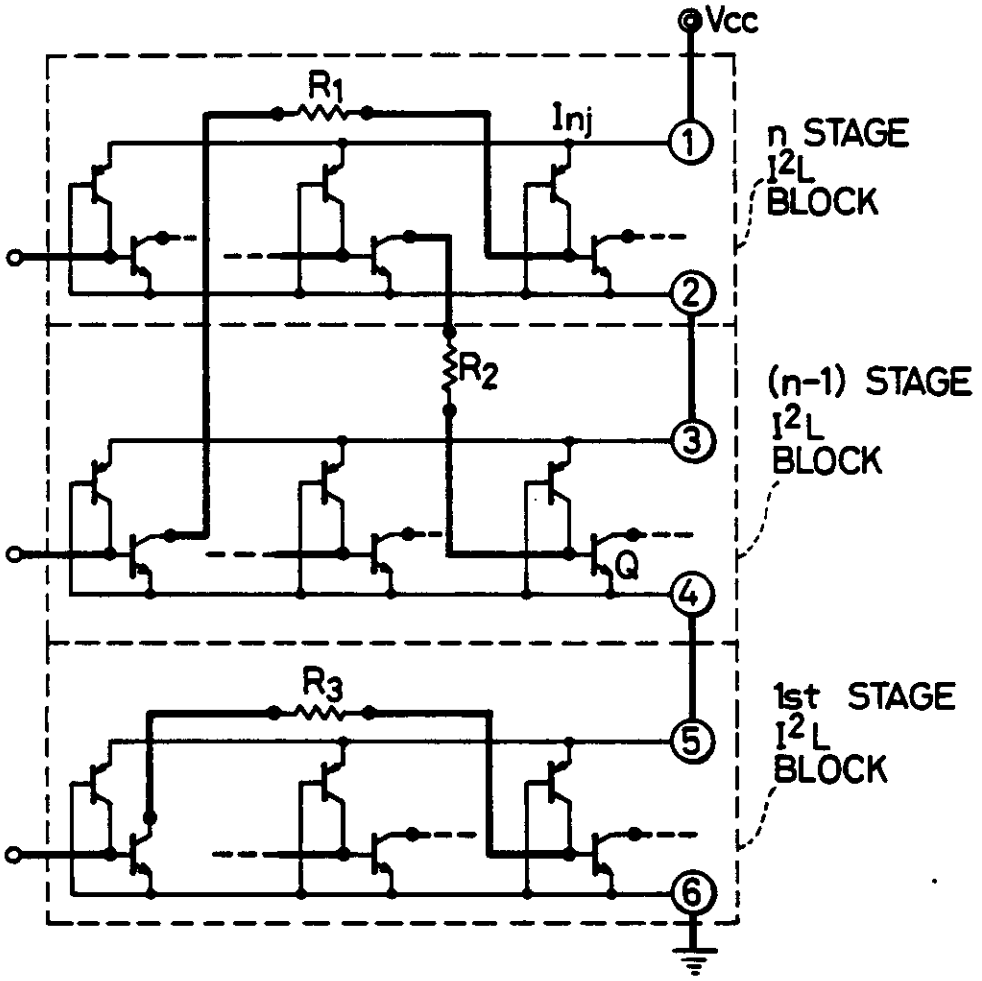

Vcc
R1
Inj
n STAGE
I2L
BLOCK
R2
(n-1) STAGE
I2L
BLOCK
Q
R3
1st STAGE
I2L
BLOCK
1
2
3
4
5
6

FIG. 4

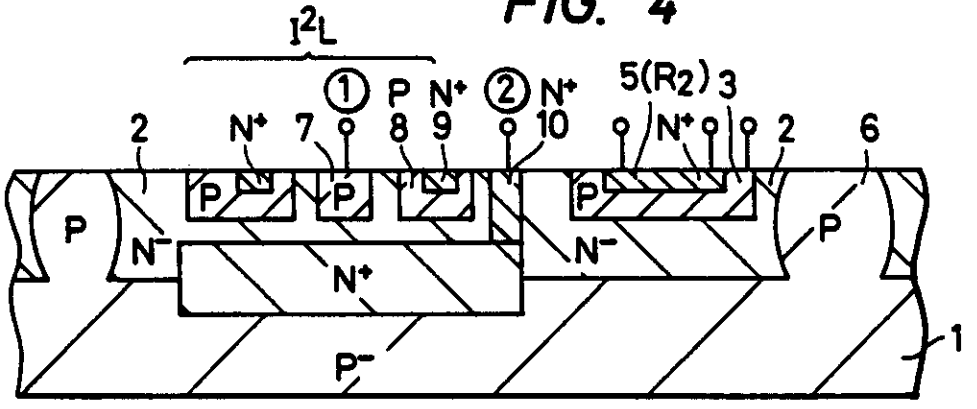

I2L
1
P
N+
2
N+
5(R2)
3
2
6
2
N+
7
8
9
10
N+
P
P
P
P
N-
N-
N+
P-
1

FIG. 5

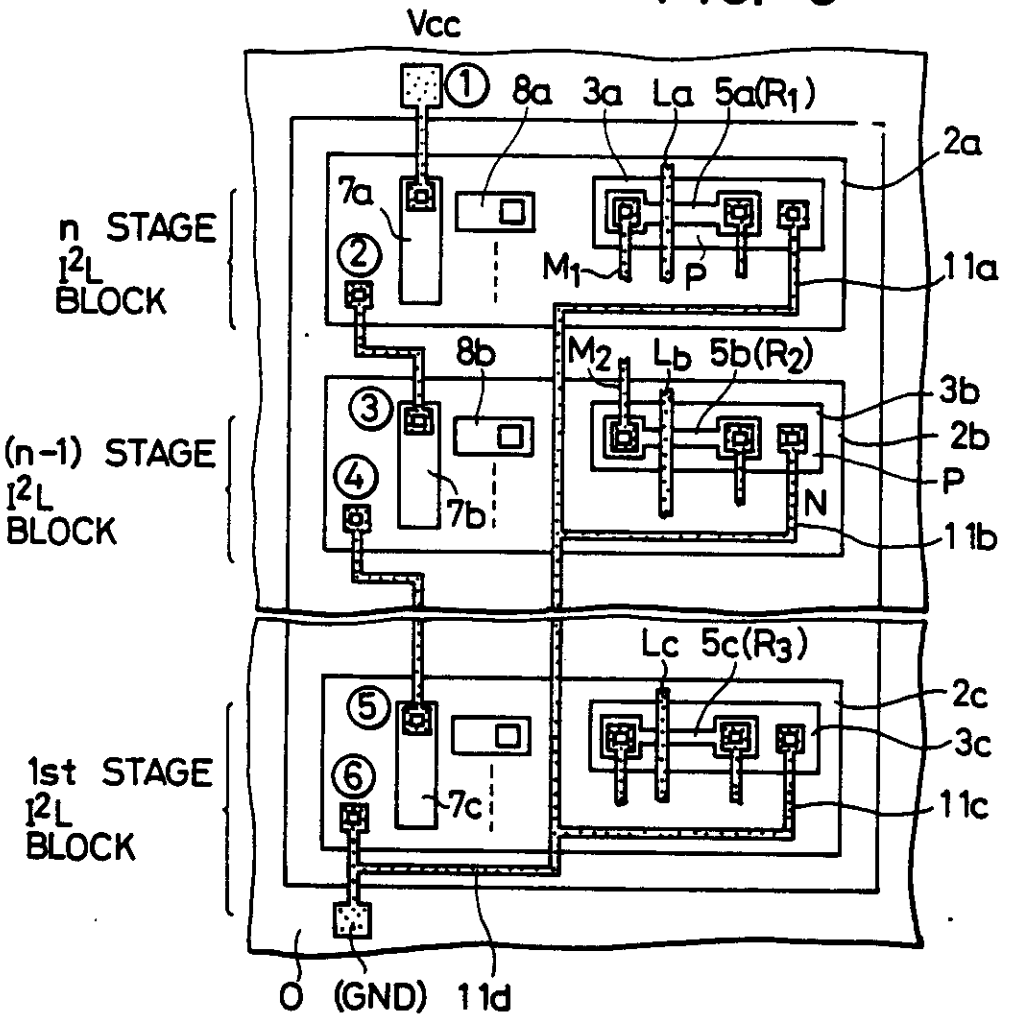

Vcc
① 8a 3a La 5a(R1)
2a
7a
n STAGE
I2L
BLOCK
②
M1
P
11a
8b
M2 Lb 5b(R2)
③
3b
2b
P
N
④
7b
11b
(n-1) STAGE
I2L
BLOCK
Lc 5c(R3)
⑤
2c
3c
⑥
7c
11c
1st STAGE
I2L
BLOCK
O (GND) 11d

FIG. 6

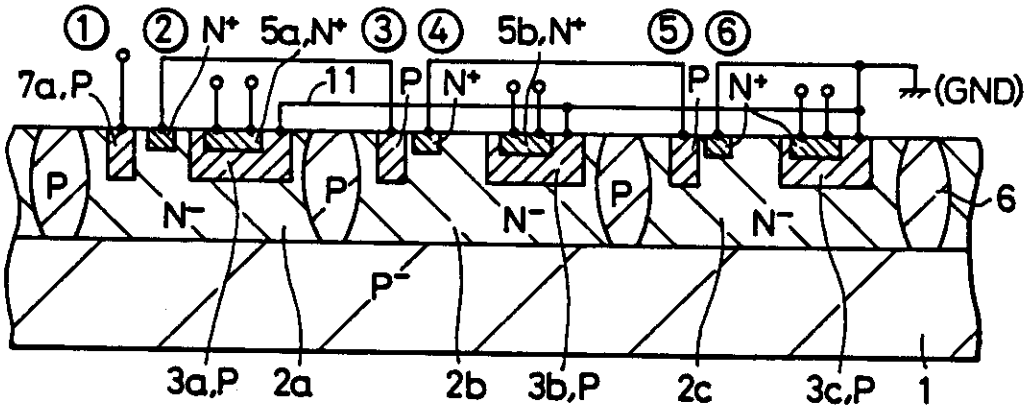

① ② N+ 5a,N+ ③ ④ 5b,N+ ⑤ ⑥
7a,P
11
P
N+
P
N+
(GND)
P
N-
P
N-
P
N-
6
P-
3a,P 2a 2b 3b,P 2c 3c,P 1

FIG. 7

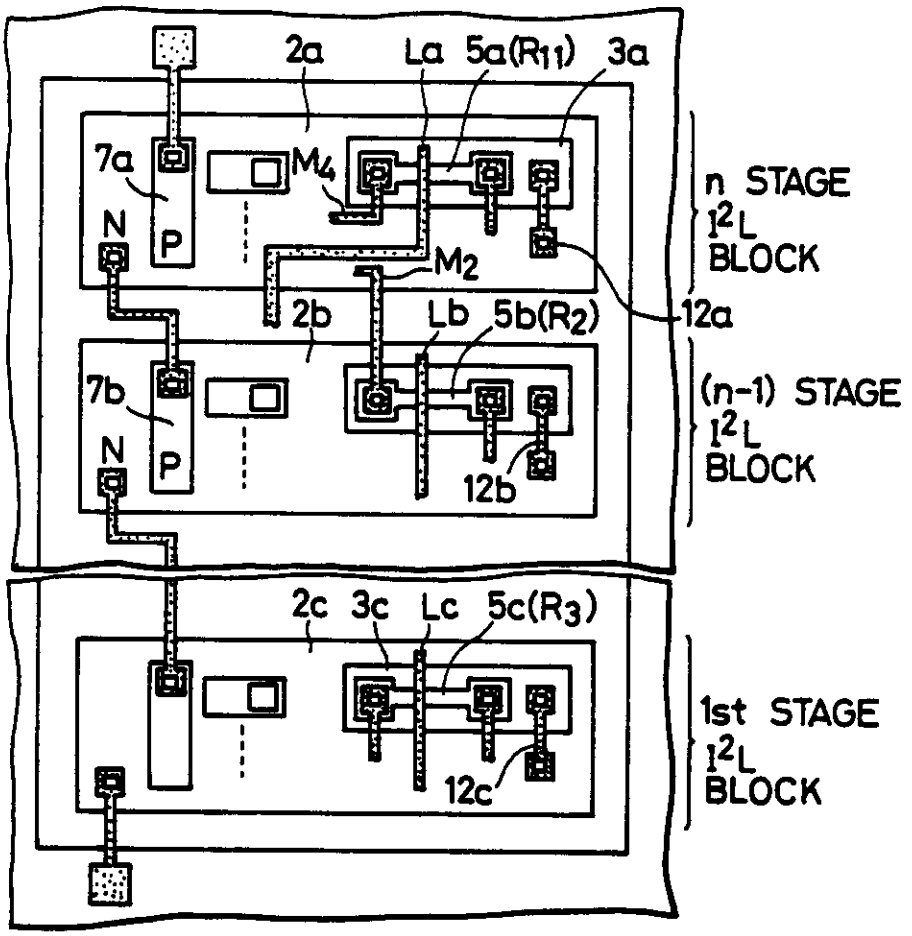

2a
La
5a(R11)
3a
7a
M4
N
P
M2
2b
Lb
5b(R2)
12a
n STAGE
I2L
BLOCK
7b
N
P
12b
(n-1) STAGE
I2L
BLOCK
2c
3c
Lc
5c(R3)
12c
1st STAGE
I2L
BLOCK

FIG. 8

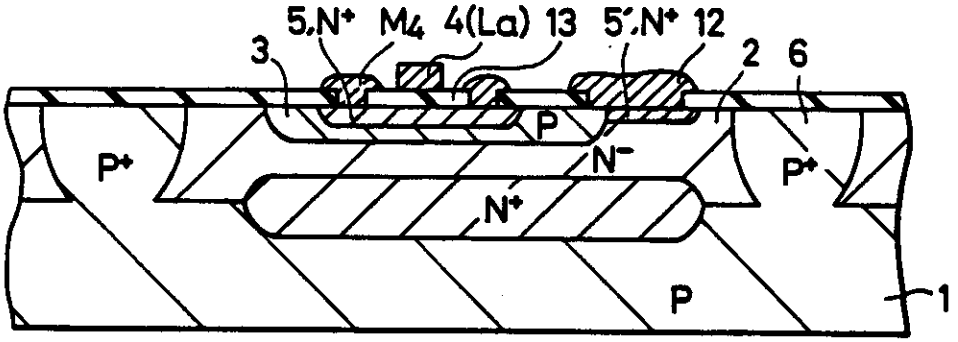

5,N+
M4
4(La)
13
5',N+
12
3
2
6
P
N-
P+
P+
N+
P
1

FIG. 9

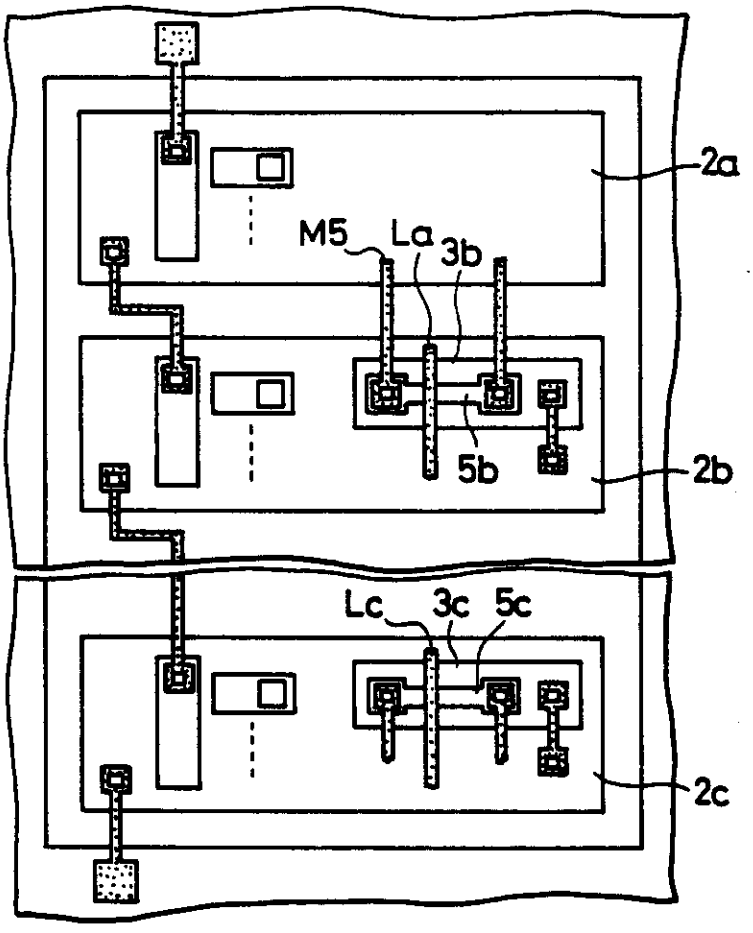
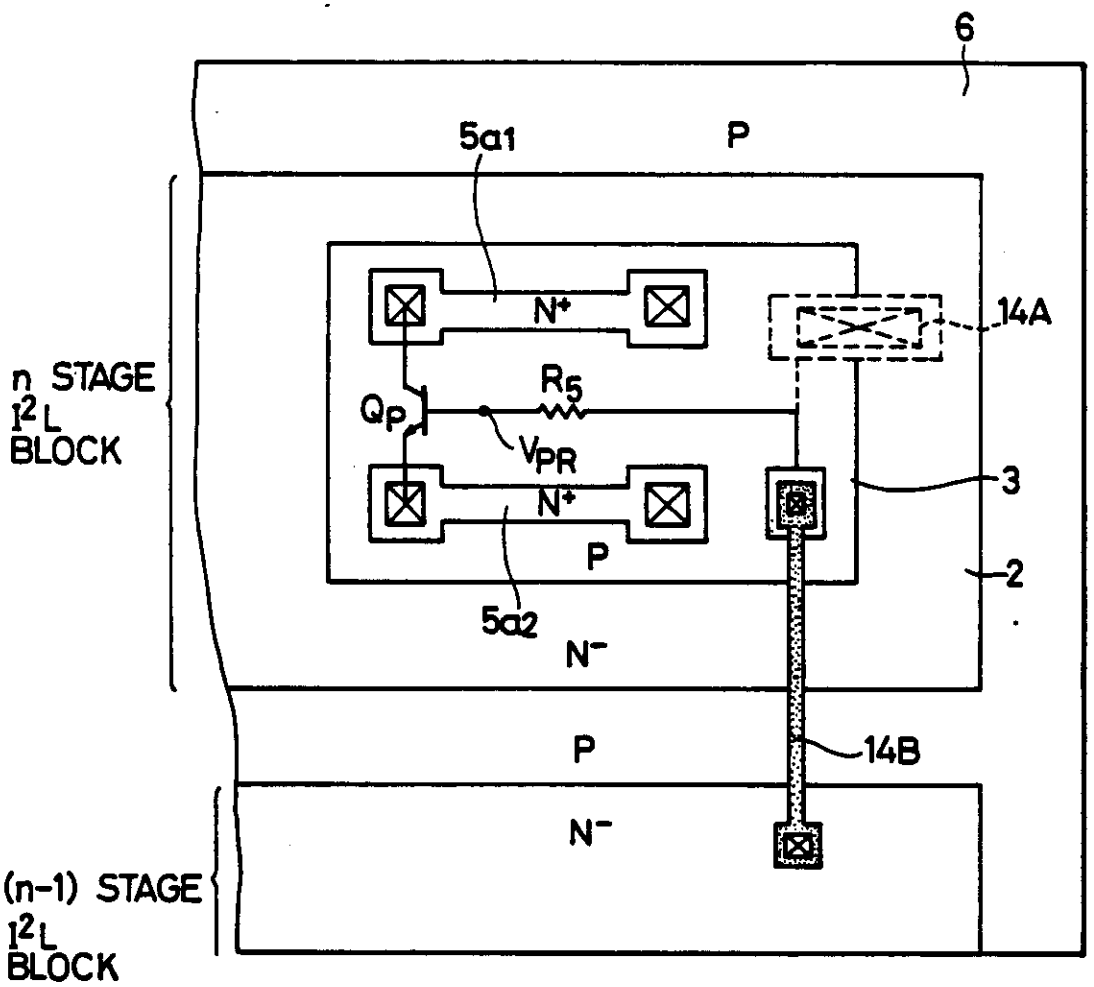


FIG. 10


6
5a1
P
N+
14A
n STAGE
I²L
BLOCK
R5
QP
VPR
N+
3
P
2
5a2
N⁻
P
14B
N⁻
(n-1) STAGE
I²L
BLOCK

An integrated injection logic semiconductor integrated circuit Device

The present invention relates to an integrated injection logic semiconductor integrated circuit device.

The number of gates in such devices increases with the increase in the range of uses to which they are put, and the consumption of electric power increases correspondingly.

An integrated injection logic (hereinafter referred to as I^2L) circuit construction which is called stacked I^2L has been employed in order to reduce the power consumption of I^2L circuits which have increased numbers of gates. The stacked I^2L construction consists of a plurality of I^2L blocks, each formed of a plurality of I^2L elements that provide a logic structure in an electrically isolated semiconductor region, the I^2L blocks being connected in series between a reference potential (earth potential) and a predetermined supply potential.

In order to increase the degree of freedom in the wiring layout of stacked I^2L devices and to increase the degree of integration, it is possible to attempt to form many cross-under wirings, which utilize a diffusion layer in the semiconductor.

We have previously proposed cross-under wirings of the construction shown in Figure 1 of the accompanying drawings for use in stacked I^2L devices. As shown in Figure 1, the cross-under wiring is formed by forming an N^+-type diffusion wiring layer 5, which crosses an aluminium wiring 4, on a portion of the surface of an N^--type epitaxial layer 2 on a P^--type silicon substrate 1, with an intermediate P-type diffusion layer 3. The reason for using the N^+-type diffusion wiring layer 5 as a cross-under wiring is because the N^+-type diffusion wiring layer 5 is formed simultaneously with the formation of the collector region (N^+-type diffusion layer) of the inverse transistor of an I^2L element, and because the N^+-type diffusion wiring layer 5 has an impurity concentration greater than that of the P-type diffusion layer 3 and, hence, has a low sheet resistance, lending itself well for being used as a cross-under wiring.

In stacked I^2L devices, it is accepted practice to electrically connect the I^2L blocks by under wirings, and to extend the wiring layer in a given I^2L block into other I^2L blocks by detour. With reference to Figure 2, N^--type epitaxial layers 2a, 2b and 2c electrically isolated by the p-type isolation layer 6 are used as I^2L blocks having quite different potentials from each other. For instance, in the case of a three-stage stacked I^2L IC shown in Figure 2, the N^--type epitaxial layer 2a has a potential V_{2a} = 1.4 volts, the N^--type epitaxial layer 2b has a potential V_{2b} = 0.7 volts, and the N^--type epitaxial layer 2c

has a potential V_{2c} = 0 volt. Therefore, when the N^+-type diffusion cross-under wiring layers 5a, 5b, 5c are formed in the N^--type epitaxial layers 2a,2b,2c, the N^+-type diffusion cross-under wiring layers being in contact with the wiring layers that electrically connect the I^2L blocks and being further in contact with the detouring wiring layers, there arises a problem with regard to potentials of the P-type diffusion layers 3a, 3b, 3c that are formed to provide PN junctions to electrically isolate the N^+-type diffusion cross-under wiring layers from the N^--type epitaxial layers 2a,2b,2c. The cause, it has been found, is that part of the cross-under wiring construction serves as a parasitic NPN transistor Q_p which is made up of N^+-type diffusion wiring layer 5, P-type diffusion layer 3 and N^--type epitaxial layer 2 as shown in Fig. 1. Here, it is supposed that the cross-under wiring construction of Fig. 1 exists in an I^2L block (a third stage block) in which the operational voltage ranges from 1.4 volts to 2.1 volts. That is, it is supposed that the cross-under wiring construction exists in the N^--type epitaxial layer 2a shown in Fig. 2 of the accompanying drawings. In Fig. 1, furthermore, the wiring layer M extends from the second stage I^2L block in which the operational voltage lies between 1.4 volts and 0.7 volts (i.e. extends from the I^2L

block that exists in the N^--type epitaxial layer 2b shown in Fig. 2) and connects to the N^+-type diffusion wiring layer 5. In the above-mentioned cross-under wiring construction, the P-type diffusion layer 3 has a potential of 1.4 volts, which is the same as the potential of the N^--type epitaxial layer 2. When the wiring layer M has a potential of 0.7 volts, therefore, a forward bias is applied to the PN junction J between the N^+-type diffusion layer 5 and the P-type diffusion layer 3, and the parasitic NPN transistor Qp operates.

Operation of such a parasitic NPN transistor becomes a problem in a portion where the wiring layer which extends from a low-potential driving I^2L block to a high-potential driving I^2L blcok, crosses under the diffusion layer in the high-potential driving I^2L block. The action of the parasitic NPN transistor makes it impossible to properly operate the inverse transistor of an I^2L element that is connected via the cross-under diffusion layer.

According to the present invention there is provided an integrated injection logic semiconductor integrated circuit device including :

(a) first, second and third semiconductor regions that are electrically isolated from each other;

(b) a first integrated injection logic block including a plurality of integrated injection logic elements formed in the first semiconductor region;

(c) a second integrated injection logic block including a plurality of integrated injection logic elements formed in the second semiconductor region;

(d) a third integrated injection logic block including a plurality of integrated injection logic elements formed in the third semiconductor region;

(e) first, second and third metal wiring layers formed in said first, second and third integrated injection logic blocks, respectively;

(f) a first cross-under semiconductor layer which crosses under and is electrically isolated from the first metal wiring layer formed in the first semiconductor region;

(g) a second cross-under semiconductor layer which crosses under and is electrically isolated from the second metal wiring layer formed in the second semiconductor region;

(h) a third cross-under semiconductor layer which crosses under and is electrically isolated from the third metal wiring layer formed in the third semiconductor region;

(i) a first semiconductor layer which has a conductivity type opposite to that of said first cross-under semiconductor layer, and which is located adjacent to said first cross-under semiconductor layer to electrically isolate said first cross-under semiconductor layer from said first semiconductor region;

(j) a second semiconductor layer which has a conductivity type opposite to that of said second cross-under semiconductor layer, and which is located adjacent to said second cross-under semiconductor layer to electrically isolate said second cross-under semiconductor layer from said second semiconductor region; and

(k) a third semiconductor layer which has a conductivity type opposite to that of said third cross-under semiconductor layer, and which is located adjacent to said third cross-under semiconductor layer to electrically isolate said third cross-under semiconductor layer from said third semiconductor region;

wherein said first, second and third semiconductor regions are provided with potentials set at levels which are different from each other, and wherein said first, second and third semiconductor layers are provided with potentials set at levels to prevent a forward bias from being applied across said first cross-under semiconductor layer and said first semiconductor layer, across said second cross-under semi-

conductor layer and said second semiconductor layer, or across said third cross-under semiconductor layer and said third semiconductor layer.

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying drawings, wherein :

Fig. 3 is a diagram of a stacked I^2L circuit to which the present invention can be applied;

Fig. 4 is a sectional view showing a cross-under wiring in an I^2L block;

Fig. 5 is a plan view of a stacked I^2L IC according to a first embodiment of the present invention;

Fig. 6 is a sectional view which corresponds to Fig. 5;

Fig. 7 is a plan view of a stacked I^2L IC according to a second embodiment of the present invention;

Fig. 8 is a sectional view showing a portion of the cross-under wiring of Fig.7;

Fig. 9 is a plan view of a stacked I^2L IC according to a third embodiment of the present invention; and

Fig. 10 is a plan view showing a portion of the cross-under wiring according to a further embodiment of the present invention.

Fig. 3 shows a portion of the stacked I^2L circuit, and illustrates I^2L blocks of the n-th stage, (n-1)th stage, and the first stage, as well as the manner in which they are interconnected. In Fig. 3, thick solid lines represent metal wiring layers for connecting I^2L elements within the I^2L blocks and for connecting the I^2L blocks. Resistors R_1,R_3 equivalently demonstrate cross-under wiring layers (diffusion layers) formed in a semiconductor integrated circuit device. A resistor R_2 has a resistance greater than those of the resistors R_1,R_3, works to shift the level and to properly operate the transistor Q of the (n-1)th stage, and further works as a cross-under wiring.

The I^2L block in each stage has been independently formed in an N^--type epitaxial semiconductor layer 2 which is electrically isolated from its counterparts by a P^--type semiconductor substrate 1 and a P-type isolation layer 6, as shown in Fig. 4. That is P-type semiconductor layers 7,8, and N^+-type semiconductor layers 9,10 are selectively formed in the isolated N^--type epitaxial semiconductor layer 2. The P-type semiconductor layer 7 serves as an injector region, i.e. serves as an emitter of a lateral PNP transistor, the N^--type epitaxial semiconductor layer 2 serves as a base of the transistor, and the P-type semiconductor layer 8 serves as a collector of the transistor. Moreover, the N^--type epitaxial semiconductor layer 2 serves as an emitter of an inverse NPN transistor, the P-type semiconductor layer 8 serves as a base of the

transistor, and the N^+-type semiconductor layer 9 serves as a collector of the transistor. Thus, an I^2L element (a circuit element having a logic function) is constructed. Therefore, a plurality of the thus constructed I^2L elements are formed in each of the epitaxial semiconductor layers that are isolated from each other, to constitute the individual I^2L blocks.

In Fig. 4, the N^+-type semiconductor layer 5 formed in the P-type semiconductor layer 3 serves as a diffusion resistance for shifting the level, which also serves as a cross-under wiring, as mentioned above, and forms a resistor R_2 as shown in Fig. 3.

In accordance with the present invention, the stacked I^2L circuit is formed in a semiconductor substrate as illustrated in the following embodiments.

Embodiment 1:

Fig. 5 illustrates a stacked I^2L IC in which the P-type layers 3a, 3b and 3c are connected to a minimum potential or to ground potential (GND) in order to isolate cross-under wiring layers (N^+-type layers) 5a, 5b and 5c from the N^--type epitaxial layers 2a, 2b and 2c.

The stacked I^2L IC of Fig. 5 consists of I^2L blocks in three stages. In this case, potentials of the N^--type epitaxial layers in the I^2L block of the n-th stage (third stage), I^2L block of the (n-1)th stage (second stage) and I^2L block of the first stage, are held at 1.4 volts, 0.7 volts and 0 volt, respectively. In each of the I^2L blocks

as will be obvious from Fig. 5, furthermore, potentials of the P-type layers 3a,3b,3c where cross-under wiring layers 5a,5b,5c are formed under the metal wiring layers (aluminum layers) La,Lb,Lc, are maintained at a minimum potential, i.e. maintained at ground potential (0 volt) being connected through wirings 11a,11b,11c. This makes it possible to prevent the parasitic transistor operation that will be established by the cross-under wiring layers (N^+-type layers) which have a high potential, the P-type layers and the N^--type epitaxial layers. That is, a metal wiring layer M_1 which extends from the I^2L block of the (n-1)th stage is connected to the cross-under wiring layer 5a. Accordingly, the cross-under wiring layer 5a has applied to it a potential (0.7 volts to 1.4 volts) which is higher than the potential (0 volt) of the P-type layer 3a. Therefore, a reverse bias is applied across the cross-under wiring layer 5a and the P-type layer 3a, and no parasitic transistor operation takes place at the position of the cross-under wiring layer 5a. Further, a metal wiring layer M_2 extending from the I^2L block of the n-th stage is connected to the cross-under wiring layer 5b. Therefore, the cross-under wiring layer 5b has applied to it a potential (1.4 volts to 2.1 volts) which is higher than the potential (0 volt) of the P-type layer 3b. Consequently, a reverse bias is applied across the cross-under wiring layer 5b and the P-type layer 3b, so that no parasitic transistor operation takes place at the position of the cross-under wiring layer

5b. Furthermore, a metal wiring layer M_3 in the I^2L block of the first stage is connected to a cross-under wiring layer 5c. Therefore, the cross-under wiring layer 5c has applied to it a potential (0.7 volts) which is equal to, or greater than, the potential (0 volt) of the P-type layer 3c. Accordingly, no forward bias is ever applied across the cross-under wiring layer 5c and the P-type layer 3c.

As mentioned above, no forward bias is applied across the cross-under wiring layers 5a,5b,5c and the P-type regions 3a,3b,3c, and, hence, no parasitic transistor operation takes place. Fig. 6 is a sectional view which schematically illustrates the wiring circuit of Fig. 5.

According to the above-mentioned embodiment, the P-type layers 3a,3b and 3c are maintained at ground potential in order to prevent the occurrence of parasitic transistor operation. Therefore, the number of metal wiring layers connected to the P-type layers increases, resulting in a decrease in the degree of integration of the semiconductor integrated circuit device.

In preventing the occurrence of parasitic transistor operation, it will be understood that the P-type layers in the I^2L blocks need not necessarily be maintained at a minimum voltage, provided the wiring layers extending from the low-potential driving I^2L blocks to the high-potential driving I^2L blocks, do not cross under the metal wiring layers in the high-potential driving I^2L blocks. The following embodiment is to realize a semiconductor

integrated circuit device which is constructed in a highly integrated form compared with the above-mentioned embodiment 1, by taking this point into consideration.

Embodiment 2:

Fig. 7 illustrates a stacked I^2L IC in which the P-type regions 3a,3b,3c where cross-under wiring layers (N^+-type layers) 5a,5b,5c of each of the blocks are formed, have potentials that are set to be equal to the potentials of the N^--type epitaxial layers 2a,2b,2c.

In Fig. 7, P-type layers 3a,3b,3c are electrically connected to the N^--type epitaxial layers 2a,2b,2c by metal wiring layers (aluminum layers) 12a,12b,12c, respectively. In practice, each of the metal wiring layers 12a,12b,12c is formed on an N^+-type layer 5' which electrically connects the N^--type epitaxial layer 2 to the P-type layer 3, like a metal wiring layer (electrode) 12 of Fig. 8, in which a metal wiring layer (aluminum layer) 4 formed on an SiO_2 film 13 traverses the cross-under wiring layer 5, and corresponds to the metal wiring layer La of Fig. 7. The metal wiring layer 4 (La) extends from the I^2L block (low-potential driving I^2L block) of the (n-1)th stage to the I^2L block (high-potential driving I^2L block) of the n-th stage, and does not use a cross-under wiring layer in the I^2L block of the n-th stage. The N^+-type layer 5 allows the wiring layer M_4 in the I^2L block of the n-th stage to cross under the metal wiring layer 4 (La).

Table 1 shows potentials V_{epi}, V_P and V_N of the

N^--type epitaxial layer, P-type layer and N^+-type layer in the cross-under wiring layers 5a,5b (diffusion resistors R_{11},R_2) of the stacked I^2L IC thus constructed.

TABLE 1

	R_{11}	R_2
Potential V_{epi} of N^--type epitaxial layer (fixed potential) in volts	$(n-1)\cdot V_F$	$(n-2)\cdot V_F$
Potential V_P of P-type layer (fixed potential) in volts	$(n-1)\cdot V_F$	$(n-2)\cdot V_F$
Potential V_N of cross-under wiring layer (variable potential) in volts	$(n-1)\cdot V_F$ to $n\cdot V_F$	$(n-1)\cdot V_F$ to $n\cdot V_F$

V_F: forward bias = 0.7 volts
n: number of stages

As will be obvious from Table 1, the potential of the P-type layer never becomes lower than the potential of the cross-under wiring layer. According to this embodiment, therefore, no parasitic transistor operation develops even when the potential of the P-type layer is changed from ground potential to the potential of the N^--type epitaxial

layer in which the P-type layer is formed. For instance, in the case of the stacked I^2L IC of three stages as shown in Fig. 7 the potential of the P-type layer 3a in which the cross-under wiring layer 5a (diffusion resistance R_{11}) is formed, is 1.4 volts which is equal to the potential of the N^--type epitaxial layer. On the other hand, the cross-under wiring layer 5a is provided with a potential of 1.4 volts to 2.1 volts. Therefore, forward bias is never applied across the cross-under wiring layer 5a and the P-type layer 3a. The potential of the P-type layer 3b in which the cross-under wiring layer 5b (diffusion resistance R_2) is formed, is 0.7 volts which is equal to the potential of the N^--type epitaxial layer. The cross-under wiring layer 5b, on the other hand, is connected to the metal wiring layer M_2 which extends from the I^2L block of the third stage, and is provided with a potential of 1.4 volts to 2.1 volts. Therefore, forward bias is never applied across the cross-under wiring layer 5b and the P-type layer 3b.

In the stacked I^2L IC of this embodiment, tne wiring regions can be greatly reduced compared with the stacked I^2L IC of the above-mentioned first embodiment. That is, since the potential of the P-type layer is set to be equal to the potential of the N^--type epitaxial layer in which the P-type region is formed, a long wiring for ground potential can be eliminated, and the shortest wiring is required to connect to the neighbouring N^--type epitaxial layer. To realize a semiconductor integrated circuit

device of a highly integrated form while preventing the occurrence of parasitic transistor operation, according to this embodiment, the wiring layer which extends from a low-potential driving I^2L block to a high-potential driving I^2L block should not use cross-under wiring, and the cross-under wiring layer should be connected to a metal wiring layer which accomplishes electrical connection within a single I^2L block only.

In the case of a wiring layer M_2 extending from a high-potential driving I^2L block to a low-potential driving I^2L block as will be obvious from the above-mentioned embodiments 1 and 2, no parasitic transistor operation takes place even when the cross-under wiring layer 5b is used. Below is mentioned an embodiment in which this technical idea is positively utilized.

Embodiment 3:

Fig. 9 illustrates a stacked I^2L IC in which the metal wiring layer M_5 of the high-potential driving I^2L block is allowed to run into a low-potential driving I^2L block in detour due to the requirement of wiring layout, and use is made of the cross-under wiring layer 5b.

In Fig. 9, potentials of the P-type layers 3b,3c in which cross-under wiring layers (diffusion resistances) 5b, 5c are formed, are set to be equal to the potentials of the N^--type epitaxial layers 2b,2c in which the P-type layers are formed. The potentials of the P-type layers 3b,3c may instead be maintained at a minimum potential (ground

potential).

The above stacked I^2L IC prevents the operation of a parasitic transistor that will be established by the N^--type epitaxial layer 2b, P-type layer 3b, and cross-under wiring layer (N^+-type layer) 5b, because of the same reasons as mentioned in the embodiment 2. In particular, the potentials of the N^--type expitaxial layer 2b and the P-type layer 3b do not become equal to the potential of the cross-under wiring layer 5b, but are necessarily smaller than the potential of the cross-under wiring layer 5b by at least a forward bias voltage level (0.7 volts), to provide increased margin. In this circuit, also, the wiring regions can be greatly reduced on account of the same reasons as mentioned in the second embodiment.

The stacked I^2L IC of the third embodiment can be modified as mentioned below.

(1) In Fig. 9, the cross-under wiring layer 5b contacting to the metal wiring layer M_5 may be formed in the I^2L block in which the cross-under wiring layer 5c has been formed.

In this case, the potential of the P-type layer 3c is lower than the potential of the P-type layer 3b, and the parasitic transistor does not operate.

(2) The cross-under wiring layer 5b may be formed in the N^--type epitaxial layer 2a (I^2L block of the n-th stage) instead of the N^--type epitaxial layer 2b (I^2L block of the (n-1)th stage), and the potential of the P-type

layer may be set to be equal to the potential of the N^--type epitaxial layer 2b (I^2L block of the (n-1)th stage) to isolate the cross-under wiring layer 5b from the N^--type epitaxial layer 2a.

In this case, the potential of the P-type layer is lower than the potential of the N^--type epitaxial layer 2a, and forward bias is not applied across the P-type layer and the N^--type epitaxial layer 2a. The cross-under wiring layer is provided with a potential higher than the potential of the P-type layer, and forward bias is not applied across the cross-under wiring layer and the P-type layer. It is therefore possible to prevent the occurrence of parasitic transistor operation.

When the potential of the P-type layer is set to be lower than the potential of the N^--type epitaxial layer, it is possible to form a plurality of cross-under wiring layers close to each other in the P-type layer. This point will be described below in detail.

Fig. 10 illustrates a portion of a stacked I^2L IC in which two cross-under wiring layers $5a_1$,$5a_2$ are formed close to each other in a P-type layer 3.

When the two cross-under wiring layers $5a_1$,$5a_2$ are formed close to each other in the P-type layer 3 as shown in Fig. 10, however, there arises the problem of a parasitic lateral transistor Qp made up of the two cross-under wiring layers (N^+-type layers) $5a_1$,$5a_2$, and the P-type layer 3. Namely, parasitic lateral transistor operation will develop

(case A), or will not develop (case B), depending upon the conditions.

Table 2 shows potentials of the cross-under wiring layers $5a_1$, $5a_2$, and of the P-type layer in these cases A and B.

TABLE 2

	Case A	Case B
Potential V_{N1} of first cross-under wiring layer $5a_1$ (varying potential) in volts	$(n-1)\cdot V_F$ to $n\cdot V_F$	$(n-1)\cdot V_F$
Potential V_P of P-type layer 3 (fixed potential) in volts	$(n-1)\cdot V_F$	$(n-2)\cdot V_F$
Potential V_{N2} of second cross-under wiring layer $5a_2$ (varying potential) in volts	$(n-1)\cdot V_F$ to $n\cdot V_F$	$(n-1)\cdot V_F$ to $n\cdot V_F$

The above-mentioned cases A and B will be described below in detail in connection with a three-stage stacked I^2L IC (n=3).

(1) Case A:

As shown in dotted lines in Fig. 10, the P-type layer

3 is connected to the N^--type epitaxial layer 2 through an electrode 14A, to maintain the potential of the P-type layer 3 at 1.4 volts. When the potential of the first cross-under wiring layer $5a_1$ is V_{N1} = 2.1 volts, and the potential of the second cross-under wiring layer $5a_2$ is V_{N2} = 1.4 volts, the potential of a portion of the P-type layer (base) 3 rises, so that the parasitic lateral transistor Qp will operate. This is because the P-type layer 3 has a low impurity concentration and, hence, has resistance R_5 which causes the potential V_{PR} of a portion of the P-type layer 3 to become greater than 1.4 volts. Therefore, a voltage greater than 0.7 volts is applied across the P-type layer (base) 3 and the second cross-under wiring layer (emitter) $5a_2$, so that the transistor Qp will operate. Further, when the first cross-under wiring layer $5a_1$ has a potential V_{N1} = 1.4 volts, and the second cross-under wiring layer $5a_2$ has a potential V_{N2} = 2.1 volts, the parasitic lateral transistor Qp will also operate. In this case, the first cross-under wiring layer $5a_1$ serves as an emitter, and the second cross-under wiring layer $5a_2$ serves as a collector.

(2) Case B:

As shown in bold lines in Fig. 10, the potential of the P-type layer 3 is set to be equal to the potential (0.7 volts) of the N^--type epitaxial layer in the I^2L block of the (n-1)th stage by a metal wiring layer 14B. That is, the potential of the P-type layer 3 is set to be lower than

the potential of the N^--type epitaxial layer 2.

When the first cross-under wiring layer $5a_1$ has a potential V_{N1} = 2.1 volts, and the second cross-under wiring layer $5a_2$ has a potential V_{N2} = 1.4 volts, the potential of a portion of the P-type layer (base) 3 rises as illustrated in the case A. However, since the potential of the rest of the P-type layer 3 remains at 0.4 volts, the potential V_{PR} at this portion of the P-type layer never rises about 1.4 volts. Therefore, the parasitic lateral transistor Qp does not operate.

When the potential of the P-type layer is set to be lower than the potential of the N^--type epitaxial layer as in the above-mentioned case B, the parasitic lateral transistor does not operate even when a plurality of cross-under wiring layers are formed in the P-type layer close to each other.

Therefore, in the case of a stacked I^2L which requires a plurality of cross-under wiring layers formed close to each other in the P-type layer, it is desired that the P-type layer is electrically connected to a lower potential, e.g. to the N^--type epitaxial layer in the I^2L block of the previous stage.

Attention is drawn to our copending application No. 83.01731, (Serial No. 2,113,915) from which this application has been divided.

CLAIMS:

1. An integrated injection logic semiconductor integrated circuit device including:

(a) first, second and third semiconductor regions that are electrically isolated from each other;

(b) a first integrated injection logic block including a plurality of integrated injection logic elements formed in the first semiconductor region;

(c) a second integrated injection logic block including a plurality of integrated injection logic elements formed in the second semiconductor region;

(d) a third integrated injection logic block including a plurality of integrated injection logic elements formed in the third semiconductor region;

(e) first, second and third metal wiring layers formed in said first, second and third integrated injection logic blocks, respectively;

(f) a first cross-under semiconductor layer which crosses under and is electrically isolated from the first metal wiring layer formed in the first semiconductor region;

(g) a second cross-under semiconductor layer which crosses under and is electrically isolated from the second metal wiring layer formed in the second semiconductor region;

(h) a third cross-under semiconductor layer which crosses under and is electrically isolated from the third metal wiring layer formed in the third semiconductor region;

(i) a first semiconductor layer which has a conductivity type opposite to that of said first cross-under semiconductor layer, and which is located adjacent to said first cross-under semiconductor layer to electrically isolate said first cross-under semiconductor layer from said first semiconductor region;

(j) a second semiconductor layer which has a conductivity type opposite to that of said second cross-under semiconductor layer, and which is located adjacent to said second cross-under semiconductor layer to electrically isolate said second cross-under semiconductor layer from said second semiconductor region; and

(k) a third semiconductor layer which has a conductivity type opposite to that of said third cross-under semiconductor layer, and which is located adjacent to said third cross-under semiconductor layer to electrically isolate said third cross-under semiconductor layer from said third semiconductor region;

wherein said first, second and third semiconductor regions are provided with potentials set at levels which are different from each other, and wherein said first, second and third semiconductor layers are provided with potentials set at levels to prevent a forward bias from being applied across said first cross-under semiconductor layer and said first semiconductor layer, across said second cross-under semi-

conductor layer and said second semiconductor layer, or across said third cross-under semiconductor layer and said third semiconductor layer.

2. An integrated injection logic semiconductor integrated circuit device according to claim 1, wherein the potential of said second semiconductor region is maintained higher than the potential of said first semiconductor region, and the potential of said third semiconductor region is maintained higher than the potential of said second semiconductor region.

3. An integrated injection logic semiconductor integrated circuit device according to claim 2, wherein the potentials of said first, second and third semiconductor layers are maintained equal to the potential of said first semiconductor region.

4. An integrated injection logic semiconductor integrated circuit device according to claim 2, wherein said first, second and third semiconductor layers are electrically connected to said first, second and third semiconductor regions, respectively.

5. An integrated injection logic semiconductor integrated circuit device according to claim 2, wherein said third semiconductor layer is electrically connected to said second semiconductor region.

6. An integrated injection logic semiconductor integrated circuit device according to claim 5, wherein a fourth cross-under semiconductor layer having the conductivity type same as that of said third cross-under semiconductor layer, is formed in said third semiconductor layer close to said third cross-under semiconductor layer.

7. An integrated injection logic semiconductor integrated circuit device according to any one of the preceding claims 2 to 6, wherein said third metal wiring layer is electrically connected to an integrated injection logic element in the second integrated injection logic block.

Publication No.
2133622 A dated 25 July 1984

Patent Granted:
EFFECT FROM SECTION 25(1) 20 NOV 1985

Application No.
~~8014880~~ filed on 21 January 1983
8403188

Priority claimed:
25 January 1982 in Japan doc: 57/008932

Title:
An integrated injection logic semiconductor integrated circuit device

Applicant:
Hitachi Ltd (Japan), 6 Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo, Japan.

Inventors:
Setsuo Ogura, 1421-D202 Kaminakai-cho, Takasaki-shi, Gunma, Japan.

Shizuo Kondoh, 1421-C303 Kaminakai-cho, Takasaki-shi, Gunma, Japan.

Classified to:
H1K

Examination requested 8 February 1984

Address for Service:
Newburn Ellis & Co, 2/3 Cursitor Street, London EC4A 1BQ.

Printed by the Patent Office at St. Mary Cray, 08 JUN 84