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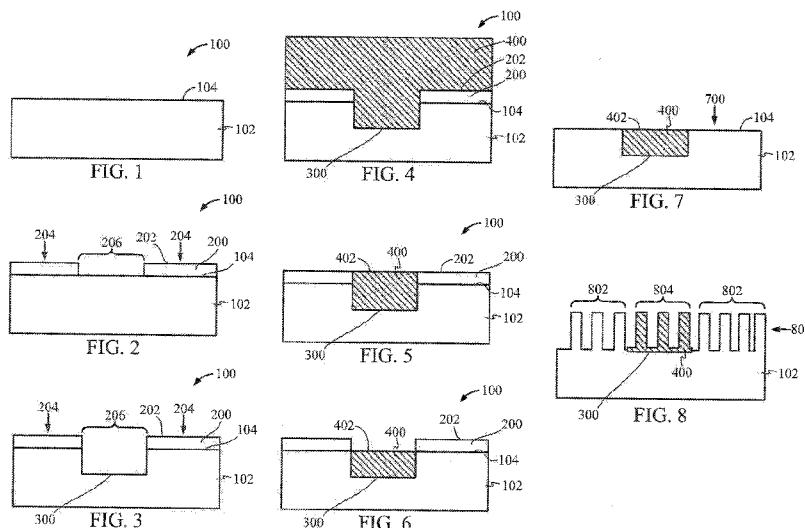
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(54) Title: METHOD OF FORMING FINS FROM DIFFERENT MATERIALS ON A SUBSTRATE



(57) Abstract: A method of forming fins of different materials includes providing a substrate with a layer of a first material having a top surface, masking a first portion of the substrate leaving a second portion of the substrate exposed, etching a first opening at the second portion, forming a body of a second material in the opening to a level of the top surface of the layer of the first material, removing the mask, and forming fins of the first material at the first portion and forming fins of the second material at the second portion. A finFET device having fins formed of at least two different materials is also disclosed.

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METHOD OF FORMING FINS FROM DIFFERENT MATERIALS ON A SUBSTRATE

Field of the Disclosure

[0001] The present disclosure is directed to a method of forming fins from different materials on a substrate and to a substrate having fins formed from different materials and, more specifically, toward a method of forming fins on a multi-layer substrate wherein some of the fins are formed from the material of a first layer of the substrate and some of the fins are formed from a material of a second layer of the substrate and toward a substrate having such fins.

Background

[0002] FinFET devices include a plurality of fins that may be used to form channels of a finFET transistor. It is sometimes desirable to form the fins from different materials. For example, it may be desirable to form some fins from a Group III – Group V material, indium arsenide or indium gallium arsenide, for example, another group of fins from germanium and, optionally, a third group of silicon fins. In order to form fins from different materials, it has heretofore been necessary to form an appropriate buffer layer for the particular layer of fin material on a layer of silicon to provide a suitable substrate on which to grow a given type of material. This is relatively easy when fins are all formed from the same material. However, forming fins from two or three different materials requires two or three buffer layers, and this complicates the substrate manufacturing process. It would therefore be desirable to produce fins from different materials in an efficient manner.

SUMMARY

[0003] An exemplary embodiment includes a method of forming fins of different materials. The method includes providing a substrate comprising a layer of a first material having a top surface, masking a first portion of the substrate to form a mask while leaving a second portion of the substrate exposed, and etching a first opening at the second portion. The method also includes forming a body of a second material in the opening to a level of the top surface of the layer of the first material, removing the mask and forming fins of the first material at the first portion and forming fins of the second material at the second portion.

[0004] Another embodiment includes a finFET device having fins formed of at least two different materials. The device comprises a substrate having a first layer having a top surface and a first oxide layer on the first layer top surface. The first oxide layer has a top surface, and the first oxide layer covers a first portion of the first layer and does not cover a second portion of the first layer. A first body of material is formed at the second portion of the first layer, and the first body of material has a top surface even with the top surface of the first oxide layer. A first set of fins is formed of a first material on the first oxide layer, and a second set of fins formed of a second material is formed on the first body of material.

[0005] An additional embodiment includes a method of forming fins of different materials. The method includes providing a substrate comprising a layer of a first material, a first oxide layer on the layer of the first material, a layer of a second material on the first oxide layer, and a second oxide layer on the layer of the second material. The substrate also includes a layer of a third material on the second oxide layer, and the layer of the third material has a top surface that forms a top surface of the substrate. The method also includes etching a first opening at a first location on the substrate through the layer of the third material and through the second oxide layer to the layer of the second material and forming a body of the second material in the first opening to a level of the top surface of the substrate. The method also includes etching a second opening at a second location on the substrate through the layer of the third material, the second oxide layer, the layer of the second material and the first oxide layer to the layer of the first material and forming a body of the first material in the second opening to a level of the top surface of the substrate. In addition, the method includes forming first fins comprising the second material at the first location, forming second fins comprising the first material at the second location and forming third fins comprising the third material at a third location.

[0006] Another embodiment includes a method of forming fins of different materials. The method includes steps for providing a substrate comprising a layer of a first material having a top surface, steps for masking a first portion of the substrate to form a mask while leaving a second portion of the substrate exposed, and steps for etching a first opening at the second portion. The method also includes steps for forming a body of a second material in the opening to a level of the top surface of the layer of the first material, steps for removing the mask, and steps for forming fins of the first material at

the first portion and forming fins of the second material at the second portion.

[0007] An additional embodiment includes a finFET device having fins formed of at least two different materials. The device comprises a substrate having a first layer having a top surface and a first oxide layer on the first layer top surface, the first oxide layer having a top surface. The first oxide layer covers a first portion of the first layer and does not cover a second portion of the first layer. A first body of material is formed at the second portion of the first layer, the first body of material having a top surface even with the top surface of the first oxide layer. First fin means for forming a first portion of a semiconductor device are provided, and second fin means for forming a second portion of a semiconductor device are provided.

[0008] Another embodiment includes a method of forming fins of different materials. The method includes steps for providing a substrate comprising a layer of a first material, a first oxide layer on the layer of the first material, a layer of a second material on the first oxide layer, a second oxide layer on the layer of the second material and a layer of a third material on the second oxide layer. The layer of the third material has a top surface forming a top surface of the substrate. The method also includes steps for etching a first opening at a first location on the substrate through the layer of the third material and through the second oxide layer to the layer of the second material and steps for forming a body of the second material in the first opening to a level of the top surface of the substrate. The method also includes steps for etching a second opening at a second location on the substrate through the layer of the third material, the second oxide layer, the layer of the second material and the first oxide layer to the layer of the first material and steps for forming a body of the first material in the second opening to a level of the top surface of the substrate. In addition, the method includes steps for forming first fins comprising the second material at the first location, steps for forming second fins comprising the first material at the second location and steps for forming third fins comprising the third material at a third location.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying drawings are presented to aid in the description of embodiments of the invention and are provided solely for illustration of the embodiments and not limitation thereof.

[0010] FIGS. 1-8 are elevational views schematically showing a wafer during different

processing stages according to a first embodiment.

- [0011] FIGS. 9-15 are elevational views schematically showing a wafer during processing stages according to a second embodiment.
- [0012] FIGS. 16-23 are elevational views schematically showing a wafer during processing stages according to a third embodiment.
- [0013] FIGS. 24-31 are elevational views schematically showing a wafer during processing stages according to a fourth embodiment.
- [0014] FIGS. 32-45 are elevational views schematically showing a wafer during processing stages according to a fifth embodiment.
- [0015] FIGS. 46-52 are elevational views schematically showing a wafer during processing stages according to a sixth embodiment.
- [0016] FIG. 53 is a flowchart illustrating a method according to an embodiment.
- [0017] FIG. 54 is a flowchart illustrating a method according to another embodiment.
- [0018] FIG. 55 is a schematic diagram of an exemplary wireless communication system in which embodiments of the disclosure may be used.

DETAILED DESCRIPTION

- [0019] Aspects of the invention are disclosed in the following description and related drawings directed to specific embodiments of the invention. Alternate embodiments may be devised without departing from the scope of the invention. Additionally, well-known elements of the invention will not be described in detail or will be omitted so as not to obscure the relevant details of the invention.
- [0020] The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any embodiment described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments. Likewise, the term “embodiments of the invention” does not require that all embodiments of the invention include the discussed feature, advantage or mode of operation.
- [0021] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of embodiments of the invention. As used herein, the singular forms “a”, “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises”, “comprising”, “includes”, and/or “including”, when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or

components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0022] Further, many embodiments are described in terms of sequences of actions to be performed by, for example, elements of a computing device. It will be recognized that various actions described herein can be performed by specific circuits (e.g., application specific integrated circuits (ASICs)), by program instructions being executed by one or more processors, or by a combination of both. Additionally, these sequence of actions described herein can be considered to be embodied entirely within any form of computer readable storage medium having stored therein a corresponding set of computer instructions that upon execution would cause an associated processor to perform the functionality described herein. Thus, the various aspects of the invention may be embodied in a number of different forms, all of which have been contemplated to be within the scope of the claimed subject matter. In addition, for each of the embodiments described herein, the corresponding form of any such embodiments may be described herein as, for example, “logic configured to” perform the described action.

[0023] FIG. 1 is a substrate 100 comprising a silicon layer 102 having a top surface 104. In FIG. 2, a nitride hardmask 200 having a top surface 202 has been applied to a first portion 204 of the substrate 100 leaving a second portion 206 of the substrate 100 unmasked. In FIG. 3, an etching process has formed an opening 300 in the substrate 100 at the unmasked second portion 206 of the substrate. FIG. 4 shows a silicon-germanium (“SiGe”) layer 400 that is grown or otherwise formed on the substrate 100 in the opening 300 and over the top surface 202 of the nitride hardmask 200. Beneficially, SiGe can be grown directly on silicon without forming a separate buffer layer. In FIG. 5, the SiGe layer 400 has been chemically and/or mechanically removed down to the level of the top surface 202 of the nitride hardmask 200. Oxidizing SiGe causes it to condense, and multiple oxidation processes reduce the height of the SiGe layer 400 until a top surface 402 of the SiGe layer 400 is even with the top surface 104 of the silicon layer 102, as illustrated in FIG. 6, and the nitride hardmask 200 is removed as shown in FIG. 7. The result is a structure 700 comprising the silicon layer 102 with the body 400 of SiGe contained therein. A plurality of fins 800 are formed in the structure 700 in a conventional manner as illustrated in FIG. 8. A first subset 802 of the fins are formed of the silicon layer 102, and a second subset 804 of the fins are formed from the body 400 of SiGe. A finFET device (not illustrated) can be formed, on

a semiconductor die, for example, from the device of FIG. 8, which finFET device will have some fins formed of silicon and other fins formed of germanium.

[0024] A process according to a second embodiment is illustrated in FIGS 9-15. FIG. 9 illustrates a substrate 900 that includes a silicon layer 902 having a top surface 904, a bottom oxide layer 906 on the top surface 904 of the silicon layer 902 and a top layer 908 formed of a Group III-V material such as indium arsenide or indium gallium arsenide which substrate 900 may be referred to generally as a “Group III-V on insulator.” The top layer 908 has a top surface 910. In FIG. 10, a nitride hardmask 1000 having a top surface 1002 is applied to a first portion 1004 the top surface 910 of the top layer 908 leaving a second portion 1006 of the top layer 908 exposed. As illustrated in FIG. 11, the top layer 908 and the bottom oxide layer 906 are etched to form an opening 1100 down to the level of the top surface 904 of the silicon layer 902. In FIG. 12, a SiGe layer 1200 is grown or otherwise formed in the opening 1100 and on the top surface 1002 of the nitride hardmask 1000. As in the first embodiment, the SiGe layer 1200 can be grown directly on the silicon layer 902 without the use of a buffer layer. The SiGe layer 1200 is mechanically and/or chemically modified to remove the portions thereof that are not in or over the opening 1100, and the SiGe layer 1200 is thereafter oxidized to reduce its thickness to the level of the top surface 910 of the top layer 908 as illustrated in FIG. 13. The nitride hardmask 1000 is removed as shown in FIG. 14 leaving a substrate 1400 comprising the top layer 908 of Group III-V material with a body 1200 of SiGe in the top layer 908. In FIG. 15, fins 1500 are formed from the substrate 1400 including a first subset of fins 1502 formed from the Group III-V material and a second subset of fins 1504 formed from SiGe. A finFET device (not illustrated) can be formed from the device of FIG. 15, which finFET device will have some fins formed of the Group III-V material and other fins formed of SiGe.

[0025] A process according to a third embodiment is illustrated in FIGS 16-23. In FIG. 16, a substrate 1600 is provided that includes a germanium bottom layer 1602 having a top surface 1604 and an oxide layer 1606 on the top surface 1604 of the bottom layer 1602. A Group III-V top layer 1608 is formed on the oxide layer 1606 and has a top surface 1610. In FIG. 17, a nitride hardmask 1700 having a top surface 1702 is applied to a first portion 1704 of the top layer 1608 leaving a second portion 1706 exposed. In FIG. 18, the top layer 1608 and the oxide layer 1606 are etched down to the top surface 1604 of the germanium bottom layer 1602 to form an opening 1800. FIG. 19 shows a body

1900 of germanium non-selectively epitaxially deposited in the opening 1800 and over the top surface 1702 of the nitride hardmask 1700. Because the bottom layer 1602 and the body 1900 are both germanium, it is not necessary to use SiGe and, instead, the germanium of the body 1900 can be grown directly on the top surface 1604 of the bottom layer 1602. FIG. 20 illustrates a substrate 2000 after a chemical mechanical polishing process has removed the portion of the body 1900 of germanium that was outside the opening 1800, and in FIG. 21, the body 1900 of germanium in the opening 1800 is oxidized and etched to reduce its thickness to a level of the top surface 1610 of the top layer 1608. The nitride hardmask 1700 is removed in FIG. 22 to produce a substrate 2200 having a body 1900 of germanium surrounded by the Group III-V material of the top layer 1608. This substrate 2200 is processed to form fins 2300 in FIG. 23, a first subset 2302 of which are formed of the Group III-V material and a second subset 2304 of which are formed of germanium from the body 1900. A finFET device (not illustrated) can be formed from the device of FIG. 23, which finFET device will have some fins formed of the Group III-V material and other fins formed of germanium.

[0026] A process according to a fourth embodiment is illustrated in FIGS. 24-31. FIG. 24 illustrates a substrate 2400 having a silicon layer 2402 having a top surface 2404, a first oxide layer 2406, a germanium layer 2408 having a top surface 2410 on the first oxide layer 2406, a second oxide layer 2412 on the top surface 2410, and a Group III-V top layer 2414 having a top surface 2416. In FIG. 25, a nitride hardmask 2500 having a top surface 2502 is applied to a first portion 2504 of the top layer 2414 leaving a second portion 2506 of the top layer 2414 exposed. In FIG. 26, the top layer 2414 and the second oxide layer 2412 are etched at the second portion 2506 down to the top surface 2410 of the germanium layer 2408 to form an opening 2600. As shown in FIG. 27, a body 2700 of germanium is grown in the opening 2600 which extends out of the opening 2600 and onto the top surface 2502 of the nitride hardmask 2500. Because the body 2700 of germanium is grown on a germanium layer 2408, a separate buffer layer is not required. Thereafter, as illustrated in FIG. 28, the portion of body 2700 on the top surface 2502 of the nitride hardmask 2500 is chemically and/or mechanically removed, and, in FIG. 29, the body 2700 of germanium is oxidized and etched to reduce its thickness to the level of the top surface 2416 of the top layer 2414. In FIG. 30 the nitride hardmask 2500 is removed leaving a substrate 3000 comprising the top layer

2414 of the Group III-V material with a germanium body 2700 therein. The substrate 3000 is processed in a conventional manner to form fins 3100 illustrated in FIG 31, a first subset 3102 of which are formed of the Group III-V material and a second subset 3104 of which are formed of germanium from the body 2700 of germanium. A finFET device (not illustrated) can be formed from the device of FIG. 31, which finFET device will have some fins formed of the Group III-V material and other fins formed of germanium.

[0027] From the foregoing description, it will be appreciated that the embodiment of FIGS. 24-31 are somewhat similar to the embodiment of FIGS. 16-23. However, providing a silicon substrate 2400 for the germanium layer 2408 allows the substrate to be handled with conventional equipment for processing silicon while still providing a germanium layer 2408 on which to grow the germanium body 2700. The substrate 1600 of FIGS. 16-23 can be used to form fins in a manner similar to the method of FIGS 24-31 but, because it includes a germanium bottom layer 1602, the substrate 1600 must be processed by equipment specifically configured to handle germanium, which material is typically more fragile than silicon and more difficult to handle.

[0028] FIGS. 32-45 illustrate a process according to a fifth embodiment, in which fins of three different materials are formed on a substrate. FIG. 32 illustrates a substrate 3200 having a silicon layer 3202 having a top surface 3204, a first oxide layer 3206, a germanium layer 3208 having a top surface 3210 on the first oxide layer 3206, a second oxide layer 3212 on the top surface 3210, and a Group III-V top layer 3214 having a top surface 3216. In FIG. 33, a nitride hardmask 3300 having a top surface 3302 is applied to a first portion 3304 of the top layer 3214 leaving a second portion 3306 of the top layer 3214 exposed. In FIG. 34, the top layer 3214 and the second oxide layer 3212 are etched at the second portion 3306 down to the top surface 3210 of the germanium layer 3208 to form an opening 3400. FIG. 35 illustrates a body 3500 of germanium grown in the opening 3400 which extends out of the opening 3400 and onto the top surface 3302 of the nitride hardmask 3300. Because the body 3500 of germanium is grown on a germanium layer 3208, a separate buffer layer is not required. Thereafter, as illustrated in FIG. 36, the portion of body 3500 on the top surface 3302 of the nitride hardmask 3300 is chemically and/or mechanically removed, and, in FIG. 37 the body 3500 of germanium is oxidized and etched to reduce its thickness to the level of the top surface 3216 of the top layer 3214. In FIG. 38 the nitride hardmask 3300 is removed leaving a

substrate comprising the top layer 3214 of the Group III-V material with a germanium body 3500 therein, the substrate having a top surface comprising the top of the top layer 3214 of Group III-V material.

[0029] To this point, the process of the fifth embodiment is similar to the process of the fourth embodiment. However, after the substrate having a germanium body 3500 therein is formed, in the present embodiment, as illustrated in FIG. 39, a second nitride hard mask 3900 having a top surface 3902 is formed on the top surface 3802 of the substrate leaving a third portion 3904 at a location spaced from the second portion 3306 exposed. As illustrated in FIG. 40, the top layer 3214, the second oxide layer 3212, the germanium layer 3208 and the first oxide layer 3206 are etched to form an opening 4000 that extends to the top surface 3204 of the silicon layer 3202, and in FIG. 41, a body of silicon 4100 is formed on the top surface 3204 of the silicon layer 3202 which fills the opening 4000 and covers the top surface 3902 of the nitride hardmask 3900. The body of silicon 4100 is chemically and/or mechanically removed from the top surface 3902 of the nitride hardmask and oxidized, as illustrated in FIG. 43, until it is at the level of the top surface 3216 of the top layer 3214. The second nitride hardmask 3900 is removed, as illustrated in FIG. 44, leaving a substrate 4400 having a first region 3500 of germanium and a second region 4100 of silicon in the top layer 3214 of Group III-V material. This substrate 4400 is processed in a conventional manner to form a plurality of fins 4500, illustrated in FIG. 45. A first subset 4502 of the fins 4500 comprise the Group III-V material, a second subset 4504 of the fins 4500 comprise germanium from the germanium body 3500, and a third subset 4506 of the fins 4500 comprise silicon from the second region 4100 of silicon. Growing the germanium on the existing germanium layer 3208 and growing the silicon on the silicon layer 3202 allows the formation of three different types of fins for use in a finFET (not illustrated) without the need to form a buffer layer for each of the different materials.

[0030] FIGS. 46-51 illustrate a method according to a sixth embodiment. In this embodiment, with reference to FIG. 46, a silicon substrate 4600 has a silicon layer 4602 having a top surface 4604, a first oxide layer 4606 on the top surface 4604, a germanium layer 4608 on the first oxide layer 4606 and having a top surface 4610, a second oxide layer 4612 on the top surface 4610 of the germanium layer 4608. A top layer 4614 comprising a Group III-V material and having a top surface 4616 is formed on the second oxide layer 4612. A nitride hardmask 4618 having a top surface 4620 is formed on the top surface

4616 of the top layer 4614. This structure is generally similar to the structure of FIG. 33. However, in the previous embodiment, a location for forming fins of silicon was determined independently of the location for forming fins of germanium. The present embodiment allows more precise control of the relative locations of these two sets of fins. To this end, a top mask layer 4622 is applied to the top surface 4620 of the nitride hardmask 4618 with a first opening 4624 at a location for forming germanium fins and a second opening 4626 at a location for forming silicon fins, and, as illustrated in FIG. 47, a first opening 4700 is etched in the nitride hardmask 4618 at the first opening 4624, and a second opening 4702 is etched in the nitride hardmask 4618 at the second opening 4626. In FIG. 48, the first opening is filled with a shield body of material 4800, a bottom anti-reflective material (BARC) or a photoresist or organic carbon containing film, for example, which could be formed by spin coating followed by a lithographic and development process. Alternately, the body of material 4800 could comprise carbon-doped SiO_x and be deposited by a plasma enhanced chemical vapor deposition (PECVD) process followed by lithographic process and etch. At the second opening 4626 the substrate 4600 is etched through the top layer 4614, the second oxide layer 4612, the germanium layer 4608 and the first oxide layer 4606 to the silicon layer 4602, forming an opening 4802. In FIG. 49, a body 4900 of silicon is grown in the opening 4802 up to the top mask layer 4622. Subsequently, as illustrated in FIG. 50, the shield body of material 4800 is removed, and an opening 5002 is formed at the first opening 4624 of the top mask layer 4622. At this additional opening 5002, the top layer 4614 and second oxide layer 4612 are etched to the level of the germanium layer 4608, and, as illustrated in FIG. 51, a body 5102 of germanium is grown in the opening 5002 up to the top mask layer 4622. The top mask layer 4622 and the nitride hardmask 4618 are then removed to leave a substrate 5200 having a germanium body 5102 and a silicon body 4900 each surrounded by the top layer 4614 formed of the Group III-V material, which substrate can be formed into a substrate having three different types of fins substantially as shown in FIG. 45.

[0031] A method according to an embodiment is illustrated in FIG. 53 and includes a block 5300 of providing a substrate comprising a layer of a first material having a top surface, a block 5302 of masking a first portion of the substrate leaving a second portion of the substrate exposed, a block 5304 of etching a first opening at the second portion, a block 5306 of forming a body of a second material in the opening to a level of the top surface

of the layer of the first material, a block 5308 of removing the mask and a block 5310 of forming fins of the first material at the first portion and forming fins of the second material at the second portion.

Another method according to an embodiment is illustrated in FIG. 54 and includes a block 5400 of providing a substrate comprising a layer of a first material, a first oxide layer on the layer of the first material, a layer of a second material on the first oxide layer, a second oxide layer on the layer of the second material and a layer of a third material on the second oxide layer, the layer of the third material having a top surface forming a top surface of the substrate. The method also includes a block 5402 of etching a first opening at a first location on the substrate through the layer of the third material and through the second oxide layer to the layer of the second material, a block 5404 of forming a body of the second material in the first opening to a level of the top surface of the substrate, a block 5406 of etching a second opening at a second location on the substrate through the layer of the third material, the second oxide layer, the layer of the second material and the first oxide layer to the layer of the first material, a block 5408 of forming a body of the first material in the second opening to a level of the top surface of the substrate and a block 5410 of forming first fins comprising the second material at the first location, forming second fins comprising the first material at the second location and forming third fins comprising the third material at a third location.

- [0032] Figure 55 illustrates an exemplary wireless communication system 5500 in which one or more embodiments of the disclosure may be advantageously employed. For purposes of illustration, Figure 55 shows three remote units 5520, 5530, and 5550 and two base stations 5540. It will be recognized that conventional wireless communication systems may have many more remote units and base stations. The remote units 5520, 5530, and 5550 include integrated circuit or other semiconductor devices 5525, 5535 and 5555 (including finFET's having fins of different materials as disclosed herein), which are among embodiments of the disclosure as discussed further below. Figure 55 shows forward link signals 5580 from the base stations 5540 and the remote units 5520, 5530, and 5550 and reverse link signals 5590 from the remote units 5520, 5530, and 5550 to the base stations 5540.
- [0033] In Figure 55, the remote unit 5520 is shown as a mobile telephone, the remote unit 5530 is shown as a portable computer, and the remote unit 5550 is shown as a fixed location remote unit in a wireless local loop system. For example, the remote units may be any

one or combination of a mobile phone, hand-held personal communication system (PCS) unit, portable data unit such as a personal data or digital assistant (PDA), navigation device (such as GPS enabled devices), set top box, music player, video player, entertainment unit, fixed location data unit such as meter reading equipment, or any other device that stores or retrieves data or computer instructions, or any combination thereof. Although Figure 55 illustrates remote units according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. Embodiments of the disclosure may be suitably employed in any device having active integrated circuitry including memory and on-chip circuitry for test and characterization.

- [0034] Further, those of skill in the art will appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.
- [0035] The methods, sequences and/or algorithms described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor.
- [0036] Accordingly, an embodiment of the invention can include a computer readable media embodying a method for forming a substrate having fins of different materials. Accordingly, the invention is not limited to illustrated examples and any means for

performing the functionality described herein are included in embodiments of the invention.

[0037] While the foregoing disclosure shows illustrative embodiments of the invention, it should be noted that various changes and modifications could be made herein without departing from the scope of the invention as defined by the appended claims. The functions, steps and/or actions of the method claims in accordance with the embodiments of the invention described herein need not be performed in any particular order. Furthermore, although elements of the invention may be described or claimed in the singular, the plural is contemplated unless limitation to the singular is explicitly stated.

CLAIMS**WHAT IS CLAIMED IS:**

1. A method of forming fins of different materials comprising:
providing a substrate comprising a layer of a first material having a top surface;
masking a first portion of the substrate to form a mask leaving a second portion of the substrate exposed;
etching a first opening at the second portion;
forming a body of a second material in the first opening to a level of the top surface of the layer of the first material;
removing the mask; and
forming fins of the first material at the first portion and forming fins of the second material at the second portion.
2. The method of claim 1, wherein the first material is silicon.
3. The method of claim 1, wherein the first material is a Group III-V material.
4. The method of claim 3, wherein the second material is germanium.
5. The method of claim 3, wherein the second material is silicon germanium.
6. The method of claim 3, wherein the substrate comprises a layer of the second material and a layer of a first oxide on the layer of the second material, the layer of the first material being located on the layer of the first oxide and wherein etching a first opening at the second portion comprises etching a first opening through the layer of the first material and the layer of the first oxide to the layer of the second material.
7. The method of claim 3, wherein the substrate comprises a layer of a third material and a layer of a first oxide on the layer of the third material, the layer of the first material being located on the layer of the first oxide and wherein etching a first

opening at the second portion comprises etching a first opening through the layer of the first material and the layer of the first oxide to the layer of the third material.

8. The method of claim 7, wherein the third material is silicon and the second material is silicon-germanium.

9. The method of claim 1, wherein the substrate comprises a layer of a third material, a first oxide layer on the layer of the third material, a layer of the second material on the first oxide layer, and a second oxide layer on the layer of the second material and wherein the layer of the first material is located on the second oxide layer and wherein etching a first opening at the second portion comprises etching a first opening through the layer of the first material and the second oxide layer to the layer of the second material.

10. The method of claim 9, including etching a second opening at a third portion of the substrate through the layer of the first material, the second oxide layer, the layer of the second material and the first oxide layer to the layer of the third material and forming a body of the third material in the second opening to a level of the top surface of the layer of the first material and forming fins of the third material at the third portion.

11. The method of claim 9, wherein masking a first portion of the substrate includes leaving a third portion of the substrate exposed and including etching a second opening at the third portion of the substrate through the layer of the first material, the second oxide layer, the layer of the second material and the first oxide layer to the layer of the third material and forming a body of the third material in the second opening to a level of the top surface of the layer of the first material and forming fins of the third material at the third portion.

12. A finFET device having fins formed of at least two different materials comprising:

a substrate having a first layer having a top surface;

a first oxide layer on the first layer top surface, the first oxide layer having a top

surface, the first oxide layer covering a first portion of the first layer and not covering a second portion of the first layer;

a first body of material at the second portion of the first layer, the first body of material having a top surface even with the top surface of the first oxide layer;

a first set of fins formed of a first material on the first oxide layer; and

a second set of fins formed of a second material on the first body of material.

13. The FinFET device of claim 12, wherein the first layer comprises the second material.

14. The finFET device of claim 12, wherein the substrate comprises a third material different than the first material and the second material.

15. The finFET device of claim 14, wherein the second material comprises germanium.

16. The finFET device of claim 14, wherein the substrate comprises a second layer and a second oxide layer on the second layer, wherein the first layer is located on the second oxide layer, and including a second body of material extending from the second layer through the second oxide layer, the first layer and the first oxide layer, the second body of material having a top surface even with the top surface of the first oxide layer, the second body of material and the second layer being formed of a third material, and a third set of fins formed of the third material on the second body of material.

17. The finFET device of claim 16, wherein the second material comprises germanium and the third material comprises silicon.

18. The finFET device of claim 12 integrated into at least one semiconductor die.

19. A device, selected from a group consisting of a set top box, music player, video player, entertainment unit, navigation device, communications device, personal digital assistant (PDA), fixed location data unit, and a computer, into which the finFET

device of claim 12 is integrated.

20. A method of forming fins of different materials comprising:

providing a substrate comprising a layer of a first material, a first oxide layer on the layer of the first material, a layer of a second material on the first oxide layer, a second oxide layer on the layer of the second material and a layer of a third material on the second oxide layer, the layer of the third material having a top surface forming a top surface of the substrate;

etching a first opening at a first location on the substrate through the layer of the third material and through the second oxide layer to the layer of the second material;

forming a body of the second material in the first opening to a level of the top surface of the substrate;

etching a second opening at a second location on the substrate through the layer of the third material, the second oxide layer, the layer of the second material and the first oxide layer to the layer of the first material;

forming a body of the first material in the second opening to a level of the top surface of the substrate; and

forming first fins comprising the second material at the first location, forming second fins comprising the first material at the second location and forming third fins comprising the third material at a third location.

21. The method of claim 20, wherein the first fins, the second fins and the third fins extend from a plane of a top surface of the second oxide layer.

22. The method of claim 20, wherein a height of the first fins is substantially equal to a height of the second fins and the height of the second fins is substantially equal to a height of the third fins.

23. The method of claim 20, wherein the first material comprises silicon, the second material comprises germanium and the third material comprises a Group III-V material.

24. A method of forming fins of different materials comprising:

steps for providing a substrate comprising a layer of a first material having a top surface;

steps for masking a first portion of the substrate to form a mask while leaving a second portion of the substrate exposed;

steps for etching a first opening at the second portion;

steps for forming a body of a second material in the first opening to a level of the top surface of the layer of the first material;

steps for removing the mask; and

steps for forming fins of the first material at the first portion and forming fins of the second material at the second portion.

25. The method of claim 24, wherein the steps for masking a first portion of the substrate include steps for leaving a third portion of the substrate exposed and including steps for etching a second opening at the third portion of the substrate through the layer of the first material, the second oxide layer, the layer of the second material and the first oxide layer to the layer of the third material and steps for forming a body of the third material in the second opening to a level of the top surface of the layer of the first material and steps for forming fins of the third material at the third portion.

26. A finFET device having fins formed of at least two different materials comprising:

a substrate having a first layer having a top surface;

a first oxide layer on the first layer top surface, the first oxide layer having a top surface, the first oxide layer covering a first portion of the first layer and not covering a second portion of the first layer;

a first body of material at the second portion of the first layer, the first body of material having a top surface even with the top surface of the first oxide layer;

first fin means for forming a first portion of a semiconductor device; and

second fin means for forming a second portion of a semiconductor device.

27. A method of forming fins of different materials comprising:

steps for providing a substrate comprising a layer of a first material, a first oxide layer on the layer of the first material, a layer of a second material on the first oxide

layer, a second oxide layer on the layer of the second material and a layer of a third material on the second oxide layer, the layer of the third material having a top surface forming a top surface of the substrate;

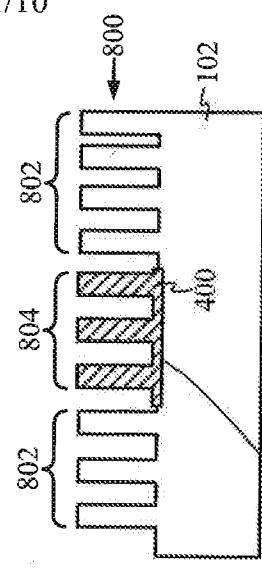
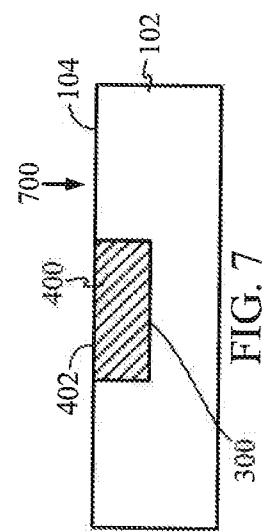
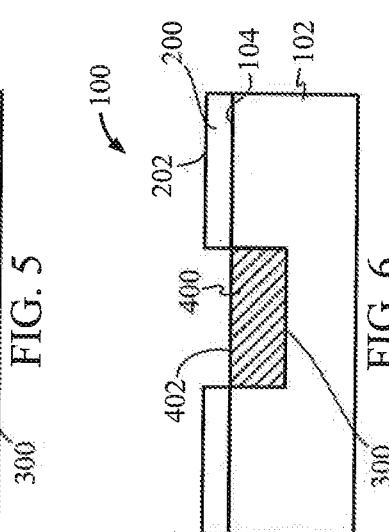
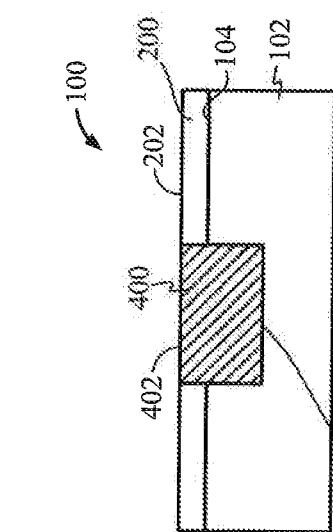
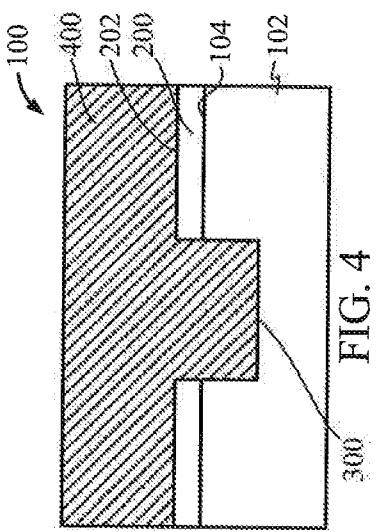
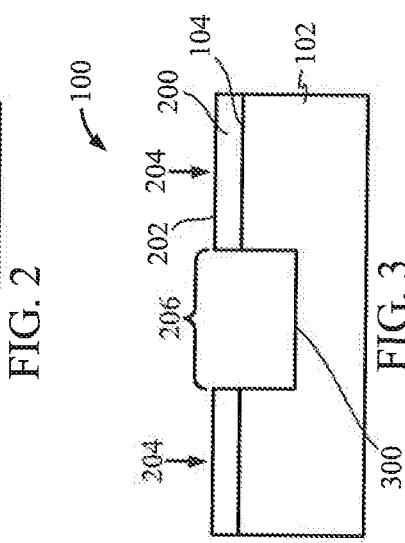
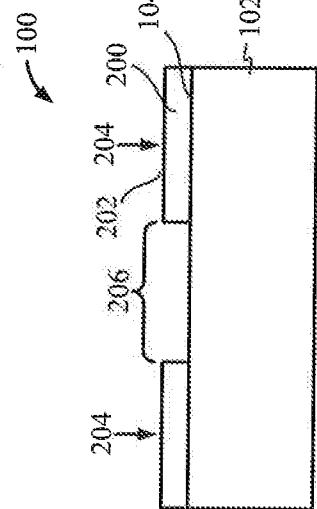
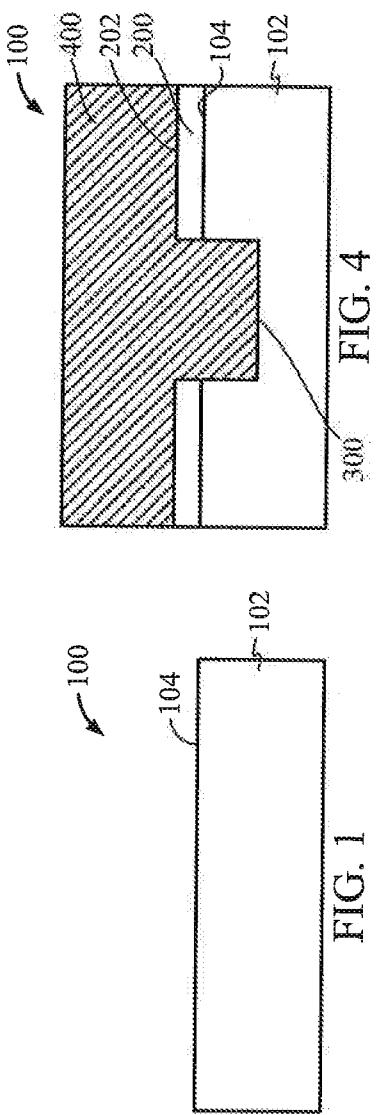
steps for etching a first opening at a first location on the substrate through the layer of the third material and through the second oxide layer to the layer of the second material;

steps for forming a body of the second material in the first opening to a level of the top surface of the substrate;

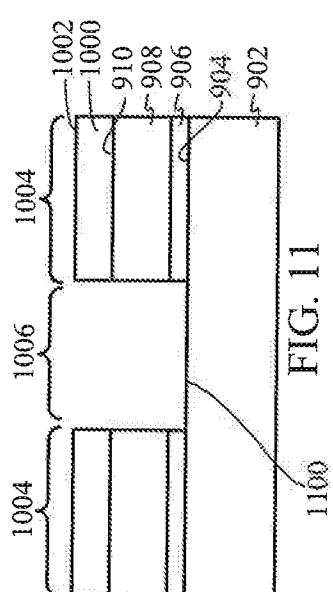
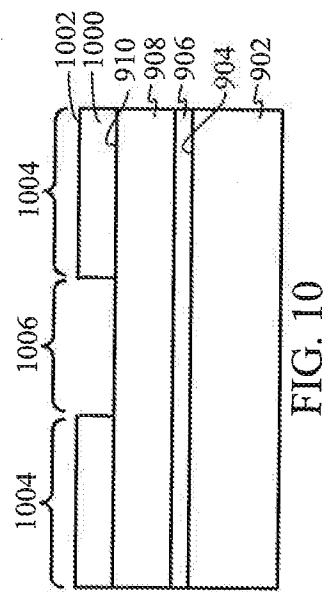
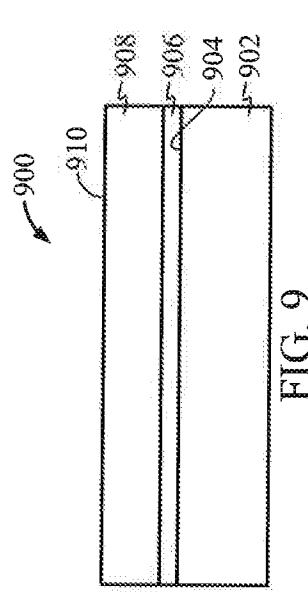
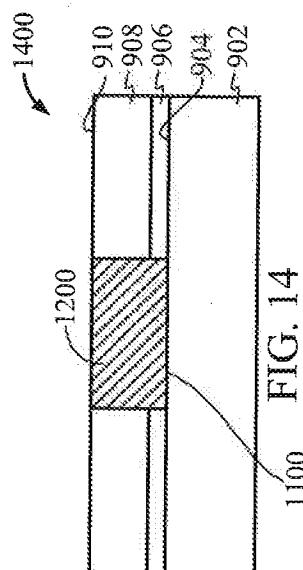
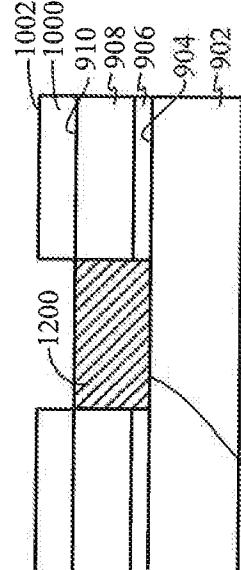
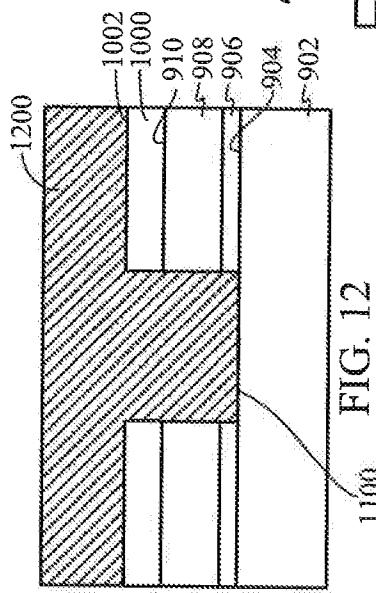
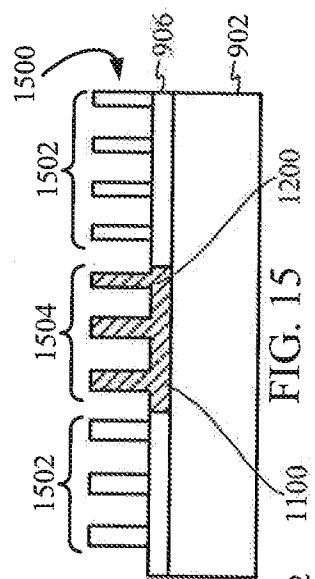
steps for etching a second opening at a second location on the substrate through the layer of the third material, the second oxide layer, the layer of the second material and the first oxide layer to the layer of the first material;

steps for forming a body of the first material in the second opening to a level of the top surface of the substrate; and

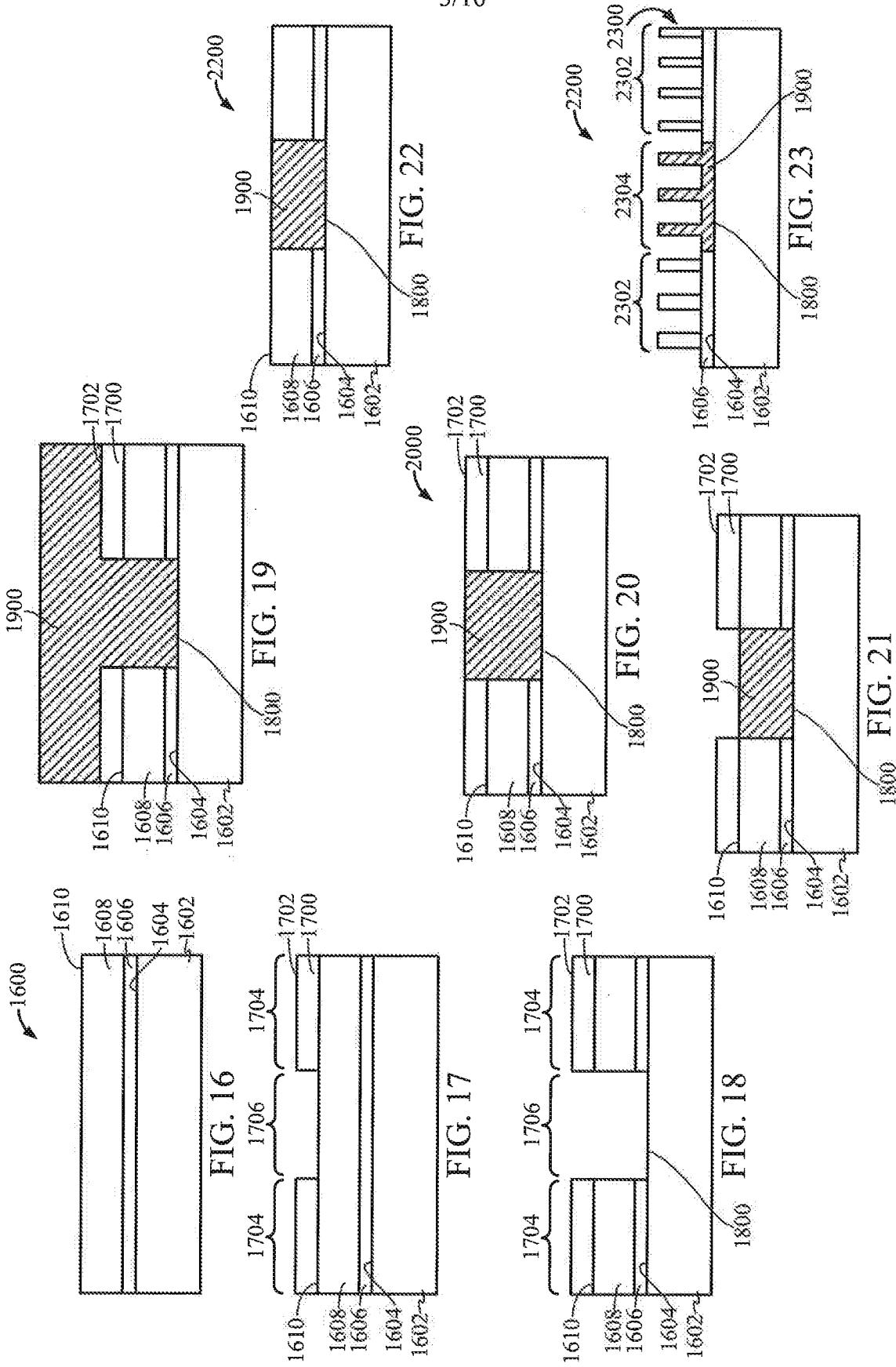
steps for forming first fins comprising the second material at the first location, steps for forming second fins comprising the first material at the second location and steps for forming fins comprising the third material at a third location.



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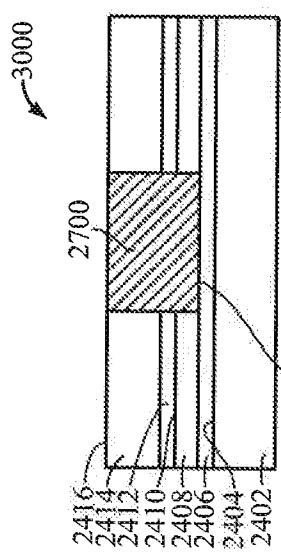


FIG. 30

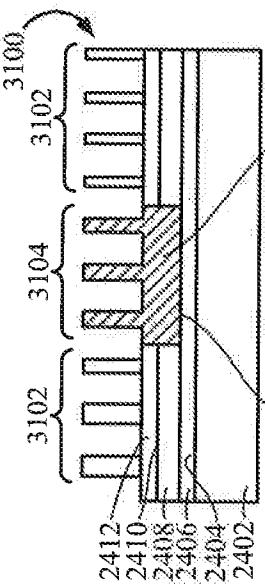


FIG. 31

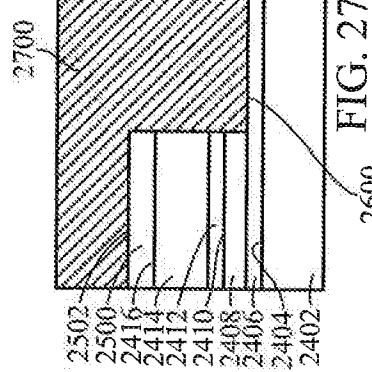


FIG. 27

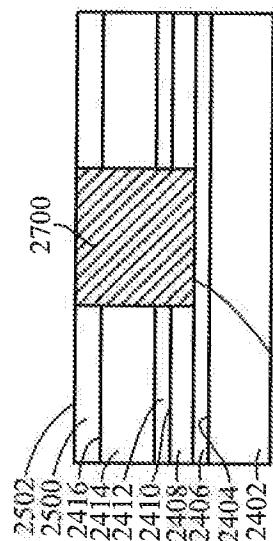


FIG. 28

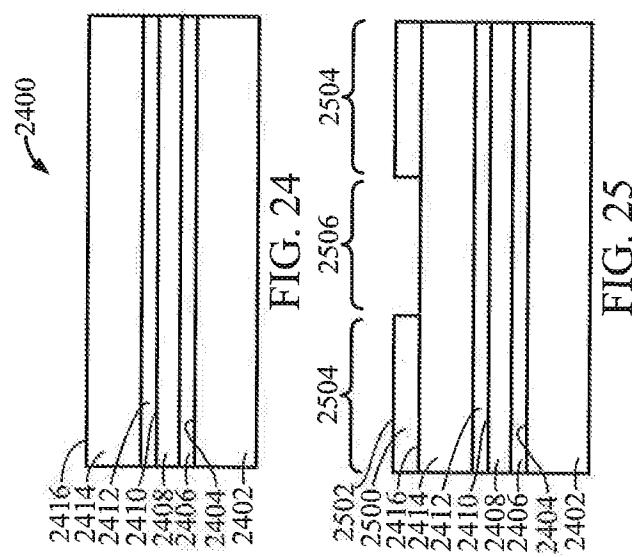


FIG. 24

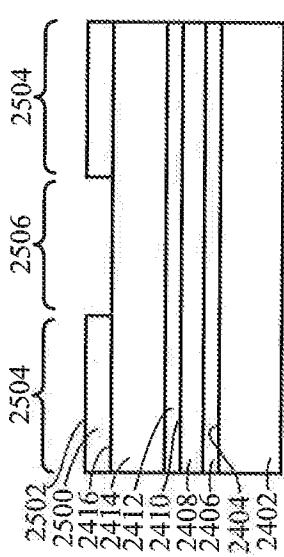


FIG. 25

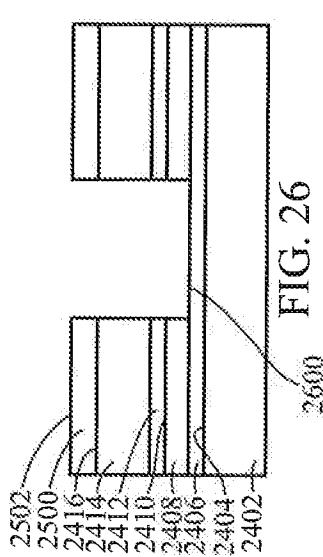


FIG. 26

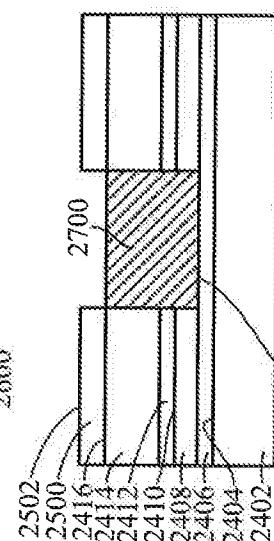


FIG. 29

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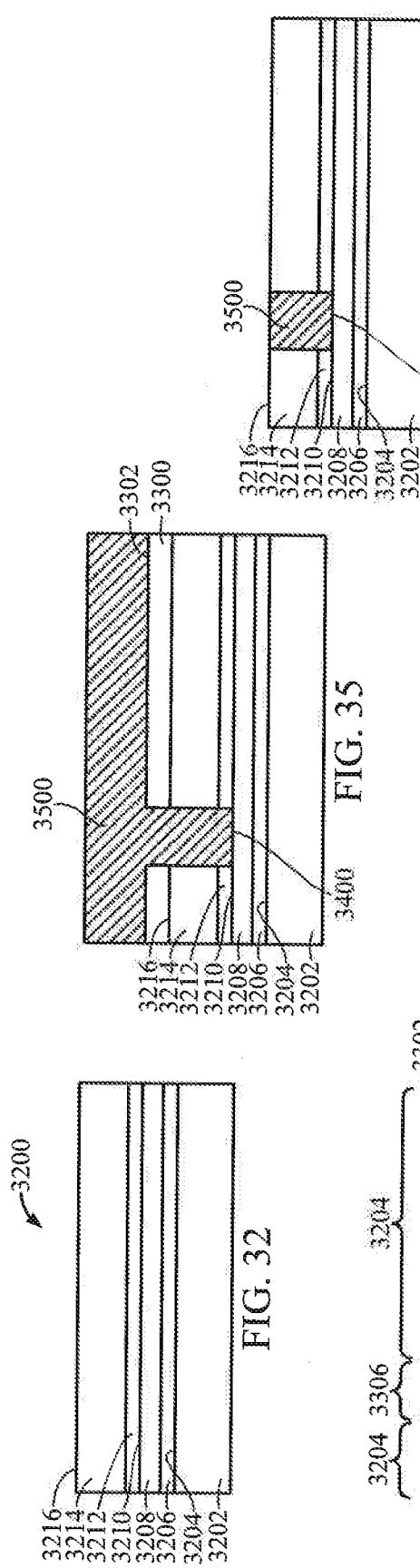


FIG. 32

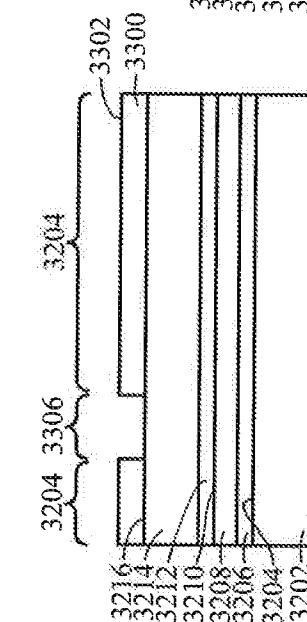
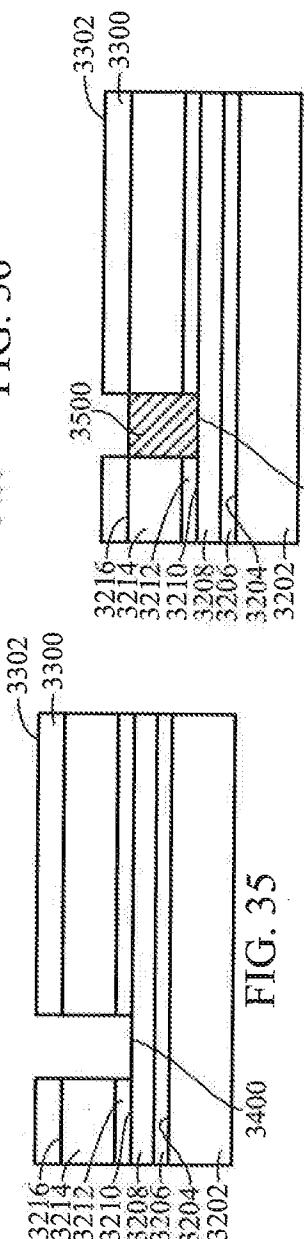


FIG. 34



3400 FIG. 35

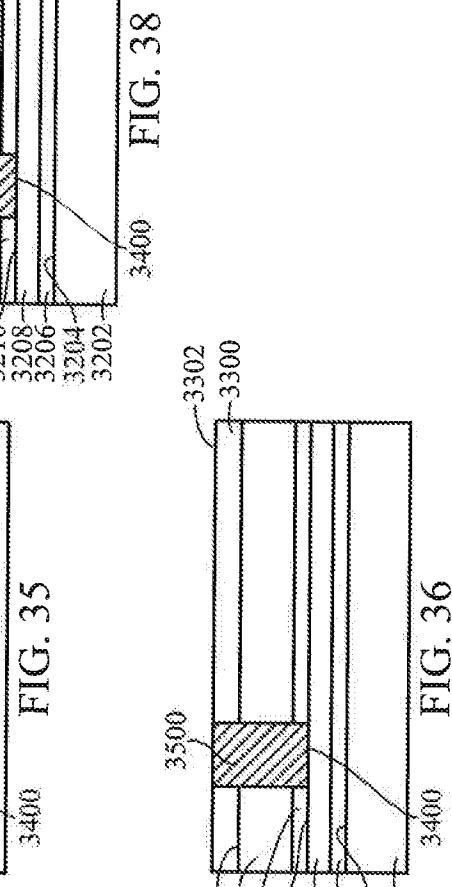
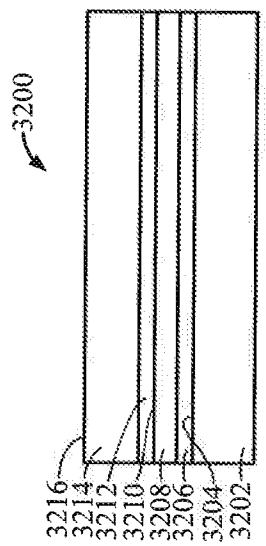
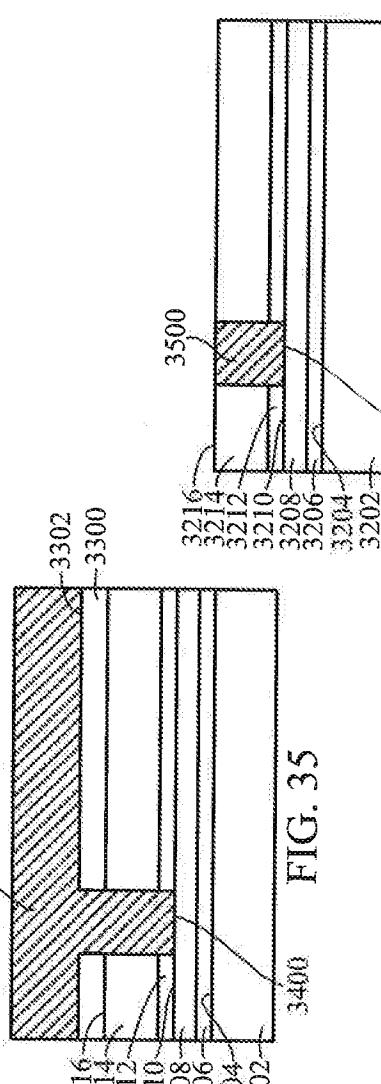


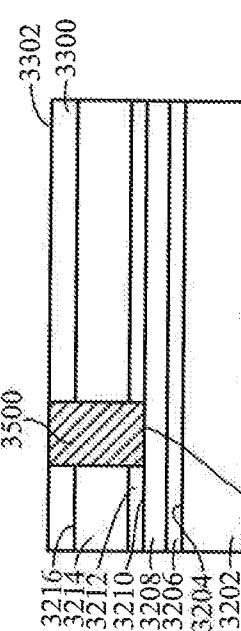
FIG. 35
3400



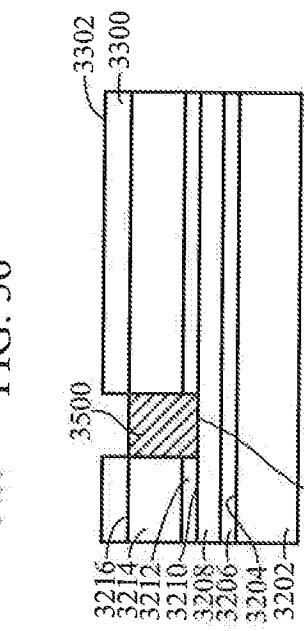
3000



3400 FIG. 35

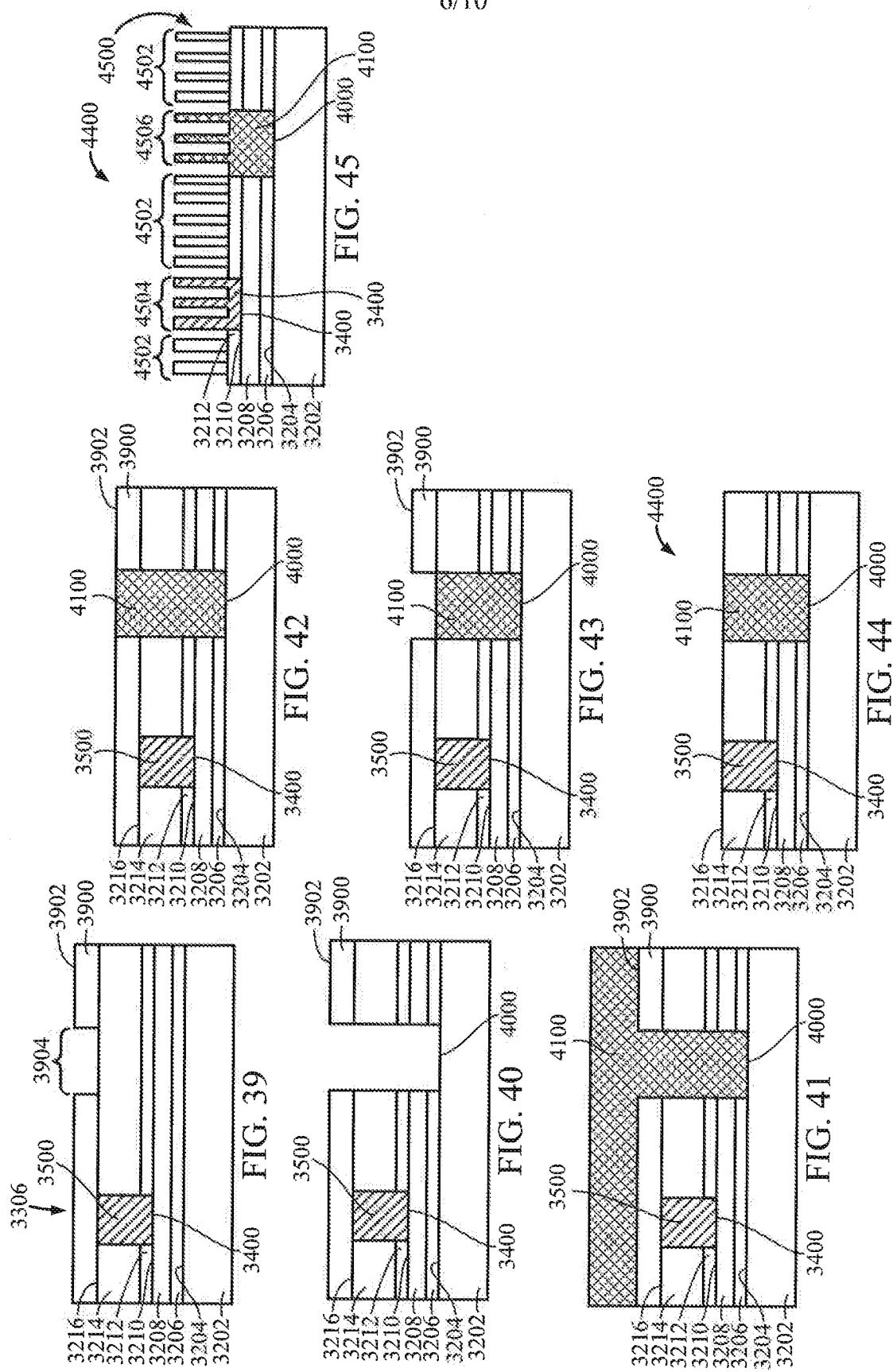


3400 FIG. 36

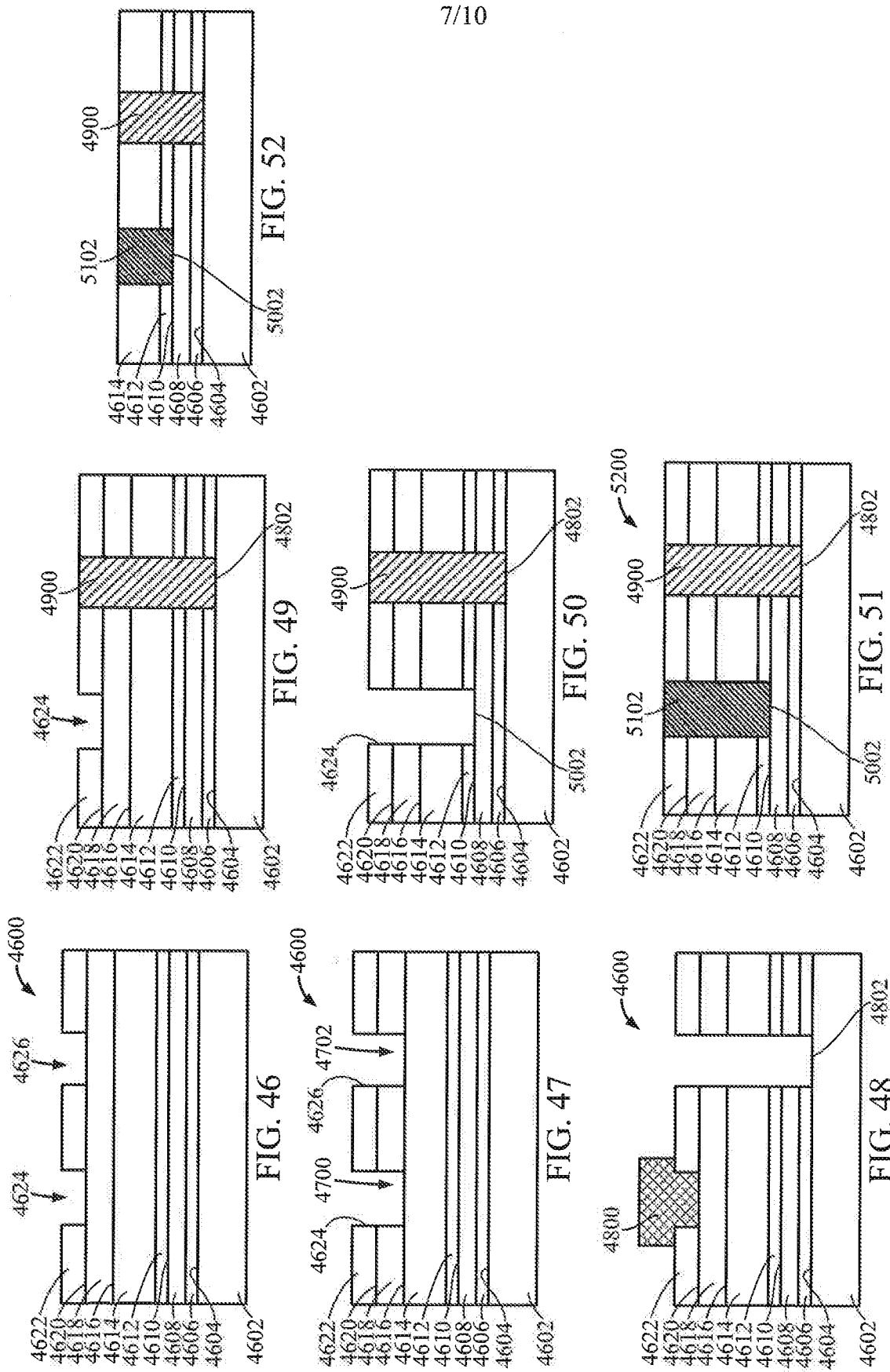


3400 FIG. 37

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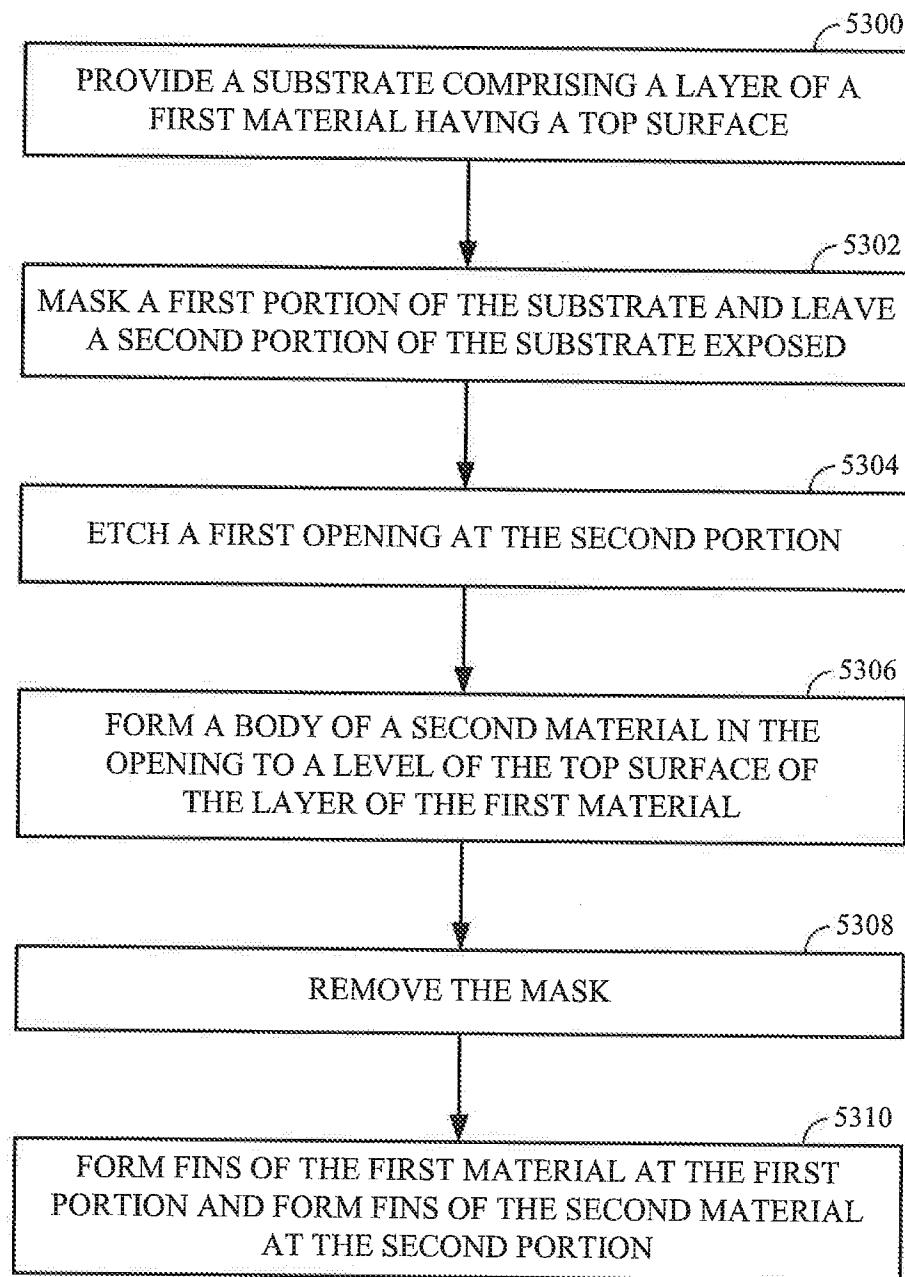


FIG. 53

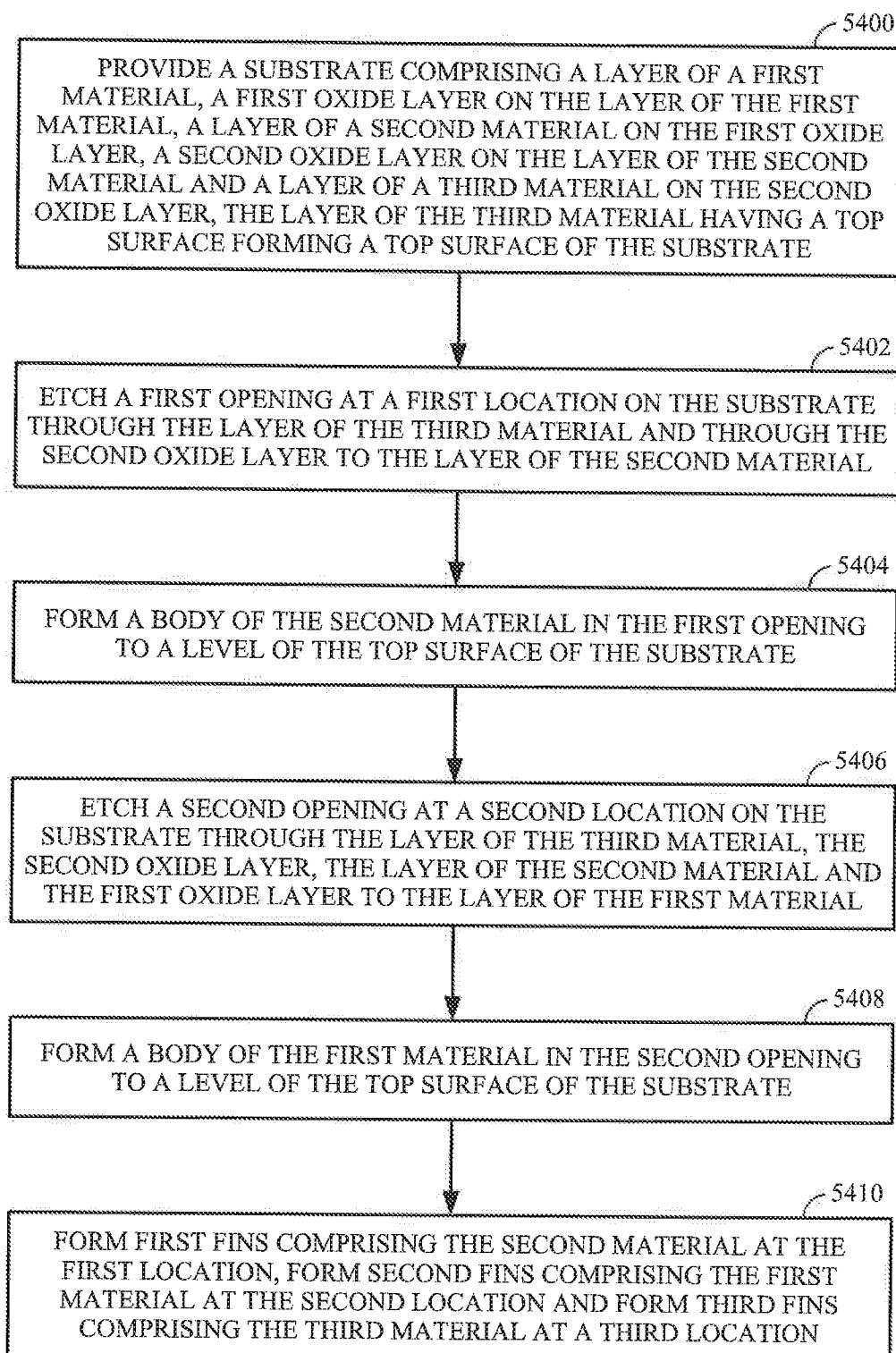


FIG. 54

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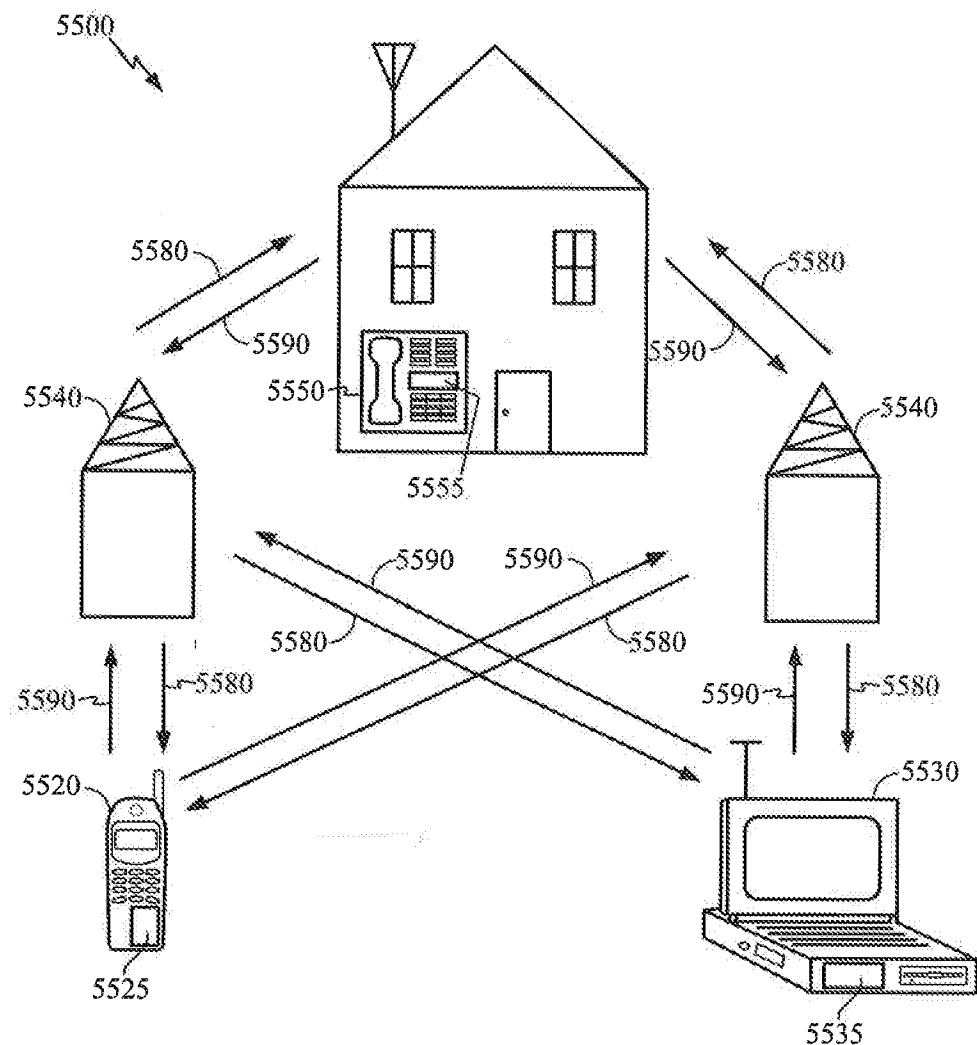


FIG. 55

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 130698WO	FOR FURTHER ACTION <small>see Form PCT/ISA/220 as well as, where applicable, item 5 below.</small>	
International application No. PCT/US2014/048270	International filing date (day/month/year) 25 July 2014 (25-07-2014)	(Earliest) Priority Date (day/month/year) 1 August 2013 (01-08-2013)
Applicant QUALCOMM INCORPORATED		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

the international application in the language in which it was filed
 a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

b. This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).
c. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. **Certain claims were found unsearchable** (See Box No. II)

3. **Unity of invention is lacking** (see Box No III)

4. With regard to the **title**,

the text is approved as submitted by the applicant
 the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

the text is approved as submitted by the applicant
 the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 1-8

as suggested by the applicant
 as selected by this Authority, because the applicant failed to suggest a figure
 as selected by this Authority, because this figure better characterizes the invention

b. none of the figures is to be published with the abstract

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/048270

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/8234 H01L21/84 H01L27/12 H01L21/8258
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/224875 A1 (ANDERSON BRENT A [US] ET AL) 13 October 2005 (2005-10-13)	1-15, 17-19, 24,26
Y	the whole document	6-11,16, 20-23, 25,27
X	----- US 2010/044758 A1 (COHEN GUY M [US] ET AL) 25 February 2010 (2010-02-25) ----- paragraph [0034] - paragraph [0044] ----- -/-	1-8, 12-15, 18,19, 24,26

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search 12 November 2014	Date of mailing of the international search report 18/11/2014
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Hoffmann, Niels

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/048270

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/020515 A1 (WHITE TED R [US] ET AL) 24 January 2008 (2008-01-24) paragraph [0027] - paragraph [0028] paragraph [0033] -----	1-8, 12-15, 18,19, 24,26
X	US 2005/017377 A1 (JOSHI RAJIV V [US] ET AL) 27 January 2005 (2005-01-27) paragraph [0042] - paragraph [0043] -----	1-5,24
A	DE 10 2004 057764 A1 (ADVANCED MICRO DEVICES INC [US]) 8 June 2006 (2006-06-08) paragraph [0012] - paragraph [0013] -----	1-27
Y	US 2006/118918 A1 (WAITE ANDREW M [US] ET AL WAITE ANDREW MICHAEL [US] ET AL) 8 June 2006 (2006-06-08) the whole document -----	6-11,16, 20-23, 25,27
A	US 2013/119507 A1 (LEE SANG-MOON [KR] ET AL) 16 May 2013 (2013-05-16) the whole document -----	1-27
A	HISASHI SHICHIJO ET AL: "MONOLITHIC PROCESS FOR CO-INTEGRATION OF GAAS MESFET AND SILICON CMOS DEVICES AND CIRCUITS", IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 37, no. 3, 1 March 1990 (1990-03-01), pages 548-555, XP000102339, ISSN: 0018-9383, DOI: 10.1109/16.47756 the whole document -----	1-27

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2014/048270

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			WO 2006062796 A2		15-06-2006
US 2013119507	A1	16-05-2013	KR 20130054010 A		24-05-2013
			US 2013119507 A1		16-05-2013