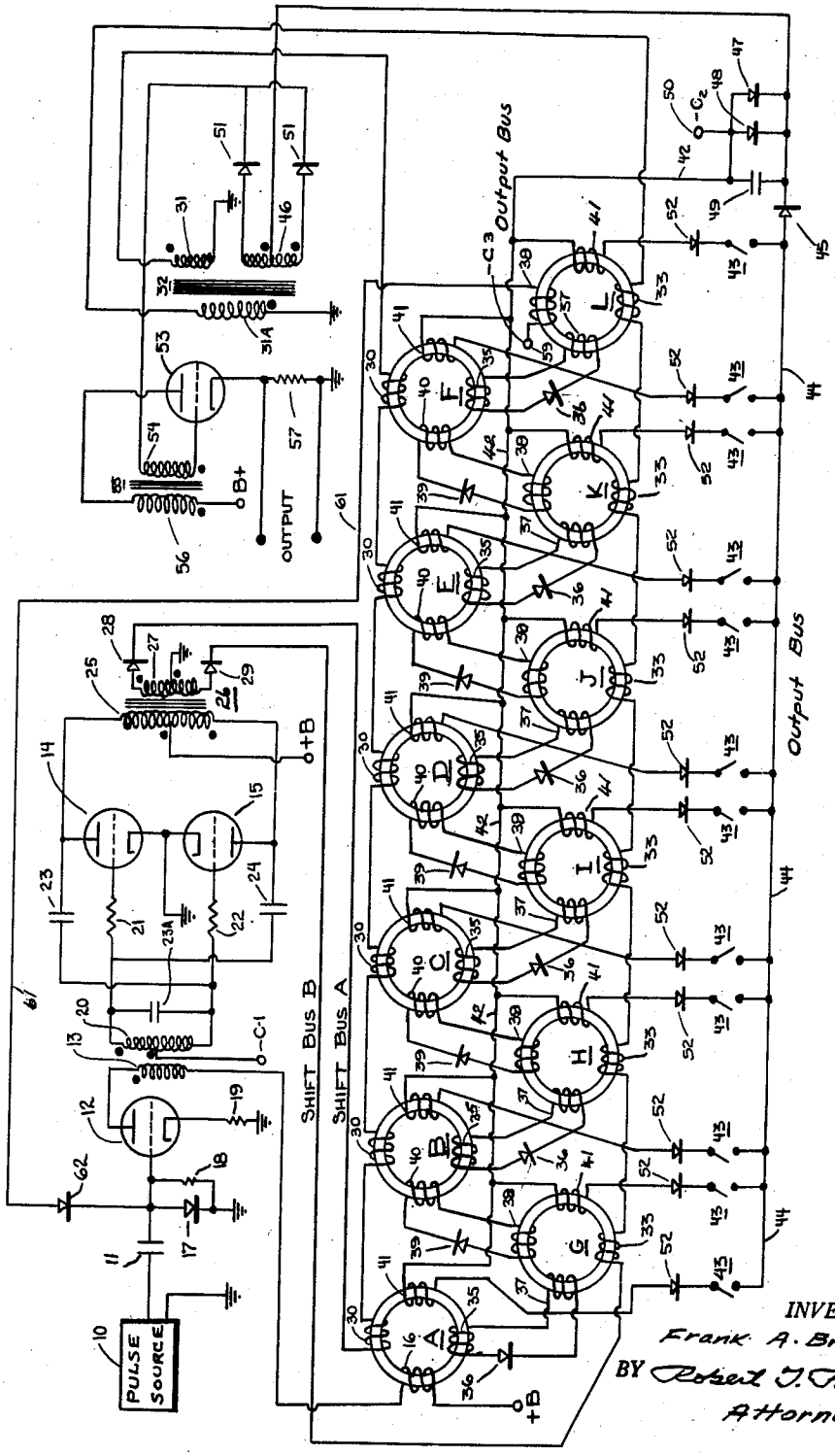
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BEACON CODERS

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INVENTOR.
Frank A. Browne, Jr.
BY Robert J. Palmer
Attorney

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BEACON CODERS

Frank A. Browne, Jr., Brookline, Mass., assignor to American Machine & Foundry Company, a corporation of New Jersey

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This invention relates to radar-beacon coders and has as an object the reduction of the number of vacuum tubes and of other components required in beacon coders.

Radar beacons are widely used for the recognition of objects. For example, the IFF system sends a pulse challenge signal from a station to an airplane or ship within its range, and equipment on a friendly airplane or ship receives the challenge and automatically transmits a signal in the form of a prearranged code to the station. Beacons are also used to accept radar signals from an approaching airplane and then to radiate a coded signal which indicates to the airplane navigation aid in the form of range and direction. Beacons are also contemplated for the handling of airplane landings at congested airports.

Beacon coders are used to provide, upon receipt of an initiating trigger pulse, a coded signal at the output. Such a coded signal is a binary number the digits of which appear in time sequence, the time interval between two digits being accurately determined. A voltage spike appearing at the beginning of any interval denotes a "one" in the binary number system, while the absence of any such spike indicates a "zero." A ranging spike always appears at the beginning of the first interval. This spike is used by the interrogating radar to determine the distance to the beacon.

The generation of the code symbol may be visualized by considering a commutator arrangement. The segments of the commutator are connected through switches to an output bus. The brush of the commutator is connected to one terminal of a direct-current voltage supply, the other terminal serving as the electrical return point for the system. Contact by the brush with those segments, the switches of which are closed, produce voltage pulses or "ones" at the output. The segments the switches of which are open, have no effect upon the output, and, hence, produce "zeros." Prearranged codes thus can be provided by varying the number and position of the open and closed switches.

Prior beacon coders have been electronic, employing, in general, a chain of regenerative trigger circuits arranged in tandem and so connected that one will fire the next in order after a predetermined delay. The trigger circuits are connected to the output bus by switches, a closed switch corresponding to a "one." Thus if a chain is activated by applying a trigger to its input, a pulse will step down the line, energizing the output bus through the closed switches to produce the code. This stepping pulse corresponds to the brush of the commutator, and the trigger circuits to the segments. Each trigger circuit of such prior coders has consisted of either a blocking oscillator or a "one-shot" multivibrator including at least one or two triode tubes, respectively. A separate trigger circuit is required for every digit in a code so that where large numbers of digits are involved correspondingly large numbers of vacuum tubes are required.

In general, the number of unique codes desired for an

airborne or portable beacon, far exceeds the number desired in fixed beacons which are used as aids to navigation. As a result, simpler smaller and lighter coders than previously have been provided, are needed. This invention fills such a need.

This invention uses magnetic binaries instead of multivibrators for providing the digits in a coder, and requires only four triode vacuum tubes (two dual triode tubes) or their functional equivalents, such as, "transistors," "magnetic," or "dielectric" amplifiers. As the number of digits in a code is increased, more magnetic binaries are required, and the size of the tubes may have to be increased, but the number of tubes required remains at four.

Magnetic binary shift registers and the magnetic binaries used therein are fully described in an article by An Wang and Way Dong Woo published on pages 49–54, volume 21, the January 1950 issue, of the Journal of Applied Physics. It is believed, therefore, that it is not necessary in the present disclosure, to give more than the following brief description of magnetic binaries and shift registers employing same.

A magnetic binary core is capable of being magnetized to saturation in either of two directions. Two states are said to arise from the two directions: a positive or active state, in which the direction of retentivity is opposite to that which would result from the application of a shift pulse to a shift winding on the core, and a negative, or inactive state in which the direction of retentivity is the same as that which would result from the application of a shift pulse. When applied to a core in the active state, a shift current pulse causes the inactive state to appear. When applied to a core already in the inactive state, a shift pulse causes no change in state.

A core in the active, or positive state, is said to contain a binary digit "one," and a core in the negative, or inactive state, is said to contain the digit "zero." A single bit of information is called a "baud." When a core shifts from one state to another, a voltage is induced in all of the windings on it. A shift current pulse will have no substantial effect on a core in an inactive state, and substantially no voltage should be induced in its windings.

A magnetic binary shift register has a line of storage cores and another line of temporary storage cores. If a "one" signal is stored in the first core, the application of a shift pulse to the line of storage cores will shift out the information stored in the cores and will cause the "one" to be transferred to the first core in the temporary storage line. The application of a shift pulse to the temporary storage line will cause the "one" to be transferred to the second core in the storage line. One cycle of operation thus consists of pulsing first the storage line and then the temporary storage line. At the end of a cycle, a "one" has advanced one stage.

There has been proposed a coder using a magnetic binary shift register in which a code symbol is stored, the code being generated by reading out the contents of the register serially. The number of "ones" stored in the register is equal to the number of pulses desired in a given code, thus requiring a shift register stage for each interval in the code to be generated, regardless of whether that interval includes a "one" or a "zero."

The present invention is an improvement over such a coder in that a single "one" is stored in a magnetic binary shift register, regardless of the number of pulses to be generated, and in that only one-half a shift register stage is required for each interval in a code to be generated, regardless of whether that interval includes a "one" or a "zero."

Accordingly, another object of this invention is to reduce the number of magnetic binaries used in coders in which magnetic binary shift registers are used to generate codes.

This invention will now be described with reference to the drawing which is a circuit schematic illustrating one embodiment of the invention.

The pulse source **10** which may be a radar receiver, is connected through the coupling capacitor **11** to the control grid of the triode **12**, the anode of which is connected through the primary winding **13** of the tank circuit of the oscillator tubes **14** and **15**, and the receiving winding **16** on the binary core A to the positive terminal (B+) of a conventional anode voltage supply source which is not illustrated, and the negative terminal of which would be grounded as is conventional. The diode **17** shunted by a resistor **18** is connected between the control grid of the tube **12** and ground. The self-bias resistor **19** is connected between the cathode of the tube **12** and ground.

The secondary winding **20** of the tank circuit has its centerpoint connected to C_1-, the negative terminal of a conventional bias voltage source which is not illustrated, and the positive terminal of which would be grounded. The ends of the winding **20** are connected through the resistors **21** and **22** to the control grids of the tubes **14** and **15** respectively. The tuning capacitor **23A** is shunted across the winding **20**. The anode of the tube **14** is connected through the feed back capacitor **23** to the grid circuit of the tube **15**, and the anode of the tube **15** is connected through the feed back capacitor **24** to the grid circuit of the tube **14**. The anodes of the tubes **14** and **15** are also connected to the ends of the primary winding **25** of the transformer **26**, the centerpoint of the winding **25** being connected to B+.

One end of the secondary winding **27** of the transformer **26** is connected through the crystal diode **28** to the Shift Bus A of a magnetic binary shift register having the storage cores A—F and the temporary storage cores G—L. The other end of the winding **27** is connected through the crystal diode **29** to the Shift Bus B of the shift register, the centerpoint of the winding **27** being grounded.

The Shift Bus A is connected in series with the shift windings **30** on the storage cores, and with the winding **31** on the saturable core **32**, to ground. The Shift Bus B is connected in series with the shift windings **33** in the temporary storage cores, and with the winding **31A** on the saturable core **32**, to ground.

The storage cores have the transmitting windings **35** which are connected through the crystal diodes **36** to the receiving windings **37** in the temporary storage cores.

The temporary storage cores G—K have the transmitting windings **38** connected through the crystal diodes **39** to the receiving windings **40** of the storage cores B—F. The cores A—L have the code read-out windings **41** connected directly to the output bus **42** and connected through the crystal diodes **52**, switches **43**, where the switches are closed, to the output bus **44**.

The output bus **44** is connected in series with the crystal diode **45** to the centerpoint of the winding **46** on the saturable core **32**. The crystal diodes **47** and **48** shunted by the capacitor **49**, are connected between the output buses **44** and **42** at the output side of the diode **45**. The output bus **42** is connected at **50** to C_2-, which can be a tap on the same conventional bias supply used for C_1-. The ends of the winding **46** of the core **32** are connected through the crystal diodes **51** and the secondary winding **54** of the blocking oscillator transformer **55** to the control grid of the output tube **53**. The anode of the tube **53** is connected through the primary winding **56** of the transformer **55** to B+. The cathode of the tube **53** is connected in series with the resistor **57** to ground. The coder output is connected across the resistor **57**.

The ends of the winding **38** on core L are joined, one to the conductor **61** and the other at **59** to C_3-, which can be another tap on the supply used for C_1- and C_2-. The crystal diode **62** is connected from the conductor **61** to the grid of the triode **12**.

Operation

During a quiescent period the steady state anode current of the triode **12** flows through the winding **16** on the core A and is used to read a "one" into this core. The anode resistance of the triode damps the tank circuit including the windings **13** and **20** and prevents oscillation at this time.

An initiating positive trigger pulse from the source **10**, causes electrons to be drawn from ground through the diode **17**, and to be deposited on that plate of the capacitor **11** which is connected to the diode. When the initiating pulse vanishes, the electrons stored on the capacitor plate cause the grid of the triode **12** to be so negative that its anode current ceases, shocking the tank circuit into oscillation. The class B push-pull oscillator tubes **14** and **15** then supply shift pulses in the Shift Buses A and B. The winding polarities of the output transformer **26** and the connections of the diodes **28** and **29** are such that both the #1 and #2 pulses are produced during each cycle of operation. The first cycle of the oscillator advances the "one" stored in the core A, through core G to core B. The second cycle of the oscillator advances the "one" from core B through core H to core C, and so on, each cycle advancing the "one" one stage in the shift register.

The voltage across the winding **20** of the tank circuit is very nearly a sine wave and in the drawing, the polarities of the windings **13, 20, 25, 27** are such that immediately following the initiating trigger, triode **14** conducts, delivering a shift pulse to Shift Bus A. The initial peak amplitude of the tank voltage sinusoid is a function of the steady state anode current of the tube **12**. To ensure correct operation of the coder, the oscillator must maintain this peak amplitude for the entire time during which the shift register contains a "one." The charge placed on the grid capacitor **11** by the trigger maintains the tube **12** non-conductive until the capacitor **11** is discharged by the "one" from the winding **38** on the last core L of the shift register applied through the conductor **61** and the diode **62** to the capacitor. The grid voltage of the tube **12** then rises above cut-off; the plate resistance of the conducting tube then damps out the oscillation in the tank circuit, stopping the production of shift pulses.

The oscillator is also used to provide the timing function. Each zero-axis crossing of the oscillator tank voltage corresponds to the beginning of a time interval. In an embodiment of the invention which has been successfully operated, the oscillator period was 30 microseconds, two such intervals, each 15 microseconds long, being provided by each oscillation cycle. By properly adjusting the bias and the amount of feedback, the beginning of each interval was made to correspond with the beginning of a shift pulse.

Where the "one" is transferred from each of the cores to the next core in order, during the time of transfer, the voltage induced in the read-out winding **41** of the transmitting core is of such a polarity that current can flow through its associated diode **52**. As the "one" is shifted through the register at a rate determined by the shift pulse generator, a pulse is delivered to each switch **43** in turn. If all the switches were closed, an unbroken sequence of pulses would appear on the output buses. The formation of a pulse code is accomplished by opening certain of the switches thus causing the sequence of the output pulses to be broken in a predetermined manner.

The shift pulse oscillator and the register portions of the coder are characterized by the absence of waveforms having large rise rates. Further, at the beginnings of the time intervals in the symbol (zero-axis crossings of the oscillator tank voltage), the system signal voltages and currents are all close to zero. The coder output pulses must be delivered at these times. For providing out-

put pulses of sufficiently small duration and large peak power, a blocking oscillator is used. Sharply peaked trigger voltages are produced by the saturable transformer **32**, as close to the beginning of each time interval as possible. The baud voltage of the preceding interval is retained on the capacitor **49** and added to the peaked voltage. If the baud is a "one," the sum voltage is sufficiently large to trigger the blocking oscillator. This output circuit will be described in the following, with the given numerical values being appropriate to the use of one section of a 12AU7 twin-triode for the tube **53**.

The crystal diode **45** in the output bus **44** couples the register symbol-output line to the capacitor **49** which retains the baud and which is charged almost to the peak voltage of a "one" in an output winding **41**. This capacitor is discharged by the firing of the blocking oscillator tube **53**. The diode **45** reduces the rate of leakage of the charge from the capacitor. If all of the switches **43** are closed and the diode **45** shunted out, the charged capacitor is shunted by the back resistances of all of the output coil diodes **52** in parallel, thus increasing undesirably the rate of decay of the stored baud voltage.

The two diodes **47** and **48** which shunt the capacitor **49** serve to conduct the grid current of the blocking oscillator tube **53**. When the tube **53** fires, the capacitor **49** discharges through the conducting diodes **47** and **48**. The retained baud voltage of about 25 volts is almost immediately reduced to about one volt drop across the diodes **47** and **48**. The output winding **46** of the saturable core **32** is in series with the baud-retaining circuit and is connected to the crystal diodes **51** in a full-wave rectifier circuit which produces a unidirectional train of spikes. It will be noted that the blocking oscillator grid current produces no net M. M. F. in the spike-producing core **32**. Therefore, the impedance presented by the full-wave rectifier to the grid current is that of the two diodes **47** and **48** in parallel, plus a small inductive component due to leakage fluxes.

The peak spike voltage produced by the full-wave rectifier circuit is equal to the retained baud voltage, about 25 volts. The grid voltage at which the blocking oscillator tube **53** is just able to fire is −19 volts. The blocking oscillator bias voltage is set at −60 volts. Thus, when a "one" is being retained by the capacitor **49**, the grid voltage is −35 volts and the tube **53** cannot fire. When a spike appears the grid voltage rises toward −10 volts and the blocking oscillator fires. If a "zero" is being retained by the capacitor **49**, the spike raises the grid voltage only to about −35 volts and the blocking oscillator cannot fire.

The combined grid and anode current of the blocking oscillator tube **53** when it conducts, is about 500 milliamperes so that with a value of 160 ohms for the cathode resistor **57**, the voltage at the output terminals is about 80 volts. The blocking oscillator must be fired by the initiating trigger from the pulse source **10**, in order to provide the ranging spike which always appears at the beginning of the first interval. The means for so doing is conventional, and is not shown.

When the complete code has been generated, a voltage is induced in the winding **39** of the last core L because of the arrival there of the baud. This voltage causes the diodes **62** and **17** to conduct, thus providing a discharge path for the capacitor **11**. The tube **12** then again starts to conduct, reads another "one" into core A, and stops the shift pulse generator.

The black dots alongside the windings **13, 20, 25, 27, 31, 31A, 46, 54** and **56** are at points on such windings having the same instantaneous polarities. The diodes used in the circuit are for preventing currents from flowing in the wrong directions.

More or fewer magnetic binary cores, diodes and switches could be used depending upon the desired code. An increase in the number of cores, diodes and switches would not require, however, any additional vacuum tubes or other components.

The drawing is a circuit schematic only, and is not intended to illustrate the constructions of the transformer cores or the physical arrangements of the windings thereon. The proper polarities at the windings and the directions in which they are wound will be apparent to those skilled in shift register circuitry.

While one embodiment of the invention has been described for the purpose of illustration, it should be understood that the invention is not limited to the exact circuit and circuit components illustrated, as modifications thereof may be suggested by those skilled in the art, without departure from the essence of the invention.

What is claimed is:

1. A coder comprising a binary storage core, a binary temporary storage core, shift windings on said cores, means including a receiving winding on said storage core for storing a "one" in said storage core, means including a shift pulse generator, said shift and a transmitting winding on said first core and a receiving winding on said second core for shifting the "one" stored in the first core into the second core, means including said generator and said shift and a transmitting winding on said second core for shifting out the "one" from said second core, means for storing the voltage induced in an output winding of said first core when the "one" is shifted therefrom, a saturable core having a shift winding connected to said generator and to said shift winding on said second core, and having an output winding in which a peaked voltage is induced when said generator causes the "one" to be shifted from said second core, and means for adding said peaked and stored voltages.

2. A coder as claimed in claim 1 in which an electronic oscillator is provided, and in which the sum of the stored and peak voltages is used to fire the oscillator.

3. A coder as claimed in claim 2 in which the oscillator has a cathode to which an impedance is connected, and in which output connections are connected across said impedance.

4. A coder comprising first and second magnetic binary cores, shift and output windings on said cores, a transmitting winding on said first core, a receiving winding on said second core connected to said transmitting winding, means for supplying a first shift pulse to said shift winding on said first core for shifting out a "one" stored therein, the voltage induced in said transmitting winding when the "one" is shifted out of said first core being transmitted to said receiving winding to store the "one" in the second core, means for supplying a second pulse to the shift winding on the second core for shifting out the "one" stored therein, a saturable reactor having a first shift winding in series with said first shift pulse supplying means and the shift windings on said first cores, and having a second shift winding in series with said second shift pulse supplying means and the shift windings on said second cores, switches connecting said output windings to an output circuit, said switches determining which of said output windings are connected to said circuit, means in said output circuit for storing the voltages from such of said output windings as are connected through closed switches to said circuit, an electronic oscillator having a control electrode and a cathode, an output winding on said saturable core connected in series with said voltage storage means and said output winding, an impedance connected to said cathode, and output connections connected across said impedance.

5. A coder comprising first and second magnetic binary cores, shift and output windings on said cores, a transmitting winding on said first core, a receiving winding on said second core connected to said transmitting winding, means for supplying a first shift pulse to said shift winding on said first core for shifting out a "one" stored therein, the

voltage induced in said transmitting winding when the "one" is shifted out of said first core being transmitted to said receiving winding to store the "one" in the second core, means for supplying a second pulse to the shift winding on the second core for shifting out the "one" stored therein, an output circuit, means including switches connecting said output windings to said output circuit, said switches determining which of said output windings will deliver voltage pulses to said output circuit, said output circuit including means for storing the voltage induced in the output winding of the first core when the "one" stored therein is shifted to the second core, a saturable core having a winding connected to said last-named means for applying a second pulse and having an output winding, and means for adding the stored voltage to a peaked trigger voltage induced in said output winding of said saturable core when the "one" is shifted from the second binary core.

6. A coder as claimed in claim 5 in which the sum of the stored voltage and the peaked trigger voltage is used to fire an electronic oscillator connected in a blocking oscillator circuit, and in which output connections are connected across an impedance connected in the cathode circuit of the oscillator.

7. A coder comprising first and second magnetic binary cores, shift and output windings on said cores, a transmitting winding on said first core, a receiving winding on said second core connected to said transmitting winding, means for supplying a first shift pulse to said shift winding on said first core for shifting out a "one" stored therein, the voltage induced in said transmitting winding when the "one" is shifted out of said first core being transmitted to said receiving winding to store the "one" in the second core, means for supplying a second pulse to the shift winding on the second core for shifting out the "one" stored therein, an output circuit, means including switches connecting said output windings to said output circuit, said switches determining which of said output windings will deliver voltage pulses to said output circuit, said output circuit including means for storing the voltage induced in the output winding of the first core when the "one" stored therein is shifted to the second core, said output circuit further including means for producing a peaked trigger voltage when the "one" is shifted from the second core and including means for adding said trigger voltage to said stored voltage.

8. A coder as claimed in claim 7 in which the sum of the stored and peaked voltage is used to fire an electronic oscillator connected in a blocking oscillator circuit, and in which output connections are connected across an impedance connected in the cathode circuit of said oscillator.

9. A coder as claimed in claim 8 in which a normally conducting electronic amplifier has its anode connected to the tank circuit of the push-pull oscillator which normally is not oscillating, and in which the initiating trigger voltage causes the normally conducting amplifier to cease conducting thereby shocking the tank circuit into oscillation.

10. A coder as claimed in claim 5 in which the sum of the stored voltage and the trigger voltage is used to fire an electric oscillator having a cathode, and in which output connections are connected across an impedance connected in the cathode circuit of the oscillator.

11. A coder comprising first and second magnetic binary cores, shift and output windings on said cores, a transmitting winding on said first core, a receiving winding on said second core connected to said transmitting winding, means for supplying a first shift pulse to said shift winding on said first core for shifting out a "one" stored therein, the voltage induced in said transmitting winding when the "one" is shifted out of said first core being transmitted to said receiving winding to store the "one" in the second core, means for supplying a second pulse to the shift winding on the second core for shifting out the "one" stored therein, an output circuit, means including switches connecting said output windings to said output circuit, said switches determining which of the output windings will deliver voltage pulses to said circuit, said output circuit including means for storing the voltage pulse from an output winding on one core when a "one" is shifted from the latter to the next core in order, said output circuit further including means for generating a peaked voltage when the "one" is shifted from the last mentioned core to the next core in order and including means for adding the stored and peaked voltages.

12. A coder as claimed in claim 11 in which the sum of the stored and peaked voltages is used to fire an electronic oscillator having a cathode in the circuit of which is connected an impedance across which output connections are connected.

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