

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
11 December 2003 (11.12.2003)

PCT

(10) International Publication Number
WO 03/102962 A2

(51) International Patent Classification⁷: **G11C 16/14**

(21) International Application Number: PCT/US03/16856

(22) International Filing Date: 29 May 2003 (29.05.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/159,885 29 May 2002 (29.05.2002) US

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(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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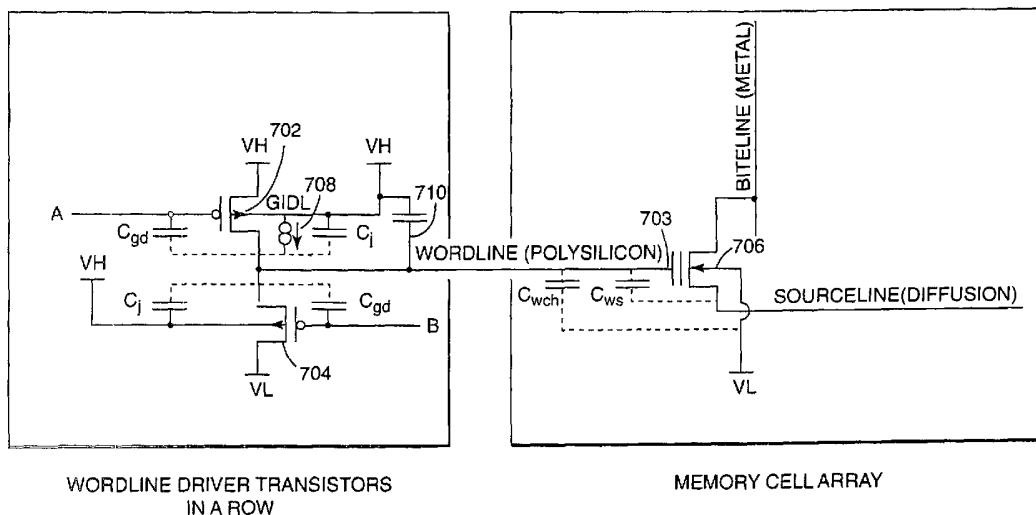
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Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND APPARATUS FOR ERASING FLASH MEMORY



(57) Abstract: Method and apparatus for the erase of non-volatile memory in which holes trapped in the tunnel oxide are reduced.

5 METHOD AND APPARATUS FOR ERASING FLASH MEMORY

Technical Field

The present invention relates in general to a method and apparatus for erasing
of a non-volatile memory device and in particular to a method and apparatus for an
10 erase operation of a memory array of a nonvolatile memory device that can reduce the
number of trapped holes in the tunnel oxide of flash memory cells.

Background

Fig. 1 illustrates a cross sectional view of a conventional flash memory cell
15 100. Memory cell 100 includes a substrate 103, a source 104, a control gate 108, a
floating gate 106 electrically isolated by an insulating layer of silicon dioxide (SiO_2)
110, and a drain 112. Memory cell 100 is thus basically an n-channel transistor with
the addition of a floating gate. Electrical access to floating gate 106 takes place only
through a capacitor network of surrounding SiO_2 layers and source 104, drain 112,
20 channel 105, and control gate 108. Any charge present on the floating gate 106 is
retained due to the inherent Si- SiO_2 energy barrier height, leading to the non-volatile
nature of the memory cell.

Programming a flash memory cell means that charge (*i.e.*, electrons) is added
to the floating gate 106. A high drain to source bias voltage is applied, along with a
25 high control gate voltage. The gate voltage inverts the channel, while the drain bias
accelerates electrons towards the drain. In the process of crossing the channel, some
electrons will experience a collision with the silicon lattice and become redirected
towards the Si- SiO_2 interface. With the aid of the field produced by the gate voltage
some of these electrons will travel across the oxide and become added to the floating
30 gate. After programming is completed the electrons added to the floating gate
increase the cell's threshold voltage. Programming is a selective operation,
performed on each individual cell.

Reading a flash memory cell takes place as follows. For cells that have been
programmed, the turn-on voltage V_t of cells is increased by the increased charge on
35 the floating gate. By applying a control gate voltage and monitoring the drain current,
differences between cells with charge and cells without charge on their floating gates
can be determined. A sense amplifier compares cell drain current with that of a

5 reference cell (typically a flash cell which is programmed to the reference level during manufacturing test). An erased cell has more cell current than the reference cell and therefore is a logical "1," while a programmed cell draws less current than the reference cell and is a logical "0."

Erasing a flash cell means that electrons (charge) are removed from the floating gate 106. Erasing flash memory is performed by applying electrical voltages to many cells at once so that the cells are erased in a "flash." A typical erase operation in a flash memory may be performed by applying a positive voltage to the source 104, a negative or a ground voltage to the control gate 108, and holding substrate 102 of the memory cells at ground. The drain 112 is allowed to float.

15 Under these conditions, a high electric field (8-10MV/cm) is present between the floating gate and the source. The source junction experiences a gated-diode condition during erase and electrons that manage to tunnel through the first few angstroms of the SiO₂ are then swept into the source. After the erase has been completed, electrons have been removed from the floating gate, reducing the cell threshold voltage V_t.

20 While programming is selective to each individual cell, erase is not, with many cells being erased simultaneously.

Stress Induced leakage current (SILC) in a flash memory occurs when there is tunneling from the floating gate through the insulating oxide surrounding it at abnormally low voltages. This can result from holes that become trapped in the tunnel oxide of the flash memory cells after the memory cell has been cycled through read, write and erase operations a number of times, *i.e.*, "stressed," and can severely degrade the performance of the memory. SILC presents a major challenge to designers and manufacturers of flash memory devices and will present even greater challenges as device size continues to be reduced and the insulating oxide surrounding the floating gate is made thinner.

Various solutions have been proposed to address the problem of SILC. For example, a triple well channel erase flash memory has been proposed in which a memory cell is fabricated inside a P-well that is, in turn, inside an N-well. Unfortunately, a triple well construction increases process complexity and memory area. Thus there is a need for a flash memory cell method and apparatus that reduces SILC as the device is cycled.

5 For the reasons stated above and for additional reasons stated hereinafter,
which will become apparent to those skilled in the art upon reading and understanding
the present specification, there is a need in the art for an improved method and
apparatus for erasing flash memory. The above-mentioned problems of traditional
flash memories and other problems are addressed by the present invention, at least in
10 part, and will be understood by reading and studying the following specification.

Brief Description of the Drawings

Figure 1 is a block diagram of a prior art flash memory cell .

15 Figure 2 shows a simplified schematic of a flash memory of an embodiment of
the present invention.

Figure 3 is a graph showing an example of a sequence of pulses for a
conventional source erase operation of a flash memory.

20 Figure 4 is a graph showing the stress induced leakage current (SILC) from
simulated application of successive erase-program cycles on an array of a flash
memory cells.

Figure 5 is a graph showing a prior art example of a sequence of pulses for an
erase operation of a flash memory built inside a triple well showing an extra step of a
channel erase.

25 Figure 6 is a graph showing an example of a sequence of pulses for an erase
operation of a flash memory to neutralize trapped holes, according to the present
invention.

Figure 7A is a graph showing an example of a sequence of pulses for an erase
operation of a flash memory to neutralize trapped holes that does not require a higher
negative voltage source, according to the present invention.

30 Figure 7B is a graph showing an additional example of a sequence of pulses
for an erase operation of a flash memory, according to the present invention.

Figure 7C is a graph showing an additional example of a sequence of pulses
for an erase operation of a flash memory

35 Figure 8 is a simplified schematic of a flash memory with P channel wordline
drivers.

Figure 9 is a side cut view of a P channel transistor showing components
relevant to parasitic capacitances.

5 Although, various embodiments have been illustrated using particular electronic components it will be understood by those of ordinary skill in the art that other circuit elements could be used to implement the invention and that the present invention is not limited to the arrangement of circuit elements disclosed. Moreover, it will also be understood in the art that the present invention could be applied to a
10 erasing memory in devices other than flash memory circuits. Therefore, the present invention is not limited to a method and apparatus for erasing flash memory.

Detailed Description

Fig. 1 shows a conventional floating gate memory cell 100 including an n+
15 type source 104, a p type channel 105, an n+ type drain 112, and a p type substrate 102. A floating gate 106 is sandwiched between an insulating dielectric layer 110 and thin tunnel oxide 114 over channel 105. Floating gate 106 is the memory storage element in a flash memory and is electrically insulated from other elements of the memory cell. Control gate 108 is located on top of the insulating dielectric 110 and is
20 positioned over floating gate 106.

Fig. 2 shows a simplified schematic of a flash memory 200 of the present invention. Flash memory 200 includes a control circuit 202 for controlling the operations of the memory such as reading, writing and erasing, column decoder 204,
25 sense amplifiers/bitline drivers 206, column multiplexer 218, wordlines 212, memory array 210, bitlines 208, and row decoder 214 with wordline drivers 216.

An example of the sequence of voltage pulses for a conventional flash memory erase operation is illustrated in Fig. 3. As can be seen, the source-drain
30 voltage is increased to about 5 to 6 V while at the same time the gate-substrate voltage is decreased to about -10 V. This potential difference is held for about 10 ms and then abruptly discharged to zero. The combination of voltage values induces an electric field across tunnel oxide 114 between floating gate 106 and source 104, resulting in tunneling that drives electrons off floating gate 106 and effectively erases
35 the memory cell. At the same time, however, the reverse bias on the junction between body 102 and source 104 injects holes into tunnel oxide 114 and some of these holes become trapped in tunnel oxide 114. Some of the trapped holes remain unneutralized

at the end of an erase operation and/or after subsequent programming. The holes trapped in tunnel oxide 114 may effectively reduce the barrier for low-field electron injection from floating gate 106 into tunnel oxide 114, thus causing SILC and SILC-related charge loss or gain for the flash cell.

An example of SILC in an array of 4096 flash memory cells having polysilicon 1 gates, connected in parallel is shown in Fig. 4. Curve 201 shows the tunnel I-V characteristics (IP1 vs. VP1) for a fresh, unstressed array in a voltage sweep (V-sweep) of the polysilicon 1 gate of the flash memory cells of the array at negative voltage with the substrate and source at ground. As curve 201 demonstrates, leakage current does not begin in a fresh, unstressed array until there is a gate-substrate potential of -10V . Curve 202 shows the result of stressing, *i.e.*, application of successive erase-program cycles on an array of floating gate cells. In this example, stressing is simulated by a constant voltage stress in which the gate-substrate is held at -10V and the source-substrate is held at 6 V , a high reverse junction bias, for 200 seconds. Curve 202 shows that onset of leakage current will occur at an abnormally low voltage of about -7V , after stressing the array. Curves 203, 204 and 205 show successive V-sweeps where the stress voltage has been removed, the gate voltage successively swept to further negative values, and the substrate and source are held at ground. Curves 203, 204 and 205 demonstrate that the SILC is suppressed and the onset of tunneling is advantageously shifted to a higher negative gate-substrate voltage after the array has been subjected to gate V-sweeps at zero voltage across the source-substrate junction. In each successive V-sweep curve, the onset of tunneling is pushed back to a higher voltage, and thus, SILC is more effectively suppressed.

Based on the results above, a qualitative model can be designed for the creation and suppression of SILC. SILC is created and/or enhanced when the gated source diode is subjected to high reverse bias and there is low tunneling current across the gate oxide. These conditions are favorable for hole generation and injection into the gate oxide. On the other hand, SILC may be suppressed when the gated source diode is subjected to a high electron tunneling current across the gate oxide at zero or low reverse current bias for the source junction.

Various approaches may be suggested based on the above model. One possible way to neutralize holes trapped in the tunnel oxide during an erase pulse is to apply a condition of uniform tunneling at high negative gate and low or zero positive

5 source voltage at the end of the erase pulse. This Prior Art approach is illustrated in Fig. 5. As can be seen, two positive 6 V pulses of about 3 ms are applied to the source (V_s) over a 10 ms erase period. A positive 6 V pulse is also applied to the substrate (V_{sub}) concurrent with the second positive source pulse. The gate-substrate voltage (V_G) is held at negative 10V for the entire 10ms period. Application of a
10 positive voltage pulse on the substrate allows the erase operation to be done in a single step channel erase. However, this also requires the added complexity of building the memory array inside a triple well.

A channel erase condition may also be realized by applying an additional voltage pulse of higher negative value to the gate (wordlines) while the source is
15 biased at the same potential as the substrate (ground), after the regular erase pulse. This procedure is illustrated in Fig. 6. As can be seen, a positive pulse of about 5V is applied between source and substrate for a period of about 10 ms. At the same time, the gate substrate voltage is taken to negative 10V. At the end of the 10ms period
20 when the source-substrate voltage is reduced to zero, the voltage between the gate and substrate is increased to negative 15 volts and held at that potential for an additional 5 ms. While this approach can be implemented on a flash memory without a triple well surrounding the array, it has the disadvantage of requiring extra erase time and the supply of a higher negative voltage.

A more convenient approach, illustrated in Fig. 7A, is to discharge the source
25 toward the substrate potential (or other area of common voltage) at the end of the regular erase pulse, while the negative voltage to the control gate (wordlines) is maintained. As can be seen, a positive pulse of about 5V is applied between source and substrate for about 10 ms. At the same time, the gate-substrate voltage is brought to negative 10 V and held for the 10 ms period. At the end of the 10 ms period, the
30 source-substrate potential is discharged rapidly, in a fraction of a millisecond, but the discharge of negative gate-substrate voltage is delayed for a time in the range of 1-100 ms. During this interval the negative voltage is allowed to float and any regulation of the voltage supplied by the negative pump is disabled. The excess negative wordline voltage thus created will be called "negative gate bootstrap" in the following
35 paragraphs. In this case, the rapidly falling source-substrate voltage will couple to the floating gates and onto the control gates (wordlines), in effect, pushing them more negative below the voltage supplied by the negative pump. Thus, the desired

5 condition of relatively high negative voltage for the wordlines and floating gates along with zero voltage source to substrate bias will be realized on a transient basis without the need for generating a higher negative voltage, or for adding extra time to the erase operation.

Fig. 7A depicts the expected behavior for the gate voltage V_{GSub} if the forced
10 discharge of the source V_{SSub} takes place in a time of a fraction of 1 millisecond or faster. The amount of the excess negative gate voltage and its gradual decrease on the waveform for V_{GSub} after the discharge of the source (V_{SSub}) and before the active discharge of the gate represent the capacitive coupling of the V_{SSub} transient and the subsequent natural decay for the voltage on the control gate (wordline) when left
15 floating. The rate of decay depends on the aggregate leakage of the gates, which in turn is determined by the structure and layout of the transistors in the periphery of the memory array which drive the cell control gates, or wordlines. Note that any leakage of the control gates through tunnel oxide as represented in Fig. 4, would not affect the rate of V_{GSub} decay in Fig. 7A since it would not contribute leakage to the control
20 gate.

To the extent that the relevant wordline drivers in the periphery are devised to have low parasitic capacitance compared to the capacitance between the source and the control gate (wordline) of the memory cells on each row, and low leakage, the excess negative voltage V_{GSub} can be larger and hold for a longer time without
25 substantial decay. In the limit of negligible parasitic capacitance and fast discharging of V_{SSub} , the maximum amplitude of excess negative gate voltage would be equal in absolute value to the amplitude of the source voltage. On the other hand, if the leakage of the wordline drivers were ideally zero, the excess negative voltage on the gate would be assumed to hold indefinitely with no decay as long as it is not
30 forcefully discharged to ground potential by external circuitry.

Thus, if the design of the memory circuit fulfills the three conditions described above, i.e.,

1. fast – shorter than 1 ms – discharging for V_{SSub} ,
- 35 2. low parasitic capacitance for wordline drivers – in the order of 1-10 fF or below, and

3. low drain leakage for the same wordline drivers – in the order of pA,

then each erase pulse represented by the waveforms in Fig. 7A can be regarded as a succession of two erase mechanisms: source erase and channel erase, and the relative duration for each mechanism can be adjusted by the designer to fit the specification for a particular memory design.

If a particular memory application requires fast erase and not very stringent retention limits for each particular cell, then such a memory can be designed with a short channel erase time compared to the source erase time. Source erase is inherently more efficient than channel erase at equal applied voltage due to a better coupling factor for the applied voltage. Thus such a design will result in a shorter total erase time, but also in poorer memory retention since the holes generated by the source erase mechanism will have a shorter time to neutralize in the subsequent channel erase part of the erase pulse. Such a design may benefit large density data storage memory in which fast erase/program rates are sought, and data correction provisions like storage of additional parity codes, can be used to correct an inherently weak retention.

At the other end of the spectrum, if a particular memory requires very good retention but does not pose a stringent limit on the erase time, the time for source erase within an erase pulse can be reduced to as little as 1 ms or less, followed by a long time for channel erase of up to 100 ms or more. In this way, most of the electrons stored on the floating gate of each cell will tunnel out during the channel erase part of the erase pulses, and the hole trapping phenomenon associated with source erase will effectively be avoided at the expense of a longer erase time. This approach may be useful in code storage applications where erasure and reprogramming operations occur rarely and do not require fast time rates, but the preservation of stored data over long periods of time is critical.

Negative gate erase can be implemented in flash memory by using a row decoder that includes either all P channel wordline driver transistors, or CMOS drivers with N channel pull-down transistors in triple well. In the following, a possible implementation of “negative gate bootstrap” for the memory with P channel

5 wordline drivers will be described. The same idea with small changes may be applied to the memory with triple-well N channel wordline drivers.

Fig. 8 depicts a design with all P channel driver circuits in the row decoder for a memory device such as memory 200 of Fig. 2, including pull-up transistor 702 and pull-down transistor 704. The circuit drives a wordline 703 coupled to memory cells
 10 706 of the memory device. The voltages V_H and V_L represent respectively the “high” and “low” voltage supply rails. Their absolute values are specific to each memory function like read, program and erase, and their relative difference $V_H - V_L$ is always positive. The values for the pull-up and pull-down signals, labeled respectively A and B, are specific to the memory function and to the selected or unselected condition of
 15 the particular row.

In particular, all rows of a memory block are selected in the erase function, and thus the signals A and B will assume the same values for all wordlines in the block to be erased. A possible set of such values is:

$$V_H = 3.3 \text{ V}; V_L = -10 \text{ V}; A = 3.3 \text{ V}; B = -10 \text{ V}$$

20 This would result in a wordline voltage of -8.5 V to -9 V depending on the threshold voltage of the P channel transistors.

In order to implement the above idea of a “negative bootstrap” for the wordlines in erase mode, the variables V_H , V_L , A, B in the schematic of Fig. 8 may be set to follow the dynamics in Fig. 7B or Fig. 7C below.

25 Capacitive components C_{ws} and C_{wch} in the flash memory array of Figure 8 represent the capacitance between a wordline and the source of all the memory cells, and respectively, the capacitance between a wordline and the channel of all the memory cells. During an erase, the channel is in accumulation state and thus electrically connected to the common substrate for all the memory cells in a block.

30 The falling edge of the source pulse V_{SSub} in Figs. 7A, 7B and 7C induces the negative bootstrap (negative overvoltage) on V_{GSub} by capacitive coupling through C_{ws} . If we ignore the parasitic capacitances of the driver transistors, the magnitude of the negative voltage overshoot can be calculated as:

$$|\Delta(V_{GSub})| = V_{SSub} * C_{ws} / (C_{ws} + C_{wch}).$$

35 Thus, the negative bootstrap will improve as C_{ws} is increased and/or C_{wch} is decreased.

5 If erase is implemented as in Fig. 7B, the parasitic capacitance components C_{gd} and C_j for all the P channel transistors in the row decoder in Fig. 8 need to be reduced in order to enhance the capacitive coupling of the wordline in the “negative bootstrap” effect. The gate-to-drain parasitic capacitance C_{gd} has a component of overlap of drain diffusion by the gate and another related to the fringing field between
10 drain surface and gate stack sidewall. Both of these components can be reduced with the help of an oxide spacer located between the gate sidewall and the adjoining drain diffusion. A low drain-to-body junction capacitance C_j can be obtained by using low doping concentration for the drain diffusion and/or low doping concentration in the channel (N well).

15 On the other hand, the dynamics of Fig. 7C can be implemented for erase. Voltages V_H and A are reduced in Fig. 7C at the end of the V_{SSub} pulse. In this case all the parasitic capacitances in Fig. 8 with the exception of C_{gd} for pull-down transistor 704 (capacitive coupling between wordline and the signal B) are in fact aiding the coupling for “negative bootstrap” and need not be minimized. The
20 coupling for negative bootstrap can be further increased in such a case by providing an extra capacitor 710 between the V_H supply and the wordline in the circuit as shown in Fig. 8.

The retention of excess negative voltage V_{GSub} during the channel erase part of the erase pulse is adversely impacted by the drain-to-body leakage of the P channel
25 transistors driving the wordline. This leakage is represented in Fig. 8 by a variable current generator 708 between the source/drain diffusion and the body of the transistor (N well). In practice, an important component of such leakage is known as gate-induced drain leakage (GIDL) and is strongly increasing with the voltage drop between gate and drain. Thus, GIDL appears of concern only for the pull-up P
30 channel transistor 702 in Fig. 8 in which the gate-to-drain voltage drop is large in erase. Such voltage drop is smaller for the erase dynamics according to Fig. 7C, this scheme appears to offer advantages in both coupling and retention for the excess negative gate voltage.

In terms of transistor structure, the features listed above for reducing the
35 parasitic gate-to-drain capacitance like a gate spacer and/or low doping concentration for the drain diffusion are also conducive to reduced GIDL. Fig. 9 depicts an exemplary P channel MOSFET structure 802 with all the components relevant to the

5 parasitic capacitances C_{gd} , C_j shown. In order to minimize parasitic capacitance and decrease GIDL the wordline drive transistors should be fabricated so that lightly doped drain (LDD) regions are present as shown in Fig. 9 so as to minimize parasitic capacitance. In addition a low k dielectric SiO₂ gate spacer may be added to reduce parasitic capacitance. Other techniques may likewise be applied to reduce parasitic
10 capacitance as would be familiar to those of ordinary skill in the art.

Thus, as can be seen from the foregoing, memory devices can be designed to comply with a fixed specified erase time and retention performance. On the other hand, a new kind of memory can be designed in which the respective durations of source erase and channel erase can be made adjustable by way of algorithm codes
15 stored in a special function register or other nonvolatile memory dedicated to such control parameters. In this way, the manufacturer can build a generic memory part and then adjust the duration for either erase mechanism at the time of manufacturing test, or else let the user make such adjustment before or after the device has been assembled in the system for the end use.

20

Conclusion

A method and apparatus for erasing flash memory has been described. The method includes supplying a negative voltage pulse to the control gate of a memory cell for an erase period, supplying a positive voltage pulse to the source of the
25 memory cell for a period that is shorter in duration than the erase period; and discharging the positive voltage pulse at the end of the second period wherein discharging the positive voltage pulse at the end of the second period effectively increases the magnitude of the negative voltage pulse.

Although specific embodiments have been illustrated and described herein, it
30 will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A method of erasing a non-volatile memory cell comprising a control gate, a floating gate, a source, a drain and a substrate, the method comprising:
 - supplying a negative voltage pulse to the control gate relative to a common voltage for an erase period;
 - supplying a positive voltage pulse to the source relative to the common voltage for a second period that is shorter in duration than the erase period; and
 - discharging the positive voltage pulse at the end of the second period,wherein discharging the positive voltage pulse at the end of the second period effectively increases the magnitude of the negative voltage pulse.
2. The method of claim 1 further comprising adjusting the length of time for the negative and positive voltage pulses to obtain a relative contribution of source erase and channel erase to achieve a desired balance between data retention and erase speed.
3. The method of claim 2 further comprising adjusting a relative contribution of source erase and channel erase to achieve a desired balance between data retention and erase speed in an erase algorithm.
4. The method of claim 3 wherein the desired balance between data retention and erase speed is configurable during a manufacturing process.
5. The method of claim 3 wherein the desired balance between data retention and erase speed is adjustable by a user.
6. The method of claim 1 wherein the second period is shorter than the erase period by about 2 ms.
7. The method of claim 1 wherein the increase in magnitude of the negative voltage pulse is greater than 3 volts.

8. A method of erasing non-volatile memory cells in a memory comprising respective sources, drains, floating gates and control gates, the method comprising:
 - applying a negative voltage relative a common voltage to the control gate of one or more of the cells beginning at a first time;
 - applying a positive voltage relative the common voltage to the source of each of the one or more cells beginning at about the same time as the first time;
 - discharging the positive voltage at a second time occurring after the first time,
 - increasing the negative voltage at the second time; and
 - discharging the negative voltage at a third time occurring after the second time.
9. The method of claim 8 wherein an increase in negative voltage at the second time is effected by a rapid discharge of the positive voltage pulse at the second time such that it couples to the control gate.
10. The method of claim 8 wherein amplitude of the negative voltage is effectively increased by using wordline drive transistors with low parasitic drain capacitance compared with a wordline capacitance.
11. The method of claim 10 wherein the low parasitic drain capacitance is obtained by adjusting a doping concentration of the wordline drive transistors.
12. The method of claim 11 wherein adjusting a doping concentration of the wordline drive transistors comprises lowering the doping concentration of a drain, a channel region near the drain, or both, of the wordline drive transistors.
13. A method of erasing non-volatile memory cells comprising respective sources, drains, floating gates and control gates, the method comprising:
 - applying a voltage of a first polarity relative a common voltage to the control gate of one or more of the cells beginning at a first time;
 - applying a voltage of a second polarity relative the common voltage to the source of each of the one or more cells beginning approximately at the first time;

discharging the voltage of the second polarity at a second time occurring after the first time,

allowing the voltage of the first polarity to float beginning at the second time;
and

discharging the voltage of the first polarity at a third time at least **two** microseconds after the second time.

14. The method of claim 13, wherein the first polarity is negative and the second polarity is positive.

15. The method of claim 13, wherein the first voltage is between 4 and 6 V.

16. The method of claim 15, wherein the second voltage is between -8 and -13V.

17. The method of claim 13 wherein the amplitude of the negative voltage is effectively increased by using wordline drive transistors with low parasitic drain capacitance compared with a wordline capacitance.

18. The method of claim 17 wherein parasitic drain capacitance of the wordline drive transistors is lowered by lightly doping the wordline drive transistors.

19. The method of claim 17 wherein parasitic drain capacitance of the wordline drive transistors is lowered by including gate spacers.

20. The method of claim 13 further comprising using wordline drive transistors with low drain leakage to reduce discharge of the voltage of the first polarity after the discharge of the voltage of the second polarity.

21. A method of erasing a non-volatile memory cell comprising a control gate, a floating gate, a source, a drain and a substrate, the method comprising:

applying a positive voltage to the source relative a common voltage for a first predetermined period;

applying a negative voltage to the control gate relative the common voltage;
discharging the positive voltage at the end of the first predetermined period;
disabling any voltage regulation of the negative voltage at the end of the first predetermined period; and

extending the time for discharge of the negative voltage by a predetermined delay period beyond the end of the first predetermined period.

22. The method of claim 21 wherein an increase in the negative voltage is effected during the predetermined delay period by rapidly discharging the positive voltage at the end of the first predetermined period.

23. The method of claim 21 wherein amplitude of the negative voltage during the predetermined delay period is increased by using wordline drive transistors with low parasitic drain capacitance compared with a wordline capacitance.

24. The method of claim 21 wherein holes are removed from a tunnel oxide between the floating gate and the source during the predetermined delay period.

25. A method of erasing a memory cell comprising a control gate, a floating gate, a source, a drain and a substrate, the method comprising:

applying a negative voltage to the control gate relative a common voltage;
applying a positive voltage to the source relative the common voltage;
discharging the positive voltage;

increasing the negative voltage at the same time that the positive voltage has been discharged; and

discharging the negative voltage after an increase in the negative voltage has been achieved.

26. The method of claim 25, wherein the negative voltage is effectively increased by rapidly discharging the positive voltage.

27. The method of claim 26 further comprising adjusting the length of time for the negative and positive voltages to obtain a relative contribution of source erase and channel erase to achieve a desired balance between data retention and erase speed.

28. The method of claim 26 further comprising adjusting a relative contribution of source erase and channel erase to achieve a desired balance between data retention and erase speed in an erase algorithm.

29. The method of claim 28 wherein the desired balance between data retention and erase speed is configurable by algorithm fuses.

30. The method of claim 28 wherein the desired balance between data retention and erase speed is adjustable by a user.

31. The method of claim 26 wherein the increase in negative voltage neutralizes holes trapped in a tunneling oxide between the floating gate and the source.

32. A method of erasing a memory cell comprising a control gate, a source, a drain and a substrate, the method comprising:
 applying a negative pulse to the control gate for an erase period;
 applying a positive pulse to the source at approximately the beginning of the erase period;
 discharging the positive pulse after a first predetermined period; and
 discharging the negative pulse after a second predetermined period, the second predetermined period being longer than the erase period.

33. The method of claim 32 wherein a number of holes trapped in a tunnel oxide located between a floating gate and a channel region are reduced during the predetermined delay period.

34. The method of claim 32 wherein the negative voltage is increased during the predetermined delay period as a result of the discharging of the positive pulse.

35. A flash memory, comprising:
at least one memory cell comprising a source, a drain, a control gate, a floating gate and a substrate; and
a memory control circuit,
a wordline;
a plurality of wordline drive transistors;
wherein the memory control circuit provides for application of a positive voltage between the source and an area of common voltage for a first predetermined period and application of a negative voltage between the gate and an area of common voltage for a second predetermined period, the second predetermined period beginning at about the same time as the first predetermined period and ending a predetermined delay after the end of the first predetermined period.
36. The flash memory of claim 35 wherein the positive voltage is discharged rapidly at the end of the first predetermined period.
37. The flash memory of claim 35 wherein the magnitude of the negative voltage effectively increases during the predetermined delay.
38. The flash memory of claim 37 wherein the magnitude of the negative voltage increases during the predetermined delay by about 5V.
39. The flash memory of claim 37 wherein a magnitude of the negative voltage effectively increases during the predetermined delay.
40. The flash memory of claim 37 wherein the positive voltage applied between the source and an area of common voltage is between 3 and 6 V.
41. The flash memory of claim 40 further comprising wordline drive transistors having a low parasitic drain capacitance compared with wordline capacitance.
42. The flash memory of claim 41 wherein the low parasitic drain capacitance is achieved, at least in part, by LDD regions.

43. The flash memory of claim 41 wherein the low parasitic drain capacitance is achieved, at least in part, by gate spacers.
44. The flash memory of claim 40 wherein the negative voltage applied before the predetermined delay between the gate and an area of common voltage is about 10 volts.
45. A method of erasing a flash memory cell, comprising a source, control gate, floating gate, drain and substrate, the method comprising:
applying a positive voltage pulse of a first predetermined duration to the source relative to a common voltage; and
approximately contemporaneously applying a negative voltage pulse of a second predetermined duration to the control gate relative to the common voltage, the second predetermined duration being longer than the first predetermined duration.
46. The method of claim 45, wherein the negative voltage effectively increases after the positive voltage has been discharged.
47. A method of decreasing holes in the tunnel oxide of a memory device comprising a source, a control gate, a floating gate, a drain and a substrate, the method comprising:
using a decrease in a source voltage to increase the magnitude of a negative voltage applied between the control gate and a common reference voltage.
48. The method of claim 47 wherein the decrease in the source voltage occurs rapidly.
49. The method of claim 47 wherein the increase in negative voltage is effected by capacitive coupling.
50. The method of claim 47 wherein the increase in negative voltage is augmented by providing a capacitor between the wordline and a positive voltage supply.

51. A method of decreasing holes in the tunnel oxide of a memory device comprising a source, a control gate, a floating gate, a drain and a substrate, the method comprising:

using a decrease in a voltage applied to the source that is positive with reference to a common voltage to couple a voltage to the control gate that is negative with reference to the common voltage.

52. The method of decreasing holes in the tunnel oxide of a memory device comprising wherein the coupling is augmented by a capacitor.

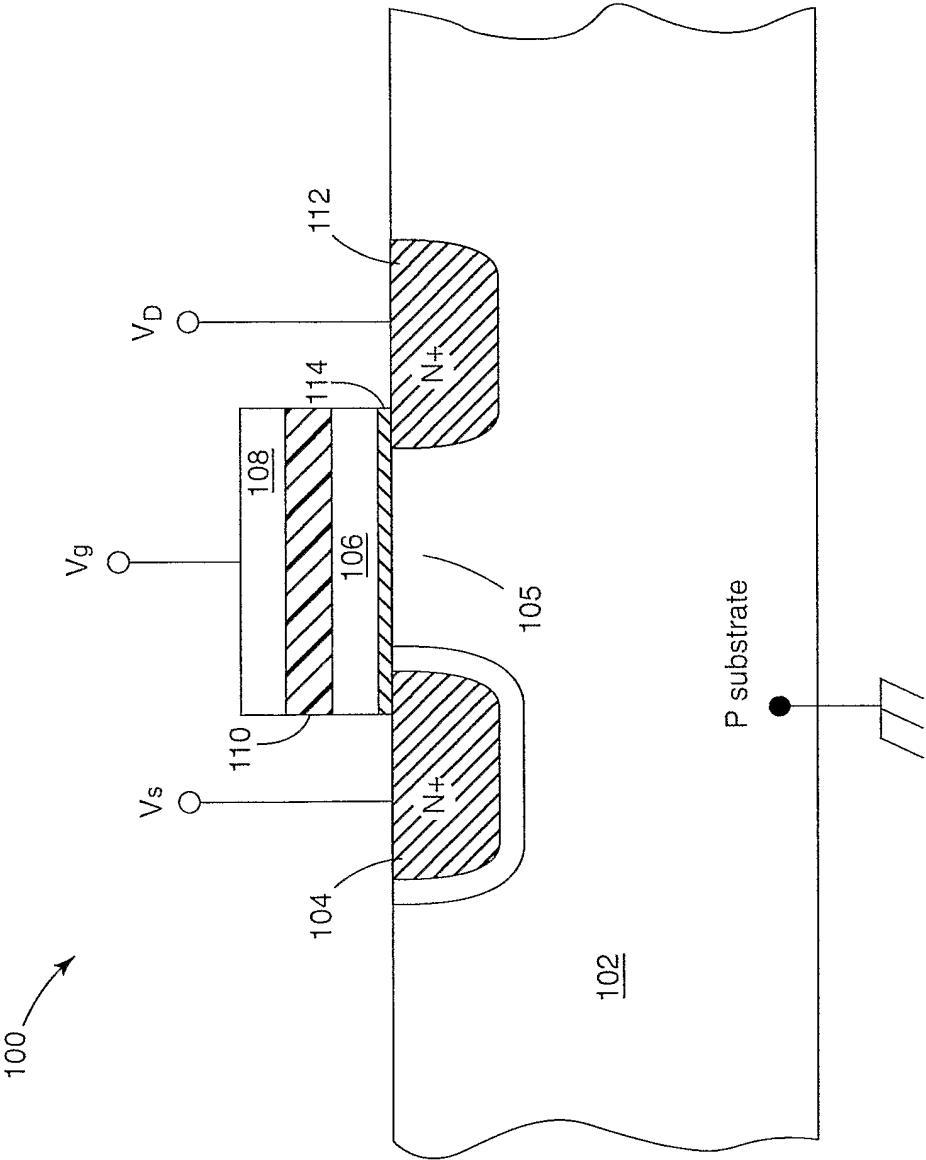


Fig. 1
Prior Art

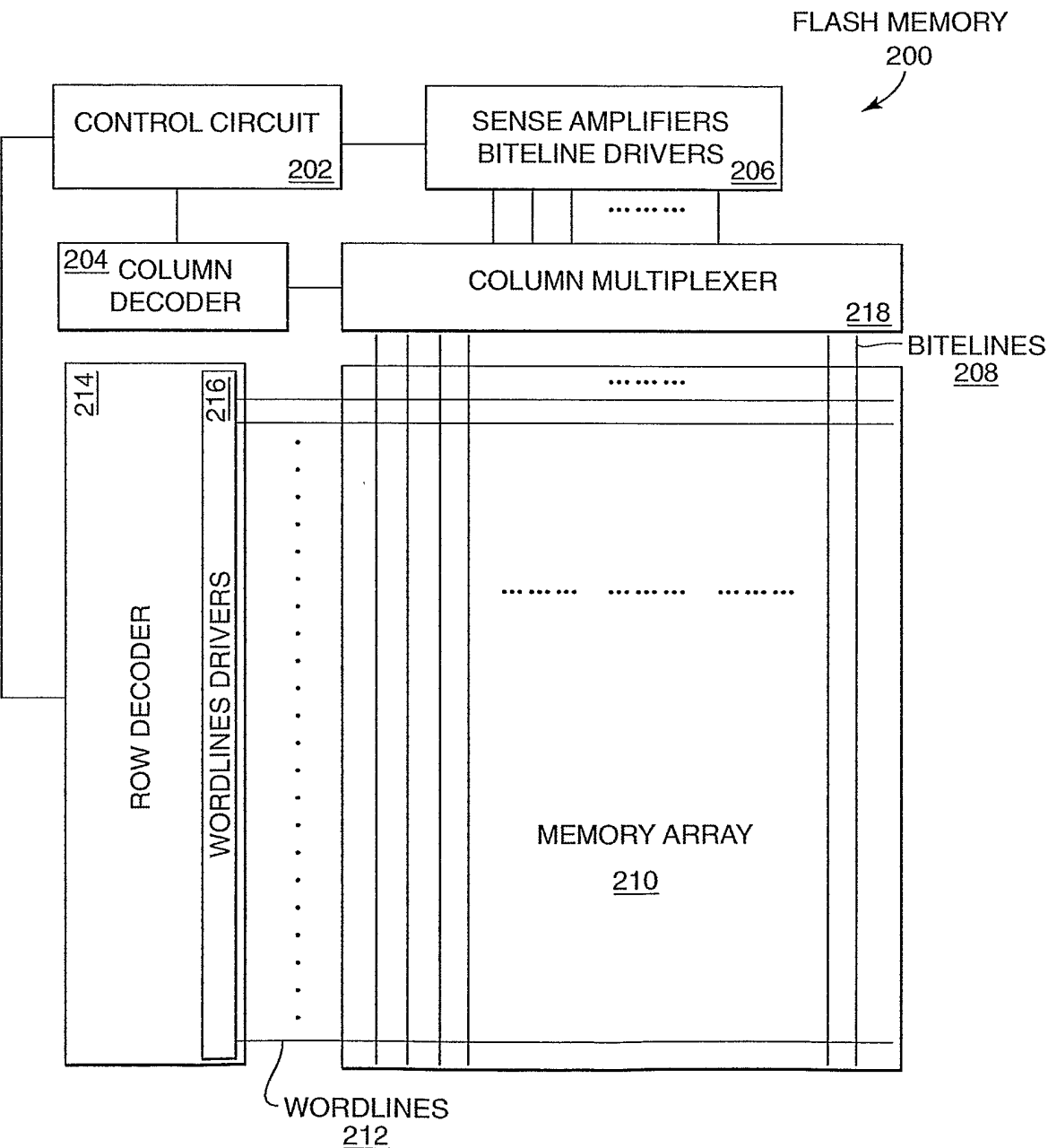


Fig. 2

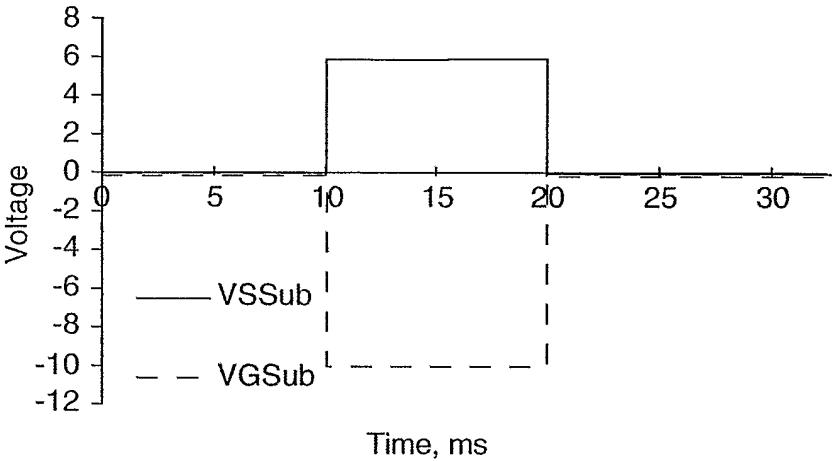


Fig. 3
Prior Art

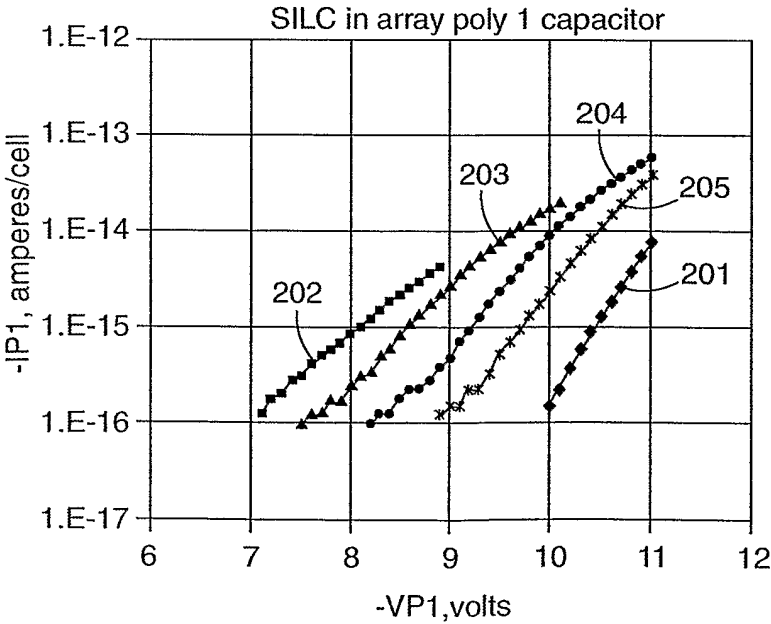


Fig. 4

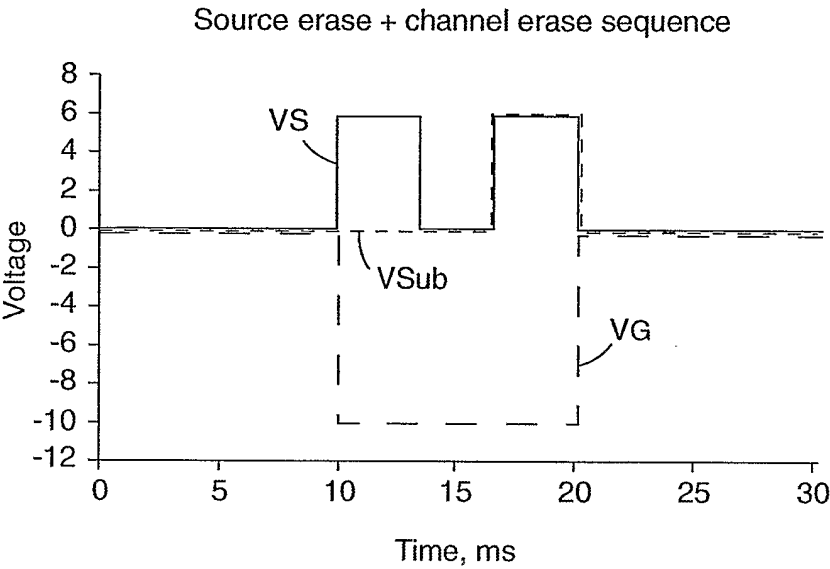


Fig. 5
Prior Art

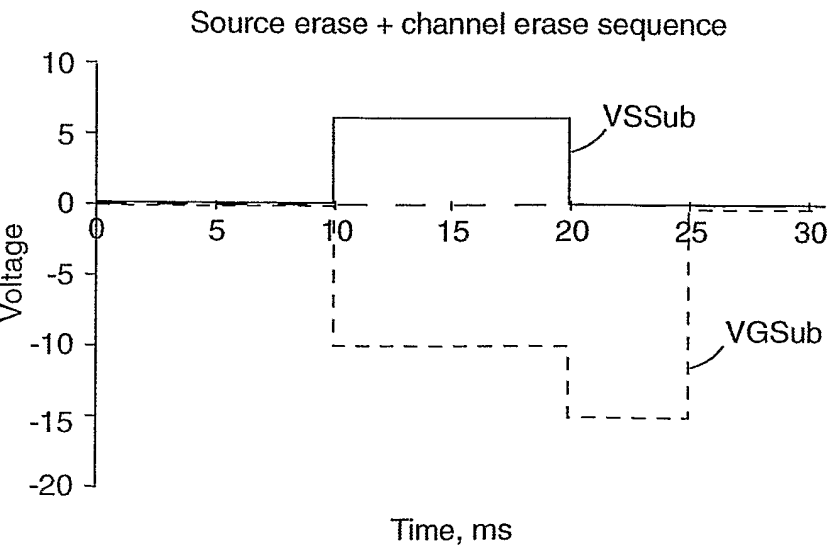
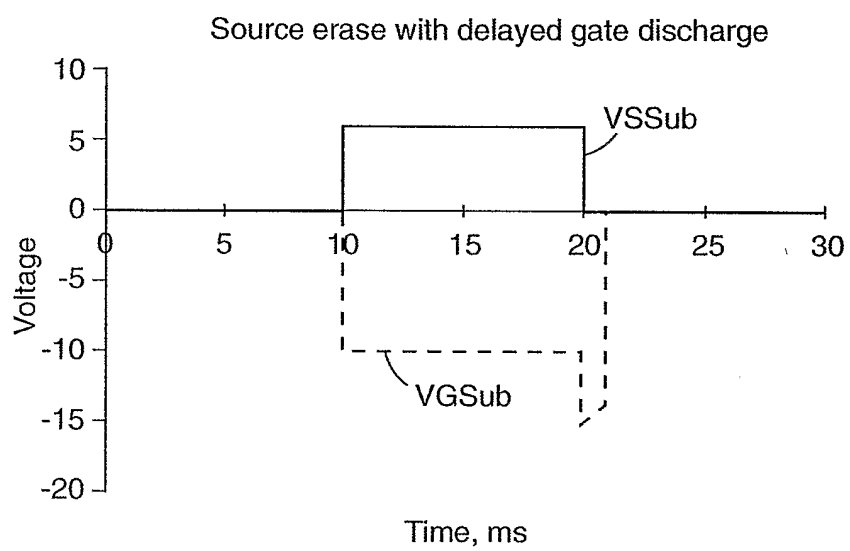


Fig. 6

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*Fig. 7A*

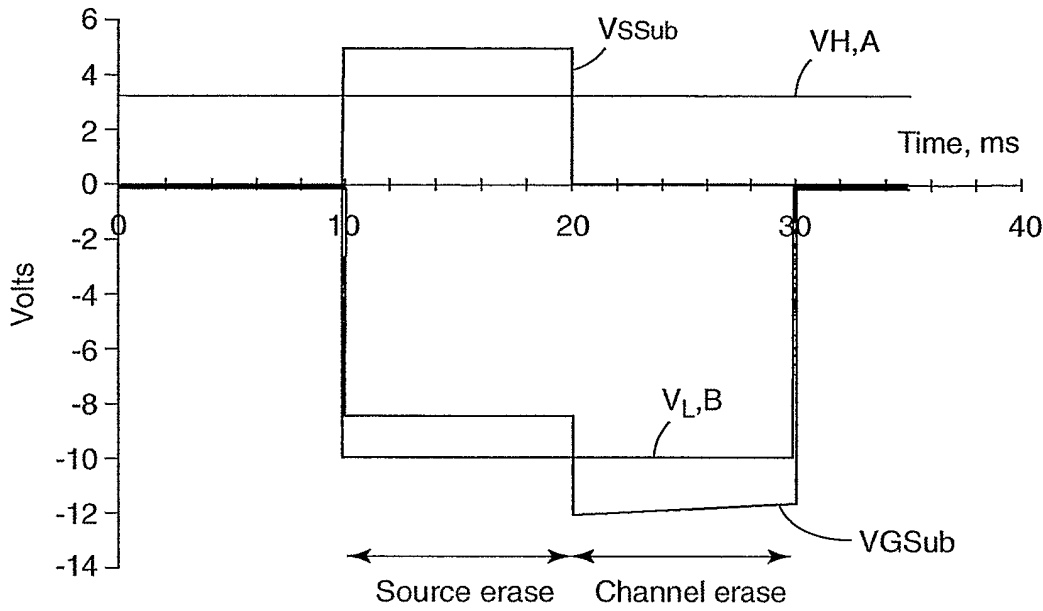


Fig. 7B

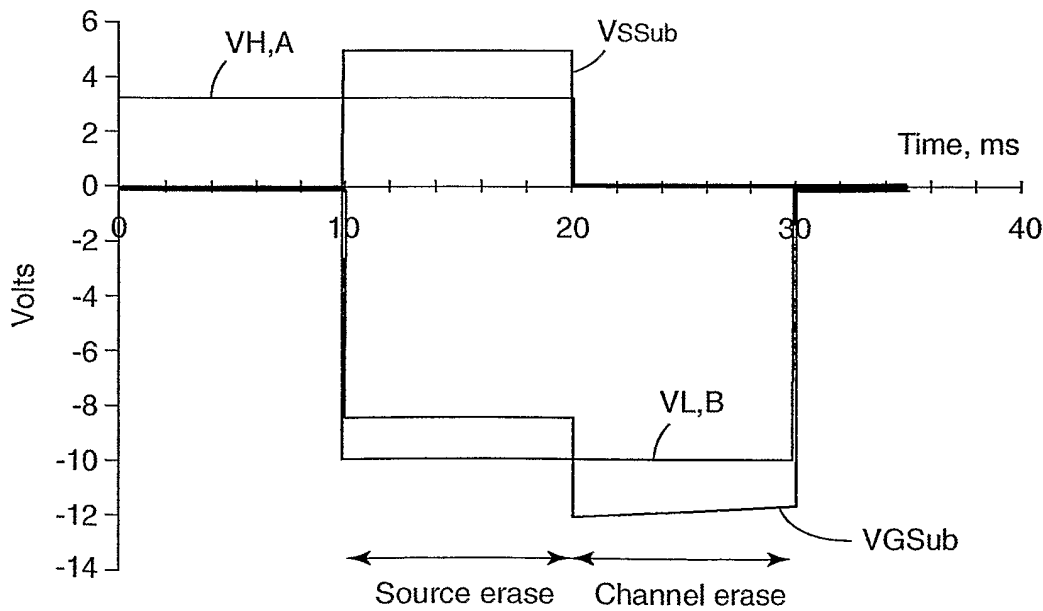


Fig. 7C

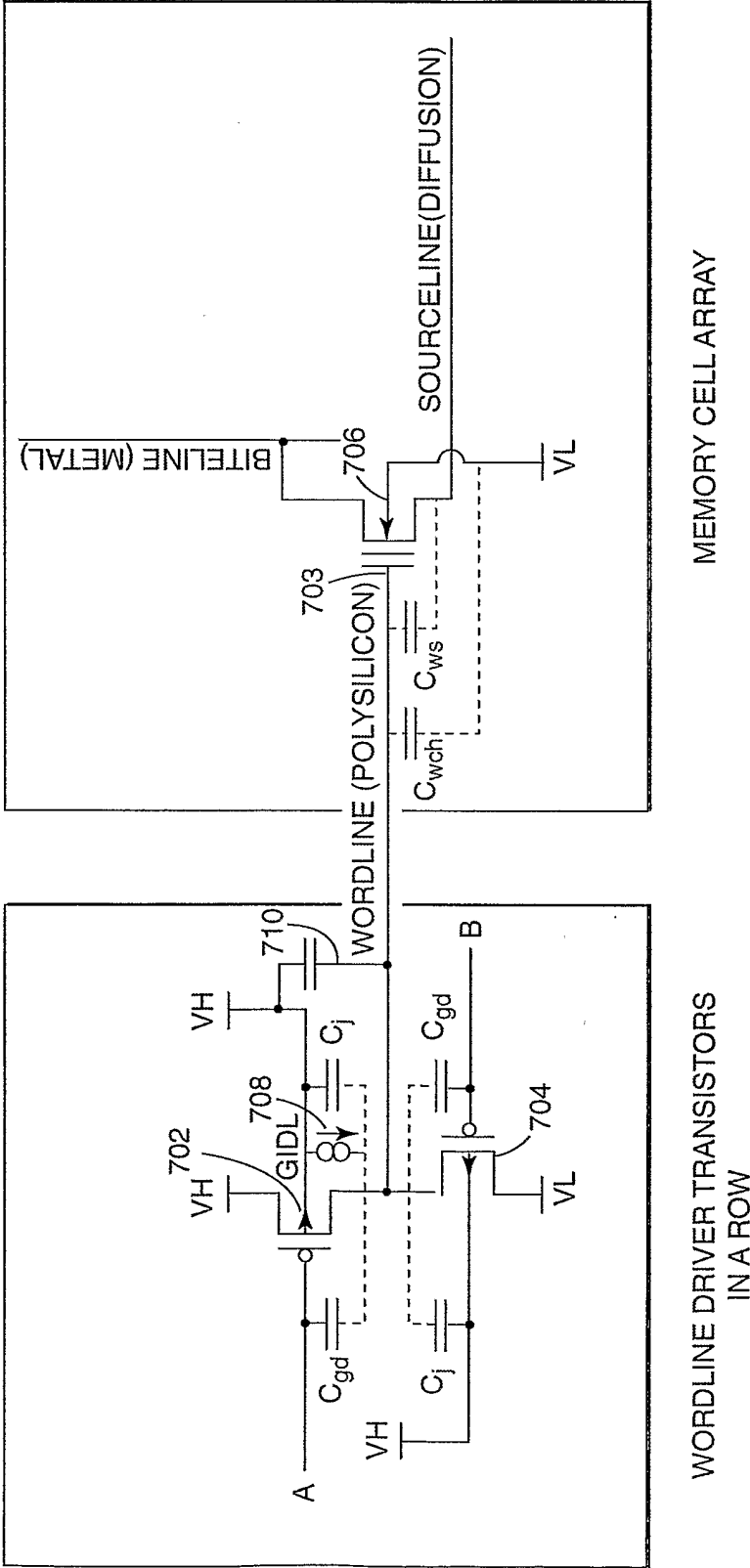


Fig. 8

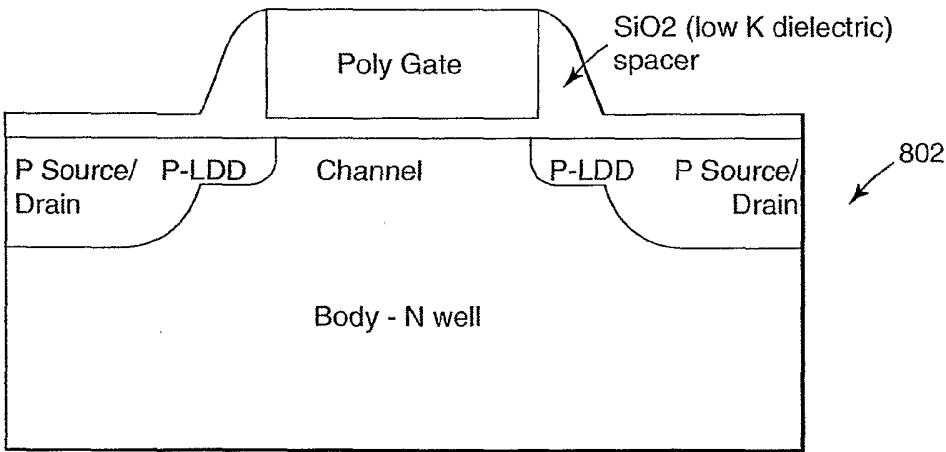


Fig. 9