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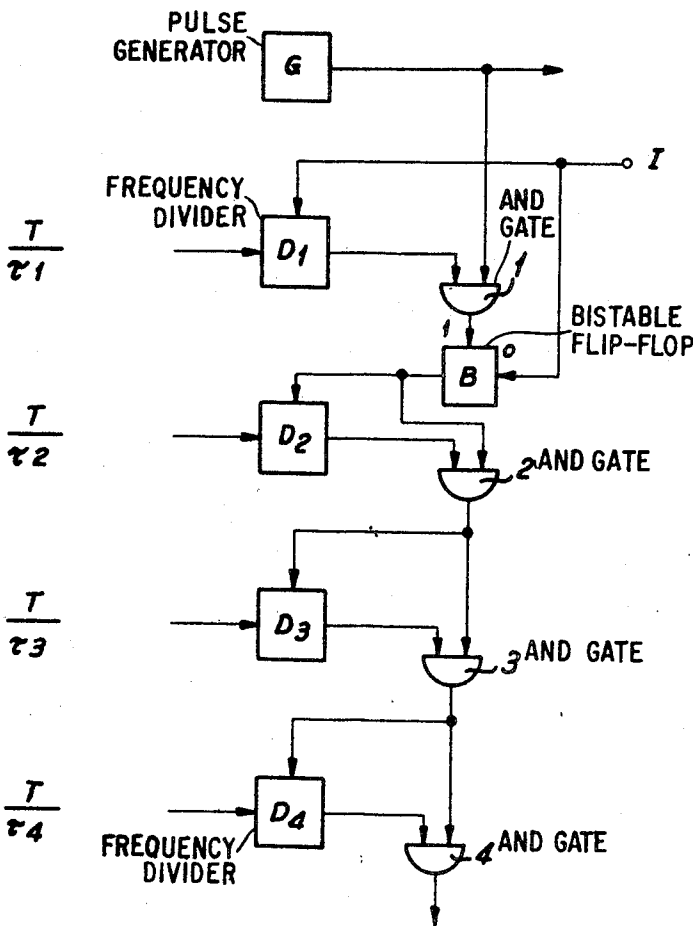
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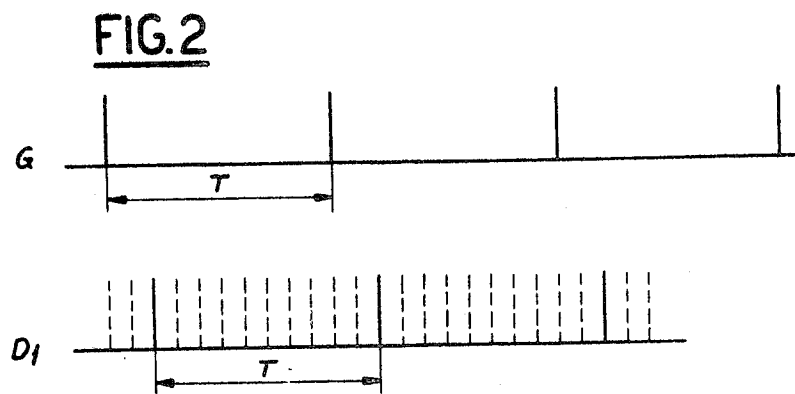
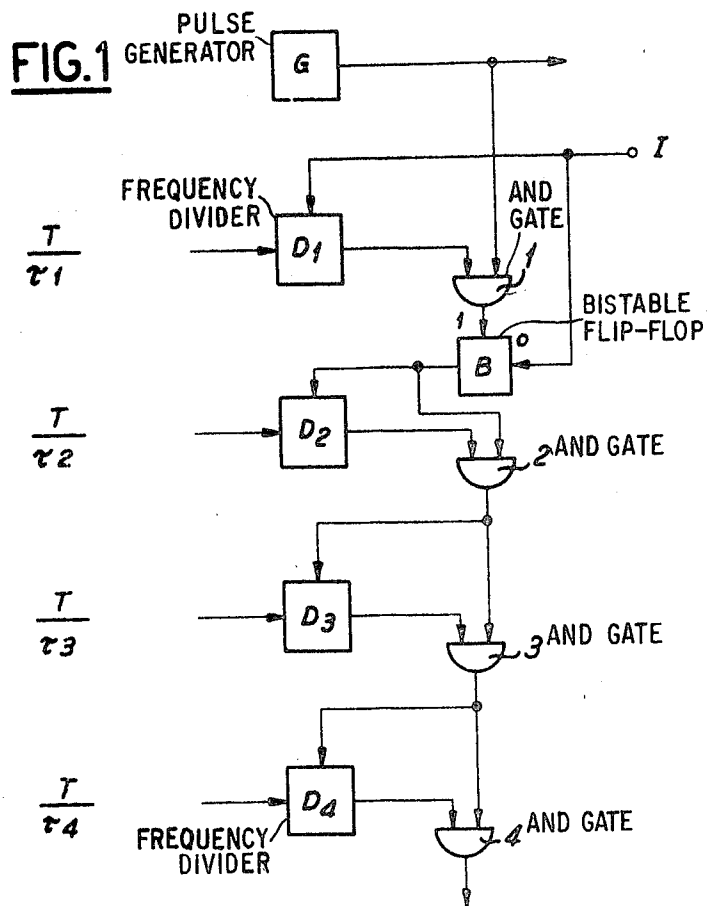
[54] **DEVICE FOR COUNTING IMPULSES**
6 Claims, 2 Drawing Figs.

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307/225, 307/295, 328/55, 328/133
[51] Int. Cl..... **H03k 21/00**
[50] Field of Search..... **328/39, 40,**
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ABSTRACT: This disclosure concerns a device for counting impulses which has a generator of reference signals emitted with a given period of repetition, at least one dephasing device delivering a periodic signal with a period equal to the reference period and whose phase is modified progressively by the impulses to be counted which are applied thereto and a comparison signal for the phase of the reference signal and the phase delivered by the dephaser, the difference in phase being proportional to the number of impulses counted.





DEVICE FOR COUNTING IMPULSES

Counting devices capable of preserving their state even during the absence of input impulses known heretofore necessitate a large number of elements and are not foolproof if one only has a limited energy.

The present invention has for its object a device for counting impulses which eliminates the above mentioned disadvantages. The device according to the invention is characterized by the fact that it comprises a generator of reference signals emitted with a given period of repetition, at least one dephaser delivering a periodic signal with a period equal to the period of reference and whose phase is modified progressively by the impulses to be counted which are applied thereto, and a circuit for comparing the phase of the reference signal and the phase delivered by the dephaser, the difference in phase being proportional to the number of impulses counted. The accompanying drawing represents by way of example one embodiment of the invention.

FIG. 1 shows a schematic block diagram of a counting device.

FIG. 2 is a diagram showing the operation of the device. The counting device shown comprises an impulse generator G giving a reference signal of a period T and four frequency dividers D1, D2, D3 and D4 having dividing factors of τ_1 , τ_2 , τ_3 , and τ_4 . These dividers are fed by impulses of periods (T/τ_1) , (T/τ_2) , (T/τ_3) and (T/τ_4) , respectively in order that they may deliver their output impulses having a period T.

The dividers are used as dephasers to obtain this dephasing, it suffices that it be possible to vary momentarily their dividing rate by plus or minus 1 by the application of an additional impulse. These additional impulses are constituted for the divider D1 by impulses to be counted applied to input 1 and for the following dividers by an impulse triggered by the previous divider.

The impulses delivered by the reference generator G and the dividers D1 are applied to a first and gate 1 whose output signal is applied to a bistable circuit B whose output signal is applied on the one hand to divider D2 and on the other hand to a second gate 2 to which is also applied the output of the divider D2. The signal delivered by gate 2 is applied on the one hand to divider D3 and on the other hand to a third gate 3 whose output signal is itself applied to divider D4 and a fourth gate 4.

The operation of the counter is as follows:

Generator G and divider D1 deliver impulses represented in FIG. 2, impulses which are generally dephased. These signals are therefore not simultaneously applied to gate 1 which remains closed.

Each time that an impulse appears at input 1, the dephasing between the impulses of generator G and those coming out of divider D1 increases until the moment when the impulse delivered by divider D1 catches the impulse of generator G which precedes it. At this moment there is coincidence at gate 1 which delivers an impulse which causes the bistable circuit B, maintained heretofore in the zero state by the impulses to be counted, which are applied thereto, to state 1, in such a way that an impulse is applied to divider D2. It appears immediately from FIG. 2 why it is necessary to have in the circuit a bistable element B. It can be seen in effect that when there is coincidence between the impulses delivered by generator G and those delivered by divider D1 and no impulse appears at the input after the first coincidence, this coincidence repeats with period T in such a way that in the absence of the bistable circuit, repeated impulses would be applied from divider D2 which would count accordingly tenths in a decimal counter for example, in the absence of impulses in input 1. Owing to bistable circuit B, a single impulse reaches divider D2, bistable B not returning to its zero state which allows it, by flipping from zero to 1, to deliver a new impulse to divider D2 when a new impulse appears at input 1.

For the following stages, it is not necessary to provide this bistable element since the following gates 2, 3 and 4 no longer receive periodic reference signals and can only be open during flipping of bistable circuit B from zero to 1. It should be men-

tioned in effect that it is not the continuous state 1 of the bistable which is applied to gate 2, which would have no sense, but an impulse obtained by a monostable circuit or an intermediate derivative circuit

The counting obtained is independent of period T. In effect, if the condition of coincidences on gate 1 is expressed algebraically:

$$xT = yT + n(T/\tau_1) \text{ or}$$

$$x = \text{whole number}$$

$$T = \text{period of the reference signal}$$

$$y = \text{whole number}$$

$$n = \text{whole number}$$

$$\tau_1 = \text{dividing rate of D1.}$$

It is seen that T disappears from the equation and that the number impulses at the output of gate 1 is equal to $n' = (n/\tau_1)$.

It is easy to demonstrate in the same manner that the number of impulses at the output of gate 2 is equal to $(n/\tau_1\tau_2)$, at the output of gate 3 $(n/\tau_1\tau_2\tau_3)$ and so forth.

It is also possible to place in a memory the information contained in the dividers D1 to D4 by means of a similar system formed of dividers D1 to D4 actuated in parallel fashion and synchronously with dividers D1 to D4.

Dividers D1 to D4 can be constituted by binary circuits or impulse accumulators.

These circuits being used as dephasers, it is evidently possible to use dephasers of known type to which there would be applied on the one hand a reference signal and on the other hand the impulses to be counted to modify by any known means the dephasing introduced by the dephaser.

I claim:

1. A device for counting impulses comprising generator means having an output for producing reference signals having a first repetitive period; first dephasing circuit means having input means for receiving input pulses to be counted and a second repetitive signal, and having output means for producing a second periodic signal at the same rate as said first repetitive period and for progressively modifying the phase of said second periodic signal in response to reception of said pulses to be counted; and comparison circuit means having two inputs connected respectively to said generator output and said output means of said dephasing circuit means and having an output for producing a comparison pulse when signals are received simultaneously at said two inputs to said comparison circuit means, whereby the phase difference at said two inputs to said comparison circuit means is proportional to the number of said pulses to be counted which are received by said dephasing circuit means.

2. A device according to claim 1, wherein said dephasing circuit means comprises a frequency divider, and in which said second repetitive signal has a frequency equal to a submultiple of said reference period, said submultiple corresponding to the dividing rate of said frequency divider.

3. A device according to claim 1, wherein said comparison circuit means comprises a first AND circuit.

4. A device according to claim 3 comprising of a second said dephasing circuit means and a second said AND circuit, said second AND circuit having two inputs and an output, and said second dephasing circuit means having input means for receiving a third repetitive signal and being coupled to said output of said first AND circuit, and said second AND circuit having one of its said inputs coupled to said output means of said second dephasing circuit means, and the other of its said inputs coupled to said output of said first AND circuit.

5. A device according to claim 4, further comprising a bistable flip-flop circuit having two inputs and one output, means coupling said pulses to be counted to one of said flip-flop inputs, the other said flip-flop input being connected to said output of said first AND circuit, and said flip-flop output being coupled to said second dephasing circuit means and to said other input of said second AND circuit.

6. A device according to claim 1, comprising a second dephasing circuit means connected in parallel and synchronized with said first dephasing circuit means for memorizing the state of said counting device.