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(54) **Title**: LDMOS DEVICE AND FABRICATION METHOD THEREOF

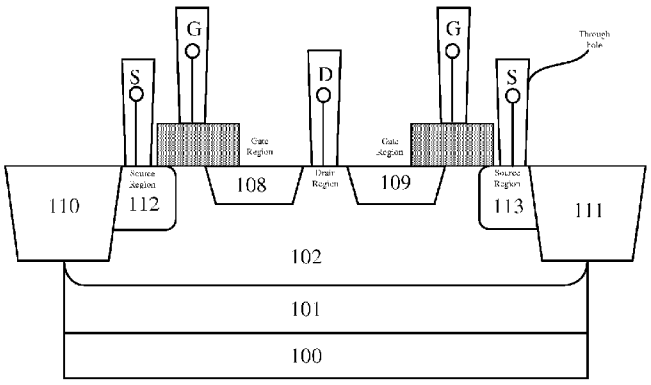

FIG. 8

(57) **Abstract**: A method of fabricating a LDMOS device includesproviding a substrate having a body layer, an epitaxial layer overlying the body layer, and a deep well region disposed in a middle portion of the epitaxial layer, forming an isolation dielectric layer on the deep well region and forming a hard mask layer on the isolation dielectric layer, forming a shallow trench in the deep well region by a mask having a drift region pattern, and forming a shallow trench dielectric layer in the shallow trench. The method further includes forming a deep trench at an edge of the deep well region, filling the deep trench with a dielectric material, and planarizing the filled deep trench and the shallow trench dielectric layer. The method also includes forming a groove above the drift region, and filling a dielectric layer in the groove.

WO 2012/079458 A1

Description

Title of Invention: LDMOS DEVICE AND FABRICATION METHOD THEREOF

[1] BACKGROUND

[2] Technical Field

[3] The present disclosure relates to fabrication methods of semiconductor, and more particularly, to a LDMOS device and fabrication methodof a LDMOS device.

[4] Discussion of Related Art

[5] As semiconductor technology continues to develop rapidly, LDMOS (lateral double-diffused metal oxide semiconductor field effect transistor, Lateral Double-diffuse MOS) devices, because of their good short channel characteristics, are widely used in mobile phones. LDMOS devices areparticularlysuitable in 900MHz cellular phone applications. As the mobile communications market (especially the cellular market) continues to grow, manufacturing processes of LDMOS devices become increasingly sophisticated.

[6] In a traditional process, the fabrication method of a LDMOS device includes forminga drift region and a source region on a substrate.In a LDMOS device, the drift region is provided between the channel region and the drain region. A field oxide layer is formed over the drift region by a local oxidation of silicon (Local Oxidation of Silicon, LOCOS) process, and the field oxide layeris used as an isolation layer. The conventional fabrication method of the LDMOS device specifically includes the following steps:

[7] (i) A thin silicon dioxide layer is grown on a silicon substrate, and then a silicon nitride layer is deposited on the silicon dioxide layer,the silicon dioxide layer is provided to avoid stress damagecaused by the silicon nitride.

[8] (ii)A photoresist is spin-coated on the silicon nitride layer, and a mask for exposure is definedon the drift region, a photoresist layerhaving a drift pattern is formed by exposing.

[9] (iii) The photoresist pattern is used as a mask for etching, a predetermined thickness of the silicon dioxide layer is retained while etching, to avoid damage.

[10] (iv) The silicon dioxide layer is grown using the local oxidation of the silicon nitride layer located outside the drift region as a mask. The thickness of the silicon dioxide layer can be determined according to the device characteristics.

[11] In step (iv), the growing silicon dioxide layer will be spread horizontally, such that a 'beak' area is formed near thesilicon nitride mask layer, which is negatively impacts further reduce the size of the LDMOS device. Generally, the field oxide layer is

formed over the drift region by LOCOS process, which is applied for a 0.25μm process. With shrinking of device dimensions, especially for 0.18μm process and below, using the above process to form field oxide layer as a barrier cannot meet the user requirements.

[12] In addition, the field oxide layer is formed above the drift region, and the thickness of the field oxide layer is rising about 50% higher over the surface of the substrate, therefore, a protruding portion is formed over the drift region. In a subsequent chemical mechanical polishing (Chemical Mechanical Polishing, CMP), due to the presence of theprotruding portion,the silicon dioxide layer near the drift region is grinded incompletely, resulting in a defective workmanship of manufacturing.

[13] Therefore, a LDMOS device and a fabrication method thereofare desired in order to overcome the above-described shortcomings.

[14] SUMMARY OF THE INVETION

[15] The present disclosure provides a LDMOS device and afabrication method of the LDMOS device. The fabrication method of the LDMOS device is compatible with conventional 0.18μm process technology and below. Furthermore, LDMOS devices manufactured by the method can achieve overall planarization of a surface of the substrate in a subsequent CMP process, and do not have the shallow trench dielectric layer protruding above the surface of the substrate, thereby reducing process defects.

[16] In one embodiment, a method of fabricating a LDMOS deviceincludes providing a substrate having a body layer, an epitaxial layer and a deep well region disposed in a middle portion of the epitaxial layer;

[17] forming an isolation dielectric layer on the epitaxial layer and a hard mask layer on the isolation dielectric layer;

[18] forming a shallow trench in the deep well of the epitaxial layer using a mask having a drift region pattern; and

[19] forming a shallow trench dielectric layer in the shallow trench.

[20] In an embodiment, the method further includes forming an anti-reflective layer on the hard mask layer.

[21] In an embodiment, forming a shallow trench in the deep well of the epitaxial layer includes:

[22] forming a photoresist layer having the drift region pattern on the anti-reflective layer and

[23] forming the shallow trench in the deep well of the epitaxial layer using the photoresist layer having the drift region pattern as a mask.

[24] In an embodiment, the shallow trench formed in the deep well of the epitaxial layer has a depth of about 100 nm.

[25] In an embodiment, the shallow trench formed in the deep well of the epitaxial layer

has an angle in a range from about 80 degrees to about 90 degrees.

[26] In a preferred embodiment, the fabrication method of LDMOS device further includes step of forming a deep trench in a middle portion of the epitaxial layer for isolating low-voltage devices after step of forming a shallow trench dielectric layer in the shallow trench.

[27] In an embodiment, the shallow trench formed in the deep well of the epitaxial layer includes N-type dopant. In another embodiment, the shallow trench includes P-type dopant.

[28] Embodiments of the present invention provide a LDMOS device. The LDMOS device includes:

[29] a substrate having a body layer, an epitaxial layer and a deep well region located in a middle portion of the epitaxial layer; and

[30] a shallow dielectric layer disposed in a middle portion of the deep well region.

[31] In an embodiment, the shallow dielectric layer has a thickness of about 100 nm.

[32] In an embodiment, the shallow dielectric layer includes an angle in a range from about 80 degrees to about 90 degrees.

[33] From the foregoing, the fabrication method of LDMOS device of the present disclosure includes: providing a substrate having a body layer, an epitaxial layer and a deep well region disposed in a middle portion of the epitaxial layer; forming an isolation dielectric layer on the epitaxial layer and forming a hard mask layer on the isolation dielectric layer; forming a shallow trench in the deep well of the epitaxial layer using a mask having a drift region pattern; and forming a shallow trench dielectric layer in the shallow trench. The fabrication method of LDMOS device of the present disclosure defines a groove above the drift region, and fills dielectric layer in the groove, therefore critical dimensions of the LDMOS device can be 0.18μm or below 0.18μm. Furthermore, LDMOS devices manufactured by the method can achieve overall planarization of a surface of the substrate in a subsequent CMP process, and do not have the shallow trench dielectric layer protruding above the surface of the substrate, thereby reducing process defects.

[34] Other advantages and novel features will become more apparent upon review of the following detailed description together with the accompanying drawings.

[35] BRIEF DESCRIPTION OF THE DRAWINGS

[36] The components in the drawings are not necessarily drawn to scale, the emphasis instead being placed upon clearly illustrating the principles of the present disclosure. Moreover, in the drawings, like reference numerals designate corresponding parts throughout several views, and all the views are schematic.

[37] FIG. 1 is a flowchart illustrating a method of fabricating a LDMOS device according to an embodiment of the present invention.

[38] FIG. 2 is a flowchart illustrating a method of fabricating a LDMOS device according to another embodiment of the present invention.

[39] FIGS. 3 through 7 are cross-sectional views of a LDMOS device in the fabrication process according to another embodiment of the present invention.

[40] FIG. 8 is a cross-sectional view of an embodiment of a LDMOS device according to another embodiment of the present invention.

[41] DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[42] The disclosure is illustrated by way of example and not by way of limitation in the figures of the accompanying drawings in which like references indicate like elements. It should be noted that references to "an" or "one" embodiment in this disclosure are not necessarily to the same embodiment, and such references mean at least one.

[43] EMBODIMENT 1

[44] According to the above mentioned conventional art, when fabricating a LDMOS device, a field oxide layer is formed above the drift region using a LOCOS process. The field oxide layer is an isolation layer of a semiconductor device having an active region, such as a high-voltage device. The field oxide layer formed by the LOCOS process is difficult to apply in the 0.18μm process and below, because of the "beak" effect. After forming the field oxide layer on the drift region, about half of the total thickness of the field oxide layer is protruding above a top surface of the substrate. The protruded portion has a step shape between the field oxide layer and the substrate. The substrate cannot be planarizated by CMP process because of the step portion, resulting in a defective workmanship of manufacturing.

[45] Referring to FIG. 1, the present disclosure provides a method of fabricating a LDMOS device. The method includes the following steps:

[46] In step 1, a substrate is provided. The substrate includes a body layer, an epitaxial layer, and a deep well region. The deep well region is disposed in the epitaxial layer.

[47] The body layer can be a silicon substrate in an embodiment. The epitaxial layer may include a lightly doped silicon layer formed on the silicon substrate. In a fabrication process of semiconductor, the epitaxial layer is a carrier formed in a process of lithography, etching, ion implantation or others.

[48] In step S1, the epitaxial layer has a deep well region, the deep well region is generally formed by high-energy, high-dose ion implantation process. The deep well region is disposed in a depth of the epitaxial layer at about 1μm. A gate region, a source region and a drain region are formed in the deep well region.

[49] In step S2, an isolation dielectric layer is formed on the epitaxial layer and a hard mask layer is formed on the isolation dielectric layer.

[50] In specific implementation process, a surface of the substrate is rinsed and dried; then, the isolation dielectric layer is formed on the epitaxial layer. The epitaxial layer is

disposed on the surface of the substrate. The isolation dielectric layer can be an oxide layer. In an embodiment, the thickness of the isolation dielectric layer is about 150 Å. The isolation dielectric layer can be formed in a high-temperature oxidation apparatus.

[51] The hard mask layer is formed on the isolation dielectric layer. In an embodiment, the hard mask layer is a silicon nitride layer. The implementation process of the silicon nitride layer is described as the following: the substrate having the isolation dielectric layer is placed in a low pressure chemical vapor deposition (LPVCD) apparatus, and the LPVCD apparatus has a relatively highheating temperature of, such as 750°C; ammonia gas and dichlorosilane gas is filled in a chamber of the LPVCD apparatus; the ammonia gas reacts with the dichlorosilane gas, and the silicon nitride layer is formed on the isolation dielectric layer. In the following steps of the fabrication method of LDMOS device, the silicon nitride layer is a solid mask layer and can be used as a polishing barrier layer for a CMP process.

[52] In step S3, a shallow trench is formed in the deep well of the epitaxial layer by a mask having a drift region pattern.

[53] Step S3 is an exposure process. Firstly, a photoresist layer is coated on the hard mask layer. Then, the photoresist layer is exposed via the mask having a drift region pattern and developed after exposure, and the photoresist layer at a top of the drift region is removed. Thereafter, a film at the top of the drift region is removed by dry etching, the hard mask layer, the isolation dielectric layer and the epitaxial layer are subsequently formed on the film, and the thickness of the epitaxial layer is thin. Finally, the shallow trench is formed over the drift region. The shallow trench has a depth of about 100 nm that is controlled by the etching time. An angle between a sloping sidewall of the shallow trench and a surface of the substrate is a range from about 80 degrees to about 90 degrees.

[54] In step S4, a shallow trench dielectric layer is formed in the shallow trench.

[55] In an embodiment, the shallow trench dielectric layer is formed in the shallow trench by a LPCVD method. The shallow trench dielectric layer can be an oxide layer, the oxide layer can be used as an isolation layer of source region devices.

[56] From the foregoing, the fabrication method of a LDMOS device of the present disclosure differs from the traditional process. For example, the traditional process adopts a LOCOS process to form a field oxide layer over the drift region, and the field oxide layer is used as an isolation layer. However, the shallow trench is formed in an epitaxial layer over the drift region, and the shallow trench dielectric layer is formed in the shallow trench as the isolation layer. The fabrication method of LDMOS device of the present disclosure forms a groove above the drift region, and fills the groove with a dielectric layer, therefore critical dimensions of the thus manufactured LDMOS device can be 0.18μm or below 0.18μm. Furthermore, LDMOS devices manufactured by this

novel method can achieve a complete planarization of the substrate surfacein a subsequent CMP process, and do nothavethe shallow trench dielectric layer protruded above the surface of the substrate, thereby reducing process defects.

[57] EMBODIMENT 2

[58] Referring to FIG. 2, a method of fabricating an LDMOS device includes the following steps:

[59] In step S11, a substrate is provided, and the substrate includes a body layer, an epitaxial layer overlying the body layer, and a deep well region disposed in a middle portion of the epitaxial layer.

[60] In an embodiment, the term 'middle portion of the epitaxial layer' refers to a region extending down to a certain depth from a surface of the epitaxial layer, which is a portion of the epitaxial layer. The term 'upper portion of the epitaxial layer' refers to a region above the surface of the epitaxial layer, and the region itself does not belong to the epitaxial layer.

[61] Referring to FIG. 3, the epitaxial layer 101 is disposed over the body layer 100, and the deep well 102 is disposed in the epitaxial layer 101.

[62] In an embodiment, the body layer 100 is a P-type silicon substrate, and the epitaxial layer 101 is a P-type silicon epitaxial layer extending from the P-type silicon substrate. The deep well 102 is a deeply doped region formed in a middle portion of the epitaxial layer 101. In an embodiment, the deep well region 102 may be a N-type dopant. In another embodiment, the deep well region 102 may be a P-type dopant.

[63] In step S12, an isolation dielectric layer, a hard mask layer, and an anti-reflective layer are subsequently formed on the deep well region.

[64] Referring to FIG. 4, the isolation dielectric layer 103 is formed on the deep well region 102, the hard mask layer 104 is formed on the isolation dielectric layer, and the anti-reflective layer 105 are formed on the hard mask layer by a thermal growth process or deposition process. The isolation dielectric layer is a silicon oxide layer, and the thickness of the isolation dielectric layer is about 150 Å. The isolation dielectric layer 103 will serve as a barrier layer to protect the source region from the chemical stain in a process of removing the hard mask layer 104. The hard mask layer 104 is a silicon nitride layer. The hard mask layer 104 is a solid mask layer and is used as a grinding end layer in a subsequent CMP process. The anti-reflective layer 105 is a silicon oxynitride layer. The thickness of the anti-reflective layer 105 is formed to be thinner than that of the photoresist layer, in order to prevent that a reflecting groove from forming in the photoresist layer when light is reflecting back to a portion of the photoresist layer that does need to be exposed in an exposure process.

[65] In step S13, a shallow trench is defined in the deep well of the epitaxial layer by a mask having a drift region pattern.

[66] Step S13 includes depositing a photoresist layer on the anti-reflectivelayer, the photoresist layer having a drift region pattern is formed on the anti-reflective layer by the mask having a drift region pattern.

[67] The photoresist layer is exposed by the mask having a drift region pattern and developed after exposure, and the photoresist layer at top of the drift region is removed, so that the photoresist layer having a drift region pattern is formed on the anti-reflective layer.

[68] In step S133, the shallow trench is formed in the deep well located in a middle portion of the epitaxial layer by the photoresist layer having a drift region pattern.

[69] Referring to FIG. 5, the anti-reflective layer 105, the hard mask layer 104, the isolation dielectric layer 103 and a part of the isolation dielectric layer 103 are etched by dry etching process, and the photoresist layer having a drift region pattern is as a mask. A first shallow trench 106 and a second shallow trench 107 are defined in the deep well 102 located in a middle portion of the epitaxial layer 101. A film disposed outside the first shallow trench 106 and the second shallow trench 107 is not etched because of protecting of the photoresist layer.

[70] The depth of the shallow trench should meet requirements of the source-drain resistance and breakdown voltage, which is due to the following reason: if the depth of the shallow trench is larger, a desired path extending from the source end to the drain end is increased, resulting in that the on-resistance is increased; if the depth of the shallow trench is smaller, the action of the gate field plate on the drift region is strengthened, such that potential lines of an edge of the gate field plate is bended seriously, resulting in lower breakdown voltage.

[71] In a preferable embodiment, the depth of the first shallow trench 106 and the second shallow trench 107 are about 100 nm. An angle between a sidewall of the first shallow trench 106 and the second shallow trench 107 and a surface of the epitaxial layer 101 are in a range from about 80 degrees to about 90 degrees.

[72] The photoresist layer is removed after forming the first shallow trench 106 and the second shallow trench 107.

[73] In step S14, a deep trench is formed in a middle portion of the epitaxial layer for isolating low-voltage devices.

[74] The process of forming the deep trench is similar to step S13. In one embodiment, the depth of the deep trench is about 400nm in the epitaxial layer, and an angle between a sloping sidewall of the deep trench and a surface of the substrate is in a range from about 80 degrees to about 90 degrees (the sidewall is perpendicular to the surface of the substrate).

[75] In an embodiment, the deep trench is formed after forming the shallow trench. The reason of forming the deep trench after the shallow trench being: when forming the

deep trench, the photoresist layer that is coated on the anti-reflective layer, and onthe bottom of the first and second shallow trenchescan be easily removed. If the shallow trench is formed after forming the deep trench, it will be difficult to remove the photoresist layer that is coated on the bottom of the deep trench.

[76] In step S15, a deep trench dielectric layer and a shallow trench dielectric layer are formed in the deep trench and the shallow trench, respectively.

[77] After forming the deep trench and the shallow trench, a trench dielectric layer is formed on the substrate by a high-density plasma chemical vapor deposition (HDPCVD) method, and then the trench dielectric layer is planarized by a CMP process. The CMP process removes the anti-reflective layer. The hard mask layer is used as a stop layer. The hard mask layer is then removed after the CMP process.

[78] Referring to FIG. 6, the thickness of the shallow trench dielectric layers 108 and 109 disposed over the drift regionis about 100 nm. The thickness of the deep trench dielectric layers 110 and 111 that are used for isolating lower-voltage devices is about 400 nm.

[79] In an embodiment, after forming the deep trench dielectric layer and the shallow trench dielectric layer, the method further includesforminga source region in the epitaxial layer (step S16).

[80] A first gate region and a second gate region are formed in the deep wellregion. The formation process of the first gate region and the second gate region is: a gate dielectric layerand a gate electrode are formed on the epitaxial layer in turn, the gate dielectric layer may be a silicon oxide layer or high dielectric constant materials such as SrTiO3, HfO2, ZrO2, or the like. The gate electrode can be polysilicon or metal. The gate dielectric layer and the gate electrode disposed outside the gate region are photolithography etched by a mask patterned according to the gate region patternto form the gate regions.

[81] Source region and drain region are formed by ion implantation process after forming the gate regions.

[82] Referring to FIG. 7, a first shallow well region 112 and a second shallow well region 113 are formed in the deep well region 102 located in a middle portion of the epitaxial layer 101. The doping types of the first shallow well region 112 and the second shallow well region 113 are the same as that of the deep well region 102. A source region and a second region (not shown) are formed in the first shallow well region 112 and the second shallow well 113, respectively. The doping type of the source region, the source region and the drain region is an opposite conductive type of that of the deep well region 102.

[83] In an embodiment, if the deep well region 102 includes an N-type dopant, the first shallow well region 112 and the second shallow well 113 will also include N-type

dopants, the first source region, the second source region and the drain region include P-type dopants, then the LDMOS device formed by the above method is a P-type LDMOS device. In another embodiment, if the deep well region 102 includes a P-type dopant, the first shallow well region 112 and the second shallow well 113 will also include P-type dopants, the first source region, the second source region and the drain region include N-type dopants, then the LDMOS device formed by the above method is an N-type LDMOS device.

[84] Dielectric layers are deposited on the gate region, the source region and the drain region, respectively. Each of dielectric layers includes a through hole. The gate region, the source region, and the drain region are connected to the respective gate electrode, source electrode, and drain electrode by metals passed through the associated through holes.

[85] The fabrication method of the LDMOS device of the present disclosure forms the shallow trench over the drift region, and the shallow trench dielectric layer is formed in the shallow trench as an isolation layer. The fabrication method of LDMOS device of the present disclosure canovercome the 'beak' effect of the LOCOS process, such that critical dimensions of the LDMOS device can be 0.18μm or below 0.18μm. The resulting size and spacing reducing of LDMOS devicesincreasesthe market competitiveness. Furthermore, LDMOS devices manufactured by the method can achieve a planarization of a surface of the substrate in a subsequent CMP process, and do not have a portion of the shallow trench dielectric layer protruding above the surface of the substrate, thereby reducing process defects of manufacturing.

[86] EMBODIMENT 3

[87] The present disclosure also provides a LDMOS device. Referring to FIG. 8, the LDMOS device includes a substrate, a first shallow trench dielectric layer 108 and a second shallow trench dielectric layer 109. The substrate includes a body layer 100, an epitaxial layer 101 overlying thebody layer, and a deep well region 102 disposed in a middle portion of the epitaxial layer 101. A first shallow trench dielectric layer 108 and a second shallow trench dielectric layer 109 are disposed in a middle portion of the deep well region 102.

[88] The first and second shallow trench dielectric layers 108 and 109 have a depth of about 100 nm, and an angle between a sidewall and a surface of the epitaxial layer 101 in the range from about 80 degrees (steep-sloped sidewall) to about 90 degrees (vertical sidewall).

[89] In an embodiment, the first and second shallow trench dielectric layers 108 and 109 are formed using the following steps: firstly, forming the isolation dielectric layer on the deep well region, forming the hard mask layer on the isolation dielectric layer, and forming the anti-reflective layer on the hard mask layer. Then, a first shallow trench

and a second shallow trench are formed over a drift region using a mask patterned after the drift region pattern. Thereafter, the first and second shallow trenches are filled with a dielectric, and the first and second shallow trenches are planarized by a CMP process.

[90] In an embodiment, the LDMOS device also includes a first deep trench dielectric layer 110, a second deep trench dielectric layer 111, a first shallow well region 112, a second shallow well region 113, a first source region (not shown), a second source region (not shown), a first gate region (not shown), a second gate region (not shown), and a drain region (not shown). The first deep trench dielectric layer 110 and the second deep trench dielectric layer 111 are disposed at the edges of the deep well region and configured to isolate lower-voltage devices. The first shallow well region 112 and the second shallow well region 113 are disposed adjacent to the respective first deep trench dielectric layer 110 and the second deep trench dielectric layer 111. The first source region and the second source region are respectively disposed in the shallow well region 112 and the second shallow well region 113. The first gate region, the second gate region, and the drain region are disposed in the deep well region 102 located in a middle portion of the epitaxial layer 101. Each gate region, each source region and each drain region are connected to the gate electrode G, the source electrode S and the drain electrode D by metal wires, respectively.

[91] The fabrication method of the LDMOS device of the present disclosure forms the shallow trenches over the drift region, the shallow trench dielectric layer has a depth of about 100 nm, and an angle between a sidewall and a surface of the epitaxial layer in the range from about 80 degrees (steep sloped sidewall) to about 90 degrees (vertical sidewall). The LDMOS device thus formed is a high-voltage device having a low drift region resistance and high breakdown voltage. In addition, the fabrication method of the LDMOS device of the present disclosure can eliminate the problem of the traditional process, in which a steep protrusion of the oxide layer is formed that prevents a complete planarization of the substrate by a conventional CMP process. The fabrication method of LDMOS device of the present disclosure canovercome the 'beak' effect of the LOCOS process, so that critical dimensions of the LDMOS device can be 0.18μm or below 0.18μm.

[92] Finally, while various embodiments have been described and illustrated, the invention is not to be construed as being limited thereto. Various modifications can be made to the embodiments by those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

Claims

[Claim 1] A method of fabricating a LDMOS device, the method comprising:
providing a substrate having a body layer, a epitaxial layer overlying the body layer, and a deep well region disposed in a portion of the epitaxial layer;
forming an isolation dielectric layer on the epitaxial layer and a hard mask layer on the isolation dielectric layer;
forming a shallow trench in the deep well region using a mask having a drift region pattern; and
forming a shallow trench dielectric layer in the shallow trench.

[Claim 2] The method of claim 1, further comprising forming an anti-reflective layer on the hard mask layer .

[Claim 3] The method of claim 2, wherein forming a shallow trench comprises:
forming a photoresist layer having the drift region pattern on the anti-reflective layer.

[Claim 4] The method of claim 1, wherein the shallow trench comprises a depth of about 100 nm.

[Claim 5] The method of claim 1, wherein the shallow trench comprises an angle ranging from about 80 degrees to about 90 degrees.

[Claim 6] The method of claim 1, further comprising forming a deep trench after forming a shallow trench dielectric layer in the shallow trench.

[Claim 7] The method of claim 6, wherein forming a deep trench comprises a high-density plasma chemical vapor deposition process.

[Claim 8] The method of claim 1, wherein the shallow trench comprises an N-type dopant.

[Claim 9] The method of claim 1, wherein the shallow trench comprises a P-type dopant.

[Claim 10] An LDMOS device comprising:
a substrate having a body layer, an epitaxial layer overlying the body layer, and a deep well region disposed in a middle portion of the epitaxial layer;
a shallow dielectric layer disposed in a portion of the deep well region;
a deep trench dielectric layer disposed at an edge of the deep well region;
a shallow well region disposed between the deep trench dielectric layer and the shallow dielectric layer, the shallow well region being adjacent thedeep trench dielectric layer;

a source region disposed in the shallow well region; and
a gate electrode overlying a portion of the shallow dielectric layer and a portion of the source region.

[Claim 11] The LDMOS device of claim 10, wherein the shallow dielectric layer comprises a thickness of about 100 nm.

[Claim 12] The LDMOS device of claim 10, wherein the shallow dielectric layer comprises an angle between a sidewall and a surface of the substrate ranging from about 80 degrees to about 90 degrees.

[Claim 13] The LDMOS device of claim 10, wherein the deep trench dielectric layer comprises a depth of about 400 nm.

[Claim 14] The LDMOS device of claim 10, wherein the body layer comprises a P-type silicon substrate and the epitaxial layer comprises an extension of the P-type silicon substrate.

[Claim 15] The LDMOS device of claim 14, wherein the deep well region comprises an N-type dopant.

[Claim 16] The LDMOS device of claim 14, wherein the deep well region comprises a P-type dopant.

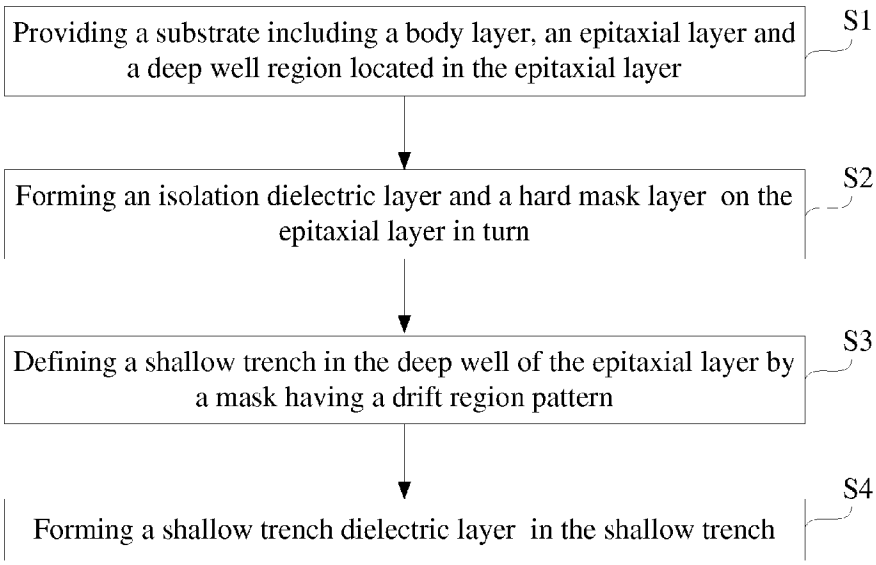
Providing a substrate including a body layer, an epitaxial layer and a deep well region located in the epitaxial layer
S1
Forming an isolation dielectric layer and a hard mask layer on the epitaxial layer in turn
S2
Defining a shallow trench in the deep well of the epitaxial layer by a mask having a drift region pattern
S3
Forming a shallow trench dielectric layer in the shallow trench
S4

FIG. 1

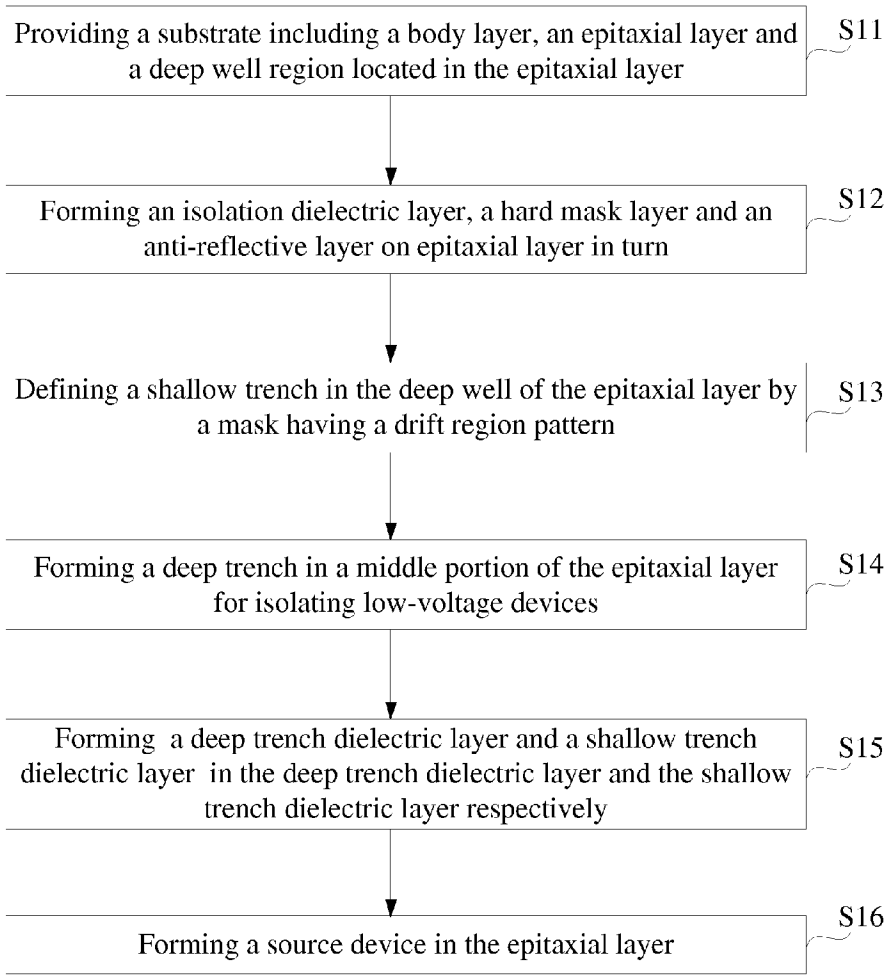
Providing a substrate including a body layer, an epitaxial layer and a deep well region located in the epitaxial layer
S11
Forming an isolation dielectric layer, a hard mask layer and an anti-reflective layer on epitaxial layer in turn
S12
Defining a shallow trench in the deep well of the epitaxial layer by a mask having a drift region pattern
S13
Forming a deep trench in a middle portion of the epitaxial layer for isolating low-voltage devices
S14
Forming a deep trench dielectric layer and a shallow trench dielectric layer in the deep trench dielectric layer and the shallow trench dielectric layer respectively
S15
Forming a source device in the epitaxial layer
S16

FIG. 2

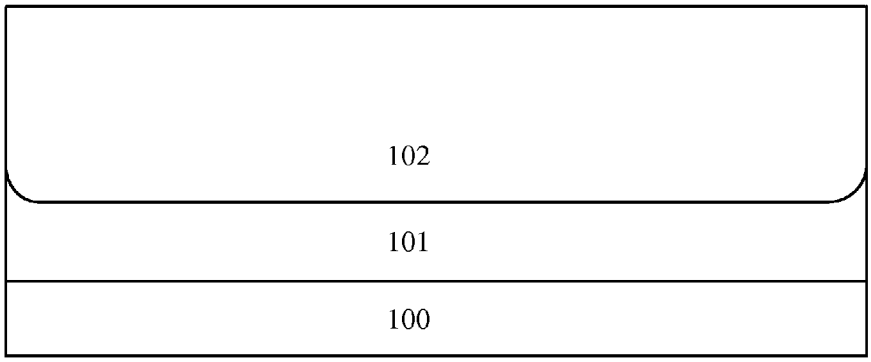

FIG. 3

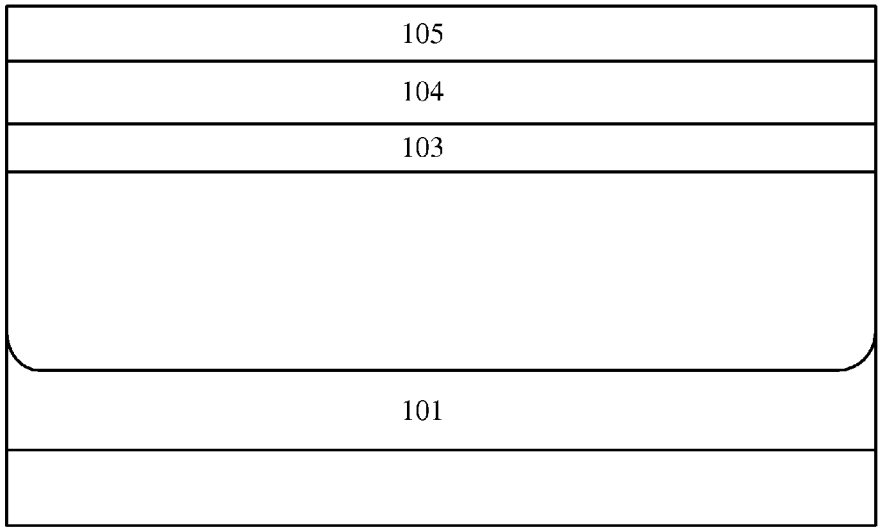

FIG. 4

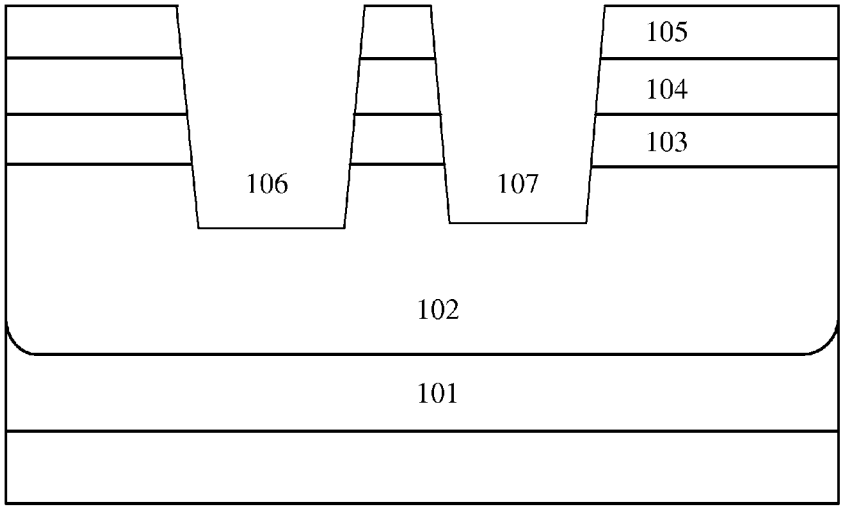
105
104
103
106
107
102
101

FIG. 5

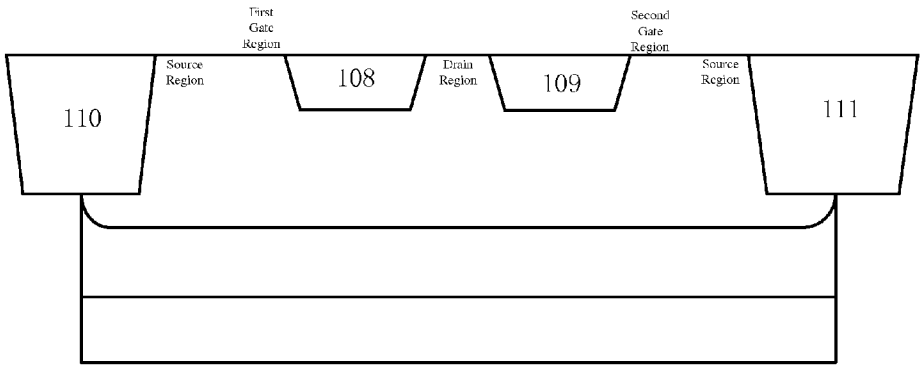
First Gate Region
Second Gate Region
Source Region
Drain Region
Source Region
108
109
110
111

FIG. 6

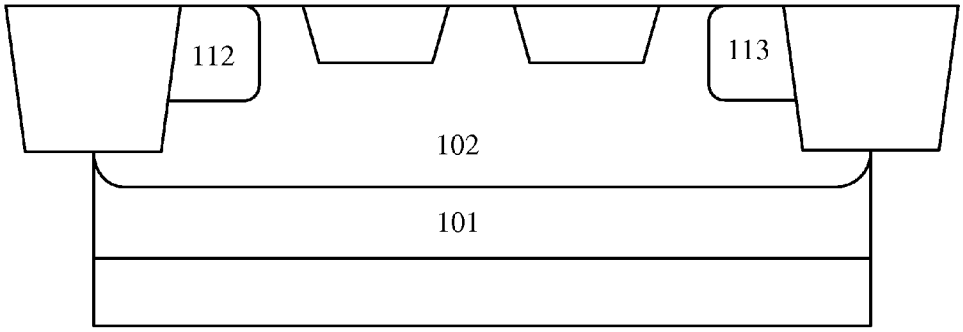
112
113
102
101

FIG. 7

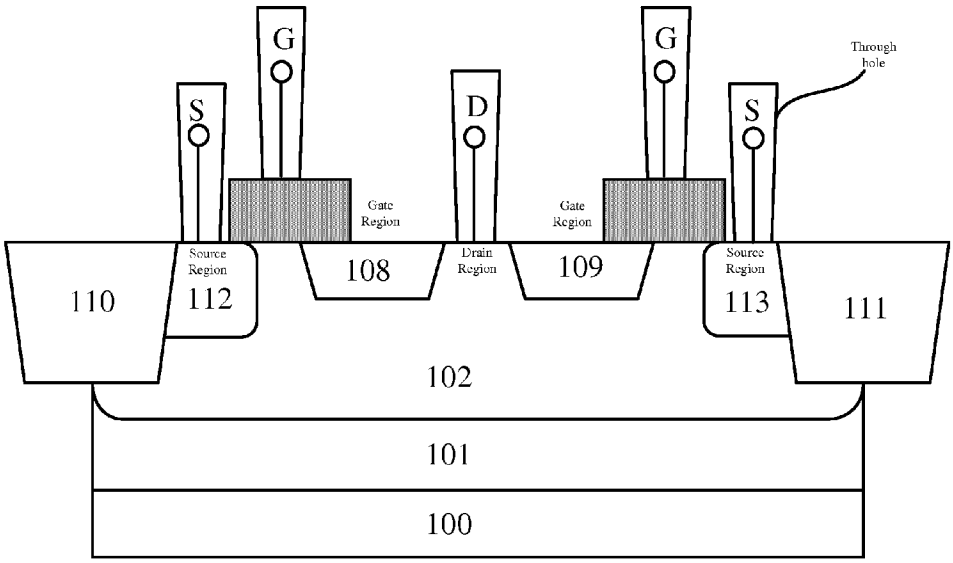
G
G
S
D
S
Through hole
Gate Region
Gate Region
Source Region
Drain Region
Source Region
110
112
108
109
113
111
102
101
100

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/083144

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI,CPRS,WPI,EPODOC: LDMOS, drift, well, dielectric, trench, depth, isolate, beak, size

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US2010/0006937A1(LEE)14 Jan.2010(14.01.2010) specification: paragraph 0027-paragraph 0053, Figs.1-8	1-16
X	US7728388B1(UNITED MICROELECTRONICS CORP.) 01 Jun.2010(01.06.2010) specification: column 2, line 63-column 4, line 50, Fig. 2	10-16
A	US2009/0020813A1(VOLDMAN) 22 Jan.2009(22.01.2009) the whole document	1-16

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 Feb. 2012(20.02.2012)	**22 Mar. 2012 (22.03.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer Zhi,Yue Telephone No. (86-10)62411788

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/083144

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US2010/0006937A1	14.01.2010	CN101625998A	13.01.2010
		KR20100006342A	19.01.2010
		TW201003917A	16.01.2010
		KR100974697B1	06.08.2010
US7728388B1	01.06.2010	US2010155895A1	24.06.2010
US2009/0020813A1	22.01.2009	NONE	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/083144

A. CLASSIFICATION OF SUBJECT MATTER:

H01L 21/336(2006.01)i

H01L 21/762(2006.01)i

H01L 29/78(2006.01)i

H01L 29/06(2006.01)i