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(54) **ARRAY OF THIN-FILM PHOTOVOLTAIC CELLS HAVING A TOTALLY SEPARATED INTEGRATED BYPASS DIODE AND A PANEL INCORPORATING THE SAME**

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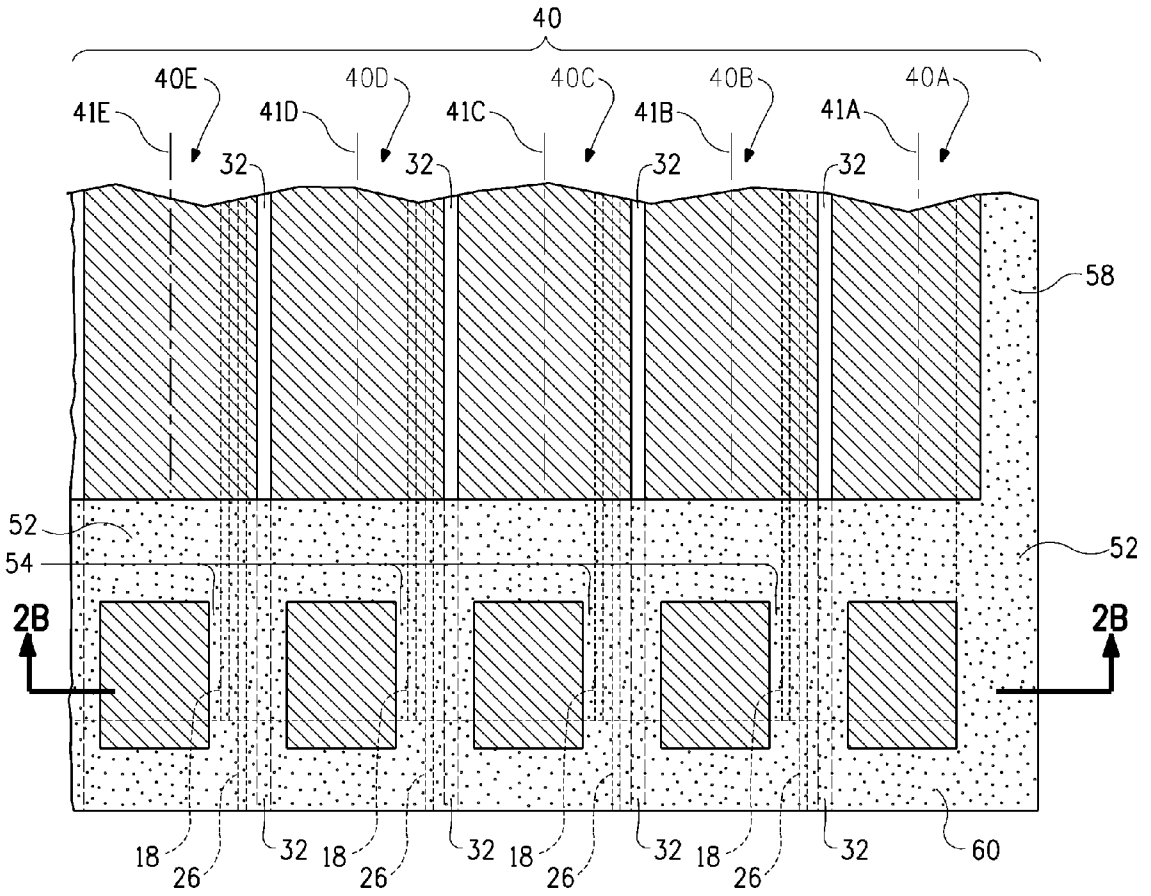
Publication Classification

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H01L 31/05 (2006.01)

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(57) **ABSTRACT**

An array of at least three series-connected solar cells has a cell level integrated bypass diode formed by total separation from a selected parent cell. The material of the first type of the diode is connected to the material of the second type of any one chosen solar cell in the array. The material of the second type of the diode is connected with the material of the first type of the one chosen solar cell in the array so that the diode is connected in parallel and in opposition to the one chosen solar cell.



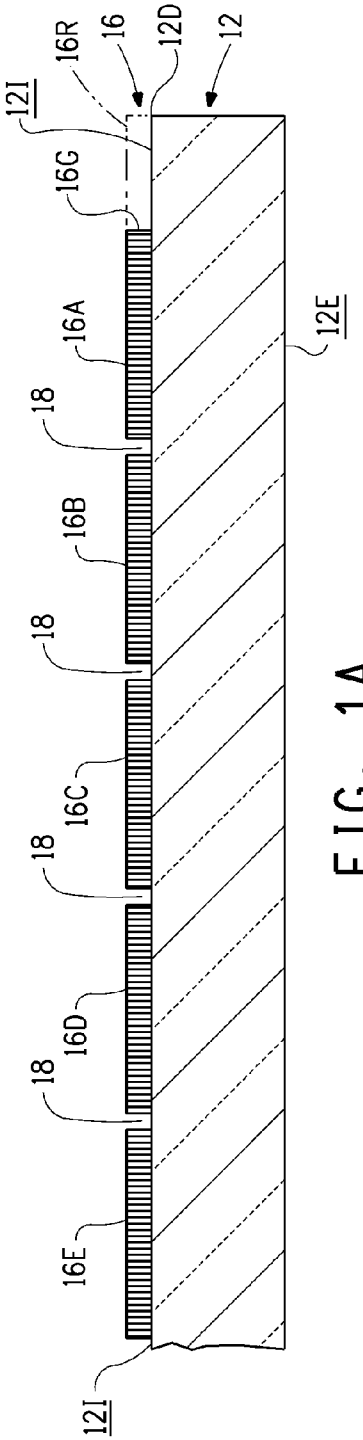


FIG. 1A
(Prior Art)

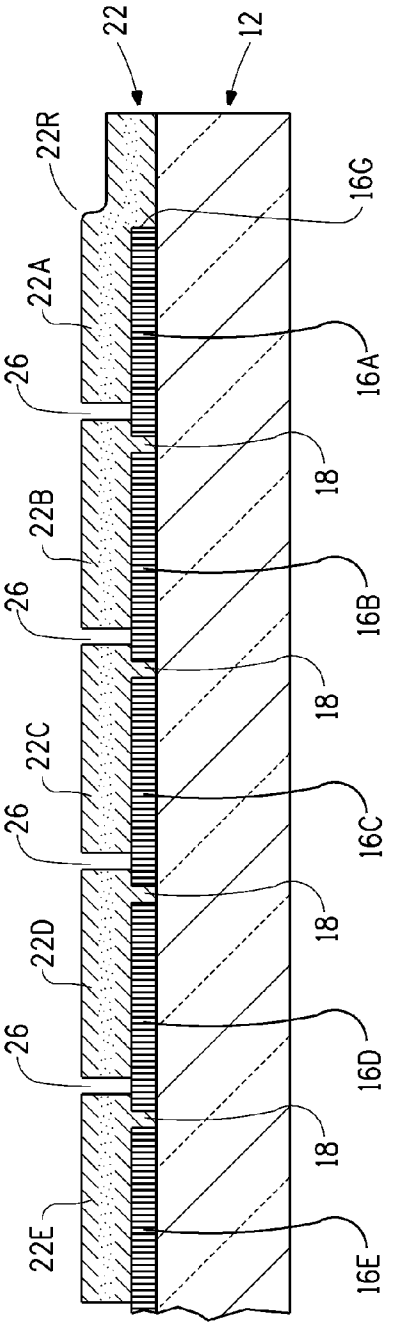


FIG. 1B
(Prior Art)

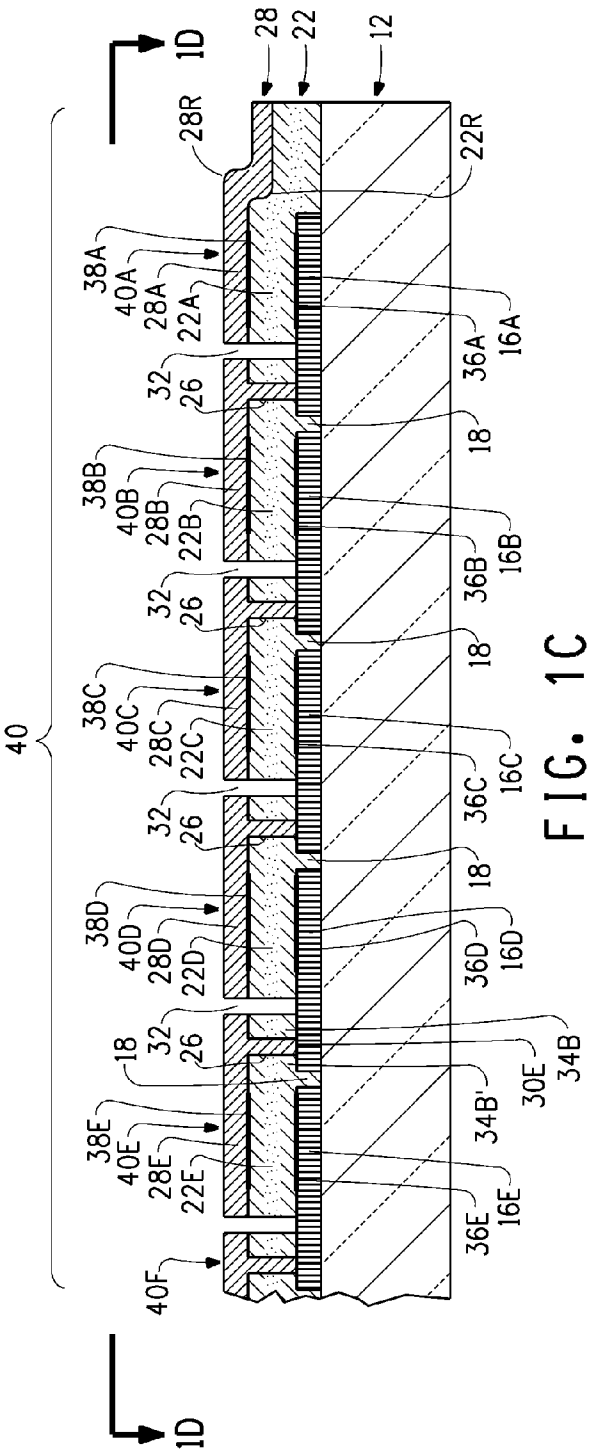


FIG. 1C
(Prior Art)

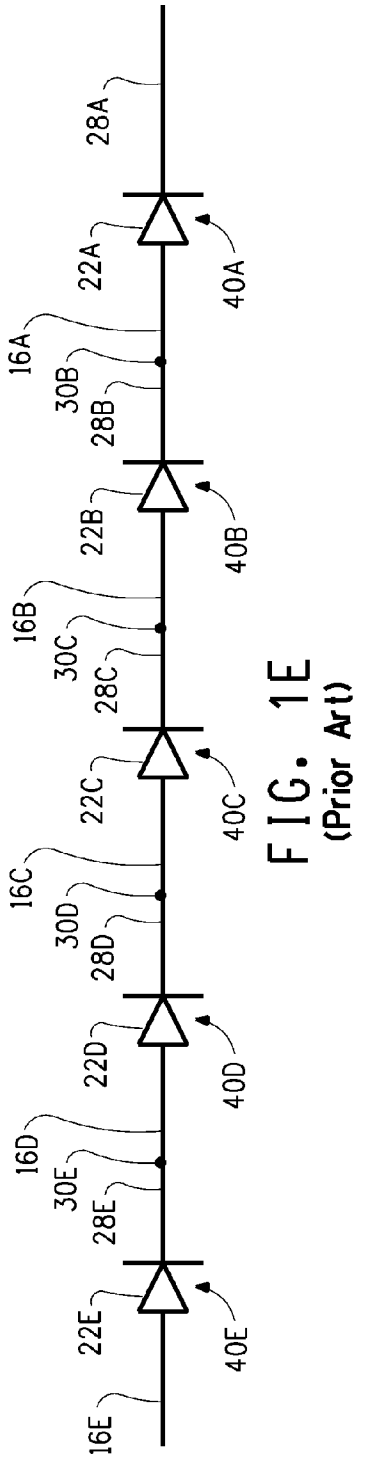


FIG. 1E
(Prior Art)

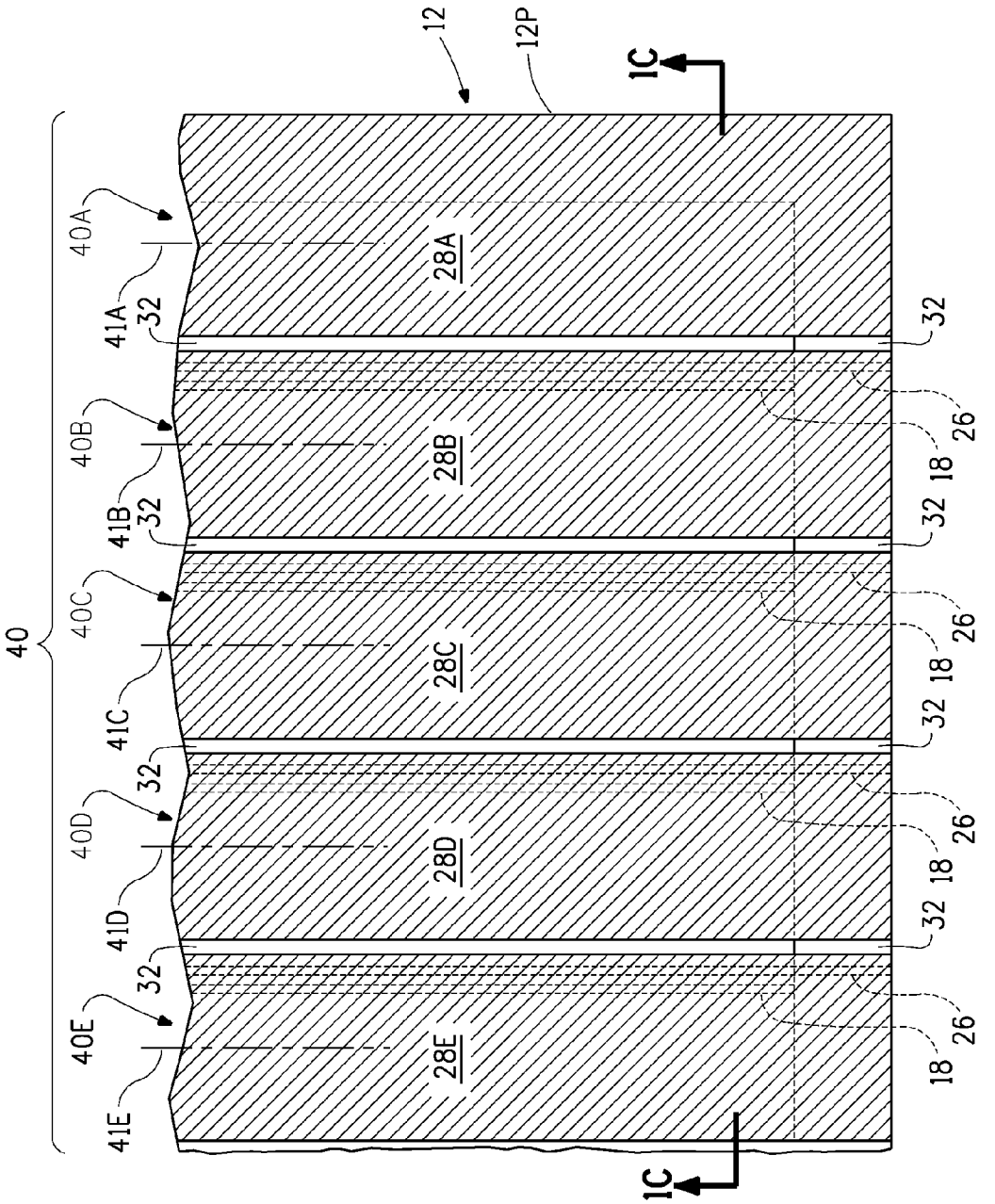


FIG. 1D
(Prior Art)

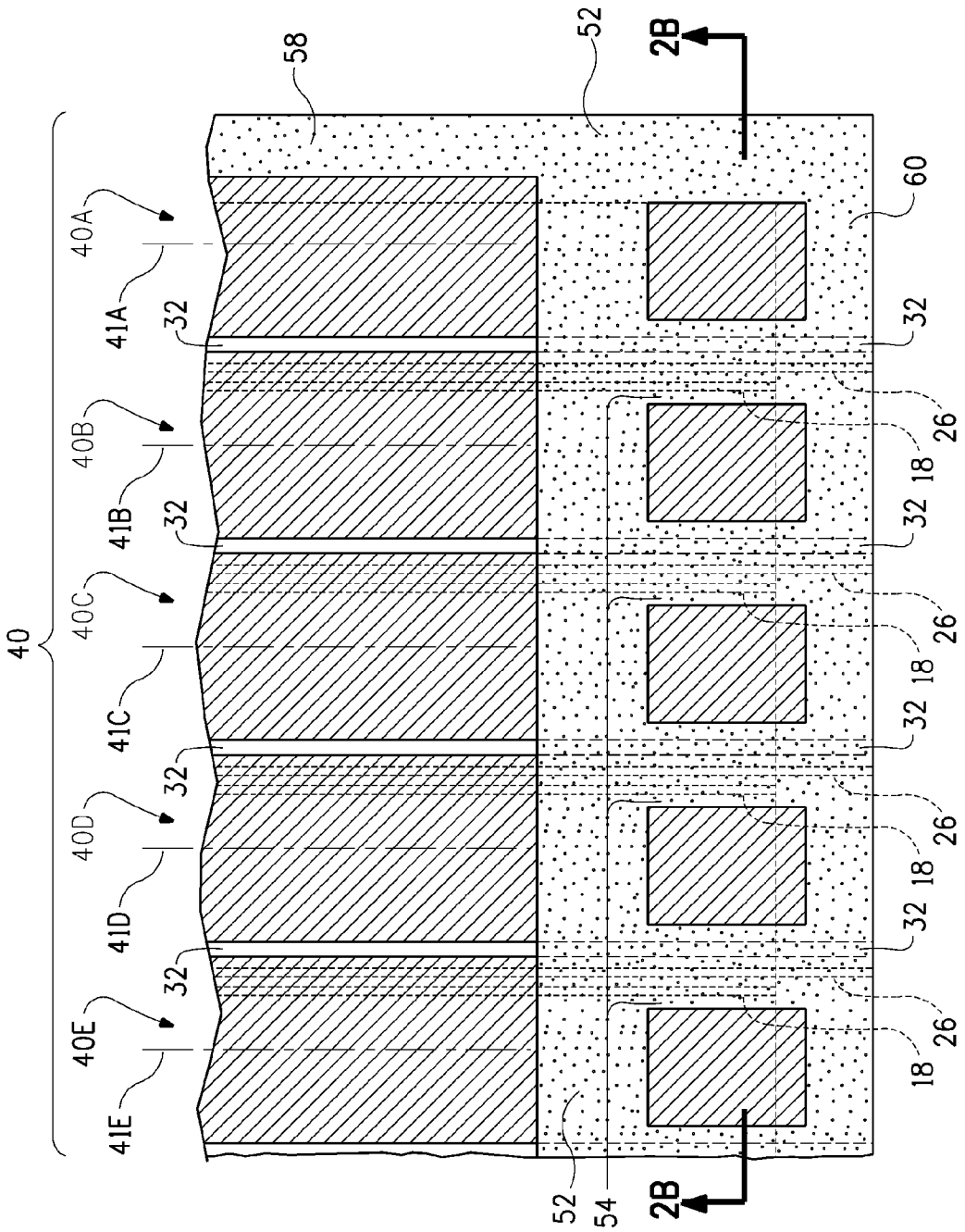


FIG. 2A

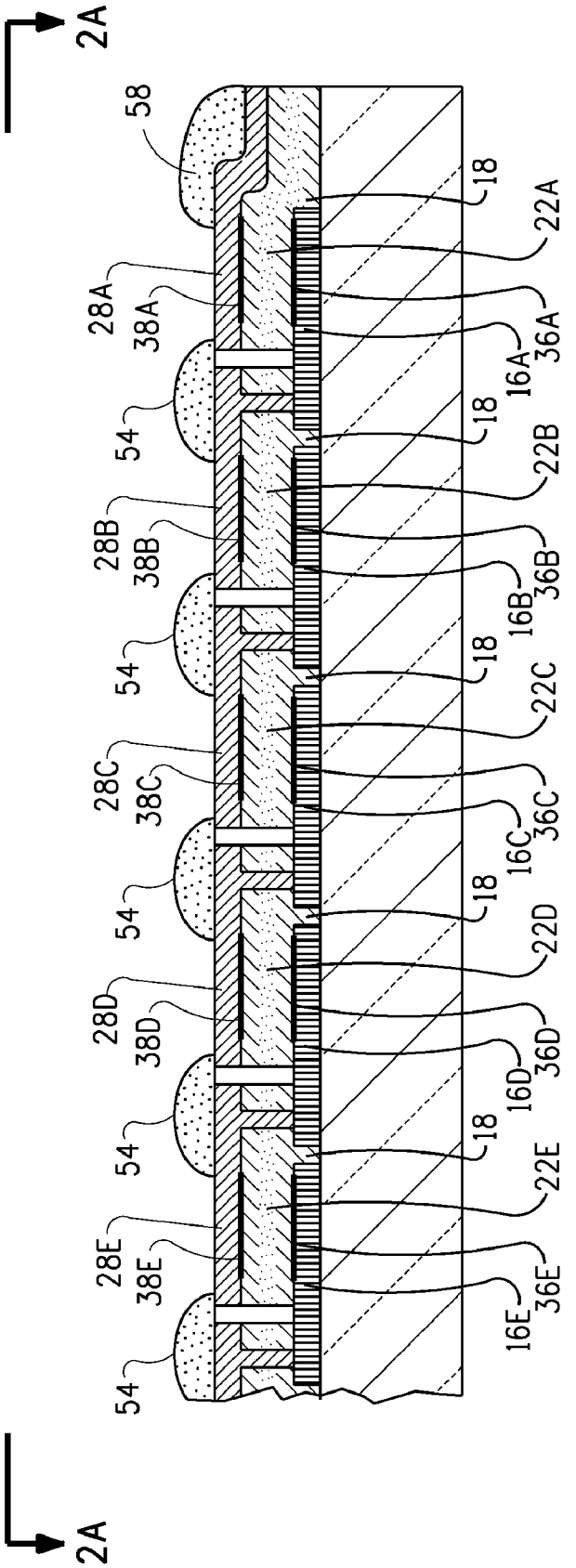

2A
58
18
22A
28A
38A
36A
16A
54
18
22B
28B
38B
36B
16B
54
18
22C
28C
38C
36C
16C
54
18
22D
28D
38D
36D
16D
54
18
22E
28E
38E
36E
16E
54
2A

FIG. 2B

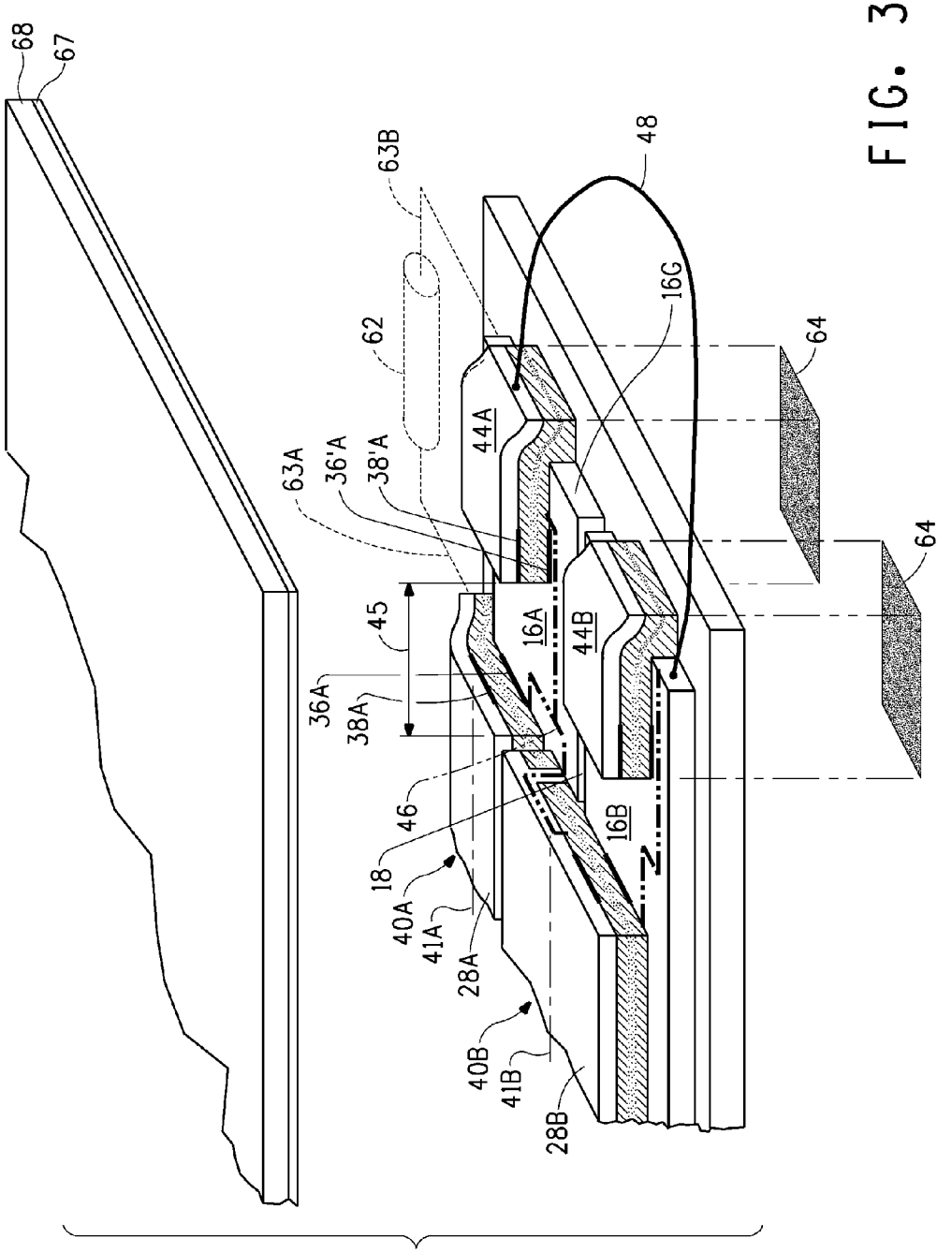

68
67
63B
48
62
16G
64
63A
36'A
38'A
44A
45
16A
44B
64
36A
38A
46
16B
18
40A
41A
28A
40B
41B
28B

FIG. 3A

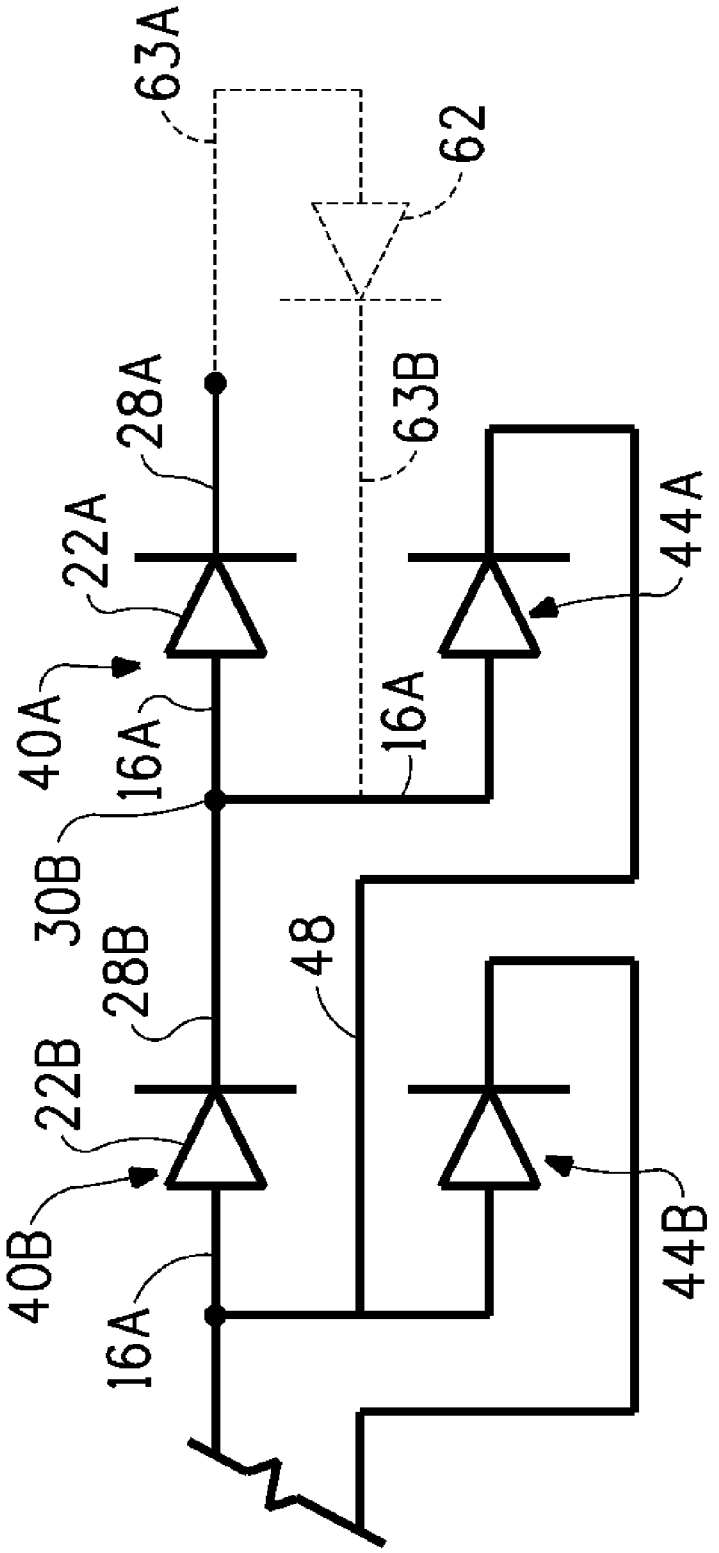


FIG. 3B

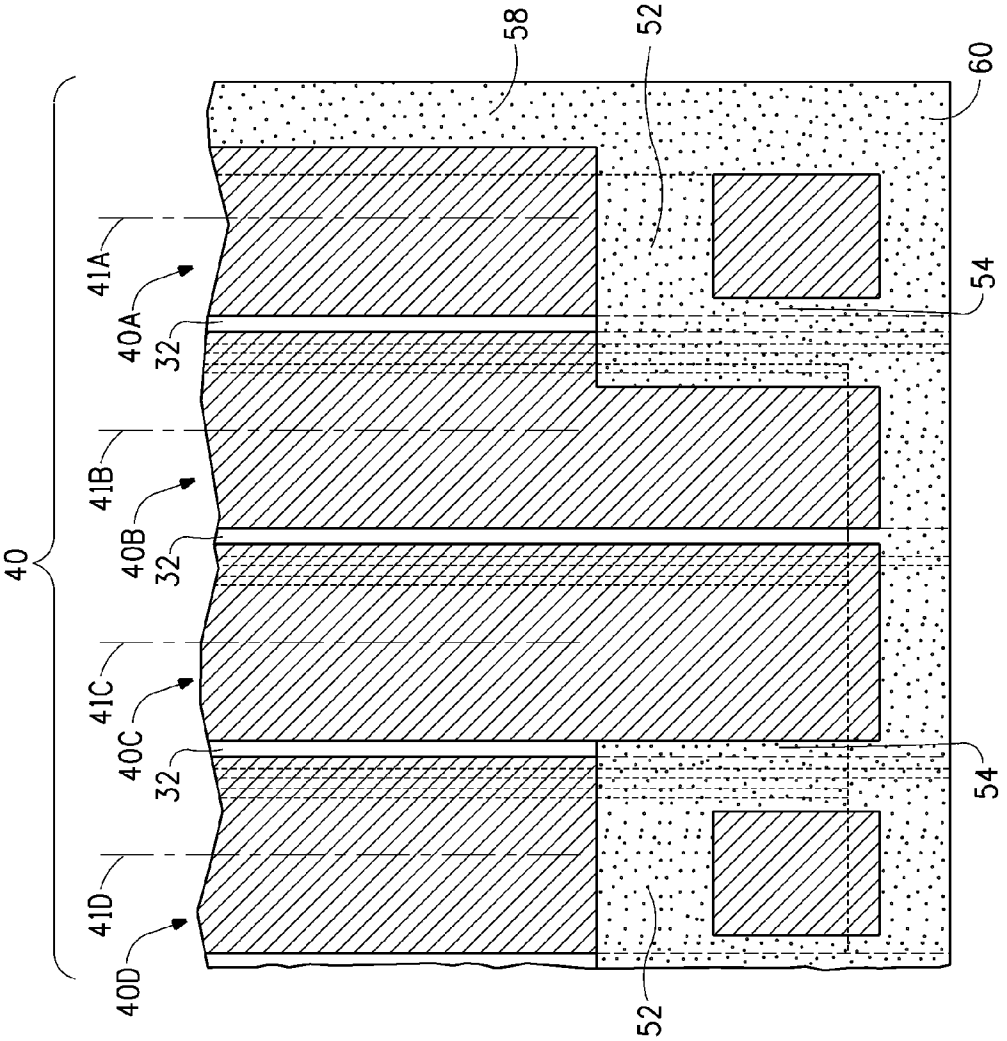


FIG. 4A

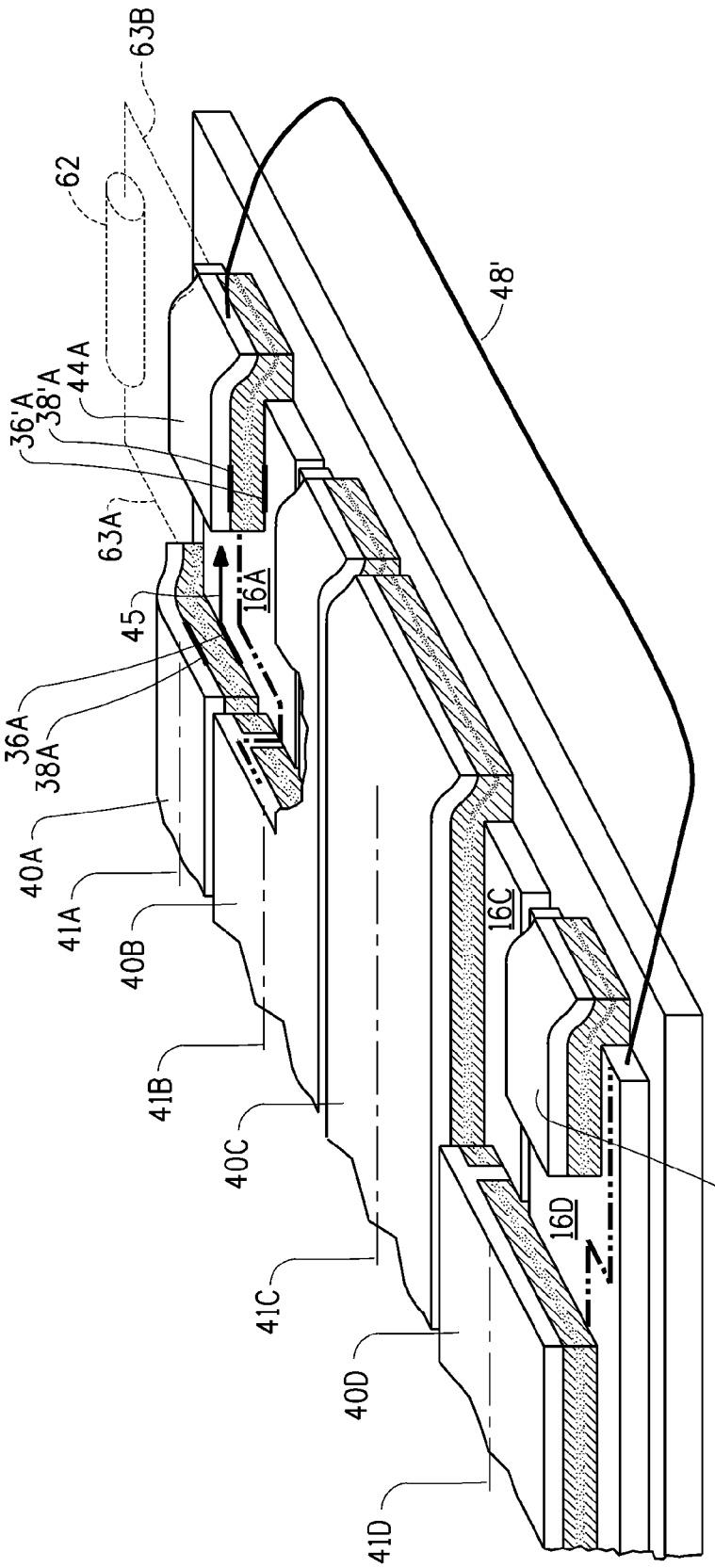

63B
62
48'
44A
36'A
38'A
63A
16A
45
36A
38A
40A
41A
40B
41B
40C
41C
40D
41D
16C
16D
44D

FIG. 4B

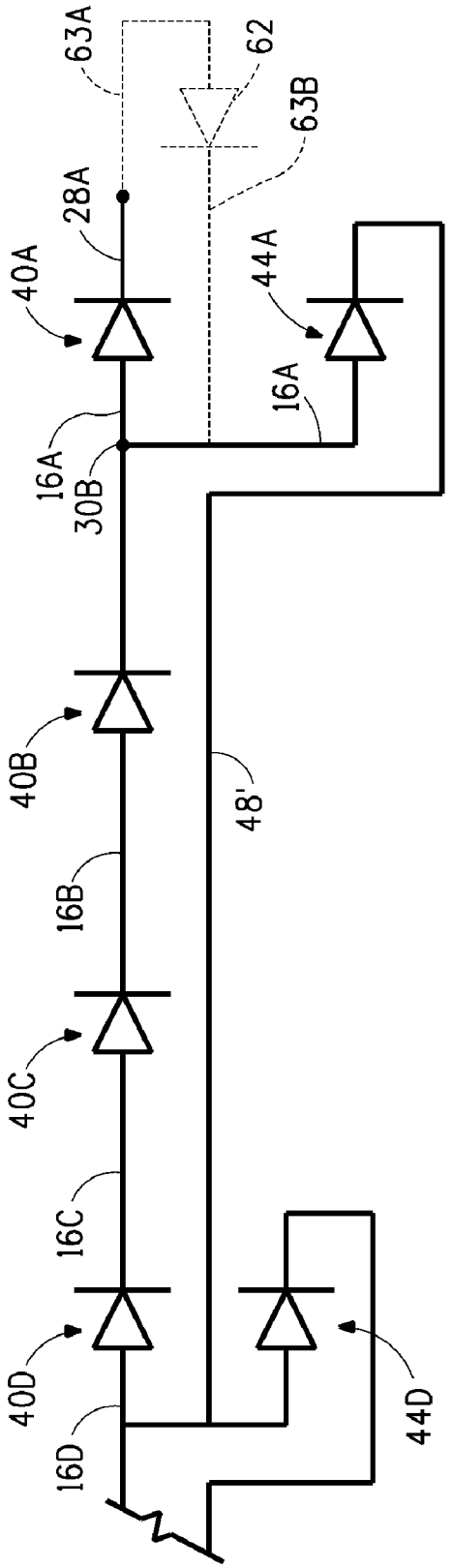


FIG. 4C

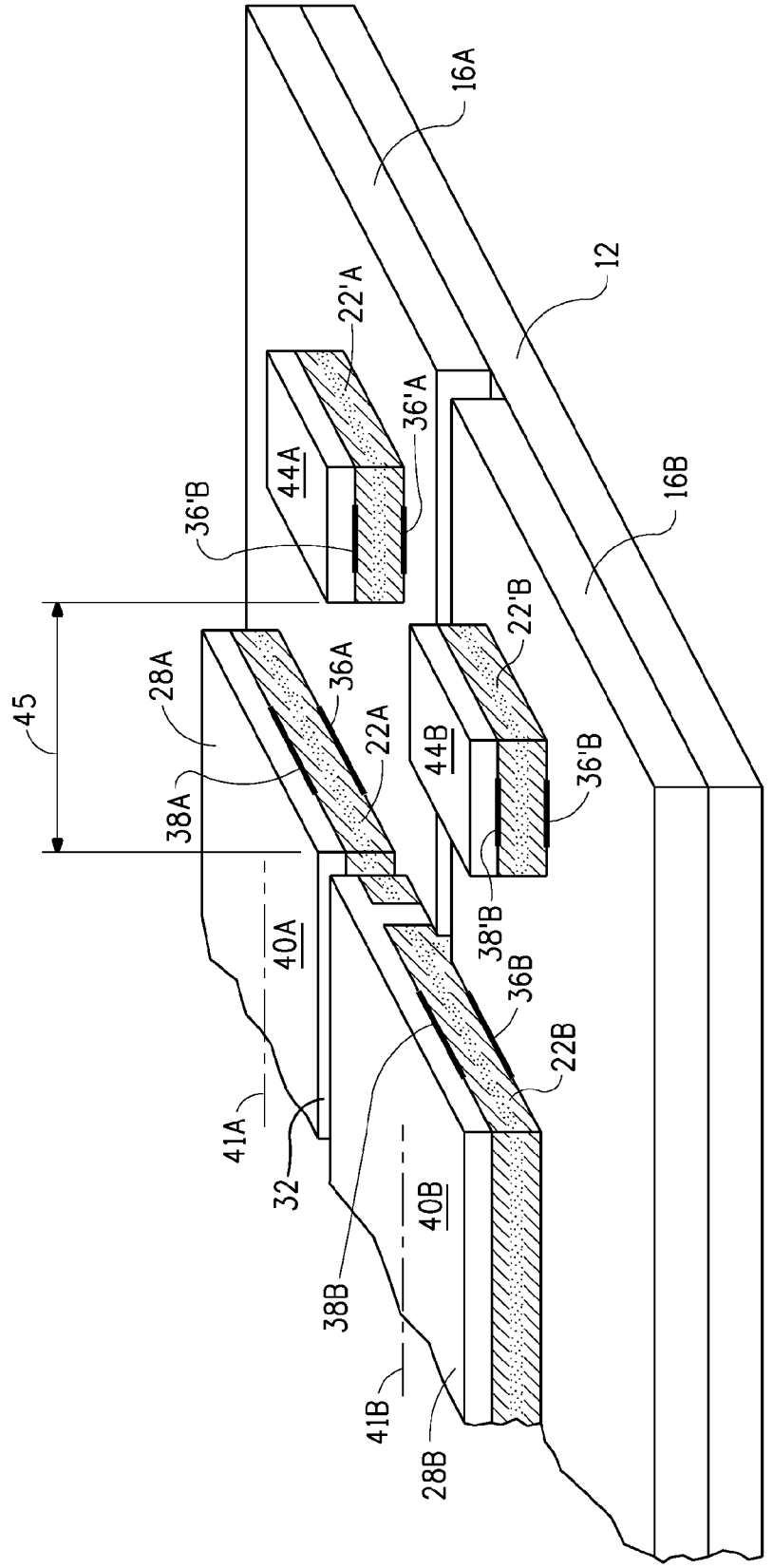

16A
12
22'A
36'A
44A
36'B
16B
22'B
28A
36A
45
22A
44B
36'B
38A
38'B
40A
36B
22B
41A
32
40B
38B
41B
28B

FIG. 5

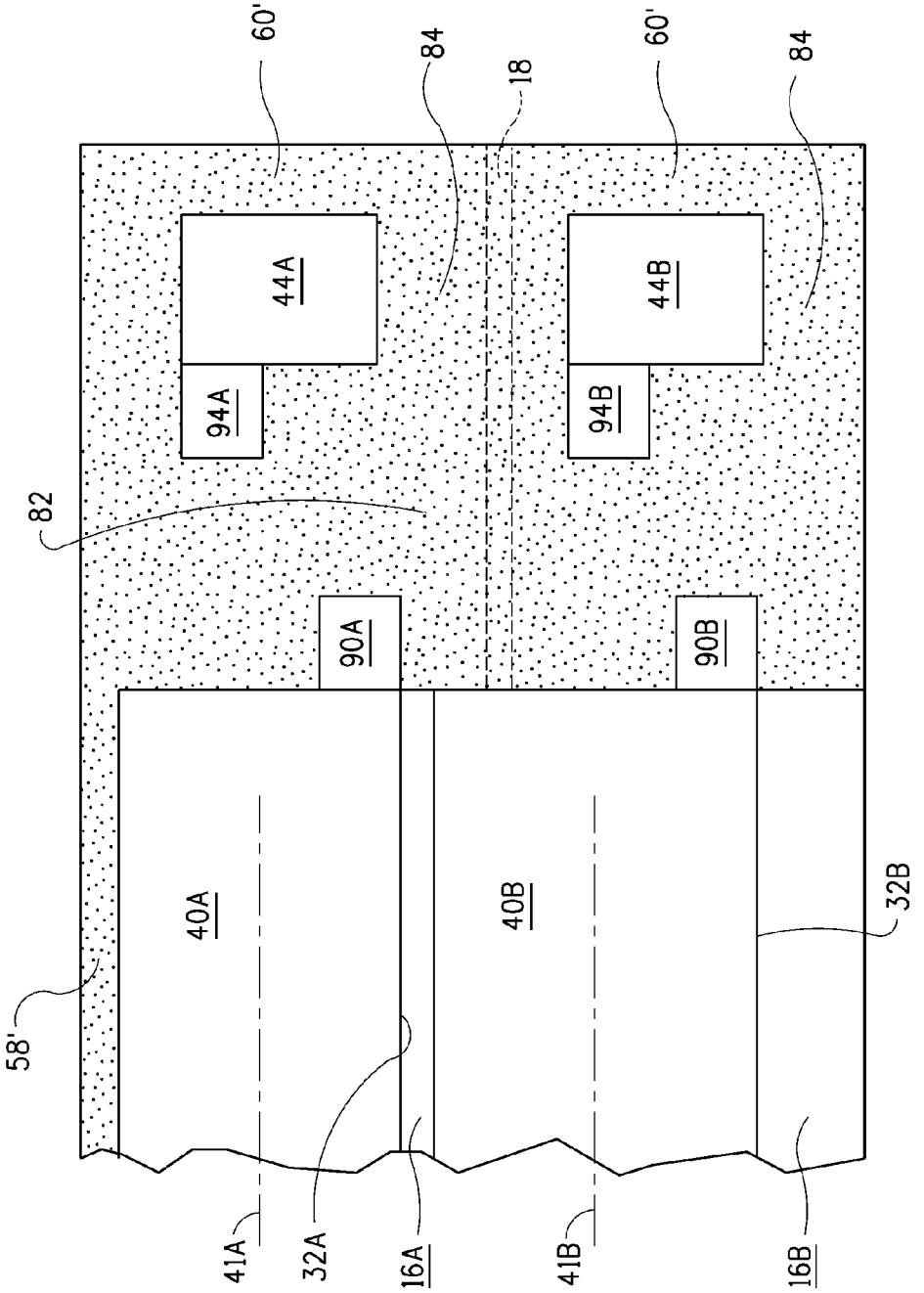

60'
84
18
60'
84
44A
44B
94A
94B
82
90A
90B
40A
40B
32B
58'
41A
32A
16A
41B
16B

FIG. 6A

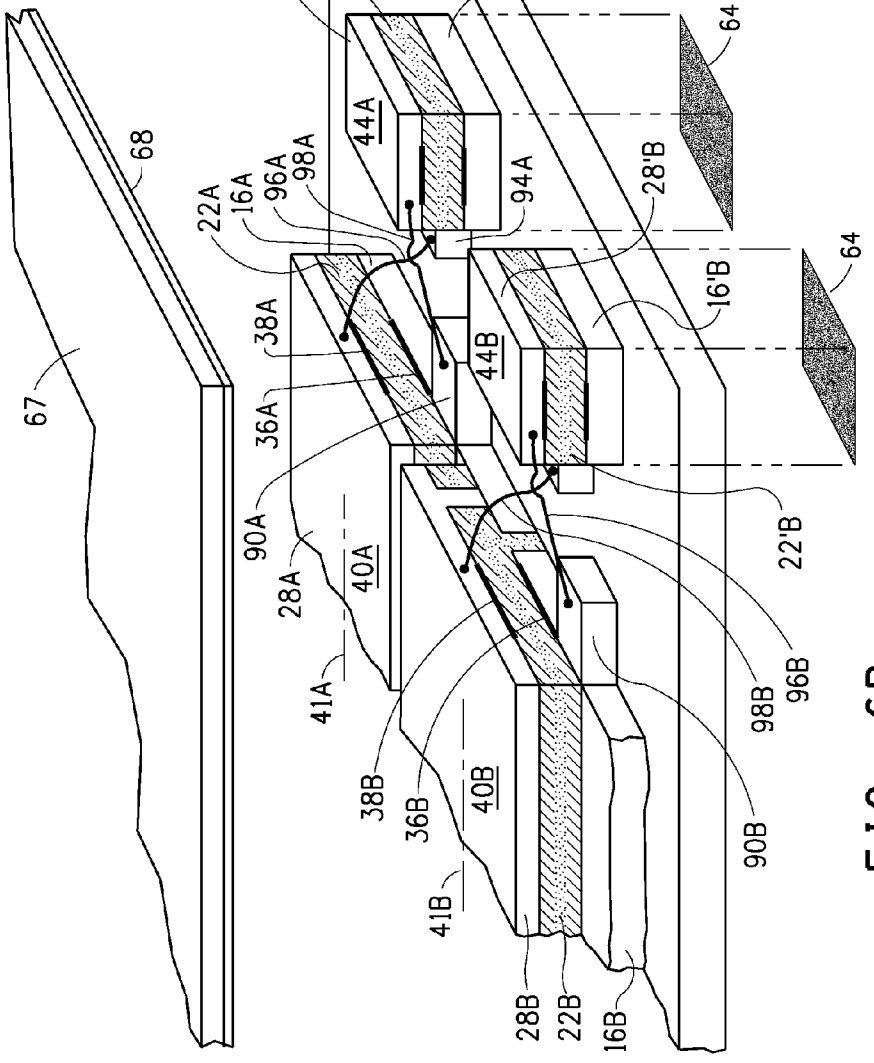

67
68
12
28'A
22'A
16'A
64
44A
96A
98A
22A
16A
94A
28'B
64
38A
16'B
44B
36A
90A
22'B
28A
40A
41A
96B
98B
38B
36B
40B
90B
41B
28B
22B
16B

FIG. 6B

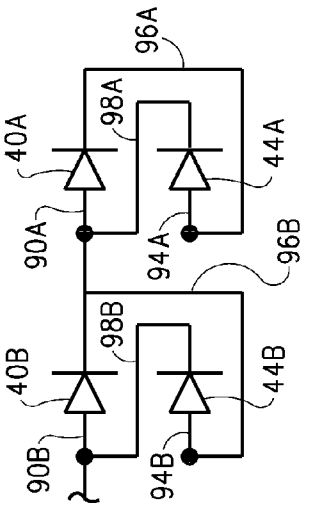

96A
98A
40A
44A
90A
94A
96B
98B
40B
44B
90B
94B

FIG. 6C

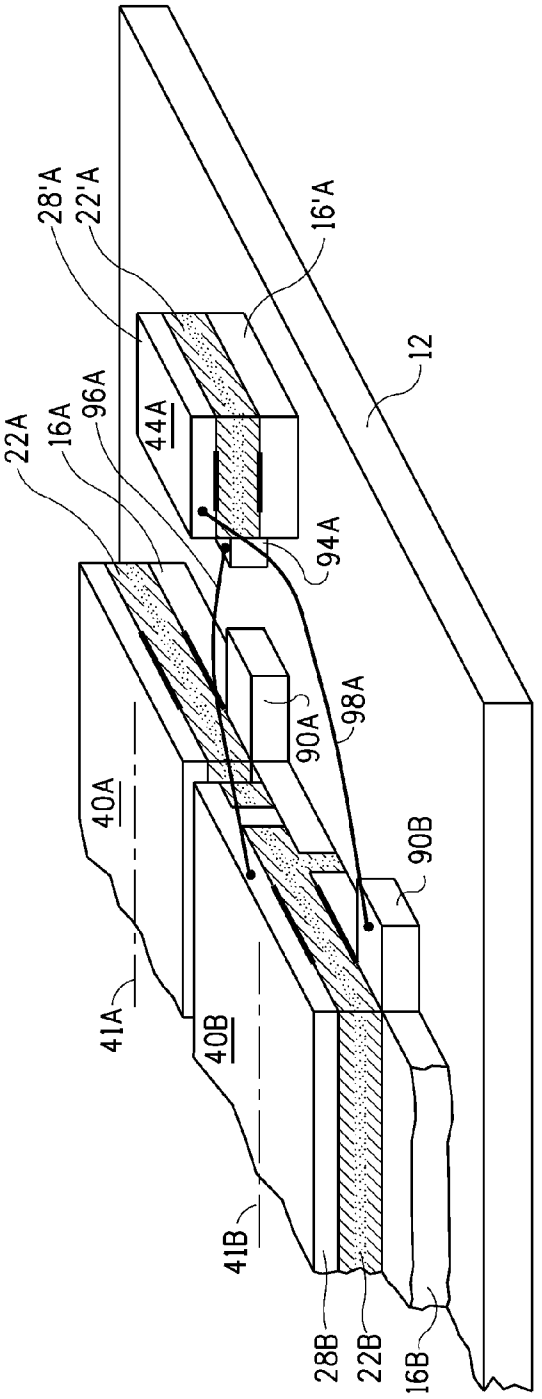

28'A
22'A
16'A
12
22A
16A
96A
44A
94A
98A
90A
40A
90B
41A
40B
41B
28B
22B
16B

FIG. 6D

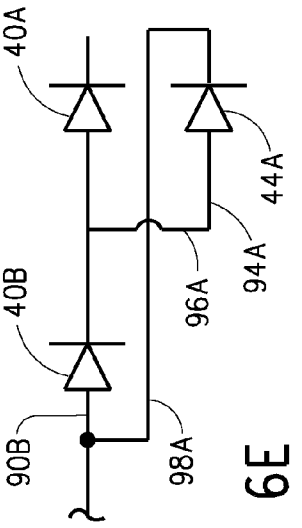

40A
44A
94A
96A
40B
90B
98A

FIG. 6E

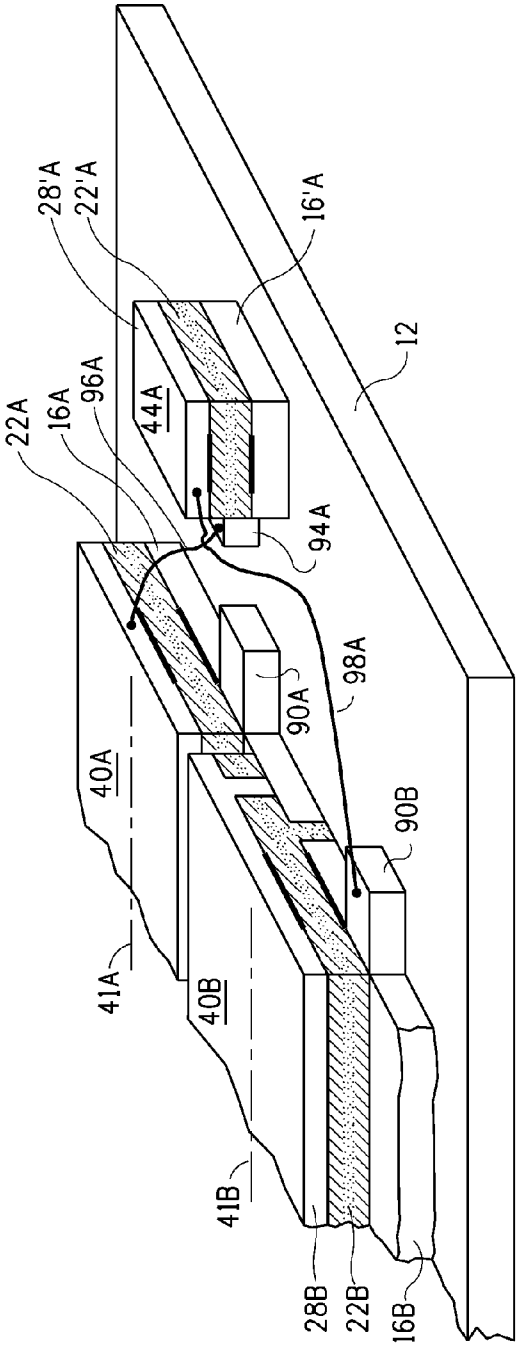

28'A
22'A
16'A
12
22A
16A
96A
44A
94A
98A
90A
40A
90B
41A
40B
41B
28B
22B
16B

FIG. 6F

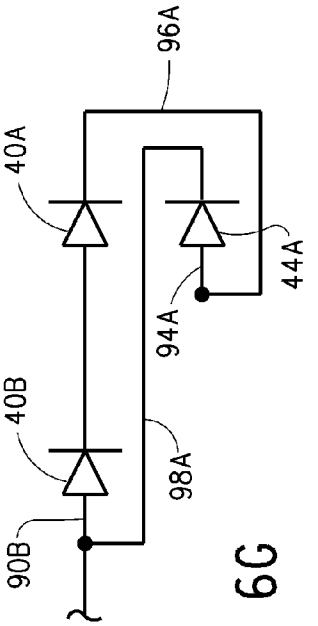

96A
40A
44A
94A
40B
98A
90B

FIG. 6G

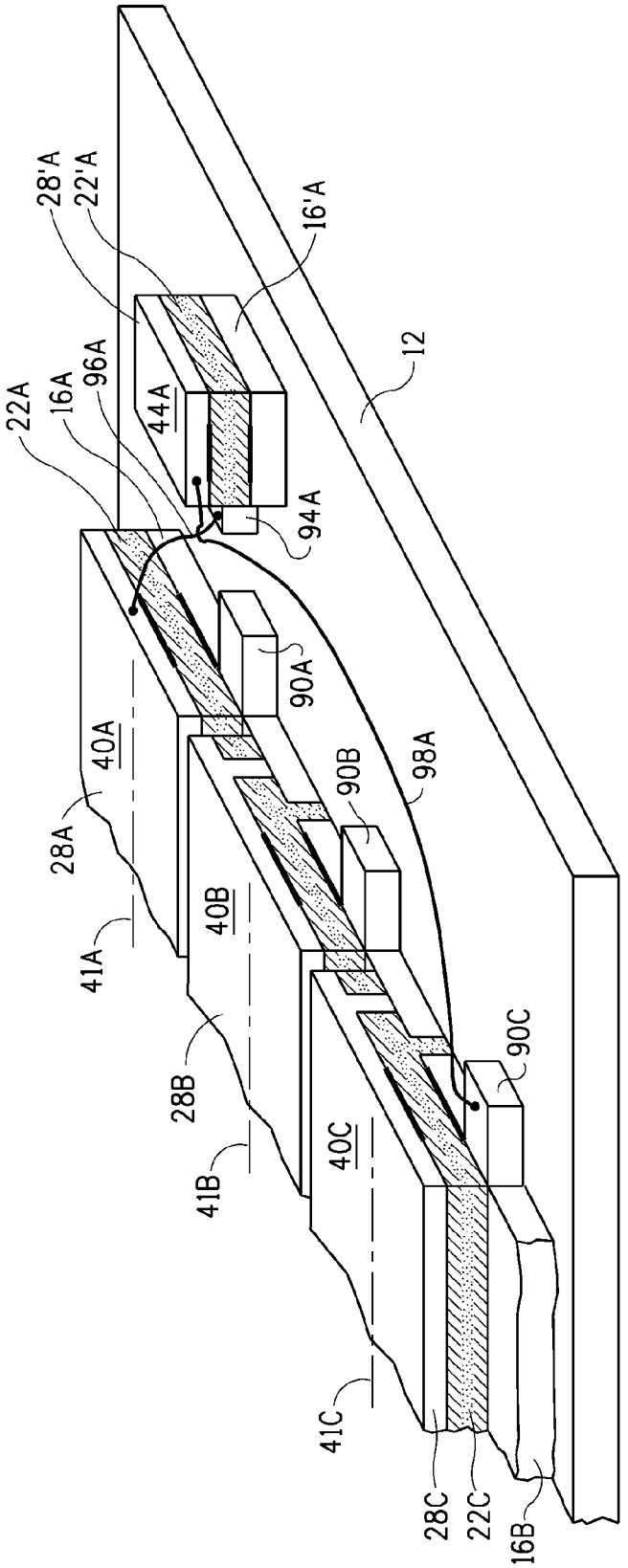

28'A
22'A
16'A
12
22A
16A
96A
44A
94A
90A
98A
90B
40A
28A
40B
41A
28B
41B
40C
90C
41C
28C
22C
16B

FIG. 6H

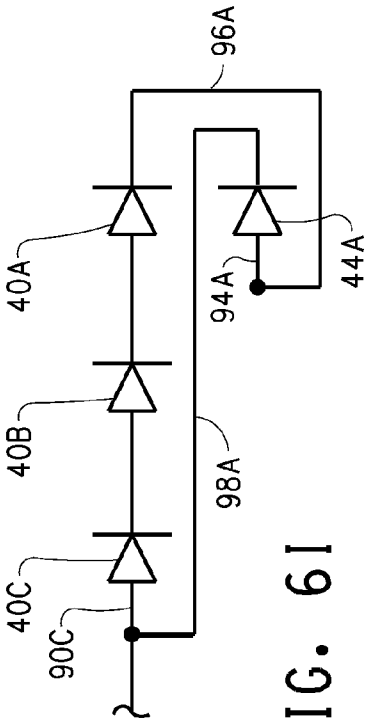

96A
40A
94A
44A
40B
98A
40C
90C

FIG. 6I

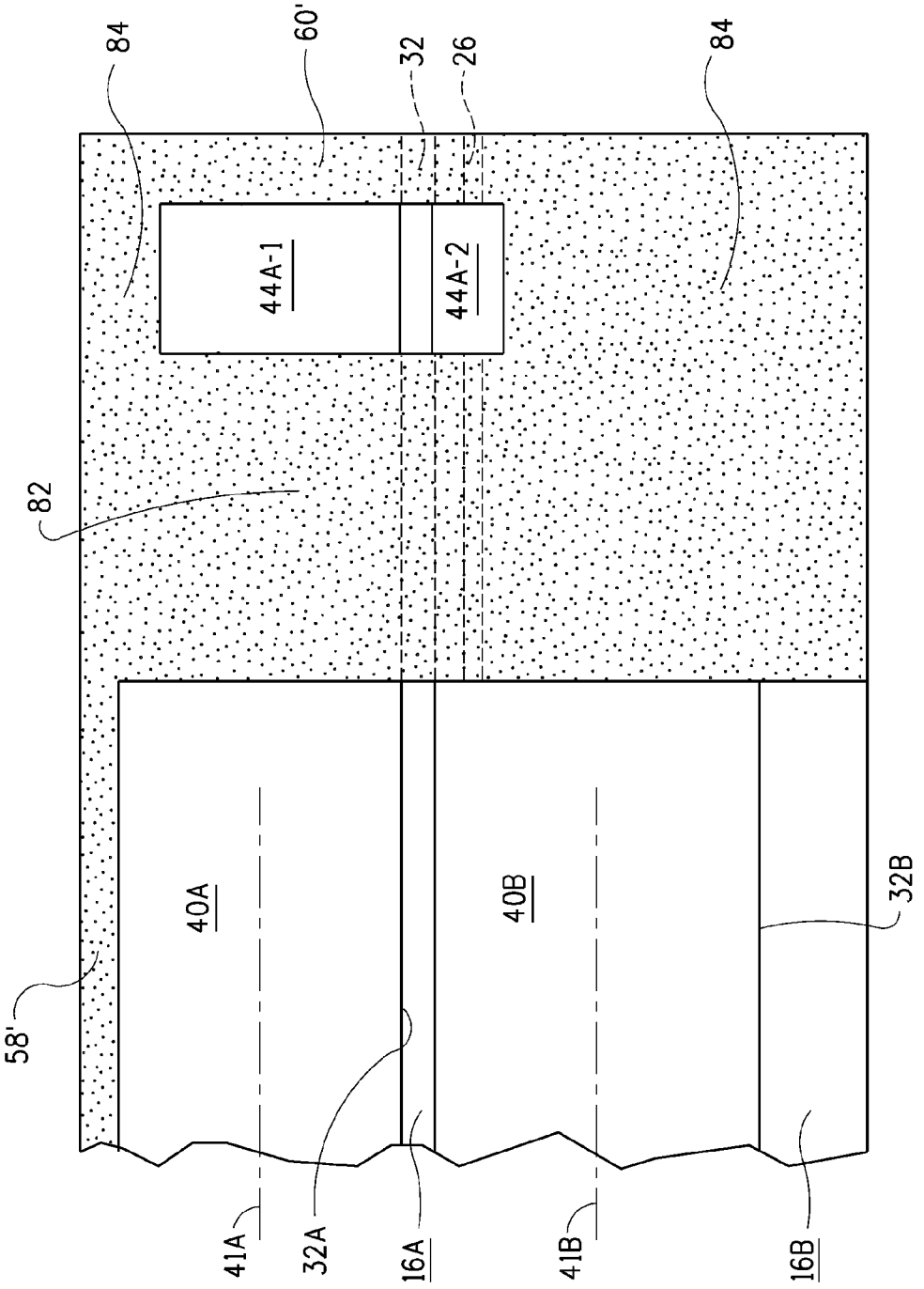


FIG. 7A

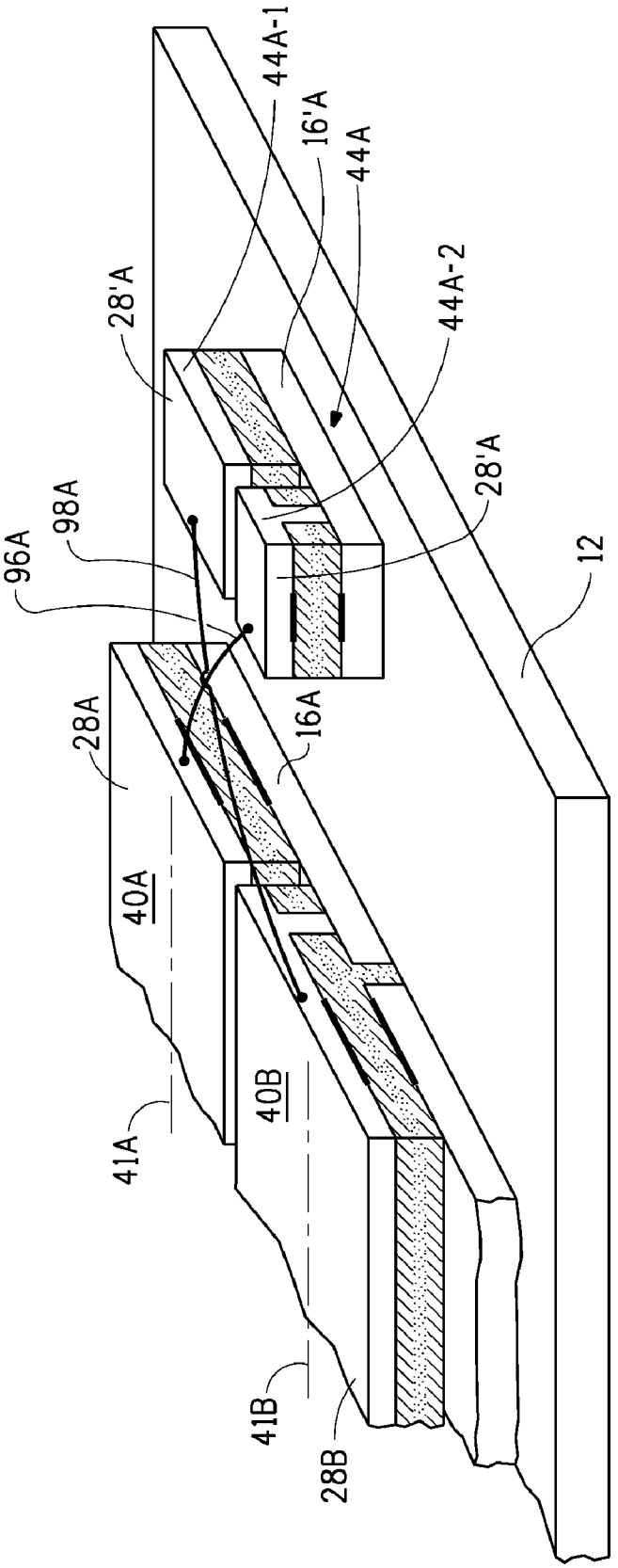


FIG. 7B

ARRAY OF THIN-FILM PHOTOVOLTAIC CELLS HAVING A TOTALLY SEPARATED INTEGRATED BYPASS DIODE AND A PANEL INCORPORATING THE SAME

CLAIM OF PRIORITY

[0001] This application claims priority from each of the following United States Provisional Applications, each of which is hereby incorporated by reference:

[0002] (1) Method For Producing A Thin-Film Photovoltaic Cell Having An Etchant-Resistant Electrode And An Integrated Bypass Diode And A Panel Incorporating The Same, Application Ser. No. 61/414,464, filed Nov. 17, 2010 (CL4618);

[0003] (2) A Thin-Film Photovoltaic Cell Having An Etchant-Resistant Electrode And An Integrated Bypass Diode And A Panel Incorporating The Same, Application Ser. No. 61/414,467, filed Nov. 17, 2010 (CL5112);

[0004] (3) Method For Producing An Array Of Thin-Film Photovoltaic Cells Having An Etchant-Resistant Electrode And An Integrated Bypass Diode Associated With A Plurality Of Cells And A Panel Incorporating The Same, Application Ser. No. 61/414,479, filed Nov. 17, 2010 (CL5230);

[0005] (4) Array Of Thin-Film Photovoltaic Cells Having An Etchant-Resistant Electrode And An Integrated Bypass Diode Associated With A Plurality Of Cells And A Panel Incorporating The Same, Application Ser. No. 61/414,486, filed Nov. 17, 2010 (CL5231);

[0006] (5) Method For Producing An Array Of Thin-Film Photovoltaic Cells Having A Totally Separated Integrated Bypass Diode And Method For Producing A Panel Incorporating The Same, Application Ser. No. 61/485,695, filed May 13, 2011 (CL5113);

[0007] (6) Array Of Thin-Film Photovoltaic Cells Having A Totally Separated Integrated Bypass Diode And A Panel Incorporating The Same, Application Ser. No. 61/485,740, filed May 13, 2011 (CL5114);

[0008] (7) Method For Producing An Array Of Thin-Film Photovoltaic Cells Having A Totally Separated Integrated Bypass Diode Associated With A Plurality Of Cells And Method For Producing A Panel Incorporating The Same, Application Ser. No. 61/485,745, filed May 13, 2011 (CL5232); and

[0009] (8) Array Of Thin-Film Photovoltaic Cells Having A Totally Separated Integrated Bypass Diode Associated With A Plurality Of Cells And A Panel Incorporating The Same, Application Ser. No. 61/485,751, filed May 13, 2011 (CL5233).

CROSS-REFERENCE TO RELATED APPLICATIONS

[0010] Subject matter disclosed herein is disclosed in the following copending applications, all filed contemporaneously herewith and all assigned to the assignee of the present invention:

[0011] Method For Producing A Thin-Film Photovoltaic Cell Having An Etchant-Resistant Electrode And An Integrated Bypass Diode And A Panel Incorporating The Same, application Ser. No. _____, filed Nov. 17, 2010 (CL4618);

[0012] A Thin-Film Photovoltaic Cell Having An Etchant-Resistant Electrode And An Integrated Bypass Diode And A Panel Incorporating The Same, application Ser. No. _____, filed Nov. 17, 2010 (CL5112);

[0013] Method For Producing An Array Of Thin-Film Photovoltaic Cells Having An Etchant-Resistant Electrode And An Integrated Bypass Diode Associated With A Plurality Of Cells And A Panel Incorporating The Same, application Ser. No. _____, filed Nov. 17, 2010 (CL5230);

[0014] Array Of Thin-Film Photovoltaic Cells Having An Etchant-Resistant Electrode And An Integrated Bypass Diode Associated With A Plurality Of Cells And A Panel Incorporating The Same, application Ser. No. _____, filed Nov. 17, 2010 (CL5231);

[0015] Method For Producing An Array Of Thin-Film Photovoltaic Cells Having A Totally Separated Integrated Bypass Diode And Method For Producing A Panel Incorporating The Same, application Ser. No. _____, filed May 13, 2011 (CL5113);

[0016] Method For Producing An Array Of Thin-Film Photovoltaic Cells Having A Totally Separated Integrated Bypass Diode Associated With A Plurality Of Cells And Method For Producing A Panel Incorporating The Same, application Ser. No. _____, filed May 13, 2011 (CL5232); and

[0017] Array Of Thin-Film Photovoltaic Cells Having A Totally Separated Integrated Bypass Diode Associated With A Plurality Of Cells And A Panel Incorporating The Same, application Ser. No. _____, filed May 13, 2011 (CL5233).

BACKGROUND OF THE INVENTION

[0018] 1. Field of the Invention

[0019] This invention relates to a method for producing a thin-film photovoltaic cell having a cell level integrated bypass diode and to the photovoltaic cell produced thereby; and, in particular, to a method which employs one or more chemical etchant(s) to separate a portion of a photovoltaic cell and, by appropriate electrical interconnection, to utilize the separated portion to define a bypass diode for a cell.

[0020] 2. Description of the Art

[0021] A photovoltaic cell converts solar radiant energy (sunlight) incident thereon into electrical energy as the result of the photovoltaic effect. Of particular recent interest is the large-scale and cost-effective conversion of solar radiation into electricity using arrays of photovoltaic cells assembled into photovoltaic panels.

[0022] A typical first generation photovoltaic panel involves first producing a large number of photovoltaic cells from thinly sliced substrates of single or polycrystalline silicon. Cells approximately fifteen centimeters square (15 cm×15 cm) are cut from silicon wafers a few hundred microns in thickness and are connected electrically in series to form strings. Multiple strings are further connected in series or in parallel, arranged on a supporting glass pane, and encapsulated with polymeric resin and film to form a photovoltaic module. The module is usually provided with a frame to form the photovoltaic panel.

[0023] A second generation photovoltaic panel involves utilizing a thin-film of semiconductor material, for example hydrogenated amorphous silicon (a-Si:H), as the active photovoltaic material. The a-Si:H film is deposited on a supporting superstrate in a glow discharge of silane gas. Resulting thin-film silicon devices exhibit solar conversion efficiencies in excess of ten percent (10%). A unit cell and the tandem cell or multi-junction amorphous silicon solar cell can only pro-

vide a small output voltage of up to a few volts (a single junction ~0.9 V; tandem junction ~1.6V; multi-junction, depending upon the number of junctions, more than 2 V). So, a number of solar cells are typically electrically interconnected in series to produce working voltages.

[0024] When all cells in an array are illuminated, each cell will be forward biased. However, if one or more of the cells is partially shaded or shadowed (i.e., not illuminated), such as by falling leaves, snow, or if there are physical differences in the cells such as caused by cell breakage, this mismatch in the properties of interconnected cells can create operating problems for series connected solar cells. This mismatch of different cell in output can dramatically decrease the output current of the entire module, and in some cases the mismatched unit cell merely functions as a load to cause heat generation or reverse bias. The excess heat or the strong reverse bias voltage may permanently damage the unit cell or possibly melt the encapsulate material.

[0025] To guard against such damage it is known to provide a protective bypass diode. One bypass diode may be connected across several cells, or, for enhanced reliability, each cell may have its own bypass diode connected in parallel and in an opposite direction thereto, thereby reducing the influence of such a mismatch. If the cells are working normally with fully illumination and producing energy, the bypass diodes are reverse biased and the current flow is through the cells. However, if any mismatch happens, the current flow through the cell becomes limited and reverse biased, the parallel-connected bypass diode becomes forward biased, and current flow is conducted through the bypass diode, thereby protecting the affected cell.

[0026] U.S. Pat. Pub. No. 2002/0164,834 (Boutros et al.) discloses a method for making a solar cell with an integrated bypass diode. The method comprises multiple steps of depositing layers with opposite type and different level of dopants on one surface layer of the solar cell to form a bypass diode.

[0027] U.S. Pat. No. 6,784,358 (Kukulka) shows a solar cell structure with a discrete amorphous silicon bypass diode. A discrete amorphous silicon bypass diode is supported on either the first or second metallization layer of the cell.

[0028] The above mentioned configurations, however, require additional semiconductor steps to incorporate the diode into the substrate. The approaches are complex and cause assembly difficulties, for example in the case of series connections, it is very complicated. Manufacturing cost increase commensurately.

[0029] Accordingly, in view of the foregoing, it is believed advantageous to provide an efficient method for production of photovoltaic panels with cell-level integrated bypass diodes with reduced costs.

SUMMARY OF THE INVENTION

[0030] In general, the present invention relates to a method for manufacturing a thin-film silicon photovoltaic cell having a cell level integrated bypass diode and to the photovoltaic cell produced thereby.

[0031] The method includes the formation of an array of series-connected solar cells on a support layer. The array includes at least a first, a second and a third solar cell. Each solar cell is a laminated structure comprising: a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type; a front electrode disposed in electrical contact with the semiconducting material of the first type; and a back electrode disposed in electrical contact with the semiconducting material of the second type.

[0032] In accordance with the present invention the method also includes the steps of:

[0033] separating from a selected parent solar cell at least a portion of both the back electrode and the photovoltaic junction layer; and

[0034] using the separated portion of the back electrode, connecting the semiconducting material of the second type of the separated portion of the photovoltaic junction layer to the semiconducting material of the first type of any one chosen solar cell in the array.

[0035] The semiconducting material of the first type in the separated photovoltaic portion of the junction layer may be connected to either the same or a different chosen solar cell in the array such that a bypass diode is disposed parallel with and in opposition to one or more cells in the array.

[0036] In one embodiment of the invention, during the separating step, the front electrode of the parent solar cell is left intact so that the semiconducting material of the first type of the separated portion of the photovoltaic junction layer is electrically connected with the semiconducting material of the second type of the second solar cell through physical contact between the front electrode of the first solar cell and the back electrode of the second solar cell.

[0037] In one instance of this embodiment, if the first and second solar cells are adjacent to each other, during the connecting step the semiconducting material of the second type of the separated portion of the photovoltaic junction layer is connected with the semiconducting material of the first type of the second solar cell so that a bypass diode that is connected in parallel with and in opposition to the second solar cell is defined.

[0038] In another instance of this embodiment, if the first, second and third solar cells are adjacent to each other, during the connecting step the semiconducting material of the second type of the separated portion of the photovoltaic junction layer is connected with the semiconducting material of the first type of the third solar cell, the bypass diode being connected in parallel and in opposition to both the second and third solar cells.

[0039] In yet another instance of this embodiment, if the first and second are adjacent and the third solar cell is spaced a predetermined number of solar cells away from the second solar cell, the semiconducting material of the second type of the separated portion of the photovoltaic junction layer may be connected with the semiconducting material of the first type of the third solar cell, so that the bypass diode is connected in parallel and in opposition to the second and third solar cells and to all solar cells therebetween.

[0040] In an alternate embodiment of the invention, during the separating step a portion of the front electrode is also separated from the parent solar cell thereby totally segregating the separated portions of the front electrode, back electrode and photovoltaic junction layer from the first solar cell.

[0041] The semiconducting material of the second type of the separated portion of the photovoltaic junction layer may be connected with the semiconducting material of the first type of either the parent solar cell or of any other chosen cell. The semiconducting material of the first type of the separated portion of the photovoltaic junction layer may also be connected to the semiconducting material of the second type of either the parent cell or the same or a different chosen cell.

[0042] For example, if the first and the second solar cells are adjacent to each other, and if the first solar cell is the parent solar cell, the semiconducting material of the second type of the separated portion of the photovoltaic junction layer may be connected with the semiconducting material of the first type of either the parent solar cell or the second solar cell. The semiconducting material of the first type of the separated portion of the photovoltaic junction layer may be connected to the semiconducting material of the second type of either the parent cell or the second solar cell. If the materials of the junction layer are each connected to the respective opposite polarity materials of the same cell (i.e., both to either the parent or to the second cell), then the bypass diode is connected in parallel and in opposition to that cell.

[0043] If the materials of the junction layer are connected to the opposite materials different cells (i.e., to the parent and to the second cell), then the bypass diode is connected in parallel and in opposition to those cells.

[0044] In the cell array produced as a result of the method of the present invention the bypass diode is spaced from the selected parent solar cell along the axis of the parent solar cell. In addition, in the preferred instance, corresponding interfaces between each semiconducting material and the electrode with which it is in contact in both the parent solar cell and in the bypass diode are substantially coplanar with the respective first and second interfaces defined in the parent solar cell.

BRIEF DESCRIPTION OF THE DRAWINGS

[0045] The invention will be more fully understood from the following detailed description taken in connection with the accompanying drawings, which form a part of this application, and in which:

[0046] FIGS. **1**A, **1**B and **1**C are diagrammatic, front elevation views entirely in section illustrating the structures formed in an array of photovoltaic solar cells after each of a series of process steps in accordance with one common prior art manufacturing process, while FIG. **1**D is a plan view of the array of cells shown in FIG. **1**C, and FIG. **1**E is the equivalent circuit diagram of the finished cell array;

[0047] FIG. **2**A is a plan view illustrating the array of cells shown in FIGS. **1**C and **1**D wherein an etchant is disposed in a predetermined pattern in accordance with the present invention;

[0048] FIG. **2**B is an elevation view, in section, taken along section lines **2**B-**2**B in FIG. **2**A;

[0049] FIG. **3**A is a stylized perspective view illustrating the structure of two adjacent cells and adjacent bypass diodes resulting after removal of the etchant, with one of the bypass diodes being connected in parallel opposition to one of the cells;

[0050] FIG. **3**B is an equivalent circuit diagram of the cell with opposed bypass diode arrangement shown in FIG. **3**A;

[0051] FIG. **4**A is a plan view generally similar to FIG. **2**A illustrating the array of cells shown in FIGS. **1**C and **1**D wherein an etchant is disposed in an alternative predetermined pattern in accordance with the present invention;

[0052] FIG. **4**B is a stylized perspective view generally similar to FIG. **3**A illustrating the structure of four adjacent cells and adjacent bypass diodes resulting after removal of the etchant disposed in accordance with the pattern of FIG. **4**A, in which one bypass diode is associated with and able to provide bypass protection for more than one solar cell;

[0053] FIG. **4**C is an equivalent circuit diagram of the modified arrangement shown in FIG. **4**B;

[0054] FIG. **5** is a stylized perspective view illustrating the structure of two adjacent cells and adjacent bypass diodes resulting after removal of the first etching paste according to a first implementation of the second embodiment of the present invention;

[0055] FIG. **6**A is a plan view illustrating the array of cells shown in FIG. **5** wherein a second etching paste is disposed in a second predetermined pattern according to the implementation of the second embodiment of the present invention useful when the front electrode is fabricated from an etchant-resistant material;

[0056] FIG. **6**B a stylized perspective view illustrating the structure of two adjacent cells and two totally separated adjacent bypass diodes resulting after removal of the second etching paste, with the bypass diode being connected to the corresponding cell according to the second embodiment of the present invention;

[0057] FIG. **6**C is an equivalent circuit diagram of the cell with the bypass diode being connected to the corresponding cell shown in FIG. **6**B according to the second embodiment of the present invention;

[0058] FIG. **6**D is a stylized perspective view, similar to FIG. **6**B, illustrating a totally separated bypass diode connected to a chosen solar cell in the array other than the parent solar cell;

[0059] FIG. **6**E is an equivalent circuit diagram of the cell with the bypass diode being connected as shown in FIG. **6**D;

[0060] FIG. **6**F is a stylized perspective view, similar to FIG. **6**B, illustrating the structure of two adjacent cells and a single bypass diode, with the bypass diode being connected to the corresponding parent cell and at least one additional cell according to the first implementation of the second embodiment of the present invention;

[0061] FIG. **6**G is an equivalent circuit diagram of the cell with the bypass diode being connected as shown in FIG. **6**F;

[0062] FIG. **6**H is a stylized perspective view, similar to FIG. **6**F, illustrating the structure of three adjacent cells and a single bypass diode, with the bypass diode being connected to the its parent cell and at least one additional cell, with at least one intermediate cell being disposed therebetween;

[0063] FIG. **6**I is an equivalent circuit diagram of the cell with the bypass diode being connected as shown in FIG. **6**H;

[0064] FIG. **7**A is a plan view, similar to FIG. **6**A, showing the disposition of an etching paste according to an alternate implementation of the second embodiment of the present invention useful when the front electrode is fabricated from an etchant-susceptible material;

[0065] FIG. **7**B is a stylized perspective view illustrating a totally separated, dual-lobed bypass diode produced as a result of the etching paste disposed as in FIG. **7**A.

DETAILED DESCRIPTION OF THE INVENTION

[0066] Throughout the following detailed description similar reference numerals refer to similar elements in all Figures of the drawings. It should be understood that details illustrating the structure of the present invention as shown in various Figures have been stylized in form, with some portions enlarged or exaggerated, all for convenience of illustration and ease of understanding.

[0067] FIGS. **1**A through **3**B collectively illustrate the various steps in a method in accordance with a first embodiment of present invention for producing a thin-film photovoltaic

solar cell with an associated cell level integrated bypass diode. The term "cell level" as used in this application means that each bypass diode is produced from the structure of a parent solar cell and the diode is associated with and able to provide bypass protection for at least one photovoltaic solar cell.

[0068] However, it should be understood that a bypass diode formed in accordance with this embodiment of the present invention may be associated with and provide bypass protection for more than one cell, if desired. An illustration of a modified step in the method and the structure and corresponding circuit diagram of the resultant cell/bypass diode combination are shown in FIGS. **4**A, **4**B and **4**C.

[0069] The first step in the method comprises forming an array generally indicated by the reference character **40** (e.g., FIGS. **1**C, **1**D) that includes at least two or more photovoltaic solar cells on the interior surface **121** of a support layer **12**. The support layer **12** has an exterior surface **12**E. The support layer **12** can take any convenient shape but it is usually rectangular (or square) in plan (as illustrated herein). If the surface **12**E eventually defines the sun-facing top surface of a finished photovoltaic panel the support layer is usually termed a "superstrate" and is made of a etchant-resistant transparent material, typically glass or a polymer. Since in the embodiments being described the support layer does define the sun-facing surface of the array being formed, the term "superstrate" shall be used hereafter. However, it should be understood that the present invention is also applicable to an arrangement in which the support layer does not face the sun. In this instance the support layer is usually termed a "substrate". The substrate may be made of etchant-resistant glass, polymer or a non-transparent metal. Although one preferred method of realizing the array of solar cells is described in detail herein, it should be appreciated that the array may be realized using any desired fabrication method.

[0070] FIGS. **1**A through **1**C are diagrammatic front elevation views entirely in section across the width dimension of a portion of the array **40** of series-connected photovoltaic solar cells formed on the superstrate **12**. FIGS. **1**A through **1**C illustrate the structures of the solar cells produced after each of a series of process steps in accordance with one common prior art manufacturing process substantially as disclosed in U.S. Pat. No. 4,292,092 (Hanak). FIG. **1**D is a plan view of a portion of the lengthwise dimension of the cell array **40** shown in FIG. **1**C, while FIG. **1**E is a circuit diagram of the portion of the array **40** shown in FIGS. **1**C and **1**D. The portion of the array **40** illustrated in FIGS. **1**C and **1**D contains five adjacent photovoltaic solar cells, respectively indicated by reference characters **40**A, **40**B, **40**C, **40**D and **40**E, although it should be understood that any convenient number of cells greater than two may be fabricated. In a typical instance, a support layer measuring three-by-five (3×5) feet could contain an array having N solar cells, where N may be on the order of one hundred (100) solar cells, with each cell being approximately 0.35 inches in width.

[0071] FIG. **1**A shows an early step in the formation of the array **40**. In this step substantially the entire interior surface **121** of the superstrate **12** is coated with a layer of a transparent conducting oxide (TOO), generally indicated by the reference character **16**. The TCO layer usually has a thickness on the order of about one micrometer (1 μm). In the structure discussed in FIGS. **1**A through **3**B the transparent conductive oxide is an etchant-resistant electrode material. A suitable etchant-resistant TCO electrode material is halogen-doped tin oxide, such as fluorine-doped tin oxide (FTO). In a second embodiment of the invention to be described the TCO electrode material may be an etchant-resistant material or a material susceptible to either an acid or basic etchant, such as indium doped tin oxide (ITO), zinc oxide (ZnO), gallium oxide (GaO) or tin oxide.

[0072] As shown in FIG. **1**A the electrode layer **16** has a series of breaks **18** formed therein. The breaks **18** extend through the full thickness of the material of the electrode layer **16** to the surface **121** of the glass superstrate **12**. The breaks **18** subdivide the electrode layer **16** into a plurality of electrically isolated strips **16**A through **16**E. Each strip **16**A through **16**E extends lengthwise along the superstrate **12** (i.e., into the plane of FIGS. **1**A,**1**C and along the plane of FIG. **1**D). Each strip **16**A through **16**E serves to define an incident, or front, electrode for a respective solar cell **40**A through **40**E, as will be described.

[0073] The breaks **18** may be formed using a laser-scribing process. Laser scribing involves scanning a focused laser beam of sufficient power and appropriate wavelength to ablate a narrow width of the electrode layer along the scan line.

[0074] Since the electrode material is etchant-resistant it is difficult to remove chemically. Accordingly, before or after the laser scribing that produces the breaks **18** the entire peripheral margin of the electrode layer **16** is removed by mechanical action, such as grinding or sand blasting. A portion of the removed region **16**R of the electrode layer **16** is indicated in phantom lines on FIG. **1**A. Removal of the region **16**R from the margin of the electrode layer **16** exposes a portion of the interior surface **121** of the superstrate **12** and defines a peripheral edge **16**G along the width and/or length dimensions of the electrode strips. The edge **16**G is typically located at about one centimeter (1 cm) inwardly of the peripheral edge **12**P of the superstrate **12**. Since such mechanical removal is a dusty process it is usually performed away from the clean room area where the other steps of the process are performed. After mechanical removal of the electrode material the superstrate **12** is thoroughly washed in preparation for further processing steps.

[0075] As a next step, illustrated in FIG. **1**B, a photovoltaic junction layer generally indicated by the reference character **22** is deposited over the superstrate **12** and the electrode strips **16**A through **16**E thereon. In practice, the junction layer **22** is the active region of the solar cell (and any diode formed therefrom) and comprises at least one stratum of a semiconducting material of a first type (e.g., "p-type" amorphous silicon material), at least one stratum of a semiconducting material of a second type (e.g., "n-type" amorphous silicon material), and, optionally, one or more intermediate stratum (a) of an intrinsic semiconducting material. In the drawings the strata of "p-type" and the "n-type" amorphous semiconducting materials in the junction layer **22** are illustrated by hatching and any intermediate stratum(a) of intrinsic semiconducting material is indicated by stippling. As seen in FIG. **1**B the junction layer **22** extends into and fills the breaks **18** between adjacent front electrode strips. The junction layer **22** extends beyond the edge **16**G of the electrode **16**A and lies directly on the exposed glass extending along the peripheral regions of the superstrate **12**. The absence of electrode material in these peripheral regions imparts a rolled-off contour **22**R to the junction layer **22** along the portions of the perimeter of the superstrate **12** from which the front electrode is removed. It should be noted that if bypass diodes are to be

formed in accordance with either implementation of the second embodiment of the invention (to be discussed herein), the removal of electrode material from the region **16**R along the peripheral margin of the array may be omitted.

[0076] Each of the various strata of materials forming the photovoltaic junction layer may be deposited using any one of a variety of deposition techniques, including PECVD, hot wire CVD, and photochemical vapor deposition in the presence of silane and other alloying and doping gases, for example phosphine for n-type amorphous silicon and diborane for p-type amorphous silicon. Typically each silicon stratum ranges in thickness from a few hundred nanometers (amorphous silicon) to a few thousand nanometers (microcrystalline silicon), such that the overall thickness of the junction layer is on the order of few hundred nanometers to a few micrometers. The strata of "p-type" and the "n-type" materials may be reversed in a "substrate" structure which can use non-transparent material as the support layer and in which light enters from the opposite side of the cell.

[0077] Once deposited, the photovoltaic layer **22** is itself separated into adjacent strips **22**A through **22**E of semiconducting material by breaks **26**. The breaks **26** may be formed by laser scribing. The breaks **26** run parallel to but slightly displaced from the breaks **18** between adjacent front electrode strips. Each break **26** extends through the full thickness of the junction layer **22** and exposes a portion of the surface of a front electrode strip **16**A through **16**E, as the case may be.

[0078] The next step in the process of forming the array **40** of photovoltaic solar cells is shown in FIGS. **1**C and **1**D. In this step a second layer of an electrically conductive material, generally indicated by the reference character **28**, is deposited over the entire photovoltaic junction layer **22**. This second conductive layer **28** forms the back electrode of each solar cell in the array.

[0079] The conductive material of the second conducting layer **28** not only covers the entire surface of each strip **22**A through **22**E of the junction layer, but also extends into and fills the breaks **26** to make electrical contact with the surface of the front electrode strip exposed by the break **26**. The contact point between paired back and front electrodes is indicated in the Figures by reference character **30**. The back electrode layer **28** also exhibits a rolled-off contour **28**R imparted due to presence of the rolled contour **22**R of the photovoltaic layer **22** defined along the periphery of the superstrate **12**.

[0080] The material of the back electrode **28**, for example, silver, may be deposited by sputtering to a thickness on the order of a few hundred nanometers. Of course, a different conductive material may be used and applied in any convenient manner. For example, for some silicon thin-film modules, in order to improve electrical performance the back electrode may be formed from two or more layers of chemically distinct materials. Such a dual layer back electrode comprising a first stratum of zinc oxide (ZnO) and a second stratum of silver is well known.

[0081] A third laser scribing operation forms breaks **32** that run parallel to but slightly displaced from the breaks **26** in the junction layer **22**. The breaks **32** separate the second electrode layer **28** into adjacent strips **28**A through **28**E. Usually the breaks **32** also extend through the respective strips **22**A through **22**E of the photovoltaic junction layer lying beneath the electrode strips **28**A through **28**E.

[0082] The regions **34**B are electrically short-circuited "dead regions" because the front side electrode (FTO) and back side electrode (metal) are connected.

[0083] As described in U.S. Pat. No. 4,292,092 (Hanak), a continuously excited (CW) neodymium YAG laser radiating at 1.06 micrometers operated in a Q-switched mode at a pulse rate of about 36 kHz and a scribing rate of about 20 cm/sec can be used in the laser scribing process. The power for first laser scribe (breaks **18** in the TCO layer) is about 4.5 watts. The power for the laser scribe to form the breaks **26** (FIG. **1**B, TCO+a-Si) is about 1.7 watts, and the power for the laser scribe to form the breaks **32** (FIG. **1**C, a-Si+metal) is about 1.3 watts.

[0084] The net result of the combination of steps shown in FIGS. **1**A through **1**D is the formation of an array **40** comprising a plurality of individual photovoltaic solar cells **40**A through **40**E each supported on the superstrate **12**. Each solar cell **40**A through **40**E has a respective major axis **41**A through **41**E (FIGS. **1**D, **2**A, **3**A) that extends along the lengthwise dimension of the array. Each solar cell **40**A through **40**E is formed as a laminated structure comprising:

[0085] a photovoltaic junction layer (**22**A through **22**E, respectively) having at least a semiconducting material of a first type and a semiconducting material of a second type;

[0086] a respective front electrode **16**A through **16**E (in this embodiment formed of an etchant-resistant transparent conductive oxide); and

[0087] a respective back electrode **28**A through **28**E.

[0088] Each front electrode **16**A through **16**E is in electrical contact with one stratum of semiconducting material in a respective strip **22**A through **22**E of the junction layer. The interface **36**A through **36**E between a front electrode **16**A through **16**E and one of the semiconducting materials of its associated junction layer strip **22**A through **22**E is indicated in the Figures as a bold dark line. The major portion of each interface **36**A through **36**E (other than the rolled-off contour **28**R of the cell **40**A) is substantially planar and extends substantially parallel to the interior surface **121** of the superstrate **12**.

[0089] Each back electrode **28**A through **28**E is in electrical contact with one stratum of semiconducting material in its respective associated strip **22**A through **22**E of the junction layer. The major portion of the interface **38**A through **38**E between a back electrode **28**A through **28**E and one of the semiconducting materials of its associated junction layer strip **22**A through **22**E (again excluding consideration of the rolled-off contour **28**R of the cell **40**A) appear as a bold dark line in the Figures. The major portion of each interface **38**A through **38**E is also substantially planar and extends substantially parallel to the interior surface **121** of the superstrate **12**.

[0090] An equivalent electrical schematic diagram of the diode array is illustrated in FIG. **1**E. Each diode in the array is electrically connected in series with an adjacent diode by virtue of the electrical contact (for example, as illustrated at contact points **30**B through **30**E in FIG. **1**C) between the front electrode of one cell with the back electrode of an adjacent cell.

[0091] In accordance with the first embodiment of the present invention a cell level bypass diode for each solar cell is formed by separating or segregating a relatively smaller sized portion of the laminated structure from a solar cell. Each separated portion **44**A through **44**E (FIG. **3**A), when inter-

connected as will be discussed, defines the cell level bypass diode for one or more adjacent cells.

[0092] Each bypass diode may be separated from a parent solar cell by the application of at least one selected chemical etchant material deposited in a predetermined "positive" pattern over the photovoltaic cell array **40**. This technique is described more fully herein.

[0093] Alternatively, a masking paste may be applied in an inverse pattern which leaves the unmasked areas uncovered. After the masking paste is dried, the unmasked areas are exposed to a wet etchant. The unmasked areas may be exposed by applying the wet etchant directly thereto or by immersing the entire cell array into the wet etchant. The masking paste is then stripped away. In this alternative method the pattern of the mask is the invert of the "positive" pattern created when using etchant paste.

[0094] A suitable masking paste typically comprises high-boiling solvents (boiling point>180° C.), such as terpineol (1-methyl-4-(1-methylvinyl)cyclohexan-1-ol) or texanol (2,2,4-trimethyl-1,3-pentanediolmono(2-methylpropanoate)); acid-resistant polymers, such as co-polymers of methacrylic acid and methyl methacrylate, polyphenols and epoxy resins; thermal or photoinitiators; rheology modifiers, such as fumed silica or carbon black; acid-resistant fillers, such as graphite, TiO_2, alumina, or tin oxide particles; pigment particles; surfactants; and optionally monomers containing two or more reactive groups. The masking paste is formulated to provide good screen-printed fine features, long on-screen time, high etchant resistance, and ease of aqueous stripping. Masking paste compositions can also be formulated to provide features such as good environmental durability, good adhesion to the back electrode and panel encapsulant. They may be customized for color and texture.

[0095] FIGS. **2**A and **2**B show respective plan and cross sectional views of the array **40** of FIGS. **1**C and **1**D with a coating of an etchant paste disposed over the back electrode surface in accordance with a first embodiment of the method of the present invention. The positive pattern of the etchant paste is indicated in FIGS. **2**A and **2**B by the stippled hatching.

[0096] As best seen in FIG. **2**A, to separate a bypass diode from each solar cell in the array the predetermined etchant paste pattern includes a stripe **52** of paste that extends transversely across all of the solar cells **40**A through **40**E in a direction substantially perpendicular to the major axes **41**A through **41**E of the cells. The stripe **52** is intersected by a plurality of relatively shorter stripes **54** of etchant paste that are positioned as will be described between the major axes of adjacent cells and extend generally parallel to those major axes. As suggested in FIG. **4**A, if it is not desired to separate a bypass diode from a given parent solar cell, it is simply necessary to omit the portion of the stripe **52** of etchant paste over that cell or cells.

[0097] The width dimension of the stripe **52** should be sufficient to separate a junction layer of the diode being formed from its parent cell without unduly sacrificing operative surface area from that parent. A width dimension on the order of about 0.2 cm is convenient to meet these conflicting needs.

[0098] Each stripe **54** should be sufficiently wide and positioned so as to overlie at least the location of the scribed break **18** in the front electrode layer **16**. The width of each stripe **54** may optionally be sufficient to cover the break **26** or both the breaks **26** and **32**. FIGS. **2**A and **2**B and FIG. **4**A show the case in which the stripe **54** covers all three breaks **18**, **26** and **32** in the front electrode layer **16**, the photovoltaic junction layer **22**, and the back electrode layer **28**, respectively.

[0099] The etchant paste pattern may further include first and/or second edge isolation stripe(s) **58**, **60**. The first edge isolation stripe(s) **58** (only one of which is illustrated in FIGS. **2**A and **2**B and **4**A) extend(s) along one or both of the lengthwise peripheral edges of the array **40**. Additionally or alternatively, the second edge isolation stripe(s) **60** (only one being illustrated in FIGS. **2**A, **4**A) extend(s) along one or both of the widthwise peripheral edges of the array **40**. The stripes **58** and/or **60** should each have a width dimension on the order of about 0.6 cm which is generally sufficient to produce edge isolation regions for further encapsulation of the cell array.

[0100] In general, the chemical composition of the etchant paste should be properly formulated to provide effective etch removal of both the back electrode layers and the junction layers lying within the predetermined paste pattern. The etchant paste may be either acidic or basic in nature.

[0101] A suitable acidic etchant paste contains a silver and silicon etchant selected from the group consisting of nitric acid, hydrochloric acid, hydrofluoric acid, and mixtures thereof. A combination of nitric and hydrofluoric acids is preferred. The mixture of materials is carried in a polymer binder. Hydrochloric acid may be used to etch zinc oxide or metals (such as aluminum) if such are used. Referencing the dual layer back electrode structure discussed earlier, hydrochloric acid can be combined with nitric acid to form an effective etchant paste for the ZnO and silver layers. The binder comprises polymeric materials selected from the group consisting of poly(vinyl alcohol), poly(ethylene oxide), polyvinylpyrrolidone (PVP) poloxamers and mixtures thereof. Poloxamers are nonionic triblock copolymers composed of a central hydrophobic chain of polyoxypropylene, flanked by two hydrophilic chains of polyoxyethylene.

[0102] A suitable basic etchant paste contains multiple caustic etching components selected from the group consisting of alkali hydroxide (such as sodium or potassium hydroxide), ammonium hydroxide and tetramethylammonium hydroxide. The basic mixture of materials is also carried in a polymer binder.

[0103] The etchant paste can be dispensed using any suitable dispensing technique used for screen, nozzle or ink-jet printing. This is a very convenient single step patterning technique requiring minimal equipment.

[0104] These same acids or bases can be used to produce a wet acidic etchant material or a wet basic etchant material, as the case may be.

[0105] When using either an etchant paste or a wet chemical, the etchant paste or a wet chemical is allowed to chemically etch the back electrode layer and the underlying junction layer for a predetermined dwell time depending on the concentration of the etchant and the thickness of the back electrode and the silicon layer. For the thickness of the front electrode, photovoltaic and back electrode layers as discussed above, a dwell time on the order of minutes is usually sufficient. As examples, for single junction a-Si cell, a dwell time on the order of one to two minutes may be sufficient. For a tandem junction solar cell which includes microcrystalline silicon (μc-Si), a more concentrated etchant is needed, otherwise a longer dwell time, on the order of five to ten minutes, is needed.

[0106] Optionally, in order to reduce the required dwell time, the chemical etchant may be heated to a temperature in

the range from about 50° C. to about 200° C., and more particularly to a temperature in the range from about 50° C. to about 100° C. One convenient expedient for raising the temperature of the chemical etchant is to raise the temperature of the superstrate using a suitable heating apparatus, such as a hot plate.

[0107] At the expiration of the dwell time the superstrate is sprayed with high pressure water or aqueous alkaline solution in order to wash off the etchant material. This insures no etchant material is present to cause deterioration of a resultant solar panel after encapsulation.

[0108] FIG. **3**A shows a stylized perspective view of a portion of the array after removal of the etchant paste. The paste is operative to remove from each cell **40**A, **40**B selected portions of the back electrode and the photovoltaic junction layer lying within the predetermined pattern (FIG. **2**A). Because the material of the front electrode is resistant to etchant it is exposed but left intact. The Si material in the scribed break **18** between adjacent front electrode strips **16**A, **16**B is also removed. Thus, as a result of the etching action, each silicon solar cell strip which has been exposed to the etchant material is separated into two parts: viz., a major active cell (e.g., parent solar cells **40**A, **40**B) and respective bypass diodes (e.g., diodes **44**A, **44**B).

[0109] Specifically, the bypass diode **44**A includes both a portion **22'**A of a photovoltaic junction layer (separated from the photovoltaic junction layer **22**A of the parent cell **40**A) and a portion **28'**A of the back electrode (separated from the back electrode **28**A of the parent cell **40**A) (FIG. **3**A). The primed reference characters indicate that the primed elements of the bypass diode were previously integral with the corresponding elements of the solar cell. The separated portion of the junction layer **22'**A is supported by the front electrode **16**A.

[0110] Structurally, the junction layer **22'**A of the bypass diode **44**A is spaced a predetermined distance **45** in a direction substantially parallel to the major axis **41**A from the junction layer **22**A of the first cell **40**A. This predetermined distance **45** is governed by the dimension of the stripe **52** of etchant. Similarly, the lateral spacing between the adjacent bypass diodes **44**A, **44**B is governed by the dimension of the etchant stripe **54**. The dimensions of the stripes **52**, **54** are selected such that the surface area of the bypass diode **44**A is within the range from about one percent (1%) to about five percent (5%) of the surface area of the first solar cell **40**A.

[0111] In addition to the axial spacing, in the preferred instance the interface **36'**A defined within the diode **44**A between the front electrode **16**A and the one of the semiconducting strata of the separated junction layer **22'**A is substantially coplanar with the corresponding interface **36**A defined in the parent cell **40**A. Similarly, the interface **38'**A defined within the diode **44**A between the back electrode **28'**A and the other semiconducting strata of the separated junction layer **22'**A is substantially coplanar with the corresponding interface **38**A in the parent cell **40**A. However, it lies within the contemplation of the present invention that the interfaces **36**A, **36'**A may be vertically offset with respect to each other. Such a structural arrangement may be produced, for example, by forming the superstrate **12** in such a way that the regions of the superstrate on which the bypass diodes will be formed are either relatively thicker or thinner than the thickness dimension of the regions of the superstrate on which the solar cells are formed.

[0112] The bypass diode **44**B, separated by the action of the etchant from its parent solar cell **40**B, is analogously configured and supported on the front electrode **16**B.

[0113] It is noted that if edge isolation etchant stripe(s) **58** and/or **60** are deployed the action of the etchant would remove both the back electrode and the junction layers in those regions, thus exposing the peripheral margins of the superstrate and define a set-back for the diodes **44**A, **44**B from the widthwise edges of the superstrate.

[0114] The equivalent electrical schematic diagram of the interconnection of the diode **44**A with the first and second solar cells **40**A, **40**B is shown in FIG. **3**B. Electrically, the semiconducting material of the first type of the separated portion of the junction layer **22'**A of the diode **44**A is connected via the front electrode **16**A to the back electrode **28**B, as illustrated by the dot-dash connection line **46**. The front electrode **16**A thus electrically links the semiconducting material of the first type of the separated portion of the junction layer **22'**A with the semiconducting material of the first type of the solar cell **40**A and with the semiconducting material of the second type of the second solar cell **40**B (through the back electrode **28**B of the second solar cell **40**B).

[0115] A separate electrical connection **48** is defined between the semiconducting material of the second type of the separated portion of the junction layer **22'**A of the diode **44**A and the semiconducting material of the first type of the second solar cell **40**B. Specifically, this connection **48** conveniently extends between the portion of the back electrode **28'**A of the diode **44**A and the front electrode **16**B of the second solar cell **40**B. The connection **48** may be implemented by a discrete wire to connect the bypass diode **44**A with the front electrode **16**B. Alternatively, a metallization may be printed using a screen, nozzle, or ink-jet printing technique to extend over the exposed peripheral portions of the superstrate. Disposing the metallization on the bare glass of the front edge region of the superstrate avoids any shunt problem.

[0116] As a result of these electrical interconnections it may be appreciated that a cell level bypass diode (e.g., the diode **44**A) may be formed on the superstrate by separation from a parent solar cell and electrically connected in parallel and in opposition to a second solar cell (e.g., the cell **40**B). Each of the other bypass diodes separated from a cell in the array may be interconnected with the adjacent cell in a manner analogous to that described hereinabove. In such an arrangement each diode is connected in a one-to-one relationship with a solar cell.

[0117] Since the bypass diode **44**A separated from the solar cell **40**A has been interconnected with the adjacent cell **40**B an external diode **62** is connected by lines **63**A, **63**B between the respective front and back electrode **16**A, **28**A of the cell **40**A. The external diode **62** may be conveniently mounted on an edge isolation region of the superstrate. The conducting lines **63**A, **63**B may be implemented by a metal paste dispensed on by screen, nozzle, or ink-jet printing techniques, or metal wires applied by soldering or any known methods.

[0118] Alternatively, the external diode **62** can be located in a completely isolated area segregated from any part of the solar cell. Both the front and back electrodes of this external diode **62** should be segregated from main solar cells. To do so, for example, the front electrode can be cut by using laser scribing.

[0119] It should also be understood that the bypass diodes are photodiodes, and as such, generate current. But since the

area of the bypass diode used in the invention is so small compared to the active solar cells (for example less than 5%, or more particularly about 1%), the diodes won't influence the performance of the active solar cells.

[0120] The bypass diodes can also be optionally sheltered from illumination with an additional processing step that produces an opaque layer **64** on the exterior surface **12**E of the superstrate **12**. An example of an opaque layer **64** is indicated in FIG. **3**A by dashed lines. As suggested in the drawing the opaque layer **64** is positioned on the exterior surface **12**E to align with footprint of the diode **44**A, thereby shadowing the same. A suitable material for the opaque layer is dark paint or a polymer layer with dark pigment.

[0121] As noted earlier it lies within the contemplation of the present invention that a diode needs not be separated from each solar cell in the array **40**. As shown in FIG. **4**B diodes **44**A, **44**D have been separated from their parent solar cells **40**A, **40**D. As a result of a positive or inverted paste pattern deployed as shown in FIG. **4**A the cells **40**B, **40**C have been left intact. Each solar cell (as cells **40**B, **40**C) from which a diode is not separated extends for their full length along the superstrate. However, a diode, such as the diode **44**A that is formed by separation from a parent solar cell **40**A in accordance with the method of the present invention may be electrically connected in parallel and in opposition to additional cells beyond the next-adjacent (full length) solar cell **40**B. For example, as shown in FIG. **4**B the diode **44**A may be connected in parallel and opposition to a series connection that includes the next adjacent solar cell **40**B and one (or more) spaced solar cells (e.g., the cells **40**C, **40**D or therebeyond).

[0122] These electrical connections and corresponding schematic diagram are illustrated in FIGS. **4**B and **4**C. The physical connection between the anode of the bypass diode **44**A and the cathode of the next-adjacent solar cell **40**B is effected through contact between the front electrode of the bypass diode **44**A and the back electrode **28**B of the next-adjacent solar cell **40**B. The physical connection between the cathode of the bypass diode **44**A and the anode of another solar cell **40**D is effected using a separate electrical conductor **48'**.

[0123] Still further, it should also be appreciated from the foregoing that instead of using an area of a solar cell disposed near an axial end, an area of the solar cell intermediate the ends (e.g., a location near the middle of the solar cell) can also be separated and used to form the bypass diode so long as a suitable modification to the paste pattern is made. It is also within the contemplation of the invention to form several bypass diodes from a single cell. For example, the two end areas of the solar cell may be separated, and make two bypass diodes for a single solar cell.

[0124] The array of thin film solar cells and bypass diode(s) formed as described may be finished and formed into a photovoltaic panel by attaching a bus bar with solder and heat sealing with resin and fluoropolymer films, covering with an encapsulant adhesive **67** (such as EVA ethylene vinyl acetate copolymer) and a second exterior support layer **68**.

[0125] -o-0-o-

[0126] In accordance with a second embodiment of the present invention a cell level bypass diode is formed by totally separating (or segregating) a portion of the complete laminated structure from one solar cell and appropriately interconnecting the separated portion to its parent and/or to one or more additional cells. As will be developed, in connection with this embodiment of the invention, the material used to form the front electrode may be either an etchant-resistant material or an etchant-susceptible material. Depending upon the nature of the front electrode material the separation of a bypass diode from a parent cell may be effected using one of two alternative implementation modes. In a first implementation (FIGS. **5**A, **6**B) a bypass diode is separated from a parent cell using two discrete etching steps which sandwich an intermediate material conversion step. In an alternative implementation (FIG. **7**A) the diode is formed using a single etching step.

[0127] The first step in practicing either implementation of the second embodiment of the invention involves the disposition of a first etching paste in a first predetermined pattern over the back electrode surface.

[0128] The first predetermined etching paste pattern is the same as that described in the first embodiment shown in FIG. **2**A. The pattern includes a first stripe **52** of the first etching paste that extends transversely across the first solar cell **40**A in a direction substantially perpendicular to the major axis **41**A of the first cell. The first stripe **52** of the first etching paste is intersected by a plurality of relatively shorter stripes **54** that are positioned between the major axes of adjacent cells and extend generally parallel to those major axes.

[0129] The implementation of the second embodiment used when the front electrode is fabricated from an etchant-resistant material is discussed first. In this case the first etching paste used is the same as that used in the first embodiment, comprising a first acidic etchant and a binder. The first acidic etchant contains only an etchant for the semiconducting material and the back electrode. In general, the chemical composition of the first acidic etchant should be properly formulated to provide effective etch removal of both the back electrode layers and the junction layers lying within the first predetermined etching paste pattern to expose the front electrode. The binder comprises polymeric materials which is similar to those described in the first embodiment.

[0130] The first etching paste can be dispensed again using any suitable dispensing techniques such as used for screen, nozzle or ink-jet printing.

[0131] The first etching paste pattern may further include first and/or second edge isolation stripe(s) **58**, **60** similar to those in the first embodiment.

[0132] The first etching paste is allowed to chemically etch the back electrode layer and the underlying junction layer for a first predetermined dwell time depending on the concentration of the etchant and the thickness of the back electrode and the silicon layer. For the thickness of the back electrode and photovoltaic layers as discussed above, a first dwell time on the order of one to two minutes is usually sufficient.

[0133] Optionally, in order to reduce the required first dwell time, the first chemical etching paste may be heated to a temperature in the range from about 50° C. to about 200° C., and more particularly to a temperature in the range from about 50° C. to about 100° C. One convenient expedient for raising the temperature of the first chemical etching paste is to raise the temperature of the superstrate using a suitable heating apparatus, such as a hot plate.

[0134] At the expiration of the first dwell time the superstrate is sprayed with high pressure water or aqueous alkaline in order to wash off the first etching paste.

[0135] It should be noted that a first etching paste that is basic in nature may be used if the back electrode is fabricated from aluminum or from a dual layer material of aluminum and zinc oxide.

[0136] FIG. **5** shows a stylized perspective view of the array after removal of the first etching paste. The first etching paste is operative to remove from each cell **40**A, **40**B selected portions of the back electrode **28**A, **28**B and the photovoltaic junction layer **22**A, **22**B lying within the first predetermined pattern (FIG. **2**A). Because the first etching paste is operative only against the back electrode and the junction layers lying within the first predetermined paste pattern, the front electrode **16**A, **16**B is exposed but left intact. The scribed break **18** between adjacent front electrode strips **16**A, **16**B is also exposed.

[0137] Since in this discussion it is assumed that the material forming the front electrode is etchant-resistant, an intermediate material conversion step is necessary to render the region of the front electrode on which it is disposed susceptible to an etchant. A suitable conversion material is zinc powder.

[0138] Once the conversion material is applied, a second etching material is dispensed in a second predetermined pattern over the now-converted surface zinc oxide surface of the front electrode.

[0139] FIG. **6**A shows the second predetermined etching paste pattern as including a first stripe **82** of the second etching paste that extends transversely across the first solar cell **40**A in a direction substantially perpendicular to the major axis **41**A of the first cell. The first stripe **82** of the second etching paste is intersected by a plurality of a relatively shorter stripes **84** extends generally parallel to the major axes of adjacent cells.

[0140] The second predetermined etching paste pattern excludes an area adjacent to the parent solar cell and an area adjacent to the bypass diode that define the outlines conductive tabs **90**A, **94**A projecting from the front electrode of the parent solar cell **40**A and the bypass diode **44**A. These tabs **90**A, **94**A are electrically connected to semiconducting material of the first type in the solar cell **40**A and to the semiconducting material of the first type in the bypass diode **44**A. The tabs provide a convenient structure whereby a bypass diode can be interconnected to one (or more) of the cells in the array. As shown, similar tabs are provided for the other cells and the bypass diodes separated therefrom.

[0141] The second etching paste pattern may further include first and/or second edge isolation stripe(s) **58'**, **60'** if they are included in the first etching paste pattern.

[0142] A suitable second etching paste comprises a second acidic etchant and a binder. The second acidic etchant contains only an etchant for the front electrode. An example of the second acidic etchant for zinc oxide is hydrochloric acid. The second etching paste is dispensed over a portion of the exposed front electrode in the second predetermined pattern using any suitable dispensing techniques such as those described in the application of the first etching paste. The binder in the second etching paste is the same as that in the first etching paste.

[0143] The second etching paste is allowed to chemically etch the front electrode layer for a second predetermined dwell time on the order of one to two minutes depending on the concentration of the etchant and the thickness of the front electrode. Optionally, in order to reduce the required second dwell time, the second chemical etching paste may be heated to a temperature in the range from about 50° C. to about 200° C., and more particularly to a temperature in the range from about 50° C. to about 100° C. Again one convenient expedient for raising the temperature of the second etching paste is to raise the temperature of the superstrate using a suitable heating apparatus, such as a hot plate.

[0144] At the expiration of the second dwell time the superstrate is sprayed with high pressure water or aqueous alkaline in order to wash off the second etching paste.

[0145] The second etching paste may alternatively be basic in nature.

[0146] Thus, as shown in FIG. **6**B, as a result of the etching action each silicon solar cell stripe is separated into two parts: viz., a major active cell (e.g., parent solar cells **40**A, **40**B) with the conductive tab (e.g. **90**A, **90**B) and respective totally separated bypass diodes (e.g., diodes **44**A, **44**B). Each totally separated bypass diode has a respective conductive tab (e.g. **94**A, **94**B), (FIG. **6**B).

[0147] Specifically, the bypass diode **44**A includes a portion **16'**A of a front electrode layer (segregated from the front electrode layer **16**A of the parent cell **40**A), a portion **22'**A of a photovoltaic junction layer (segregated from the photovoltaic junction layer **22**A of the parent cell **40**A), and a portion **28'**A of the back electrode (segregated from the back electrode **28**A of the parent cell **40**A). It is stated for clarity that the primed reference characters indicate that the primed elements of the bypass diode were previously integral with the corresponding elements of the solar cell but are now totally separated therefrom. The segregated portion of the junction layer **22'**A is supported by the front electrode **16'**A.

[0148] The interface **36'**A defined within the diode **44**A between the front electrode **16'**A and the one of the semiconducting strata of the segregated junction layer **22'**A is substantially coplanar with the corresponding interface **36**A defined in the parent cell **40**A. Similarly, the interface **38'**A defined within the diode **44**A between the back electrode **28'**A and the other semiconducting strata of the segregated junction layer **22'**A is substantially coplanar with the corresponding interface **38**A in the parent cell **40**A.

[0149] Structurally, the junction layer **22'**A of the bypass diode **44**A is spaced a predetermined distance **45** in the direction of the major axis **41**A from the junction layer **22**A of the first cell **40**A. This predetermined distance **45** is governed by the dimension of the stripe **52** of the first etching paste. Similarly, the lateral spacing between the adjacent bypass diodes **44**A, **44**B is governed by the dimension of the etching paste stripe **54**. The dimensions of the stripes **52**, and **54** are selected such that the surface area of the bypass diode **44**A is within the range from about 1% to about 5% of the surface area of the first solar cell **40**A.

[0150] It is noted that if edge isolation etching paste stripe (s) **58** and/or **60** are deployed the action of the first and the second etching paste would remove the back electrode, the junction layers, and the front electrode in those regions, thus obviating the need for the removal of material in the region **16**R as discussed in connection with the first embodiment.

[0151] The semiconducting material of the first type of the separated portion of the junction layer **22'**A of the diode **44**A is connected with the semiconducting material of the second type of the parent solar cell **40**A through the tab **94**A of the front electrode of bypass diode **44**A and the back electrode of the parent cell **40**A by a conductor **96**A. The semiconducting material of a first type of the solar cell **40**A is connected with the semiconducting material of the second type of the bypass diode (**44**A) through the tab **90**A of front electrode of parent cell **40**A and the back electrode of bypass diode **44**A by a conductor **98**A. In FIG. **6**B the conductors **96**A, **98**A (and **96**B, **98**B) are implemented using metal wire. The equivalent

electrical schematic of the interconnection of the diode **44**A with the first solar cell **40**A is shown in FIG. **6**C.

[0152] Each of the other bypass diodes segregated from a cell in the array may be interconnected with the corresponding parent cell in a manner analogous to that described hereinabove.

[0153] Since the bypass diode is completely separated from its parent cell it is not necessary that the diode so formed be connected electrically across its parent. That is to say, a diode produced from any selected parent cell may be connected in parallel with and in opposition to any cell (or cells) in the array.

[0154] For example, as shown in FIGS. **6**D, **6**E the diode **44**A, totally separated from its parent cell **40**A, may be connected to the chosen cell **40**B. To effect this connection the tab **94**A projecting from the front electrode **16**'A of the diode **44**A may be connected via the conductor **96**A to the back electrode **28**B of the chosen cell **40**B. The tab **90**B projecting from the front electrode **16**B of the cell **40**B is connected via the conductor **98**A to the back electrode **28**'A of the diode **44**A. FIG. **6**E is the schematic diagram of this connection.

[0155] The conducting lines **96**A, **98**A (**96**B, **98**B, etc.) may be alternatively implemented by a metallization dispensed on by screen, nozzle, or ink-jet printing techniques, or by a flexible circuit.

[0156] It should also be understood that the bypass diodes are photodiodes, and as such, generate current. But since the area of the bypass diode used in the invention is so small compared to the active solar cells (<5%; for example, about 1%), the diodes won't influence the performance of the active solar cells.

[0157] The bypass diodes can also be optionally sheltered from illumination with an additional processing step that produces the opaque layer **64** on the exterior surface **12**E of the superstrate **12** (FIG. **6**B).

[0158] The array of thin film solar cells and bypass diode(s) formed as described may be finished into a photovoltaic panel by attaching a bus bar with solder and heat sealing with resin and fluoropolymer films, covering with an encapsulant adhesive **67** (such as EVA ethylene vinyl acetate copolymer) and a second exterior support layer **68** (broken away for clarity of illustration in FIG. **6**B).

[0159] As alluded to earlier, a bypass diode **44**A may be connected in parallel with an opposition more than one cell in the array. FIGS. **6**F and **6**G illustrate a situation in which a diode **44**A is connected to provide a bypass function for one chosen cell, e.g., the parent cell **40**A, and any other chosen cell, e.g., the cell **40**B. In FIG. **6**F the one chosen cell **40**A and the other chosen cell **40**B are adjacent. (It is again noted that the parent cell of the diode **44**A needs not be selected as the one chosen cell.) The connection is effected through a conductor **96**A extending between the tab **94**A and the back electrode **28**A of the one chosen cell and the conductor **98**A between the back electrode **28**'A of the diode **44**A and the tab **40**B of the other chosen cell **40**B.

[0160] FIGS. **6**H and **6**I illustrate an arrangement in which a single diode **44**A is connected across cells **40**A, **40**B, **40**C. In this situation the one chosen cell (the cell **40**A) and the other chosen cell (in this case, the cell **40**C) are not adjacent.

[0161] Instead of using a second etching paste, it should be appreciated that once the front electrode has been exposed by the action of the first (acidic or basic) etching paste, the front electrode may be removed using a laser.

[0162] -o-0-o-

[0163] The implementation of the second embodiment utilized when the front electrode is fabricated from an etchant-susceptible material is next discussed in connection with FIGS. **7**A and **7**B. A suitable etchant-susceptible material useful for the front electrode is selected from the group consisting of: indium-tin oxide (ITO), zinc oxide (ZnO), gallium oxide (GaO) and tin oxide.

[0164] In this instance an etching paste operative against all of the layers of the laminate is dispensed in the desired pattern (e.g, the pattern as shown in FIG. **7**A in which the diode to be formed overlies the second scribe **26** and the third scribe **32**). A suitable etching material for this purpose may be either acidic or basic in nature (if the front electrode is zinc oxide and the back electrode is either aluminum or a dual layer aluminum-zinc oxide).

[0165] As illustrated in FIG. **7**B the etching material removes all the material from the laminate and forms a bypass diode having two lobes **44**A-**1**, **44**A-**2**. The lobes **44**A-**1**, **44**A-**2** share the same front electrode.

[0166] The front electrode **16**'A of the bypass diode is connected from the lobe **44**A-**2** via the conductor **96**A to the back electrode **28**A of the solar cell **40**A. The back electrode **28**'A of the lobe **44**A-**1** of the bypass diode is connected via the conductor **98**A to the front electrode **16**A of the cell **40**A (through the back electrode **28**B of the cell **40**B. As in the case of other connections, metal wires, flexible circuits or a metallization may be used to implement the conductors **96**A, **98**A.

[0167] It should be appreciated that any of the etching steps outlined above in connection with second embodiment may be alternatively implemented using the "inverse" techniques discussed earlier in connection with the first embodiment. In these cases a masking paste may be applied in an inverse pattern which leaves the unmasked areas uncovered. After the masking paste is dried, the unmasked areas are exposed to a wet etchant. The unmasked areas may be exposed by applying the wet etchant directly thereto or by immersing the entire cell array into the wet etchant. The masking paste is then stripped away. In this alternative method the pattern of the mask is the invert of the "positive" pattern created when using etchant paste. The masking paste mentioned earlier may be used.

[0168] -o-0-o-

[0169] It should be apparent from the foregoing that in accordance with either embodiment of the present invention it is possible to utilize a small amount of silicon thin-film solar cells (preferably along the end area), all solar cells in the panel are protected by the bypass diodes.

[0170] Those skilled in the art, having the benefit of the teachings of the present invention may impart modifications thereto. Such modifications are to be construed as lying within the contemplation of the present invention, as defined by the appended claims.

What is claimed is:

1. An array of thin-film solar cells having a cell level integrated bypass diode, the array comprising:

a support layer;

an array of solar cells connected in electrical series supported on the support layer, the array including at least a first, a second and a third solar cell, each solar cell having a major axis extending therethrough,

each solar cell being formed as a laminated structure comprising:

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

a bypass diode supported on the support layer, the bypass diode being formed through total separation from a selected parent solar cell, the bypass diode including:

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

a first electrical conductor connecting the semiconducting material of the first type of the bypass diode with the semiconducting material of the second type of a chosen solar cell in the array; and

a second electrical conductor connecting the semiconducting material of the second type of the bypass diode with the semiconducting material of the first type of the chosen solar cell in the array,

whereby, the bypass diode is connected in parallel and in opposition to the one chosen solar cell.

2. The thin-film solar cell array of claim **1** wherein

the one chosen solar cell is the selected parent solar cell.

3. The thin-film solar cell array of claim **1** wherein

the one chosen solar cell is a solar cell different from the selected parent solar cell.

4. The thin-film solar cell array of claim **3** wherein

the selected parent solar cell and the one chosen solar cell are adjacent to each other.

5. The thin-film solar cell array of claim **3** wherein

the parent solar cell and the one chosen solar cell are separated from each other by at least another solar cell.

6. The thin-film solar cell array of claim **1** wherein:

the front electrodes of the parent solar cell, of the one chosen solar cell and of the bypass diode are fabricated from an etchant resistant material; and wherein

a first conductive tab projects from the front electrode of the bypass diode;

a second conductive tab projects from the front electrode of the one chosen solar cell;

the semiconducting material of the first type of the bypass diode is connected using the first conductive tab; and wherein,

the semiconducting material of the first type of the one chosen solar cell is connected using the second conductive tab.

7. The thin-film solar cell array of claim **6** wherein,

in the selected parent cell,

the semiconducting material of the first type and the front electrode define a first interface, and

the semiconducting material of the second type and the back electrode define a second interface; and wherein

in the bypass diode,

the semiconducting material of the first type and the front electrode of the bypass diode define a first interface,

the semiconducting material of the second type and the back electrode of the bypass diode define a second interface, wherein

the first and second interfaces defined within the bypass diode are substantially coplanar with the respective first and second interfaces defined in the selected parent solar cell.

8. The thin-film solar cell array of claim **7** wherein

the bypass diode is spaced from the selected parent solar cell in a direction substantially parallel to the major axis of the parent solar cell.

9. The thin-film solar cell array of claim **6** wherein

the bypass diode is spaced from the selected parent solar cell in a direction substantially parallel to the major axis of the parent solar cell.

10. The thin-film solar cell array of claim **1** wherein,

in the selected parent cell,

the semiconducting material of the first type and the front electrode define a first interface, and

the semiconducting material of the second type and the back electrode define a second interface; and wherein

in the bypass diode,

the semiconducting material of the first type and the front electrode of the bypass diode define a first interface,

the semiconducting material of the second type and the back electrode of the bypass diode define a second interface, wherein

the first and second interfaces defined within the bypass diode are substantially coplanar with the respective first and second interfaces defined in the selected parent solar cell.

11. The thin-film solar cell array of claim **1** wherein

the bypass diode is spaced from the selected parent solar cell in a direction substantially parallel to the major axis of the parent solar cell.

12. The thin-film solar cell array of claim **7** wherein

the one chosen solar cell is the selected parent solar cell.

13. The thin-film solar cell array of claim **7** wherein

the one chosen solar cell is a solar cell different from the selected parent solar cell.

14. The thin-film solar cell array of claim **13** wherein

the selected parent solar cell and the one chosen solar cell are adjacent to each other.

15. The thin-film solar cell array of claim **13** wherein

the parent solar cell and the one chosen solar cell are separated from each other by at least another solar cell.

16. The thin-film solar cell array of claim **9** wherein

the one chosen solar cell is the selected parent solar cell.

17. The thin-film solar cell array of claim **9** wherein

the one chosen solar cell is a solar cell different from the selected parent solar cell.

18. The thin-film solar cell array of claim **17** wherein

the selected parent solar cell and the one chosen solar cell are adjacent to each other.

19. The thin-film solar cell array of claim **17** wherein

the parent solar cell and the one chosen solar cell are separated from each other by at least another solar cell.

20. The thin-film solar cell array of claim **7** further comprising:

a protective layer disposed over the bypass diode to shelter the same from illumination.

21. The thin-film solar cell array of claim **9** further comprising:

a protective layer disposed over the bypass diode to shelter the same from illumination.

22. The thin-film solar cell array of claim **10** further comprising:

a protective layer disposed over the bypass diode to shelter the same from illumination.

23. The thin-film solar cell array of claim **11** further comprising:

a protective layer disposed over the bypass diode to shelter the same from illumination.

24. The thin-film solar cell array of claim **1** further comprising:

a protective layer disposed over the bypass diode to shelter the same from illumination.

25. The thin-film solar cell array of claim **1** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

26. The thin-film solar cell array of claim **9** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

27. The thin-film solar cell array of claim **10** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

28. The thin-film solar cell array of claim **11** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

29. The thin-film solar cell array of claim **1** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

30. The thin-film solar cell array of claim **1** wherein

the first and second conductors are wires.

31. The thin-film solar cell array of claim **1** wherein

the first and second conductors are flex circuits.

32. The thin-film solar cell array of claim **1** wherein

the first and second conductors are metallizations.

33. A thin-film solar cell array having a cell level integrated bypass diode, the cell comprising:

a support layer;

an array of solar cells connected in electrical series supported on the support layer, the array including at least a first, a second and a third solar cell, each solar cell being formed as a laminated structure comprising:

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

the semiconducting material of the first type of and the front electrode define a first interface, and

the semiconducting material of the second type and the back electrode define a second interface; and

a bypass diode supported on the support layer, the bypass diode being formed through total separation from the selected parent solar cell, the bypass diode including

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

a first interface being defined between the semiconducting material of the first type and the front electrode of the bypass diode, and

a second interface being defined between the semiconducting material of the second type and the back electrode;

the first and second interfaces defined within the bypass diode are substantially coplanar with the respective first and second interfaces defined in the selected parent solar cell;

a first electrical conductor connecting the semiconducting material of the first type of the photovoltaic junction layer of the bypass diode with the semiconducting material of the second type of a chosen solar cell in the array; and

a second electrical conductor connecting the semiconducting material of the second type of the photovoltaic junction layer of the bypass diode with the semiconducting material of the first type of the chosen solar cell in the array,

whereby, the bypass diode is connected in parallel and in opposition to the one chosen solar cell.

34. The thin-film solar cell array of claim **33** wherein:

the front electrodes of the parent solar cell, of the one chosen solar cell and of the bypass diode are fabricated from an etchant resistant material; and wherein

a first conductive tab projects from the front electrode of the bypass diode;

a second conductive tab projects from the front electrode of the one chosen solar cell;

the semiconducting material of the first type of the bypass diode is connected using the first conductive tab; and wherein,

the semiconducting material of the first type of the one chosen solar cell is connected using the second conductive tab.

35. The thin-film solar cell array of claim **34** wherein

the one chosen solar cell is the selected parent solar cell.

36. The thin-film solar cell array of claim **34** wherein

the one chosen solar cell is a solar cell different from the selected parent solar cell.

37. The thin-film solar cell array of claim **36** wherein

the selected parent solar cell and the one chosen solar cell are adjacent to each other.

38. The thin-film solar cell array of claim **36** wherein

the parent solar cell and the one chosen solar cell are separated from each other by at least another solar cell.

39. The thin-film solar cell array of claim **34** further comprising:

a protective layer disposed over the bypass diode to shelter the same from illumination.

40. The thin-film solar cell array of claim **34** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

41. The thin-film solar cell array of claim **33** further comprising:

a protective layer disposed over the bypass diode to shelter the same from illumination.

42. The thin-film solar cell array of claim **33** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

43. The thin-film solar cell array of claim **33** wherein

the first and second conductors are wires.

44. The thin-film solar cell array of claim **33** wherein

the first and second conductors are flex circuits.

45. The thin-film solar cell array of claim **33** wherein

the first and second conductors are metallizations.

46. A thin-film solar cell array having a cell level integrated bypass diode, the cell comprising:

a support layer;

an array of solar cells connected in electrical series supported on the support layer, the array including at least a first, a second and a third solar cell, each solar cell having a major axis extending therethrough, each solar cell being formed as a laminated structure comprising:

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

a bypass diode supported on the support layer, the bypass diode being formed through total separation from the selected parent solar cell, the bypass diode including

the bypass diode being spaced a predetermined distance from the parent solar cell in a direction substantially parallel to the major axis of the parent solar cell;

a first electrical conductor connecting the semiconducting material of the first type of the photovoltaic junction layer of the bypass diode with the semiconducting material of the second type of a chosen solar cell in the array; and

a second electrical conductor connecting the semiconducting material of the second type of the photovoltaic junction layer of the bypass diode with the semiconducting material of the first type of the chosen solar cell in the array,

whereby, the bypass diode is connected in parallel and in opposition to the one chosen solar cell.

47. The thin-film solar cell array of claim **46** wherein:

the front electrodes of the parent solar cell, of the one chosen solar cell and of the bypass diode are fabricated from an etchant resistant material; and wherein

a first conductive tab projects from the front electrode of the bypass diode;

a second conductive tab projects from the front electrode of the one chosen solar cell;

the semiconducting material of the first type of the bypass diode is connected using the first conductive tab; and wherein,

the semiconducting material of the first type of the one chosen solar cell is connected using the second conductive tab.

48. The thin-film solar cell array of claim **47** wherein

the one chosen solar cell is the selected parent solar cell.

49. The thin-film solar cell array of claim **47** wherein

the one chosen solar cell is a solar cell different from the selected parent solar cell.

50. The thin-film solar cell array of claim **49** wherein

the selected parent solar cell and the one chosen solar cell are adjacent to each other.

51. The thin-film solar cell array of claim **49** wherein

the parent solar cell and the one chosen solar cell are separated from each other by at least another solar cell.

52. The thin-film solar cell array of claim **47** further comprising:

a protective layer disposed over the bypass diode to shelter the same from illumination.

53. The thin-film solar cell array of claim **46** further comprising:

a protective layer disposed over the bypass diode to shelter the same from illumination.

54. The thin-film solar cell array of claim **46** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

55. The thin-film solar cell array of claim **46** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

56. The thin-film solar cell array of claim **46** wherein

the first and second conductors are wires.

57. The thin-film solar cell array of claim **46** wherein

the first and second conductors are flex circuits.

58. The thin-film solar cell array of claim **46** wherein

the first and second conductors are metallizations.

59. A photovoltaic panel comprising:

a) a transparent support layer;

b) an array of solar cells connected in electrical series supported on the support layer, the array including at least a first, a second and a third solar cell, each solar cell having a major axis extending therethrough,

each solar cell being formed as a laminated structure comprising:

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

a bypass diode supported on the support layer, the bypass diode being formed through total separation from a

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

a first electrical conductor connecting the semiconducting material of the first type of the bypass diode with the semiconducting material of the second type of a chosen solar cell in the array; and

a second electrical conductor connecting the semiconducting material of the second type of the bypass diode with the semiconducting material of the first type of the chosen solar cell in the array,

whereby, the bypass diode is connected in parallel and in opposition to the one chosen solar cell; and

c) a backing support layer disposed over the thin-film solar cell array.

60. The photovoltaic panel of claim **59** wherein:

the front electrodes of the parent solar cell, of the one chosen solar cell and of the bypass diode are fabricated from an etchant resistant material; and wherein

a first conductive tab projects from the front electrode of the bypass diode;

a second conductive tab projects from the front electrode of the one chosen solar cell;

the semiconducting material of the first type of the bypass diode is connected using the first conductive tab; and wherein,

the semiconducting material of the first type of the one chosen solar cell is connected using the second conductive tab.

61. The photovoltaic panel of claim **60** wherein,

in the selected parent cell,

the semiconducting material of the first type and the front electrode define a first interface, and

the semiconducting material of the second type and the back electrode define a second interface; and wherein

in the bypass diode,

the semiconducting material of the first type and the front electrode of the bypass diode define a first interface,

the semiconducting material of the second type and the back electrode of the bypass diode define a second interface, wherein

the first and second interfaces defined within the bypass diode are substantially coplanar with the respective first and second interfaces defined in the selected parent solar cell.

62. The photovoltaic panel of claim **60** wherein,

the bypass diode is spaced from the selected parent solar cell in a direction substantially parallel to the axis of the parent solar cell.

63. The photovoltaic panel of claim **61** further comprising:

a protective layer disposed on the first support layer over the bypass diode to shelter the same from illumination.

64. The photovoltaic panel of claim **62** further comprising:

a protective layer disposed on the first support layer over the bypass diode to shelter the same from illumination.

65. The thin-film solar cell array of claim **61** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

66. The thin-film solar cell array of claim **62** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

67. The thin-film solar cell array of claim **59** wherein

the first and second conductors are wires.

68. The thin-film solar cell array of claim **59** wherein

the first and second conductors are flex circuits.

69. The thin-film solar cell array of claim **59** wherein

the first and second conductors are metallizations.

70. A photovoltaic panel comprising:

a) a transparent support layer;

b) an array of solar cells connected in electrical series supported on the support layer, the array including at least a first, a second and a third solar cell, each solar cell being formed as a laminated structure comprising:

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

the semiconducting material of the first type of and the front electrode define a first interface, and

the semiconducting material of the second type and the back electrode define a second interface; and

a bypass diode supported on the support layer, the bypass diode being formed through total separation from the selected parent solar cell, the bypass diode including

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

a first interface being defined between the semiconducting material of the first type and the front electrode of the bypass diode, and

a second interface being defined between the semiconducting material of the second type and the back electrode;

the first and second interfaces defined within the bypass diode are substantially coplanar with the respective first and second interfaces defined in the selected parent solar cell;

a first electrical conductor connecting the semiconducting material of the first type of the photovoltaic junction layer of the bypass diode with the semiconducting material of the second type of a chosen solar cell in the array; and

a second electrical conductor connecting the semiconducting material of the second type of the photovoltaic junction layer of the bypass diode with the semiconducting material of the first type of the chosen solar cell in the array,

whereby, the bypass diode is connected in parallel and in opposition to the one chosen solar cell; and

c) a backing support layer disposed over the thin-film solar cell array.

71. The photovoltaic panel of claim **70** wherein:

the front electrodes of the parent solar cell, of the one chosen solar cell and of the bypass diode are fabricated from an etchant resistant material; and wherein

a first conductive tab projects from the front electrode of the bypass diode;

a second conductive tab projects from the front electrode of the one chosen solar cell;

the semiconducting material of the first type of the bypass diode is connected using the first conductive tab; and wherein,

the semiconducting material of the first type of the one chosen solar cell is connected using the second conductive tab.

72. The photovoltaic panel of claim **71** further comprising:

a protective layer disposed on the first support layer over the bypass diode to shelter the same from illumination.

73. The thin-film solar cell array of claim **71** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

74. The photovoltaic panel of claim **70** further comprising:

a protective layer disposed on the first support layer over the bypass diode to shelter the same from illumination.

75. The thin-film solar cell array of claim **70** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

76. The thin-film solar cell array of claim **70** wherein

the first and second conductors are wires.

77. The thin-film solar cell array of claim **70** wherein

the first and second conductors are flex circuits.

78. The thin-film solar cell array of claim **70** wherein

the first and second conductors are metallizations.

79. A photovoltaic panel comprising:

a) a transparent support layer;

b) an array of solar cells connected in electrical series supported on the support layer, the array including at least a first, a second and a third solar cell, each solar cell having a major axis extending therethrough, each solar cell being formed as a laminated structure comprising:

a photovoltaic junction layer including a semiconducting material of a first type and a semiconducting material of a second type,

a front electrode disposed in electrical contact with one of the semiconducting materials, and

a back electrode disposed in electrical contact with the second one of the semiconducting materials;

a bypass diode supported on the support layer, the bypass diode being formed through total separation from the selected parent solar cell, the bypass diode including

each layer of the bypass diode being spaced a predetermined distance from the corresponding layer of the parent solar cell in a direction parallel to the major axis of the parent solar cell;

a first electrical conductor connecting the semiconducting material of the first type of the photovoltaic junction layer of the bypass diode with the semiconducting material of the second type of a chosen solar cell in the array; and

a second electrical conductor connecting the semiconducting material of the second type of the photovoltaic junction layer of the bypass diode with the semiconducting material of the first type of the chosen solar cell in the array,

whereby, the bypass diode is connected in parallel and in opposition to the one chosen solar cell; and

c) a backing support layer disposed over the thin-film solar cell array.

80. The thin-film solar cell array of claim **79** wherein:

the front electrodes of the parent solar cell, of the one chosen solar cell and of the bypass diode are fabricated from an etchant resistant material; and wherein

a first conductive tab projects from the front electrode of the bypass diode,

a second conductive tab projects from the front electrode of the one chosen solar cell;

the semiconducting material of the first type of the bypass diode is connected using the first conductive tab; and wherein,

the semiconducting material of the first type of the one chosen solar cell is connected using the second conductive tab.

81. The photovoltaic panel of claim **80** further comprising:

a protective layer disposed on the first support layer over the bypass diode to shelter the same from illumination.

82. The thin-film solar cell array of claim **80** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

83. The photovoltaic panel of claim **79** further comprising:

a protective layer disposed on the first support layer over the bypass diode to shelter the same from illumination.

84. The thin-film solar cell array of claim **79** wherein

the bypass diode and the parent solar cell each have a predetermined planar surface area, and wherein

the surface area of the bypass diode is within the range from about 1% to about 5% of the surface area of the parent solar cell.

85. The thin-film solar cell array of claim **79** wherein

the first and second conductors are wires.

86. The thin-film solar cell array of claim **79** wherein

the first and second conductors are flex circuits.

87. The thin-film solar cell array of claim **79** wherein

the first and second conductors are metallizations.

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