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(54) Title: HIGH SPEED, EFFICIENT SIC POWER MODULE

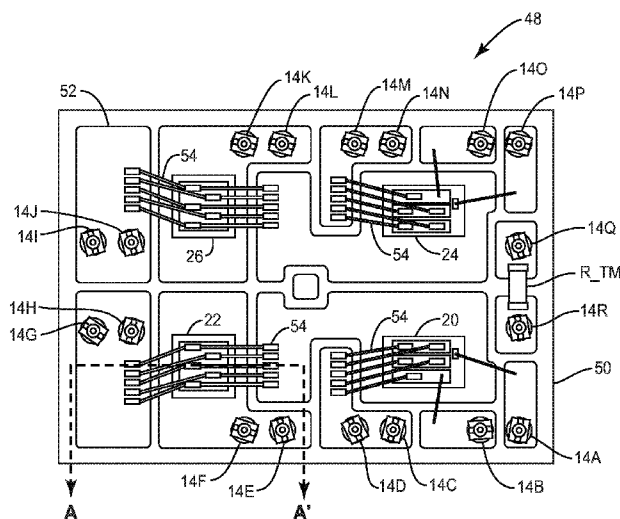


FIG. 7

(57) Abstract: A power converter module includes an active metal braze (AMB) substrate, power converter circuitry, and a housing. The AMB substrate includes an aluminum nitride base layer, a first conductive layer on a first surface of the aluminum nitride base layer, and a second conductive layer on a second surface of the aluminum nitride base layer opposite the first surface. The power converter circuitry includes a number of silicon carbide switching components coupled to one another via the first conductive layer. The housing is over the power converter circuitry and the AMB substrate. By using an AMB substrate with an aluminum nitride base layer, the thermal dissipation characteristics of the power converter module may be substantially improved while maintaining the structural integrity of the power converter module.



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***HIGH SPEED, EFFICIENT SIC POWER MODULE***Field of the Disclosure

**[0001]** The present disclosure relates to power converter modules, and specifically to high-frequency power converter modules utilizing silicon carbide (SiC) components.

Background

**[0002]** Power converter modules (which, as referred to herein may also include power inverter modules) are standalone devices that may perform a variety of functions within a power converter system. For example, power converter modules may include boost converters, buck converters, half-bridge converters, and full-bridge converters. Conventional power converter modules generally include power converter circuitry utilizing silicon (Si) switching components. While effective in many applications, using power converter circuitry with silicon (Si) switching components generally limits the switching frequency at which the power converter circuitry can operate. The lower the switching frequency of the components in the power converter circuitry, the larger the filtering components such as inductors and capacitors utilized in a power converter system need to be. Accordingly, filtering components used along with power converter circuitry using silicon (Si) switching components must be quite large, thereby driving up the cost of the power converter system. Further, at high switching frequency, silicon (Si) switching components are often associated with relatively low efficiency and low power density.

Summary

**[0003]** The present disclosure relates to power converter modules, and specifically to high-frequency power converter modules utilizing silicon carbide (SiC) components. In one embodiment, a power converter module includes an active metal braze (AMB) substrate, power converter circuitry, and a housing. The AMB substrate includes an aluminum nitride base layer, a first conductive

layer on a first surface of the aluminum nitride base layer, and a second conductive layer on a second surface of the aluminum nitride base layer opposite the first surface. The power converter circuitry includes a number of silicon carbide switching components coupled to one another via the first conductive layer. The housing is over the power converter circuitry and the AMB substrate. By using an AMB substrate with an aluminum nitride base layer, the thermal dissipation characteristics of the power converter module may be substantially improved while maintaining the structural integrity of the power converter module.

**[0004]** In one embodiment, the first conductive layer is directly on the first surface of the aluminum nitride base layer and the second conductive layer is directly on the second surface of the aluminum nitride base layer.

**[0005]** In one embodiment, the first conductive layer is etched to form a desired connection pattern between the silicon carbide switching components. The silicon carbide switching components may be coupled to the first conductive layer via one or more wirebonds such that the power switching path has a maximum length of about 50 mm and the gate control path has a maximum length of about 20 mm. By minimizing the power switching path length and gate control path length, the stray inductance in the power converter module is reduced.

**[0006]** In one embodiment, the power converter circuitry is a boost converter configured to receive a direct current (DC) input voltage and provide a stepped-up DC output voltage. The power converter circuitry may include a silicon carbide metal-oxide-semiconductor field-effect transistor (MOSFET) coupled in series with a silicon carbide Schottky diode. Further, the power converter circuitry may be configured to provide an output voltage greater than 650V, an output power greater than 900W, and operate at a switching frequency greater than 40kHz. The switching losses of the power converter circuitry may be between 5 mJ/A and 100 mJ/A. The insulating base layer may have a minimum thermal conductivity of 30 W/m-K in order to provide low thermal resistance between the power converter circuitry and the second conductive layer.

**[0007]** In one embodiment, the power converter circuitry is one of a buck converter, a half-bridge converter, a full-bridge converter, a single-phase inverter, a three-phase inverter, and multilevel topologies like neutral point clamped (NPC) and transistor-type neutral point clamped (TNPC).

5 **[0008]** In one embodiment, a method for manufacturing a power converter module comprises providing an active metal braze (AMB) substrate, providing power converter circuitry, and providing a housing. The AMB substrate includes an aluminum nitride base layer, a first conductive layer on a first surface of the aluminum nitride base layer, and a second conductive layer on a second surface  
10 of the aluminum nitride base layer opposite the first surface. The power converter circuitry includes a number of silicon carbide switching components coupled to one another via the first conductive layer. The housing is provided over the power converter circuitry and the AMB substrate. By using an AMB substrate with an aluminum nitride base layer, the thermal dissipation  
15 characteristics of the power converter module may be substantially improved while maintaining the structural integrity of the power converter module.

**[0009]** Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the  
20 accompanying drawing figures.

#### Brief Description of the Drawing Figures

**[0010]** The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with  
25 the description serve to explain the principles of the disclosure.

**[0011]** Figure 1 is an isometric view of a power converter module according to one embodiment of the present disclosure.

**[0012]** Figure 2 is a side view of a power converter module according to one embodiment of the present disclosure.

30 **[0013]** Figure 3 is a schematic of power converter circuitry in a power converter module according to one embodiment of the present disclosure.

**[0014]** Figure 4 is a schematic of a boost converter including power converter circuitry shown according to one embodiment of the present disclosure.

**[0015]** Figure 5 is a schematic of a boost converter including power converter circuitry according to an additional embodiment of the present disclosure.

5 **[0016]** Figure 6 is a schematic of a boost converter including power converter circuitry according to an additional embodiment of the present disclosure.

**[0017]** Figure 7 is a top view of power converter circuitry according to one embodiment of the present disclosure.

**[0018]** Figure 8 is a cross-sectional view of a substrate and the power  
10 converter circuitry shown in Figure 3 according to one embodiment of the present disclosure.

#### Detailed Description

**[0019]** The embodiments set forth below represent the necessary information  
15 to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that  
20 these concepts and applications fall within the scope of the disclosure and the accompanying claims.

**[0020]** It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from  
25 another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

**[0021]** It will be understood that when an element such as a layer, region, or  
30 substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements

may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

**[0022]** Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

**[0023]** The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

**[0024]** Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further

understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

5   **[0025]**   In light of the above, there is a need for power converter circuitry with improved performance. Specifically, there is a need for power converter circuitry capable of efficiently operating at high switching frequencies and high power densities.

10   **[0026]**   Figures 1 and 2 show an isometric view and a side view, respectively, of a power converter module 10 according to one embodiment of the present disclosure. The power converter module 10 includes a housing 12, a number of input/output (I/O) pins 14, and a number of mounting holes 16. The housing 12 may be formed of a plastic material and have a footprint of approximately 31mm x 66mm x 16mm such that the power converter module 10 is compatible with  
15   existing power converter systems that accept power converter modules of this size. Notably, the principles of the present disclosure may be applied to housings of any material type and size. The I/O pins 14 are coupled to various points in power converter circuitry (not shown) contained within the housing 12, as discussed in detail below.

20   **[0027]**   Figure 3 is a schematic showing details of power converter circuitry 18 within the housing 12 of the power converter module 10 according to one embodiment of the present disclosure. The power converter circuitry 18 is divided into two parts (referred to herein as “channels”), and includes a first metal-oxide-semiconductor field-effect transistor (MOSFET) 20 coupled in series  
25   with a first diode 22 and a second MOSFET 24 coupled in series with a second diode 26. Specifically, the first MOSFET 20 includes a gate contact (G), a source contact (S), and a drain contact (D). The gate contact (G) of the first MOSFET 20 is coupled to a first one of the I/O pins 14A. The source contact (S) of the first MOSFET 20 is coupled to a second, a third, and a fourth one of the I/O pins 14B, 14C, and 14D. A cathode of the first diode 22 is coupled to a fifth and a sixth one  
30   of the I/O pins 14E and 14F. The drain contact (D) of the first MOSFET 20 is

coupled to a ninth and a tenth one of the I/O pins 14G and 14H and to the anode of the first diode 22.

**[0028]** Similarly, the second MOSFET 24 includes a gate contact (G), a source contact (S), and a drain contact (D). The drain contact (D) of the second MOSFET 24 is coupled to an eleventh and a twelfth one of the I/O pins 14I and 14J and to the anode of the second diode 26. The cathode of the second diode 26 is coupled to a thirteenth and a fourteenth one of the I/O pins 14K and 14L.

The source contact (S) of the second MOSFET 24 is coupled to a fifteenth, a sixteenth, and a seventeenth one of the I/O pins 14M, 14N, 14O. The gate contact (G) of the second MOSFET 24 is coupled to an eighteenth one of the I/O pins 14P. A temperature measurement resistor R<sub>TM</sub> is coupled between a nineteenth and a twentieth one of the I/O pins 14Q and 14R.

**[0029]** The first MOSFET 20 and the first diode 22 (i.e., a first channel), along with one or more external components, form first boost converter circuitry, while the second MOSFET 24 and the second diode 26 (i.e., a second channel), along with one or more external components, form second boost converter circuitry.

Because the separate boost converter circuitry operates in the same manner, the principles of operation thereof will now be discussed as they relate to the first boost converter circuitry. In operation, a direct current (DC) voltage is placed across the source contact (S) and the drain contact (D) of the first MOSFET 20. In some embodiments, the DC voltage delivered to the drain contact (D) of the first MOSFET 20 may be provided via a boost inductor (not shown). Further, a switching control signal is provided to the gate contact (G) of the first MOSFET 20, generally by gate driver circuitry (not shown). The resulting voltage across the cathode of the first diode 22 and the source contact (S) of the first MOSFET 20 is a stepped-up DC output voltage. Accordingly, the first boost converter circuitry and the second boost converter circuitry may be used to appropriately scale high-power DC voltages, which may be especially useful in applications such as solar power systems.

**[0030]** Notably, the first MOSFET 20 and the second MOSFET 24 each include a gate return terminal (I/O pin 14B and I/O pin 14O, respectively) coupled

to the source contact (S) thereof. Notably, these gate return terminals are located as close to the first MOSFET 20 and the second MOSFET 24, respectively, as possible, such that a parasitic inductance between the gate return terminal and the source contact (S) is minimized. Generally, this increases the achievable turn-on and turn-off speed of the first MOSFET 20 and the second MOSFET 24, thereby improving the performance of the power converter circuitry 18 by reducing switching losses.

**[0031]** Any of the first MOSFET 20, the first diode 22, the second MOSFET 24, and the second diode 26 are silicon carbide devices, which may be referred to as switching devices. As discussed herein, switching devices are devices capable of selectively delivering power to a load. In one embodiment, the first diode 22 and the second diode 26 are Schottky diodes. Accordingly, the performance of the power converter module 10 may be significantly improved. Specifically, because silicon carbide devices are majority carrier devices, they do not suffer from reductions in switching speed due to recombination of minority carriers that produce tail or reverse recovery currents. In one embodiment, recovery currents in conventional silicon PiN diodes are on the order of ~7000nC, while recovery currents in the power converter circuitry 18 are less than ~120nC (> 16x reduction). Accordingly, silicon carbide devices can be operated at much higher speeds than conventional silicon devices, which provides several performance benefits for the power converter module 10 discussed below. The first boost converter circuit and the second boost converter circuit may be referred to as “channels.” Each one of these channels may provide an output voltage between 650V and 1200V, an output current from 10A to 50A (e.g., 10A, 20A, 30A, 40A, and 50A), and an output power between 900W and 30kW. Further, each one of these channels may provide an efficiency between about 96% and 99.5%, and switching losses less than or equal to about 300W when operated at switching speeds greater than 40kHz.

**[0032]** In addition to the performance benefits afforded by utilizing silicon carbide devices in the power converter module 10, using silicon carbide devices also provides cost savings. Specifically, the size of filtering components such as

inductors and capacitors used in a power converter system in which the power converter module 10 is incorporated is inversely proportional to the switching frequency of the power converter module. Further, the size of filtering components is proportional to the cost thereof. Accordingly, by using silicon carbide switching components that may be operated at high frequencies such as those above 40kHz, the size of filtering components in a power system can be drastically reduced, thereby saving cost.

**[0033]** While the power converter circuitry 18 shown in Figure 3 is shown as a two-channel boost converter, the present disclosure is not so limited. The principles of the present disclosure may be applied to power converter circuitry 18 including a buck converter, a half-bridge converter, a full-bridge converter, a single-phase inverter, a three-phase inverter, or the like.

**[0034]** Figure 4 shows boost converter circuitry 28 including a first channel of the power converter circuitry 18. The boost converter circuitry 28 includes the first MOSFET 20 and the first diode 22, a boost inductor 30, an output capacitor 32, and a voltage source 34. The boost inductor 30 is coupled between a positive output of the voltage source 34 and the drain contact (D) of the first MOSFET 20. A negative output of the voltage source 34 is coupled to the source contact (S) of the first MOSFET 20. The first diode 22 is coupled between the drain contact (D) of the first MOSFET 20 and a first load output 36 of the boost converter circuitry 28. A second load output 38 is coupled to the source contact (S) of the first MOSFET 20. The output capacitor 32 is coupled between the first load output 36 and the second load output 38.

**[0035]** In operation, a positive voltage from the voltage source 34 is delivered to the boost inductor 30, where energy can be stored as a magnetic field. A switching control signal is delivered to the gate contact (G) of the first MOSFET 20 in order to repeatedly switch the first MOSFET 20 between an off-state and an on-state. In the off-state of the first MOSFET 20, a positive potential across the first diode 22 due to a charge on the boost inductor 30 allows current from the boost inductor ( $I_{\text{BOOST}}$ ) to flow to the first load output 36 and charge the output capacitor 32. While not shown, a load will be coupled between the first

load output 36 and the second load output 38 to complete the circuit. In the on-state of the first MOSFET 20, the anode of the first diode 22 is shorted to ground, and a charge on the output capacitor 32 causes the first diode 22 to remain in a blocking mode of operation. Energy stored in the output capacitor 32 causes a current to continue to flow into the load (not shown).

**[0036]** Notably, the speed at which the first MOSFET 20 is able to transition between the off-state and the on-state determines many operational characteristics of the boost converter circuitry 28. Faster switching speeds allow the boost converter circuitry 28 to operate in a continuous conduction mode in which the current supplied by the boost inductor 30 in a single switching period is reduced. Generally, silicon devices cannot achieve speeds sufficient to operate in a continuous conduction mode, and instead must operate in a discontinuous conduction mode. The reduced current supply requirements afforded by switching the first MOSFET 20 at high speeds results in a reduced requirement for energy storage by the boost inductor 30, and reduced electromagnetic interference (EMI), which eases the design of electromagnetic filtering circuitry associated with the boost converter circuitry 28. Accordingly, the inductance of the boost converter can be reduced without affecting the performance of the boost converter circuitry 28. Generally, the inductance value of an inductor is proportional to the size thereof. Accordingly, the size of the boost inductor 30 can be reduced as well. Further, the inductance value and size of an inductor is proportional to the cost thereof. As the boost inductor 30 may be among the most expensive parts of the boost converter circuitry 28, it may be highly beneficial to utilize the high switching speed of the first MOSFET 20 in order to reduce these costs. In one embodiment, the inductance value of the boost inductor 30 may be less than 450  $\mu\text{H}$  due to the switching speeds achievable by the first MOSFET 20 as discussed herein. For example, the inductance of the boost inductor 30 may be between 25  $\mu\text{H}$  and 150  $\mu\text{H}$ , may be between 150  $\mu\text{H}$  and 300  $\mu\text{H}$ , and may be between 300  $\mu\text{H}$  and 450  $\mu\text{H}$ . Further, the total volume of the boost inductor 30 may be less than 7 cubic inches (e.g., between 1 cubic inch and 3 cubic inches, between 3 cubic inches and 5 cubic inches, and

between 5 cubic inches and 7 cubic inches) and the total weight of the boost inductor 30 may be less than 1 pound (e.g., between 0.1 pounds and 0.3 pounds, between 0.3 pounds and 0.6 pounds, and between 0.6 pounds and 0.9 pounds) in some embodiments.

5 **[0037]** Figure 5 shows the boost converter circuitry 28 according to an alternative embodiment of the present disclosure. The boost converter circuitry 28 shown in Figure 5 is substantially similar to that shown in Figure 4, except that the boost converter circuitry 28 shown in Figure 5 includes an inner-loop capacitor 40 coupled between the first load output 36 and the second load output  
10 38 (in parallel with the output capacitor 32). Notably, the inner-loop capacitor 40 is within the power converter circuitry 18 itself. Specifically, the inner-loop capacitor 40 closes the loop between the cathode of the first diode 22 and the source contact (S) of the first MOSFET 20 in as short a length as possible. This improves performance of the power converter circuitry 18 by reducing parasitic  
15 inductances and thus reducing ringing and other performance-reducing phenomena. In the embodiment shown in Figure 5, the inner-loop capacitor 40 may be a high-frequency capacitor such as a ceramic capacitor, while the output capacitor 32 may be a relatively low-frequency capacitor such as an electrolytic capacitor or polymer film capacitor. However, the output capacitor 32 and the  
20 inner-loop capacitor 40 may be any type of capacitor without departing from the principles described herein.

**[0038]** Figure 6 shows the boost converter circuitry 28 according to an additional embodiment of the present disclosure. The boost converter circuitry shown in Figure 6 is substantially similar to that shown in Figure 4, except that  
25 the boost converter circuitry 28 shown in Figure 6 includes snubber circuitry 42 coupled between the first load output 36 and the second load output 38. The snubber circuitry 42 includes a snubber capacitor 44 and a snubber resistor 46 coupled in series between the first load output 36 and the second load output 38. As discussed above, the snubber capacitor 44 and the snubber resistor 46 may  
30 be within the power converter circuitry 18 in order to reduce the length of the snubber loop between the cathode of the first diode 22 and the source contact

(S) of the first MOSFET 20. The snubber circuitry 42 effectively reduces transient signals, occurring at the cathode of the first diode 22. Specifically, ringing occurring due to swings in the current provided at the cathode of the first diode 22 may be significantly reduced by the snubber circuitry 42. Reducing this  
5 ringing prevents output overshoots and undershoots, thus increasing the reliability and performance of the boost converter circuitry 28 primarily by lowering radiated and conducted EMI.

**[0039]** Figure 7 shows a top view of a substrate 48 within the housing 12 according to one embodiment of the present disclosure. Notably, the substrate  
10 48 may be an active metal braze (AMB) substrate including an insulating aluminum nitride base layer 50 and a first conductive layer 52 on a first surface of the aluminum nitride base layer 50. As discussed herein, an active metal braze (AMB) substrate is a substrate in which conductive layers applied to a base layer have been brazed in a high temperature vacuum brazing process in order to form  
15 a strong bond between the conductive layers and the insulating base layer. In general, AMB substrates are stronger than their conventional counterparts formed from technologies such as direct bond copper (DBC) and the like. Using an AMB substrate provides the necessary strength to the aluminum nitride base layer 50 to make it viable for use in the power converter module 10, which does  
20 not include a baseplate to increase the structural integrity thereof as in conventional designs. Aluminum nitride generally has far superior thermal conduction properties when compared to conventional substrate materials such as aluminum oxide. The increased thermal conductivity afforded by the use of the aluminum nitride base layer 50 allows for the switching components in the  
25 power converter module 10 to operate at lower temperatures, which may translate into higher power levels, higher efficiency, higher reliability, or all three.

**[0040]** In other embodiments, the substrate 48 is an active metal braze (AMB) substrate including an insulating silicon nitride base layer 50 and a first  
30 conductive layer 52 on a first surface of the silicon nitride base layer 50. Silicon nitride may have similar properties to aluminum nitride as discussed above and therefore may increase the performance of the power converter module 10. In

another embodiment, the substrate 48 may be a DBC substrate including an aluminum nitride or silicon nitride base layer, which may allow for similar performance improvements to those discussed above.

**[0041]** The first conductive layer 52 is etched to form a desired pattern on the first surface of the aluminum nitride base layer 50. Wirebonds 54 connect the first MOSFET 20, the first diode 22, the second MOSFET 24, and the second diode 26 to various parts of the first conductive layer 52 in order to connect the various components as described above with respect to Figure 3. The particular pattern of the first conductive layer 52 is chosen in order to minimize the distance from the gate contact (G) of each one of the first MOSFET 20 and the second MOSFET 24 to their respective I/O pins 14, minimize the length of the wirebonds 54, and optimize current flow through the power converter module 10. In one embodiment, the pattern of the first conductive layer 52 and routing of wirebonds 54 are designed such that the power switching path has a maximum length of about 50 mm and the gate control path has a maximum length of about 20 mm. As defined herein, the gate control path is the total distance (as determined by tracing the path) between I/O pin 14O (shown in Figure 3) and I/O pin 14P (also shown in Figure 3). Further as defined herein, the power switching path is the total distance (as determined by tracing the path) between I/O pin 14E and I/O pin 14F to I/O pin 14C and I/O pin 14D (all shown in Figure 3). Minimizing the power switching path length and gate control path length reduces the stray inductance in the power converter module 10, which may be less than 15 nH according to some embodiments. In one embodiment, wirebonds 54 in the gate control path have a diameter of ~5mil, while wirebonds 54 in the power switching path have a diameter ~15mil. More or less wirebonds 54 may be used to form a particular leg of the particular conduction path based on a desired current carrying capacity thereof.

**[0042]** Figure 8 shows a cross-sectional view of the housing 12 and the substrate 48 through line A-A' shown in Figure 7. As shown in Figure 8, the substrate 48 is mounted in the housing 12 and includes the aluminum nitride base layer 50, the first conductive layer 52 on which the first diode 22 is attached

via a die attach material 56 and connected via the wirebonds 54, and a second conductive layer 58. In some embodiments, the space between the substrate 48 and the housing 12 is filled with an inert gel. Notably, as discussed above, the power converter module 10 does not include a baseplate. Accordingly, the

5 substrate 48 must be adequately rugged in order to support the power converter circuitry 18 formed on the first conductive layer 52. Further, as silicon carbide devices are generally high power density devices that produce a significant amount of heat, it is desirable for the substrate 48 to have a relatively low thermal resistance such that the substrate 48 is capable of efficiently dissipating heat.

10 Using an AMB substrate as discussed above provides a strong substrate 48 that is capable of efficiently dissipating heat. In one embodiment, the insulating base layer 50 may have a minimum thermal conductivity of 30 W/m-K in order to provide low thermal resistance between the power converter circuitry 18 and the second conductive layer 58. Accordingly, the power converter circuitry 18 may

15 be operated in order to provide additional power output, additional efficiency, or both.

**[0043]** Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed

20 herein and the claims that follow.

Claims

What is claimed is:

1. A power converter module comprising:
  - 5       • an active metal braze (AMB) substrate comprising an aluminum nitride base layer, a first conductive layer on a first surface of the aluminum nitride base layer, and a second conductive layer on a second surface of the aluminum nitride base layer opposite the first surface;
  - 10       • power converter circuitry on the AMB substrate and comprising a plurality of silicon carbide switching components coupled to one another via the first conductive layer; and
  - a housing including the AMB substrate.
2. The power converter module of claim 1 wherein the first conductive layer  
15 is directly on the first surface of the aluminum nitride base layer and the second conductive layer is directly on the second surface of the aluminum nitride base layer.
3. The power converter module of claim 1 wherein the first conductive layer  
20 is etched to form a desired connection pattern between the plurality of silicon carbide switching components.
4. The power converter module of claim 3 wherein the plurality of silicon  
25 carbide switching components are coupled to the first conductive layer via one or more wirebonds.
5. The power converter module of claim 4 wherein the first conductive layer  
is etched and the one or more wirebonds are routed such that a power switching  
path has a maximum length of about 50 mm and a gate control path has a  
30 maximum length of about 20 mm.

6. The power converter module of claim 1 wherein the power converter circuitry is a boost converter configured to receive a direct current (DC) input voltage and provide a stepped-up DC output voltage.

5 7. The power converter module of claim 6 wherein the power converter circuitry comprises a silicon carbide metal-oxide-semiconductor field-effect transistor (MOSFET) coupled in series with a silicon carbide Schottky diode.

8. The power converter module of claim 6 wherein the power converter  
10 circuitry is configured to provide an output voltage greater than 650V, an output power greater than 900W, and operate at a switching frequency greater than 40kHz.

9. The power converter module of claim 8 wherein the power converter  
15 circuitry has switching losses between 5 mJ/A and 100 mJ/A.

10. The power converter module of claim 8 wherein the AMB substrate has a thermal conductance greater than about 30 W/m-K.

20 11. The power converter module of claim 1 wherein the power converter circuitry is one of a buck converter, a half-bridge converter, a full-bridge converter, a single-phase inverter, and a three-phase inverter.

12. A method for manufacturing a power converter module comprising:  
25

- providing an active metal braze (AMB) substrate comprising an aluminum nitride base layer, a first conductive layer on a first surface of the aluminum nitride base layer, and a second conductive layer on a second surface of the aluminum nitride base layer opposite the first surface;

- providing power converter circuitry on the AMB substrate, the power converter circuitry comprising a plurality of silicon carbide switching components coupled to one another via the first conductive layer; and
- mounting the AMB substrate in a housing.

5

13. The method of claim 12 wherein the first conductive layer is directly on the first surface of the aluminum nitride base layer and the second conductive layer is directly on the second surface of the aluminum nitride base layer.

10

14. The method of claim 12 further comprising etching the first conductive layer to form a desired connection pattern between the plurality of silicon carbide switching components.

15

15. The method of claim 14 further comprising connecting the plurality of silicon carbide switching components to the first conductive layer via one or more wirebonds.

20

16. The method of claim 15 wherein the first conductive layer is etched and the one or more wirebonds are routed such that a power switching path has a maximum length of about 50 mm and a gate control path has a maximum length of about 20 mm.

25

17. The method of claim 12 wherein the power converter circuitry is a boost converter configured to receive a direct current (DC) input voltage and provide a stepped-up DC output voltage.

30

18. The method of claim 17 wherein providing the power converter circuitry comprises providing a silicon carbide metal-oxide-semiconductor field-effect transistor (MOSFET) coupled in series with a silicon carbide Schottky diode.

19. The method of claim 17 wherein the power converter circuitry is configured to provide an output voltage greater than 650V, an output power greater than 900W, and operate at a switching frequency greater than 40kHz.

5 20. The method of claim 19 wherein the power converter circuitry has switching losses between 5 mJ/A and 100 mJ/A.

21. The method of claim 19 wherein the AMB substrate has a thermal conductance greater than about 30 W/m-K.

10

22. The method of claim 12 wherein the power converter circuitry is one of a buck converter, a half-bridge converter, a full-bridge converter, and a three-phase converter.

15 23. A power converter module comprising:

- at least one silicon carbide metal-oxide semiconductor field-effect transistor (MOSFET) including a drain contact, a gate contact, and a source contact;
- at least one diode including an anode coupled to the drain contact of the at least one silicon carbide MOSFET and a cathode; and
- snubber circuitry coupled between the cathode of the at least one diode and the source contact of the at least one silicon carbide MOSFET.

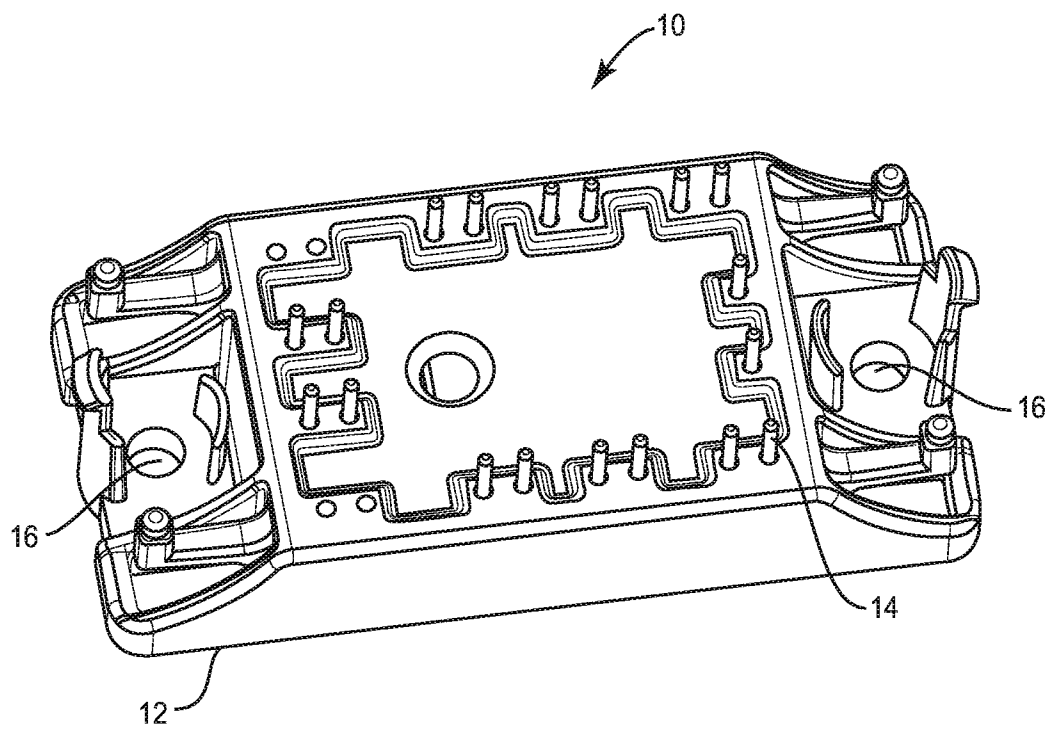
20

25 24. A power converter module comprising:

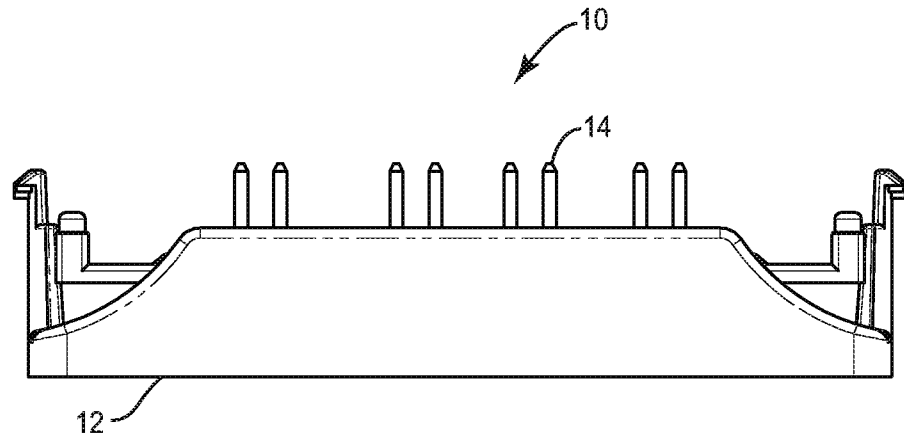
- a power module substrate;
- at least one silicon carbide metal-oxide semiconductor field-effect transistor (MOSFET) provided on the power module substrate and including a drain contact, a gate contact, and a source contact;

- at least one diode provided on the power module substrate and including an anode coupled to the drain contact of the at least one silicon carbide MOSFET and a cathode; and
- an inner-loop capacitor provided on the power module substrate and coupled between the cathode of the at least one diode and the source contact of the at least one silicon carbide MOSFET.

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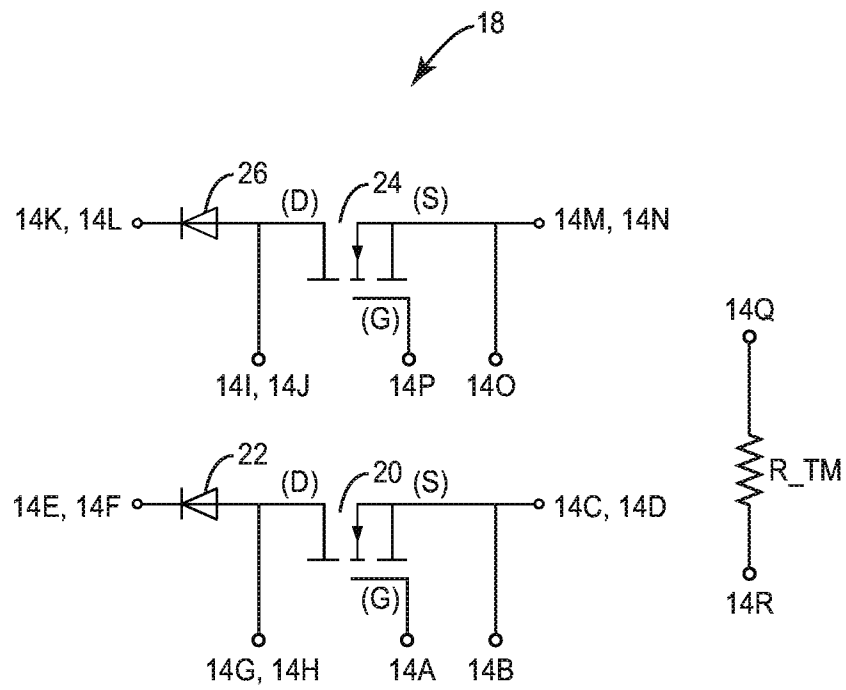


**FIG. 1**



**FIG. 2**

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**FIG. 3**

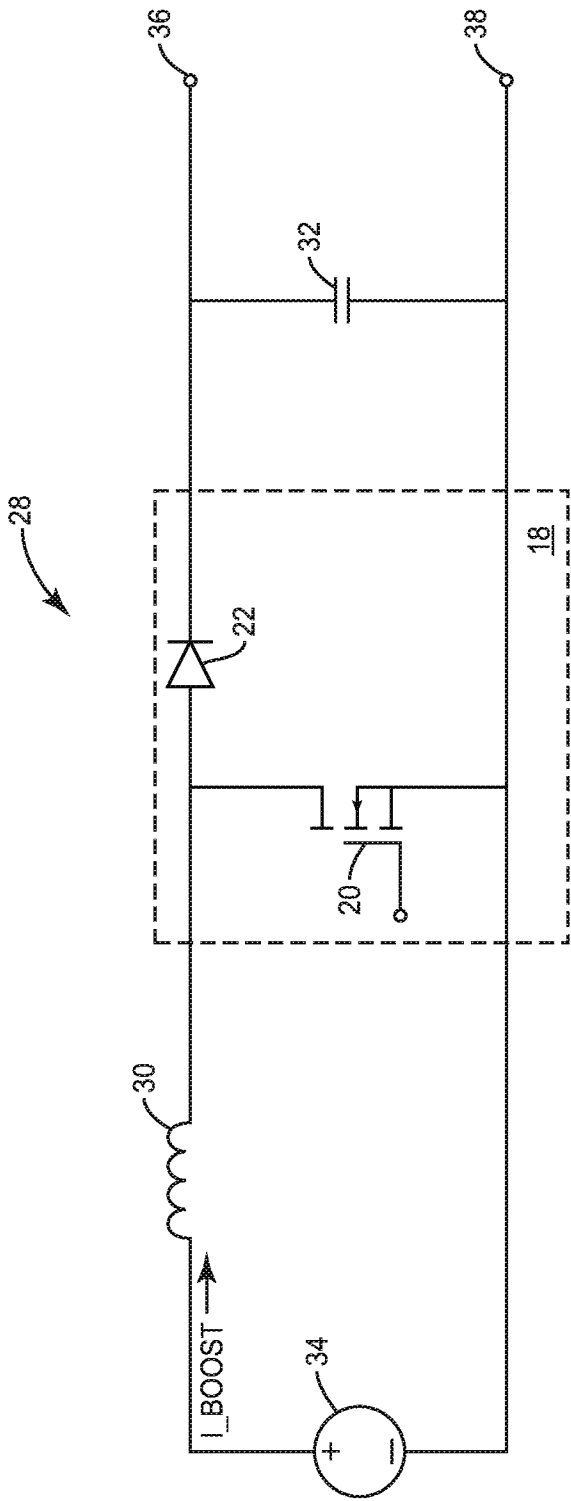


FIG. 4

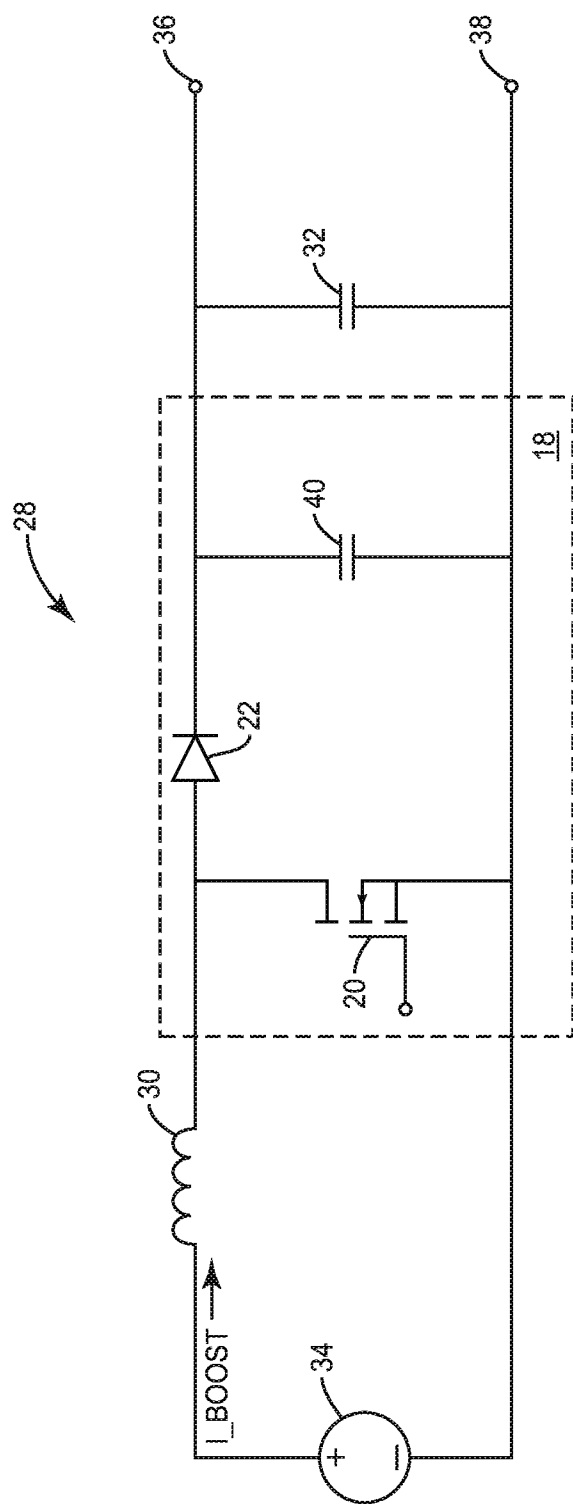


FIG. 5

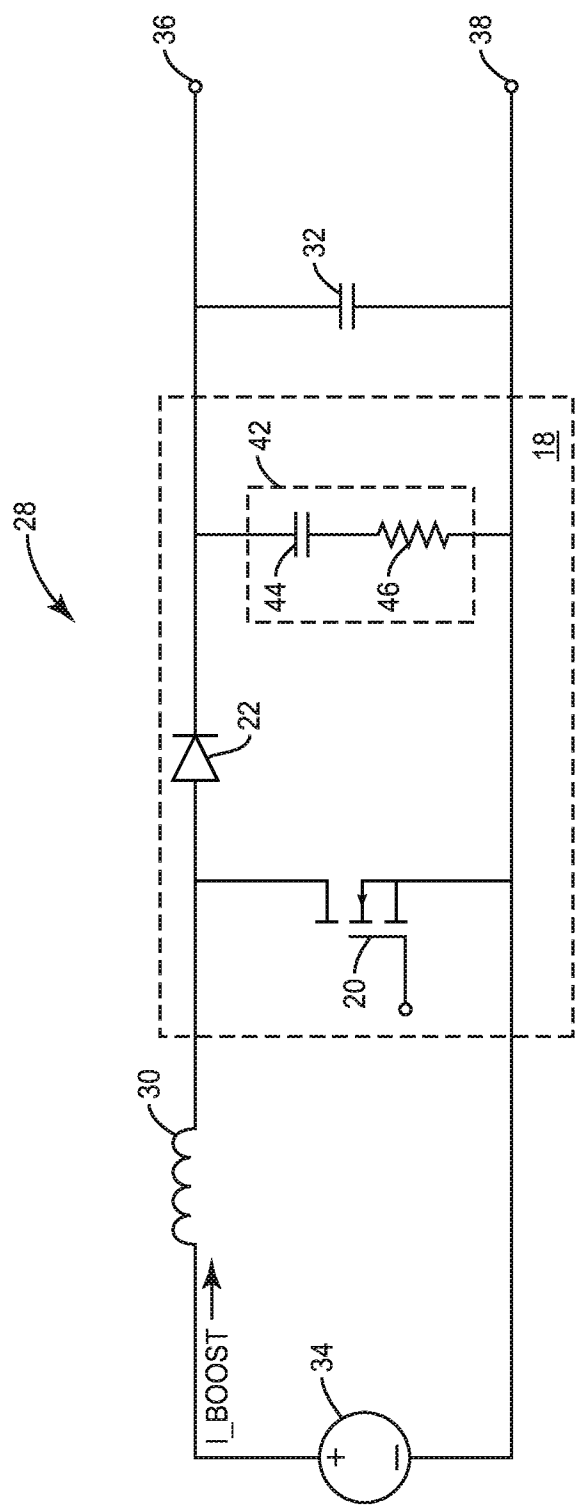


FIG. 6

7/8

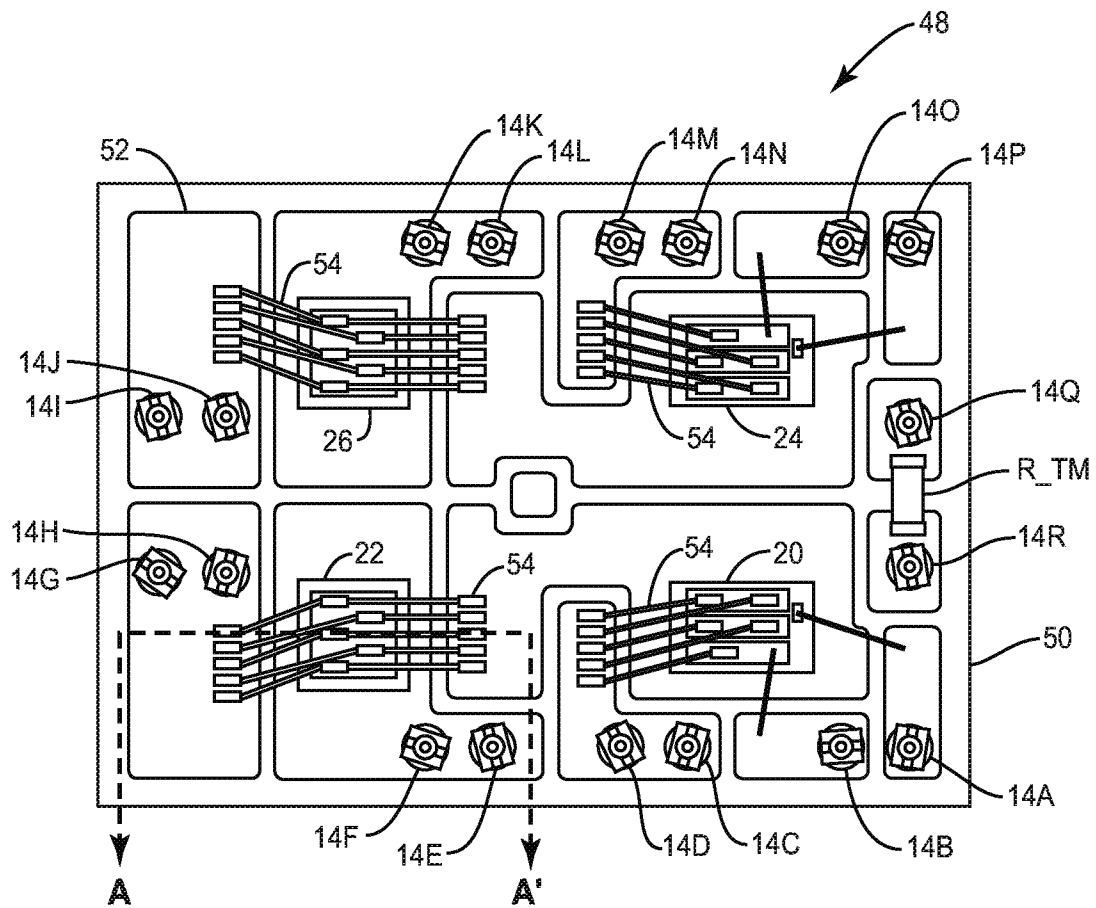


FIG. 7

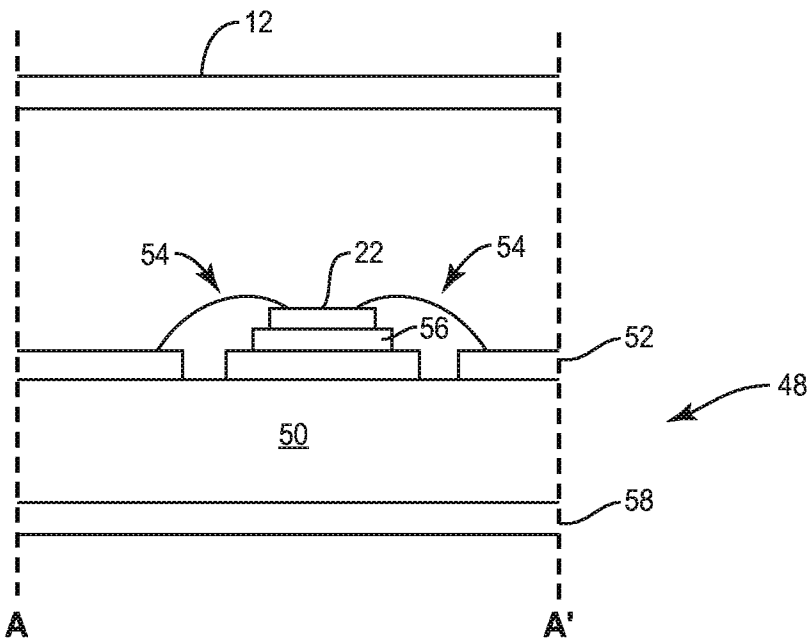


FIG. 8

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US2016/022031

## Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

## Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-22

### Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

## INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2016/022031

## A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L25/07 C04B37/02 H02M3/00 H01L23/373  
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L C04B H02M B60L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                              | Relevant to claim No. |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Y         | WO 2014/186448 A1 (CREE INC [US])<br>20 November 2014 (2014-11-20)<br>paragraphs [0061] - [0067], [0086];<br>figures 7,8,12<br>-----            | 1-22                  |
| Y         | US 2009/283309 A1 (NABA TAKAYUKI [JP] ET<br>AL) 19 November 2009 (2009-11-19)<br>paragraphs [0001], [0017], [0018],<br>[0074] - [0078]<br>----- | 1-22                  |
| A         | WO 2013/171136 A1 (SAGEM DEFENSE SECURITE<br>[FR]) 21 November 2013 (2013-11-21)<br>the whole document<br>-----                                 | 1,12                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

## \* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

8 June 2016

Date of mailing of the international search report

16/08/2016

Name and mailing address of the ISA/

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Authorized officer

Cortes Rosa, João

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2016/022031

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                                                                | Publication<br>date                                                              |
|-------------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|
| WO 2014186448 A1                          | 20-11-2014          | EP 2997596 A1<br>WO 2014186448 A1                                                                         | 23-03-2016<br>20-11-2014                                                         |
| US 2009283309 A1                          | 19-11-2009          | JP 5226511 B2<br>US 2009283309 A1<br>WO 2008004552 A1                                                     | 03-07-2013<br>19-11-2009<br>10-01-2008                                           |
| WO 2013171136 A1                          | 21-11-2013          | CA 2872065 A1<br>CN 104321870 A<br>EP 2850658 A1<br>FR 2990795 A1<br>US 2015077942 A1<br>WO 2013171136 A1 | 21-11-2013<br>28-01-2015<br>25-03-2015<br>22-11-2013<br>19-03-2015<br>21-11-2013 |

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-22

Power converter module with AMB substrate comprising conductive layers on opposite surfaces; SiC switching components coupled to one another via one of the conductive layers; and a housing.

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2. claims: 23, 24

Power converter module with substrate; SiC MOSFET on the substrate with drain, gate and source contacts; a diode on the substrate with anode coupled to drain of MOSFET and with cathode; and snubber circuitry on the substrate coupled between cathode and source contact.

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