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Suzuki et al.

[11] **3,906,256**

[45] **Sept. 16, 1975**

[54] **DRIVE PULSE GENERATOR FOR USE IN ELECTRONIC ANALOG DISPLAY CLOCK APPARATUS**

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Mar. 9, 1974 Japan 49-27546

[52] **U.S. Cl.** ..... **307/225 R**; 58/23 R

[51] **Int. Cl.**[2] **G04C 3/00**

[58] **Field of Search** ..... 307/225 R, 220; 58/23 R, 58/23 A; 331/51

[56] **References Cited**

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Primary Examiner—John Kominski
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow & Garrett

[57] **ABSTRACT**

Disclosed is a circuit for generating in a pulse motor drive coil an initial pulse motor drive pulse in a unit length of time during which a second hand is driven by one step, after resetting for time correction has been released. The output of a divider chain for frequency-dividing a standard frequency signal from a quartz oscillator into a signal having a period equal to the unit length of time is delayed by a delay circuit, and by a logic gate responsive to the output of the delay circuit and the output of the divider chain there is produced an output pulse signal having a period equal to the unit length of time and a narrower width. The output of the logic gate is supplied to a binary counter. An output circuitry responsive to the output of the binary counter and the output of the logic gate generates drive pulses in the drive coil. The reset signal is applied to the delay circuit and at least a frequency divider stage producing the signal the period of which equals the unit length of time.

3 Claims, 9 Drawing Figures

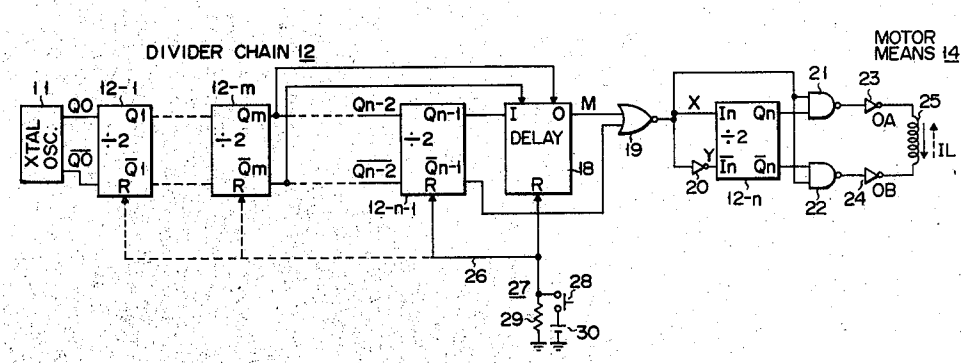


FIG. 1

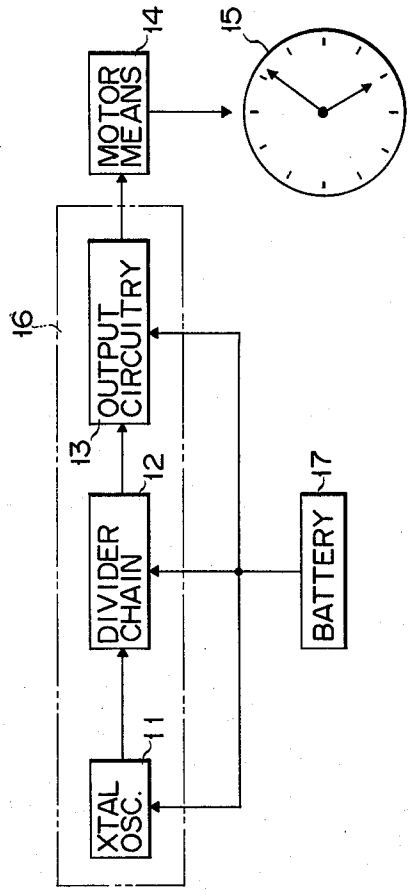

MOTOR MEANS
14
15
OUTPUT CIRCUITRY
16
13
DIVIDER CHAIN
12
BATTERY
17
XTAL OSC.
11

FIG. 2

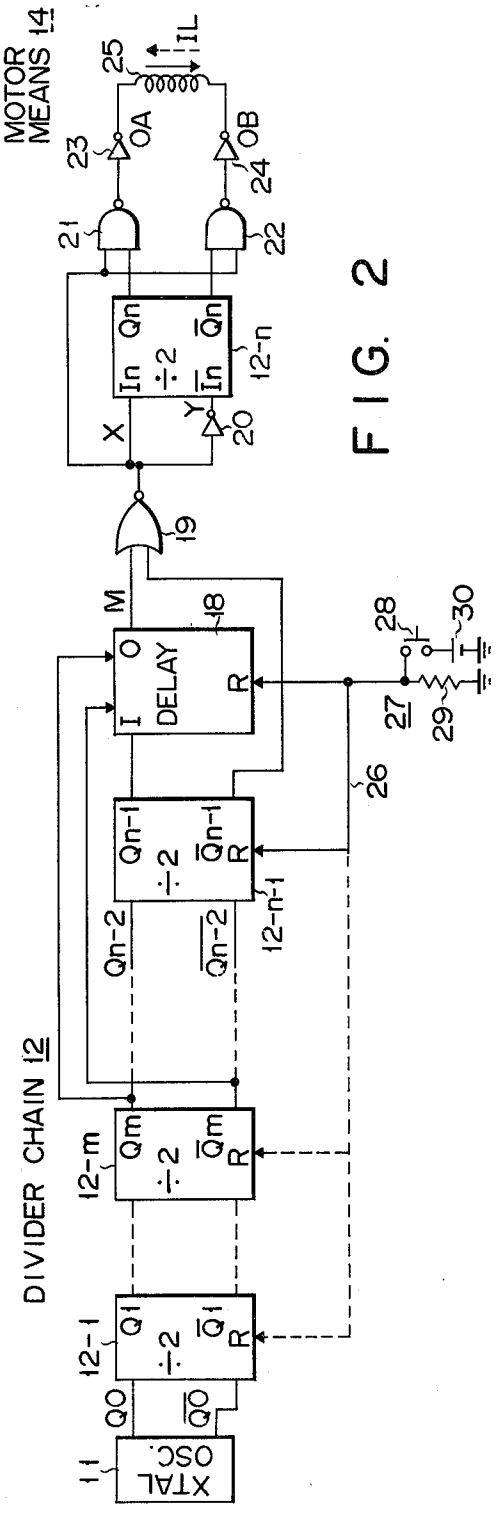

MOTOR MEANS 14
25
IL
23
OA
24
OB
21
22
In
Qn
In
Qn
÷2
12-n
X
Y
20
19
M
18
DELAY
I
O
R
28
30
27
29
26
Qn-1
Qn-1
÷2
R
12-n-1
Qn-2
Qn-2
DIVIDER CHAIN 12
Qm
Qm
12-m
Q1
Q1
12-1
Q0
Q0
XTAL OSC.
11

FIG. 3

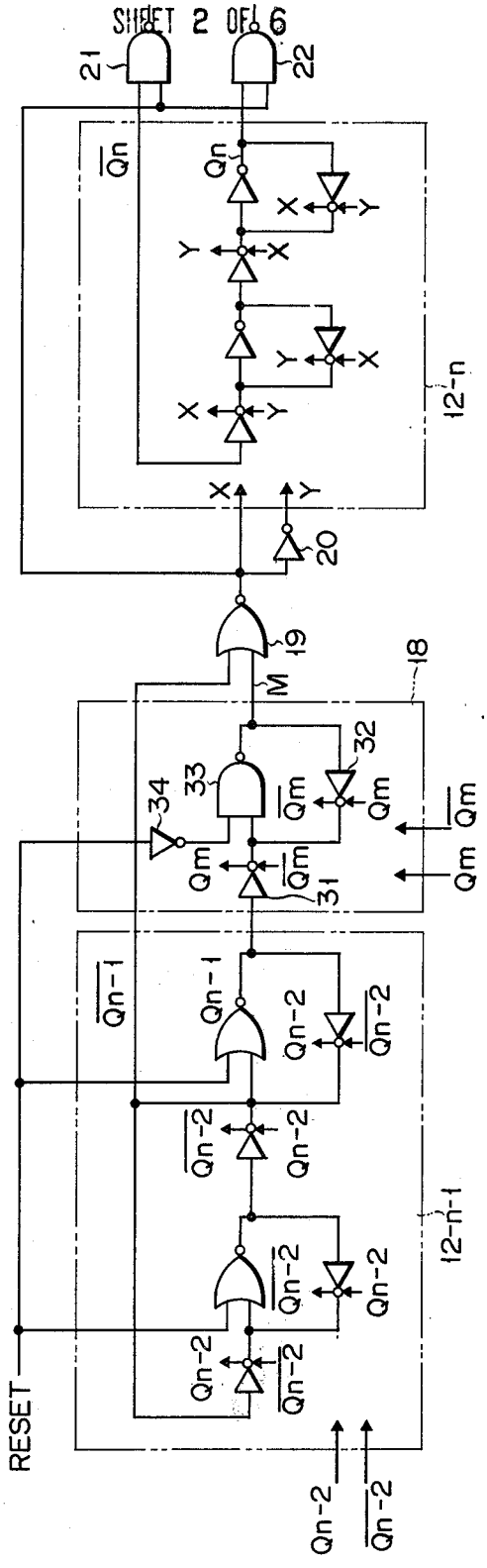


FIG. 4

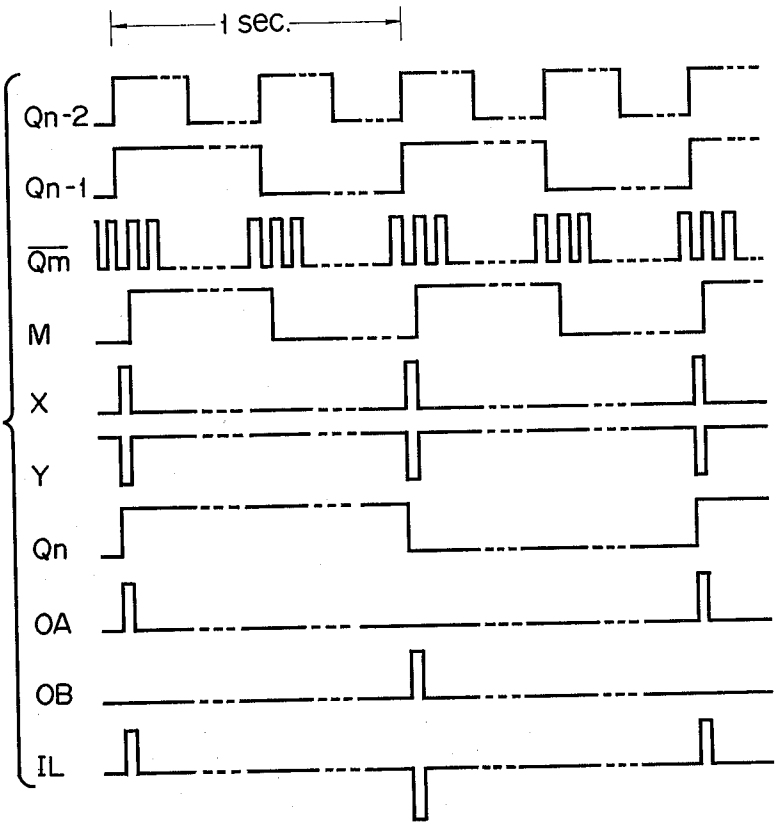


FIG. 5A

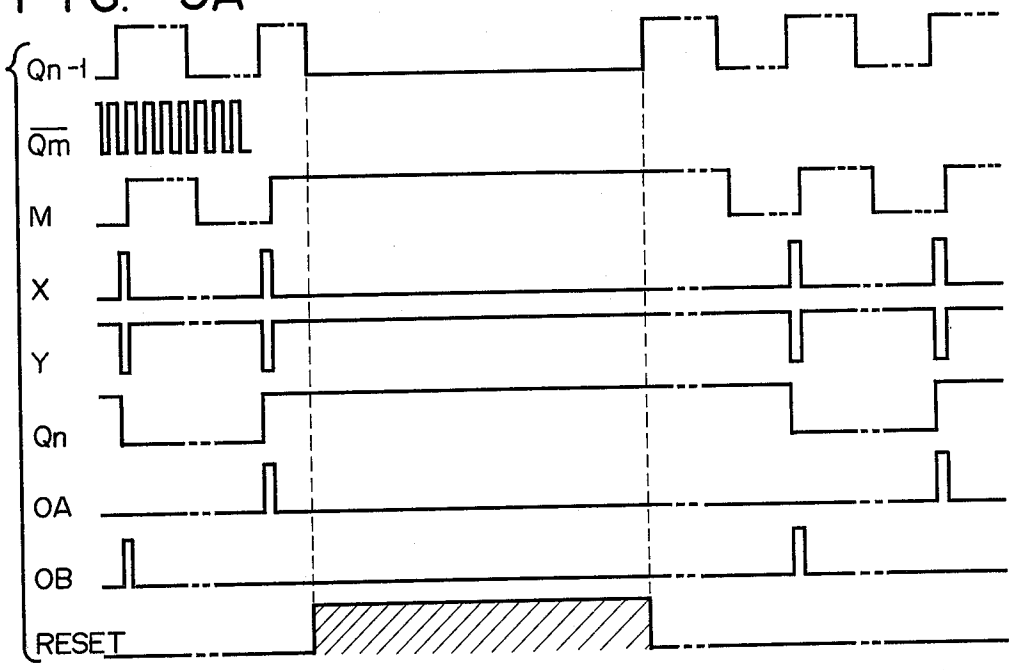


FIG. 5B

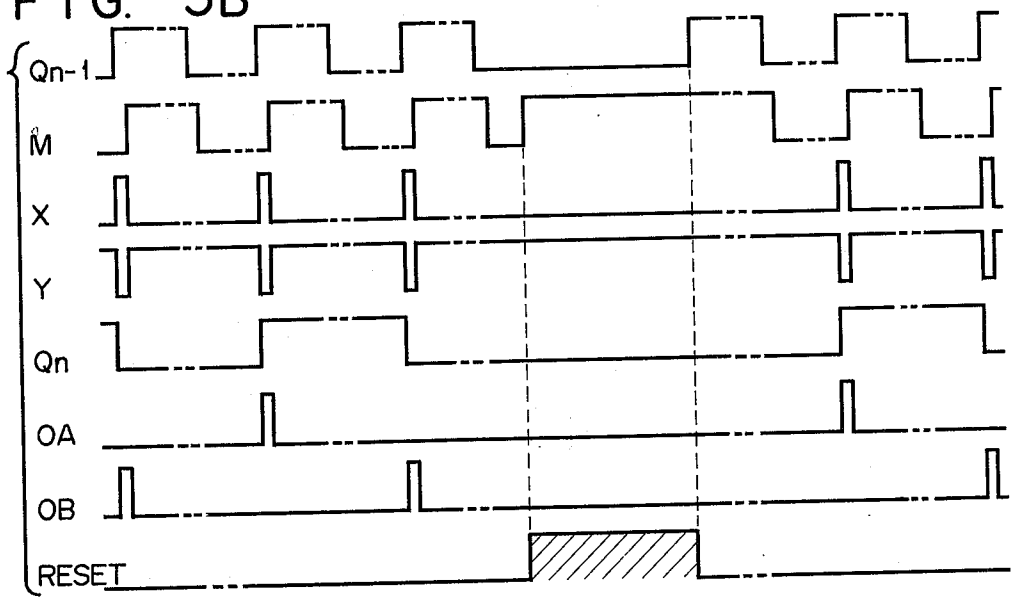
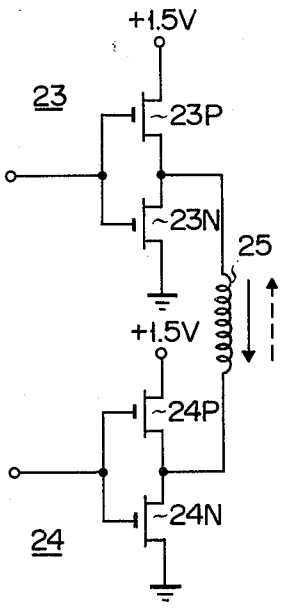


FIG. 6


+1.5V
23
~23P
~23N
25
+1.5V
~24P
~24N
24

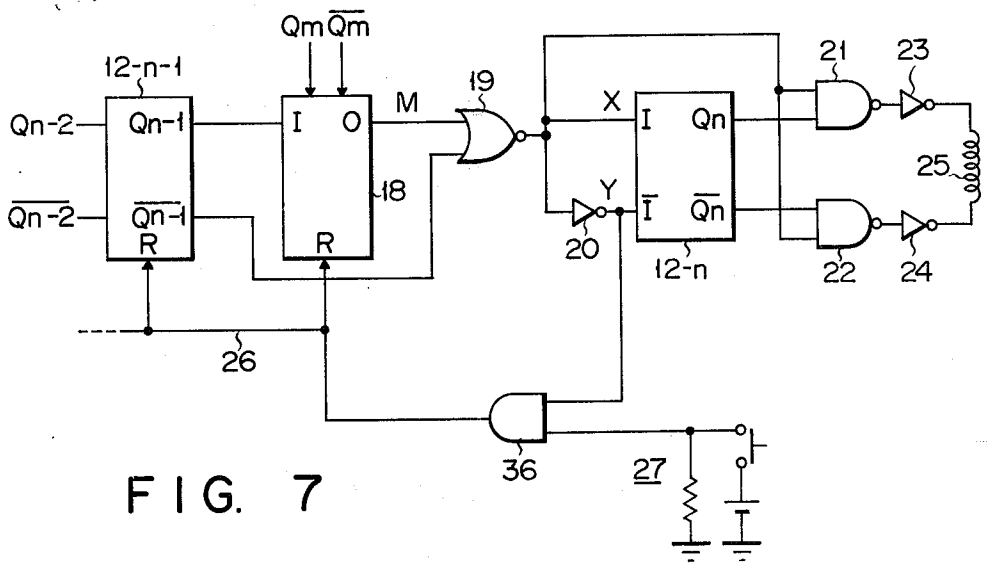
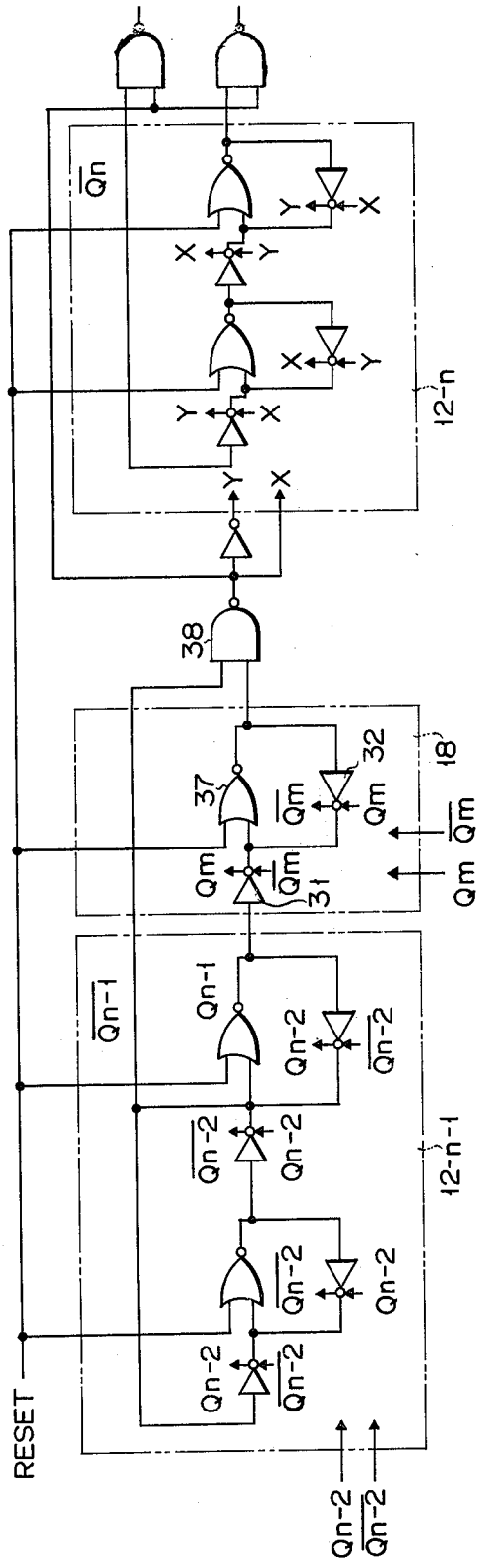

Qm Q̄m
12-n-1
Qn-2
Qn-1
Q̄n-2
Q̄n-1
R
I
O
M
18
R
19
X
Y
20
I
Qn
Ī
Q̄n
12-n
21
23
25
22
24
26
36
27

FIG. 7

FIG. 8


Qn
12-n
38
18
37
32
Qm
Qm
Qm
31
Qm Qm
Qm Qm
Qn-1
Qn-1
Qn-2
Qn-2
Qn-2
Qn-2
Qn-2
Qn-2
Qn-2
Qn-2
12-n-1
RESET
Qn-2
Qn-2

DRIVE PULSE GENERATOR FOR USE IN ELECTRONIC ANALOG DISPLAY CLOCK APPARATUS

This invention relates to a drive pulse generator for use in an electronic analog display clock apparatus, and more particularly to a drive pulse generator suited for time correction.

In the analog display clock apparatus having a quartz oscillator oscillating at a precise frequency, it is required for the purpose of step-advancing a second hand for every unit length of time, e.g., at an interval of 1 second that drive pulse currents are permitted to flow in a drive coil of a pulse motor in opposite directions at an interval of unit length of time. In the drive pulse generator for the conventional electronic analog display clock apparatus, a standard frequency signal of the quartz oscillator is frequency-divided in turn by a frequency divider chain comprised of binary counters cascade-connected in a number of n to produce an output signal having a predetermined period. The output signal of the divider chain is delayed by a delay circuit responsive to the output of the mth binary counter ($m < n$) of the divider chain by a predetermined period (equal to half the output period of the mth stage binary counter). The output of the nth stage counter; the complementary output of the delay circuit, and the complementary output of the nth stage counter; the output of the delay circuit are supplied to a pair of two-input logic gates, respectively. Further, the outputs of the pair of logic gates are supplied to a pair of inverters, respectively. Between the outputs of the pair of inverters is connected a drive coil. Where the output of the mth stage counter has a period of 2 seconds, drive pulse currents flow in the drive coil at an interval of 1 second in mutually opposite directions. The above-mentioned drive pulse generator is disclosed in Japanese magazine "Electronics," Vol. 18, No. 11, p. 1349 (1973).

When, in such a clock apparatus as mentioned above, time correction is performed, generation of a drive pulse is stopped by supplying a reset signal to the delay circuit and at least the nth stage counter. And the second hand is set to the zero portion, and thereafter when precise time information has been given, resetting is released. In this case it is necessary that a drive pulse is generated in a unit length of time, for example, in 1 second after release of resetting.

In case of the foregoing drive pulse generator, however, there is a possibility of a drive pulse being generated immediately after resetting has been released. As previously mentioned, it is required for the purpose of driving the pulse motor that pulse currents flow in the drive coil at an interval of unit length of time in mutually opposite directions. For convenience of explanation, a current pulse flowing in one direction is now referred to as "positive pulse" while a current pulse flowing in the opposite direction as "negative pulse." Where it is assumed that a pulse generated immediately after resetting has been released be a negative pulse, it is determined by the timing of resetting whether the pulse generated prior to resetting was a positive pulse or negative pulse. The negative pulse after release of resetting effected after generation of a negative pulse does not act to drive the pulse motor, whereas the negative pulse after release of resetting effected after generation of a positive pulse acts to drive the pulse motor.

Accordingly, the conventional clock apparatus is so arranged as not to be operated through a lock mechanism by a pulse generated immediately after release of resetting, and therefore becomes complicated in construction and resultantly expensive.

Accordingly, if arrangement is so made than an initial drive pulse is generated in a unit length of time after release of resetting and simultaneously has an opposite relation to a final drive pulse prior to resetting, a reliable time correction operation will become possible without using such lock mechanism to enable the clock apparatus to be manufactured inexpensively.

The object of the invention is to provide a drive pulse generator capable of generating a drive pulse in a unit length of time after release of resetting.

This invention is characterized in that between the $n-1$th stage divider and the nth stage divider of a divider chain for frequency-dividing a standard frequency signal from a crystal oscillator there are disposed a delay circuit for delaying the output of the $n-1$ th stage divider by a predetermined length of time and a logic gate responsive to the output of the delay circuit and the output of the $n-1$ th stage divider to produce an output pulse having a predetermined period and width, the nth stage divider being triggered by the output of the logic gate; and a reset signal being supplied to the delay circuit and at least the $n-1$ th stage divider.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic block diagram of a general electronic analog display clock apparatus;

FIG. 2 is a block diagram of a drive pulse generator according to an embodiment of the invention;

FIG. 3 is a detailed logic circuit diagram of part of the block diagram of FIG. 2;

FIG. 4 shows output waveforms of respective sections of FIG. 2;

FIGS. 5A and 5B are waveforms for explaining the reset operation;

FIG. 6 illustrates a connection diagram of the drive coil and inverters;

FIG. 7 is a modification of FIG. 2; and

FIG. 8 is another modification of FIG. 2.

As illustrated in FIG. 1, a conventional electronic analog display clock apparatus is comprised of a crystal oscillator 11, frequency divider chain 12, output circuitry 13 including output logic circuits and driving circuit, pulse motor means 14 and analog display section 15 having a second hand, minute hand and hour hand. The oscillator 11, divider chain 12 and output circuitry 13 constitute a drive pulse generator 16 powered from a battery 17 to generate drive pulses for driving a pulse motor 14. Particularly in case of wrist watch, it is desirable that the drive pulse generator 16 is comprised of a C-MOS integrated circuit operable with a low voltage.

FIG. 2 is a block diagram of a drive pulse generator according to the invention, the same parts and sections as those of FIG. 1 being denoted by the same reference numerals. The crystal oscillator 11 oscillates at a standard frequency of, for example, 32.768 kHz. The standard frequency signal from the oscillator 11 is frequency-divided in turn by the $n-1$ cascade-connected $\div 2$ dividers or binary counters 12-1, . . 12-m, . . . 12-$n-1$ of the divider chain 12. The number of binary counter stages of the divider chain 12 is determined by a length

of time required for the second hand of the analog display section 15 to make one step-advancement, i.e., by a unit length of time. The divider chain is adapted to frequency-divide the standard frequency signal into a signal having a period equal to the unit length of time. Accordingly, where it is desired to actuate the second hand for every second, the stage number of the divider chain is chosen to be 15 ($n-1=15$). In this case, accordingly, such signals $Qn-1$ and $\overline{Q}n-1$ having a period of 1 second as shown in FIG. 4, i.e., a frequency of 1 Hz are obtained from the $n-1$ th stage binary counter 12-$n-1$ of the divider chain 12.

The output $Qn-1$ of the $n-1$ th binary counter 12-$n-1$ is coupled to the input terminal of a delay circuit 18 which may be a half-bit shift register. This delay circuit performs the delay operation in response to the output Qm and its complement $\overline{Q}m$ of the m th stage counter 12-m ($m < n-1$) generating higher frequency signals than the $n-1$ th stage counter 12-$n-1$, and the length of time delay of the delay circuit is equal to half the length of period of the output of the mth stage counter 12-m.

The delayed output M as shown in FIG. 4 appearing at the output terminal O of the delay circuit and the complement $\overline{Q}n-1$ of $n-1$ th stage binary counter output $Qn-1$ are applied to a NOR gate 19.

From the NOR gate 19 there is derived the output X shown in FIG. 4 which has a pulse width equal to half the period of the output of the mth binary counter 12-m, i.e., a pulse width equal to the time delay length given by the delay circuit, and which has a period of 1 second. The output X of the NOR gate 19 and the complement Y thereof obtained from an inverter 20 are applied to the inputs In and $\overline{I}n$, respectively, of a binary counter 12-n to produce outputs Qn and $\overline{Q}n$ shown in FIG. 4 having a period of 2 seconds. The outputs Qn and $\overline{Q}n$ are the same as outputs obtained where the outputs $Qn-1$ and $\overline{Q}n-1$ of the $n-1$ th stage binary counter 12-$n-1$ are directly fed as trigger signals to the nth stage binary counter 12-n, but in this invention the nth stage binary counter 12-n is triggered by the output signal X and its complement Y obtained by passing the outputs $Qn-1$ and $\overline{Q}n-1$ of the $n-1$ th stage binary counter 12-$n-1$ through the delay circuit 18 and NOR gate 19. To the output side of the binary counter 12-n are connected first and second two-input NAND gates 21 and 22. To the first NAND gate 21 are coupled the output X of the NOR gate 19 and the output Qn of the binary counter 12-n. To the second NAND gate 22 are coupled the outputs X and $\overline{Q}n$. The outputs of the first and second NAND gates 21 and 22 are respectively coupled to the inputs of first and second inverters 23 and 24, between the outputs of which is connected a drive coil 25 for driving a pulse motor.

At the output of the first inverter 23 there appears an output O_A shown in FIG. 4 at an interval of 2 seconds while at the output of the second inverter 24 there appears an output O_B shown in FIG. 4 also at an interval of 2 seconds alternately with the output O_A. Accordingly, drive currents I_L are passed through the drive coil 25 correspondingly to the outputs O_A and O_B in mutually opposite directions at an interval of 1 second.

The delay circuit 18 and the binary counters of the divider chain 12 are supplied, when time correction is desired, with a reset signal from reset signal supply means 27 through a reset line 26. Since a reset button 28 is opened during the operation of the drive pulse generator, the reset line 26 is connected to ground potential through a resistor 29. When the reset button 28 is closed at the time of resetting, a positive reset signal from a battery 30 is applied to the delay circuit and binary counters. In response to the reset signal, for example, the binary counter 12-$n-1$ compulsively produces the output $Qn-1$ of zero volt irrespective of output condition, prior to resetting and the delay circuit 18 holds the output prior to resetting.

In principle it is sufficient to supply a reset signal to at least one binary counter of the divider chain 12, but where it is desired to increase "accuracy" and to reduce the power consumption at the time of resetting, supply of reset signal to all the binary counters 12-1 to 12-$n-1$ is most preferable. The accuracy used here in this specification is defined to mean a "time error" concerning the time when an initial pulse is generated after resetting has been released. However, supply of a reset signal to all the binary counters of the divider chain 12 results in an increase in the number of MOS transistors constituting each counter.

Where, for example, arrangement is so made that a reset signal is supplied to 10th and 15th stage binary counters of a divider chain comprised of 15 binary counter stages, a time error within the output period, i.e., 1/64 sec., of the ninth stage binary counter is produced concerning the time when the initial drive pulse is generated after resetting has been released. Where, as indicated by solid lines of FIG. 2, a reset signal is supplied to the delay circuit 18 and 15th stage binary counter 12-$n-1$, there exists a time error within the output period, i.e., one-half sec., of the 14th stage binary counter. But this extent of time error will practically raise no problem.

As previously mentioned, the delay circuit 18 performs the delay operation in response to the outputs Qm and $\overline{Q}m$ of the binary counter 12-m, and the length of the time delay is equal to half the period of output Qm, and the pulse motor is driven by a drive pulse having a duration equal to the half-period. Accordingly, the stage position of counters for supplying operating signals to the delay circuit 18 is determined by the length of response time of the pulse motor, and thus the stage position at which relatively low or high frequency signals are produced is not desirable.

FIG. 3 illustrates an example of a logical diagram of the binary counters 12-$n-1$ and 12-n and delay circuit 18 of FIG. 2. The binary counter 12-$n-1$ being supplied with reset signals comprised of clocked inverters and NOR gates is the same as a static binary counter with a reset terminals shown in FIGS. 6A and 6B in the copending U.S. patent application Ser. No. 333,145 filed Feb. 16, 1973. The binary counter 12-n is the same as the static binary counter shown in FIGS. 4A and 4B in the copending application. Of the binary counters of the divider chain 12, ones being supplied with reset signals may have the same construction as the binary counter 12-$n-1$ and ones being supplied with no reset signals may have the same construction as the binary counter 12-n. It should be noted, however, that those binary counters of the divider chain 12 which are operating at a relatively high frequency are not always required to be of static type but may be of dynamic type having no clocked inverter connected in parallel with a NOR gate or having no clocked inverter connected in parallel with an inverter. The delay circuit 18 is a

half-bit static shift register comprised of clocked inverters 31 and 32, NAND gate 33 and inverter 34.

FIG. 6 illustrates a connection between the drive coil 25 and the first and second inverters 23 and 24 of FIG. 2. The first inverter 23 is comprised of a P-channel MOS transistor 23P and N-channel MOS transistor 23N whose drain-source paths are series-connected across a power source. Similarly, the second inverter 24 is comprised of a P-channel and N-channel MOS transistors 24P and 24N whose drain-source paths are series-connected across a power source. The drive coil 25 is connected between the junction between the transistors 23P and 23N of the first inverter 23 and the junction between the transistors 24P and 24N of the inverter 24. Where the output of the first NAND gate 21 is zero volt and the output of the second NAND gate 22 is positive, the P-channel transistor 23P and N-channel transistor 24N are rendered both conductive to cause drive current to be flowed through the drive coil 25 in a direction indicated by an arrow of solid line. Conversely, where the output of the second NAND gate 22 is zero volt and the output of the first NAND gate 21 is positive, the transistors 24P and 23N are rendered both conductive to cause drive current to be flowed through the drive coil 25 in a direction indicated by an arrow of dotted line. where the outputs of the first and second NAND gates 21 and 22 are both positive, the N-channel transistors 23N and 24N are rendered both conductive. Accordingly, both ends of the drive coil 25 are at zero volt so that no drive current flows through the drive coil 25. Conversely, where the outputs of the first and second NAND gates 21 and 22 are zero volt, the P-channel transistors 23P and 24P are rendered both conductive to cause source voltage to be applied to both ends of the drive coil 25. Also in this case, no current is passed through the drive coil 25.

FIGS. 5A and 5B illustrate waveforms for explaining the resetting operation, FIG. 5A illustrating waveforms where resetting is effected after the output O_A has been produced from the first inverter 23; FIG. 5B illustrating waveforms where resetting is effected after the output O_B has been produced from the second inverter 24. Where resetting is effected after the output O_A has been produced, the output $Qn-1$ of the binary counter 12-$n-1$ is compulsively reduced to zero volt by the action of the NOR gate upon receipt of a positive reset signal, while the output M of the delay circuit 18 is held at the positive level prior to resetting by the action of the inverter 34 and NAND gate 33. Since the level of output M of the delay circuit 18 does not vary during resetting, the level of output X of the NOR gate 19 does not vary but is held at a level of zero volt. Accordingly, the outputs Qn and $\overline{Qn}$ of the binary counter 12-n are also held at the levels prior to resetting. For this reason, the first and second inverters 23 and 24 do not produce the outputs O_A and O_B during resetting. when resetting is released, the level of output $Qn-1$ of the binary counter 12-$n-1$, accordingly, the level of the output M of the delay circuit 18 varies to cause the NOR gate 19 to produce the output X in the unit length of time after release of resetting. For this reason, the second inverter 24 produces the output O_B. Where resetting is effected after the first inverter 23 has produced the output O_A, the second inverter 24 produces the output O_B in the unit length of time after release of resetting. Where resetting is effected after the second inverter 24 has produced the output O_B, the first inverter 23 produces the output O_A in the unit length of time after release of resetting, as illustrated in FIG. 5B. This is due to the fact that the binary counter 12-n is supplied with no reset signal to be kept at the output level prior to resetting. According to the construction of FIG. 2, therefore, it never happens that the same kind of drive pulses are generated both prior to resetting and after release of resetting. Therefore, any locking mechanism becomes unnesessary to simplify the clock apparatus construction. Strictly speaking, it is not in the unit length of time that an initial drive pulse is generated after release of resetting. As previously mentioned, the time error is produced in accordance with the stage position of a binary counter being supplied with the reset signal. For example, where the reset signal is supplied to the ninth to 15th stage binary counters, a time error within the output period, i.e., 1/128 sec., of the eighth stage binary counter is produced.

FIG. 7 is a modification of FIG. 2 wherein reset signal is applied to the delay circuit 18 and binary counters through an AND gate 36; the other input terminal of the AND gate 36 is supplied with the output Y of the inverter 20. This modification is so arranged that the resetting operation is not performed during the period in which the outputs X and Y illustrated in FIGS. 5A and 5B are produced, namely, during the period in which current is passed through the drive coil and the pulse motor is thereby operated.

FIG. 8 illustrates an embodiment so constructed that the reset signal is applied also to the binary counter 12-n.

In this embodiment, since the output level of the binary counter 12-n is also reset by the reset signal, the output produced in the unit length of time after release of resetting is limited to O_A or O_B only. The NAND gate 33 of the delay circuit 18 of FIG. 3 may be replaced by a NOR gate 37 as illustrated in FIG. 8, and in this case the inverter 34 becomes unnecessary. Where the NAND gate 33 is replaced by the NOR gate 37, the NOR gate 19 is replaced by a NAND gate 38.

Preferably, the drive pulse generator according to the invention is constituted by complementary MOS transistors, but can of course be constituted by the P-channel or N-channel MOS transistors only.

What is claimed is:

1. A drive pulse generator for use in an electronic analog display clock apparatus which is adapted to supply drive pulses to the drive coil of motor means for driving time indication hands, comprising:

a standard frequency signal source;

a frequency divider chain having binary counters cascade-connected in a number of $n-1$ and connected to receive the output of said signal source for frequency-dividing said standard frequency signal in turn;

a delay circuit connected to receive the output of the $n-1$ th stage binary counter of said frequency divider chain for delaying the output of said $n-1$ th stage binary counter in response to the output of one binary counter in said divider chain which produces a higher frequency signal than the output frequency of said $n-1$ th stage binary counter;

logic gate means connected to receive the output of said delay circuit and an output of said $n-1$ th stage binary counter for producing an output pulse signal having a predetermined period and pulse width;

a binary counter (*n*th stage) connected to receive the output of said logic gate;

logic circuit means connected to receive output of said *n*th binary counter and output of said logic gate for producing in said drive coil drive pulses passing therethrough at an interval of the predetermined period in mutually opposite directions; and

resetting means for supplying a reset signal to at least said *n*−1 stage binary counter and said delay circuit.

2. A drive pulse generator according to claim **1** wherein said logic circuit means includes first and second two-input logic gates, one side-inputs of said first and second two-input logic gates being coupled to an output of said logic gate means and the other side-inputs to the complementary outputs of said *n*th binary counter, and first and second inverters respectively connected to receive the outputs of said first and second two-input logic gates, said drive coil being connected between the outputs of said first and second inverters.

3. A drive pulse generator according to claim **1** wherein said resetting means includes means for stopping, when the output of said logic gate means is at a predetermined level, supply of the reset signal in response to said output of said logic gate means.

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