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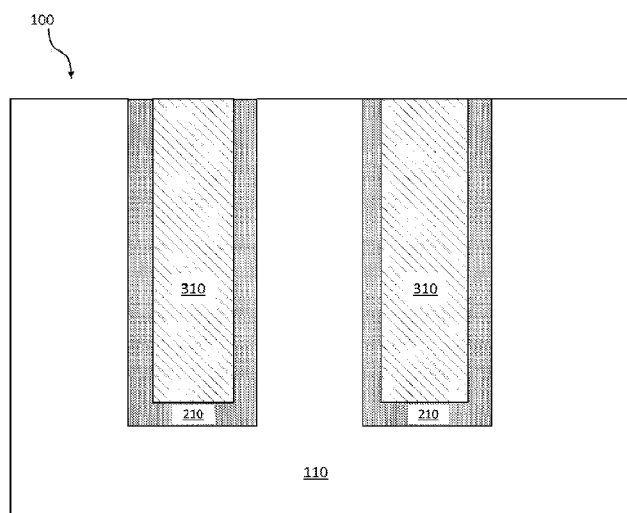


FIG 1

(57) **Abstract:** Techniques are disclosed for producing graphitic barrier layers that encapsulate or otherwise isolate a metal interconnect feature from adjacent insulator or dielectric materials. The techniques can include an on-chip synthesis method in which barrier layer precursor materials, for example, hydrocarbon-based self-assembled monolayers, are positioned between a dielectric feature and an electrically conductive metal line. Through a treatment process, such as thermal annealing, the barrier layer precursor materials are converted into a graphitic barrier layer that comprises graphene and, in some cases, is a graphene monolayer. The disclosed graphitic barrier layers may be atomically thin, have a substantially uniform thickness and may optionally conduct charge, thereby allowing the barrier layer to serve as a current shunt, capable of supporting high current densities.

GRAPHENE BARRIER FOR ELECTRICAL INTERCONNECTS

BACKGROUND

In the manufacture of integrated circuits, interconnects may be formed on a semiconductor substrate using a copper damascene process. Such a process typically begins with
5 a trench and/or via being etched into an insulator layer, a barrier material being deposited into the trench and then copper metal being deposited on the barrier material to form the interconnect. As device dimensions continue to scale down, the various interconnect features become narrower and closer together giving rise to a number of non-trivial problems.

BRIEF DESCRIPTION OF THE DRAWINGS

10 Figure 1 illustrates an example integrated circuit structure showing a graphitic barrier layer in accordance with an embodiment of the present disclosure.

Figure 2 illustrates an example technique of producing an integrated circuit comprising a graphitic barrier layer in accordance with an embodiment of the present disclosure.

15 Figures 3A-3F illustrate cross-section side views of a series of integrated circuit structures showing formation of a graphitic barrier layer in accordance with an embodiment of the present disclosure.

Figure 4 illustrates an example computing system implemented with one or more integrated circuits comprising interconnect structures configured in accordance with an embodiment of the present disclosure.

20 As will be appreciated, the figures are not necessarily drawn to scale or intended to limit the disclosure to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of a structure may have less than perfect straight lines, right angles, and some features may have surface topology or otherwise be non-smooth, given real world limitations of the processing
25 equipment and techniques used. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

Techniques are disclosed for forming integrated circuit structures that include graphitic barrier layers to separate dielectric features from neighboring electrically conductive features. In

some embodiments, the graphitic barrier layer may be synthesized on-chip, in position between the dielectric and the metal interconnect, for example, by using self-assembling materials and, in some embodiments, self-assembled monolayers (SAMs). In such embodiments, barrier layer precursor materials (e.g., SAMs) may be placed in the desired final position of the graphitic barrier layer and, while in position, may be treated (e.g., by a thermal annealing treatment) to yield a graphitic barrier layer. The disclosed techniques may provide various advantages over traditional deposition techniques of forming a barrier layer. For example, the disclosed methods and materials may allow a graphene monolayer to be produced that surrounds the metal of the interconnect structure and is substantially conformal and/or has a thickness in the sub-nanometer range. The disclosed techniques may also enhance the mechanical properties of the interconnect structure (e.g., by increasing the fracture energy between the barrier layer and the dielectric and/or the metal interconnect). The disclosed graphitic barrier layers can be used to effectively prevent the conductive interconnect metal from deleteriously migrating into the dielectric of the integrated circuit. Graphitic barrier layers as disclosed herein may have thicknesses that are in the sub-nanometer range, and may, in some embodiments, also conduct electrical current. Numerous configurations and variations will be apparent in light of this disclosure.

General Overview

It is often desirable to include barrier material between the nonconductive (e.g., the dielectric) and conductive (e.g., the copper metal) features of an integrated circuit. Barrier materials can prevent the metal interconnect from deleteriously migrating into the dielectric material, can insulate the metal and/or enhance adhesion between the dielectric and metal. However, known traditional barrier materials cannot scale beyond a few nanometers. Accordingly, as interconnect structures scale to smaller sizes, conventional barrier materials take up a progressively greater portion of the cross-sectional area of an interconnect line. As will be appreciated in light of this disclosure, replacing conventional barrier materials with a graphitic barrier layer, such as, for example, a graphene monolayer, would increase the effective conductance of an interconnect line by maximizing the proportion of cross-sectional area occupied by the conductive metal core while also providing an effective diffusion barrier between the dielectric and metal of an interconnect structure. Graphene is an atomically-thin and conductive material. While graphene may be used in some applications to provide an effective diffusion barrier, there are a number of challenges associated therewith, particularly with respect to forming graphene barriers of sub-nanometer thickness. For instance, transferring graphene or graphitic material grown on a separate substrate to an integrated circuit chip with some topography (e.g., trenches) is not trivial or otherwise readily accomplished.

Thus, and in accordance with an embodiment of the present disclosure, techniques are provided for forming graphitic barrier layers for metal interconnect structures. In one specific embodiment, self-assembling materials, such as self-assembled monolayers (SAMs), may be employed to produce graphitic barrier layers. For example, a hydrocarbon-based SAM may be positioned between the dielectric and the electrically conductive metal of an integrated circuit and then be subjected to a treatment process (e.g., a thermal annealing process). Through this process, the hydrocarbon-based SAM may be converted into a graphitic barrier layer while positioned between the dielectric and the interconnect.

The disclosed techniques of forming graphitic barrier layers may provide various advantages over known methods of depositing or growing graphene in a trench or via. For example, the disclosed techniques may be capable of producing a graphitic barrier layer having a maximum thickness of less than 2 nm or a maximum thickness in the sub-nanometer range (e.g., a thickness of less than 1, less than .75, or less than .5 nanometers). In one specific example, the graphitic barrier layer is a graphene monolayer. Additionally, the graphitic barrier layer may be substantially conformal, meaning that the layer is continuous and has a substantially uniform thickness along the interface of the metal interconnect and/or the dielectric film. Note, however, that other embodiments need not have a uniform thickness. The graphitic barrier layer may or may not conduct charge and in embodiments where the graphitic barrier layer conducts charge, the layer may serve as a current shunt capable of supporting high current densities. Numerous variations and configurations will be apparent in light of this disclosure.

Graphitic Barrier Layer(s)

Figure 1 illustrates a cross-section side view of an integrated circuit structure showing a graphitic barrier layer configured in accordance with an embodiment of the present disclosure. Specifically, Figure 1 shows a base inter-layer dielectric (ILD) layer with a metal interconnect or an otherwise electrically conductive line formed therein. Metal interconnect 310 is surrounded by graphitic barrier layer 210. As defined herein, the term graphitic barrier layer means that the defined layer comprises at least a portion of graphene. For example, in some embodiments, the graphitic barrier layer comprises at least 5%, at least 10%, at least 25%, at least 30%, at least 40%, at least 50%, at least 60%, at least 75%, at least 80%, at least 85%, at least 90%, at least 95%, or at least 99% graphene by weight based on the total weight of the graphitic barrier layer. In some embodiments, graphitic barrier layer 210 comprises one or more graphene monolayers. In some such embodiments, the graphitic barrier layer consists of or consists essentially of a single graphene monolayer. In these and other various embodiments, the graphene monolayer at least partially surrounds metal interconnect

310. If present, additional graphene monolayers may at least partially surround the innermost graphene monolayer. In addition to graphene, the graphitic barrier layer may comprise other materials, such as polymers, one or more functional groups (e.g., functional groups that line the peripheral edges of graphene structures), tantalum (Ta), tantalum nitride (TaN), tantalum cobalt (TaCo), titanium nitride (TiN), tungsten (W), tungsten nitride (WN), cobalt tungsten (CoW), molybdenum nitride (MoN), ruthenium/tantalum alloy (Ru/Ta) and known filler materials. In still other embodiments, the graphitic barrier layer may comprise only graphene (pure graphene layer, >99% graphene).

The disclosed graphitic barrier layer may be the only material separating the ILD from the metal interconnect. For example, the disclosed graphitic barrier layer may adhere to both the dielectric and the metal interconnect and, in so doing, may eliminate the need for any additional conventional barrier layer(s) and/or liner(s) to separate the metal from the dielectric. Graphitic barrier layer 210 may have a maximum thickness that is in the sub-nanometer range. For example, the graphitic barrier layer may have a maximum thickness of less than 2, less than 1.8, less than 1.75, less than 1.6, less than 1.5, less than 1.35, less than 1.2, less than 1, less than .8, less than .75, less than .6, less than .5, or less than .35 nm. In some embodiments, the thickness of the graphitic barrier layer is approximately equal to the thickness of a single graphene monolayer. The thickness of the graphitic barrier layer can be defined at any point as the distance between the ILD 110 and the metal interconnect 310.

The graphitic barrier layer may conform to the topology of underlying ILD 110 and in some such embodiments, the graphitic barrier layer may be substantially conformal. In these and other embodiments, the thickness of the graphitic barrier layer may be defined as substantially uniform, meaning that the thinnest part of the layer is within 40%, within 35%, within 30%, within 25%, within 20%, within 15%, within 10%, within 5%, or within 2% of the thickest part of the layer. Other configurations for graphitic barrier layer 210 will depend on a given application and will be apparent in light of this disclosure. Further note that the graphitic barrier layer may be continuous so as to provide no breaks through which metal could potentially diffuse into neighboring dielectric or insulator material. The uniformity and continuous nature of the graphitic barrier layer can vary from one embodiment to the next, as will be appreciated in light of this disclosure.

ILD 110 may comprise any of a wide range of dielectric materials, including, but not necessarily limited to: (1) an oxide, such as silicon dioxide (SiO_2), aluminum oxide (Al_2O_3), etc.; (2) a nitride, such as silicon nitride (Si_3N_4); (3) a carbide, such as silicon carbide (SiC); (4) a carbonitride, such as silicon carbon nitride (SiCN); (5) an oxynitride, such as silicon oxynitride

(SiO_xN_y); and/or (6) a combination of any of the aforementioned (e.g., SiCN/SiN, etc.). In some embodiments, at least the surface of ILD 110 may be functionalized, for example, to include hydrophilic or hydrophobic substituents, as desired. In some embodiments, the surface of ILD 110 includes hydroxyl groups and the surface of ILD 110 is thus hydrophilic. In still other
5 embodiments, the ILD 110 may comprise low-k dielectric materials or high-k dielectric materials, depending on the application and desired performance of the device. Other suitable materials and/or configurations for ILD 110 will depend on a given application and will be apparent in light of this disclosure.

Metal interconnect 310 may comprise any of a wide range of electrically conductive
10 metals, such as, but not necessarily limited to: copper (Cu); aluminum (Al); silver (Ag); nickel (Ni); gold (Au); titanium (Ti); tungsten (W); ruthenium (Ru); cobalt (Co); chromium (Cr); iron (Fe); hafnium (Hf); tantalum (Ta); vanadium (V); molybdenum (Mo); palladium (Pd); platinum (Pt); and/or an alloy or combination of any of the aforementioned. Although referred to throughout this disclosure as “metal,” the interconnect materials may be metallic or non-metallic
15 and may include polymeric materials, in some instances. To this end, any material having a suitable degree of electrical conductivity can be used for the one or more metal interconnects 310 of IC 100. Other suitable metals/materials for a given interconnect 310 will depend on a given application and will be apparent in light of this disclosure.

Example Methods of Manufacture

20 Graphitic barrier layers as disclosed herein may be produced by a variety of techniques. Figure 2 illustrates a method 400 of forming an integrated circuit device that includes a graphitic barrier layer in accordance with one or more embodiments of the present disclosure. Figures 3A-3F illustrate example structures that are formed when carrying out method 400 of Figure 2, in accordance with various embodiments. Note that the techniques described herein can be used in
25 any suitable structure or device that would benefit from the use of one or more graphitic barrier layers to, for example, prevent a conductive metal from migrating into a neighboring non-conductive insulating feature.

As can be seen in Figure 2, method 400 includes forming 402 a dielectric layer, such as the ILD 110 shown in Figure 3A, in accordance with an embodiment. In some cases, ILD 110
30 may be formed or deposited, on a substrate, wafer, or other suitable surface, as desired. As will be appreciated in light of this disclosure, any of a wide range of suitable deposition techniques may be utilized to form ILD 110, such as, but not necessarily limited to: physical vapor deposition (PVD); chemical vapor deposition (CVD); spin coating/spin-on deposition (SOD); and/or a combination of any of the aforementioned. Other suitable configurations, materials,

deposition techniques, and/or thicknesses for ILD 110 will depend on a given application and will be apparent in light of this disclosure. Figure 3A shows one example structure for ILD 110; however, ILD 110 may be formed in accordance with any desired structure, and may be etched or otherwise manipulated to form trenches and/or vias by any number of known techniques.

5 Method 400 continues with optionally treating 404 the surface of the dielectric layer, for example, the surface of ILD 110 shown in Figure 3A. The surface of ILD 110 may optionally be treated, for example, to render the exposed surface of ILD 110 hydrophilic (e.g., by increasing the concentration of hydroxyl groups on the surface of ILD 110). Any number of suitable treatment techniques will be apparent in light of this disclosure.

10 After ILD 110 is formed and, if desired, treated, method 400 continues with applying 406 barrier layer precursor materials 200 to the dielectric layer to form the example structure shown in FIG. 3B, in accordance with an example embodiment. Barrier layer precursor materials 200 may be applied to ILD 110 in either the liquid phase or the vapor phase. For example, the barrier layer precursor materials may be diluted in solvent and applied to the ILD
15 while in the liquid phase. Alternatively, the barrier layer precursor materials may be evaporated and deposited on ILD 110 while in the vapor phase in a process analogous to atomic layer deposition (ALD). After application, the barrier layer precursor materials may have a thickness of less than 2 nanometers, less than 1 nanometer, any thickness of the graphitic barrier layer as described above, or some other suitable thickness depending on the given target application or
20 end use.

 The barrier layer precursor materials 200 may comprise self-assembling materials and, in some embodiments, the barrier layer precursor materials may comprise one or more self-assembled monolayers (SAMs). In some embodiments where the barrier layer precursor materials comprise SAMs, the SAM molecules may include a base structure with one or more
25 attached functional groups. Examples of suitable base structures include both aliphatic and aromatic groups, such as cyclic aromatic compounds. Examples of suitable functional groups include, but are not limited to, thiols, carboxylic acids, carboxylate salts, amines (e.g., mono or poly aminated primary, secondary and tertiary amines), aniline groups, pyridyl groups and metal atoms (e.g., any metal that could catalyze an electroless reaction). Example SAMs include but
30 are not limited to silanes (for example, aliphatic and aromatic chlorosilanes, methoxy silanes and ethoxy silanes), phosphonic acids, germanes (for example, chlorogermanes) and ethylene-terminated compounds. In some embodiments, the barrier layer precursor materials may comprise one or more of the following compounds: trichloro(phenyl)silane,

diphenyldichlorogermane, 4-biphenyldimethylchlorosilane, p-aminophenyltrimethoxysilane, 4-(2-(triethoxysilyl)ethyl)pyridine and (9)-anthracenyltrimethoxysilane.

In some embodiments where the barrier layer precursor materials include SAMs, the barrier layer precursor materials may be limited to a single type of SAM molecule or may be include multiple types of SAM molecules. In these and other embodiments, the barrier layer precursor materials comprise compounds with sub-nanometer dimensions. For example, the diameter of the barrier layer precursor materials may be no greater than 2, no greater than 1.75, no greater than 1.5, no greater than 1.25, no greater than 1, no greater than .8, no greater than .75, no greater than .6, no greater than .5, no greater than .4, no greater than .3, no greater than .2, or no greater than .1 nm.

As shown in method 400, the barrier layer precursor materials may optionally be activated 407 with one or more catalysts. Suitable catalysts include, for example, metal catalysts, such as palladium, nickel, cobalt, ruthenium, platinum, gold, silver, or any other metal capable of catalyzing an electroless reaction. The catalyst(s) may be applied to the barrier layer precursor materials by any suitable method, including but not necessarily limited to PVD, CVD and ALD.

Method 400 continues with optionally depositing 408 a metal 300 onto barrier layer precursor materials 200, to form a structure as shown in Figure 3C, in accordance with an example embodiment. Metal 300 may be any material described above with respect to metal interconnect 310 or may optionally be a different type of material. In some embodiments, metal 300 may be the same as metal interconnect 310, however, in other embodiments, metal 300 may be different from metal interconnect 310. For example, in some embodiments, metal 300 may be an initial metal that is deposited onto barrier layer precursor materials and is later replaced with a different metal to form metal interconnect 310. Suitable techniques for forming metal 300 include, for example, PVD, CVD, ALD and electroplating processes. In some embodiments where the barrier layer precursor materials are activated 407 with an electroless catalyst, metal 300 may be formed by an electroless plating process. In one particular embodiment, the barrier layer precursor materials are catalytically activated (e.g., by exposure to palladium (II) chloride or a palladium, cobalt, nickel, silver, gold or ruthenium-based catalyst) and metal 300 is applied by electroless plating.

Method 400 continues with treating 412 the barrier layer precursor materials 200 to convert the barrier layer precursor materials 200 to a graphitic barrier layer 210, as shown in Figure 3D, in accordance with an example embodiment. In some embodiments, treatment of the barrier layer precursor materials 200 involves thermal treatment, such as at elevated

temperatures. In some embodiments, treatment of the barrier layer precursor materials involves heating to a temperature of at least 400, at least 500, at least 600, at least 700, at least 800, or at least 900°C. In some embodiments, the barrier layer precursor materials are heated to between 400-900°C, between 400-600°, or between 500-800°C. Concurrently with exposure to elevated
5 temperatures, the barrier layer precursor materials may also be subjected to increased pressure, including a pressure of greater than 1 atm, such as a pressure of at least 5, at least 10, at least 15, at least 20, at least 25, or at least 30 atm. As will be appreciated in light of this disclosure, in some embodiments, a lower treatment temperature may be used when a higher treatment pressure is applied. While not wishing to be bound by theory, the metal that is in contact with
10 SAMs present in the barrier layer precursor materials may act as a catalyst to facilitate the conversion of hydrocarbon materials to graphene.

As shown in method 400, the barrier layer precursor materials 200 may optionally be capped 410 with a capping material prior to treatment. Any suitable capping material, such as hermetic materials, including, for example, silicon nitride, may be used to cap the precursor
15 material. Other materials suitable for capping will be apparent in light of this disclosure. The capping material may, for example, allow the precursor materials to be subjected to higher temperatures than possible without capping. For example, an interconnect structure having the precursor materials capped may be able to withstand temperatures of 600°C or higher.

As shown in method 400, in some embodiments metal 300 may optionally be removed
20 413 to form a structure as shown in Figure 3E, according to an example embodiment. Metal 300 may be removed by any suitable process, such as by a wet etch process, or by any other process that does not damage graphitic barrier layer 210. In these and other embodiments, metal interconnect 310 may be deposited 415 after metal 300 is removed to form a structure as shown in Figure 3F, according to an example embodiment. Any suitable technique may be used to
25 deposit metal interconnect 310, such as any of the techniques discussed above with respect to depositing metal 300, or any other suitable technique.

Method 400 shows that, optionally, various features of the integrated circuit may be planarized and/or polished 414. For example, any layer described herein may be subjected to a chemical-mechanical planarization (CMP) process or other appropriate polishing/planarization
30 process as desired, for example, to allow for subsequent processing. Planarization and/or polishing may occur prior to or after treatment of the precursor barrier materials. In some embodiments, ILD 110, barrier layer precursor materials 200, graphitic barrier layer 210 one or more interconnects 310 and/or capping layer(s), if present, may undergo a CMP process to remove undesired excess.

As shown in method 400, the graphitic barrier layer and surrounding dielectric and metal interconnect may be further processed to form 416 an integrated circuit (IC) 100, shown in Figure 1. In some instances, IC 100 may be, for example, a partially processed IC with one or more devices and/or metal layers. Numerous suitable configurations will be apparent in light of this disclosure. IC 100 may either be formed prior to or after treatment of the barrier layer precursor materials to convert the barrier layer precursor materials to a graphitic barrier layer.

In some cases, the disclosed techniques may be compatible with any of a wide variety of interconnect contexts and structures. Some example structures may include, but are not necessarily limited to: single-damascene structures; dual-damascene structures (e.g., a line with an underlying via); anisotropic structures; isotropic structures; and/or any other desired IC structures, interconnects, or other conductive structures. Also, in accordance with an embodiment, the dimensions of a given interconnect may be customized as desired for a given target application or end-use. Other suitable configurations for a given interconnect will depend on a given application and will be apparent in light of this disclosure.

Additional Techniques and Considerations

It will be understood that in some embodiments where the barrier layer precursor materials comprise a hydrocarbon-based SAM, treatment of the barrier layer precursor materials (e.g., by a thermal annealing process as described herein) may convert the SAM into a graphitic barrier layer comprising, for example, a graphene monolayer. In this way, the disclosed techniques allow for an on-chip synthesis of graphene, according to an embodiment. The disclosed techniques may provide numerous advantages over traditional techniques of forming a barrier layer, such as by deposition. For example, the disclosed methods and materials may allow a graphene monolayer to be produced that surrounds the metal of the interconnect structure, is substantially conformal and/or has a thickness in the sub-nanometer range. Additionally, the disclosed techniques may aid in avoiding issues of nonuniform sidewall deposition that commonly occur with deposition of barrier layer materials. For example, the disclosed techniques can be used to minimize or prevent the need to deposit excess barrier layer materials to ensure all regions are sufficiently covered, according to some embodiments. In this way, the disclosed techniques can be used to conserve barrier layer materials and minimize the cross-sectional surface area of the interconnect structure devoted to excess barrier layer materials, according to some embodiments. The use of self-assembling barrier layer precursor materials may also minimize or eliminate structural defects common in traditional deposition approaches due to non-conformal application, according to some embodiments. Thermal treatment of the barrier layer precursor materials in the presence of the metal core may also

positively affect mechanical properties of the resultant interconnect structure. For example, the fracture energy between the metal interconnect and the dielectric may increase through the thermal treatment processes described herein.

Various methods can be used to determine whether a device has been produced using the disclosed techniques. For example, Raman spectroscopy can detect the presence of graphene, even in very low weight percentages. Additionally, known methods of structure analysis (e.g., scanning/transmission electron microscopy (SEM/TEM), composition mapping, and/or atom probe imaging/3D tomography) can be used to determine the dimensions of barrier layers of a given integrated circuit.

Example System

Figure 4 illustrates a computing system 1000 implemented with one or more integrated circuit structures configured and/or otherwise fabricated in accordance with an example embodiment of the present disclosure. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board or a daughterboard mounted on a main board or the only board of computing system 1000, etc. Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 1000 may include one or more integrated circuit structures configured with one or more conductive interconnect features having graphitic barrier layers, as variously described herein. These integrated circuit structures can be used, for instance, to implement an on-board processor cache or memory array or other circuit feature that includes interconnects. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments of the present disclosure, the integrated circuit die of the processor includes onboard memory circuitry that is implemented with one or more integrated circuit structures configured with graphitic barrier layers, as variously described herein. The term “processor” may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 may also include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more devices implemented with one or more integrated circuit structures formed as variously described herein (e.g., damascene and dual damascene graphitic barrier layers within a given interconnect layer, or other semiconductor structures that may benefit from thin graphitic barrier layers). As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any communication chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processors 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing system 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder.

5 In further implementations, the computing system 1000 may be any other electronic device that processes data or employs integrated circuit features configured with one or more conductive interconnect features having graphitic barrier layers, as variously described herein.

Further Example Embodiments

10 Numerous embodiments will be apparent, and features described herein can be combined in any number of configurations. The following examples pertain to further example embodiments, from which numerous permutations and configurations will be apparent.

Example 1 is an integrated circuit device including: an interlayer dielectric (ILD) feature; an electrically conductive interconnect feature; and a graphitic barrier layer positioned between the dielectric feature and the electrically conductive interconnect feature, the graphitic
15 barrier layer having a maximum thickness of less than 2 nanometers.

Example 2 includes the subject matter of Example 1, wherein the graphitic barrier layer has a maximum thickness of less than 1.5 nanometers.

Example 3 includes the subject matter of any of Examples 1-2, wherein the graphitic barrier layer has a maximum thickness of less than 1 nanometer.

20 Example 4 includes the subject matter of any of Examples 1-3, wherein the graphitic barrier layer has a maximum thickness of less than 0.5 nanometers.

Example 5 includes the subject matter of any of Examples 1-4, wherein the graphitic barrier layer includes at least 5% graphene by weight based on the weight of the graphitic barrier layer.

25 Example 6 includes the subject matter of any of Examples 1-5, wherein the graphitic barrier layer includes at least 25% graphene by weight based on the weight of the graphitic barrier layer.

Example 7 includes the subject matter of any of Examples 1-6, wherein the graphitic barrier layer includes at least 30% graphene by weight based on the weight of the graphitic
30 barrier layer.

Example 8 includes the subject matter of any of Examples 1-7, wherein the thickness of the graphitic barrier layer is substantially uniform, such that the thinnest part of the layer is within 35% of the thickest part of the layer.

Example 9 includes the subject matter of any of Examples 1-8, wherein the thickness of the graphitic barrier layer is substantially uniform, such that the thinnest part of the layer is within 20% of the thickest part of the layer.

Example 10 includes the subject matter of any of Examples 1-9, wherein the graphitic barrier layer includes at least one graphene monolayer.

Example 11 includes the subject matter of any of Examples 1-10, wherein the graphitic barrier consists essentially of a graphene monolayer.

Example 12 includes the subject matter of any of Examples 1-11, wherein each of the electrically conductive interconnect feature and the graphitic barrier layer has a dual-damascene cross-sectional profile.

Example 13 is an integrated circuit device including: an interlayer dielectric (ILD) feature; an electrically conductive interconnect feature; and a graphitic barrier layer positioned between the dielectric feature and the electrically conductive interconnect feature, wherein the graphitic barrier layer has a thickness that is substantially uniform, such that the thinnest part of the layer is within 35% of the thickest part of the layer.

Example 14 includes the subject matter of Example 13, wherein the thinnest part of the graphitic barrier layer is within 20% of the thickest part of the graphitic barrier layer.

Example 15 includes the subject matter of any of Examples 13-14, wherein the graphitic barrier layer has a maximum thickness of less than 2 nanometers.

Example 16 includes the subject matter of any of Examples 13-15, wherein the graphitic barrier layer has a maximum thickness of less than 1.5 nanometers.

Example 17 includes the subject matter of any of Examples 13-16, wherein the graphitic barrier layer has a maximum thickness of less than 1 nanometer.

Example 18 includes the subject matter of any of Examples 13-17, wherein the graphitic barrier layer has a maximum thickness of less than 0.5 nanometers.

Example 19 includes the subject matter of any of Examples 13-18, wherein the graphitic barrier layer includes at least 5% graphene by weight based on the weight of the graphitic barrier layer.

Example 20 includes the subject matter of any of Examples 13-19, wherein the graphitic barrier layer includes at least 25% graphene by weight based on the weight of the graphitic barrier layer.

Example 21 includes the subject matter of any of Examples 13-20, wherein the graphitic barrier layer includes at least 30% graphene by weight based on the weight of the graphitic barrier layer.

Example 22 includes the subject matter of any of Examples 13-21, wherein the graphitic barrier layer includes at least one graphene monolayer.

Example 23 includes the subject matter of any of Examples 13-22, wherein the graphitic barrier layer consists essentially of a graphene monolayer.

5 Example 24 includes the subject matter of any of Examples 13-23, wherein each of the electrically conductive interconnect feature and the graphitic barrier layer has a dual-damascene cross-sectional profile.

Example 25 is a mobile computing device including the subject matter of any of Examples 1-24.

10 Example 26 is a method of producing a graphitic barrier layer, the method including: forming a dielectric feature; applying barrier layer precursor materials to the dielectric feature; depositing an electrically conductive feature over the barrier layer precursor materials; and converting the barrier layer precursor materials to a graphitic barrier layer.

Example 27 includes the subject matter of Example 26, wherein the barrier layer
15 precursor materials comprise self-assembling compounds.

Example 28 includes the subject matter of Examples 26-27, wherein the barrier layer precursor materials are limited to a single type of self-assembling compound.

Example 29 includes the subject matter of Examples 26-27, wherein the barrier layer precursor materials include more than one type of self-assembling compound.

20 Example 30 includes the subject matter of Examples 26-29, wherein the barrier layer precursor materials include self-assembled monolayers.

Example 31 includes the subject matter of Examples 26-30, wherein the barrier layer precursor materials include hydrocarbon-based self-assembled monolayers.

Example 32 includes the subject matter of Examples 26-31, wherein the barrier layer
25 precursor materials include one or more aromatic compounds.

Example 33 includes the subject matter of Examples 26-32, wherein the barrier layer precursor materials include at least one of the following compounds: trichloro(phenyl)silane, diphenyldichlorogermane, 4-biphenyldimethylchlorosilane, p-aminophenyltrimethoxysilane, 4-(2-(triethoxysilyl)ethyl)pyridine and (9)-anthracenyltrimethoxysilane.

30 Example 34 includes the subject matter of Examples 26-33, wherein converting the barrier layer precursor materials to a graphitic barrier layer is accomplished by subjecting the barrier layer precursor materials to thermal treatment.

Example 35 includes the subject matter of Example 34, wherein thermal treatment comprises heating the barrier layer precursor materials to at least 600°C.

Example 36 includes the subject matter of Examples 34-35, wherein thermal treatment comprises heating the barrier layer precursor materials to at least 900°C.

Example 37 includes the subject matter of Examples 26-36, wherein converting the barrier layer precursor materials to a graphitic barrier layer occurs at a pressure of greater than 1
5 atm.

Example 38 includes the subject matter of Examples 26-37, wherein converting the barrier layer precursor materials to a graphitic barrier layer occurs at a temperature of at least 400°C and a pressure of greater than 1 atm.

Example 39 includes the subject matter of Examples 26-38, wherein applying the
10 barrier layer precursor materials occurs in the liquid phase.

Example 40 includes the subject matter of Examples 26-38, wherein applying the barrier layer precursor materials occurs in the vapor phase.

Example 41 includes the subject matter of Examples 26-40 and further includes capping the barrier layer precursor materials prior to converting the barrier layer precursor
15 materials to a graphitic barrier layer.

Example 42 includes the subject matter of Example 41, wherein capping the barrier layer precursor materials is accomplished by depositing a hermetic layer onto the barrier layer precursor materials.

Example 43 includes the subject matter of Example 42, wherein the hermetic layer
20 includes silicon nitride.

Example 44 includes the subject matter of Examples 26-43 and further includes treating a surface of the dielectric feature prior to applying the barrier layer precursor materials.

Example 45 includes the subject matter of Example 44, wherein treating a surface of the dielectric feature renders the surface of the dielectric feature hydrophilic.

Example 46 includes the subject matter of Examples 26-45 and further includes
25 activating the barrier layer precursor materials with one or more catalysts.

Example 47 includes the subject matter of Example 46, wherein the one or more catalysts include at least one of the following metals: palladium, nickel, cobalt, ruthenium, platinum, gold and silver.

Example 48 includes the subject matter of Examples 26-47, wherein after converting
30 the barrier layer precursor materials to a graphitic barrier layer the electrically conductive feature is removed and a separate electrically conductive feature is applied to the graphitic barrier layer.

Example 49 includes the subject matter of Examples 26-48 and further includes incorporating the graphitic barrier layer into an integrated circuit device.

Example 50 is an apparatus configured to perform the subject matter of one or more of Examples 26-49.

Example 51 is an integrated circuit device formed by the subject matter of any of Examples 26-49.

5 The foregoing description of example embodiments of the present disclosure has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the present disclosure to the precise form disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the present disclosure be limited not by this detailed description, but rather by the claims appended hereto.

10

CLAIMS

What is claimed is:

1. An integrated circuit device, comprising:
an interlayer dielectric (ILD) feature;
an electrically conductive interconnect feature; and
5 a graphitic barrier layer positioned between the dielectric feature and the electrically conductive interconnect feature, the graphitic barrier layer having a maximum thickness of less than 2 nanometers.
2. The device of claim 1, wherein the graphitic barrier layer has a maximum thickness of less than 1 nanometer.
- 10 3. The device of claim 1, wherein the graphitic barrier layer comprises at least 5% graphene by weight based on the weight of the graphitic barrier layer.
4. The device of claim 1, wherein the graphitic barrier layer comprises at least 25% graphene by weight based on the weight of the graphitic barrier layer.
5. The device of any one of claims 1-4, wherein the thickness of the graphitic barrier
15 layer is substantially uniform, such that the thinnest part of the layer is within 35% of the thickest part of the layer.
6. The device of any one of claims 1-4, wherein the thickness of the graphitic barrier layer is substantially uniform, such that the thinnest part of the layer is within 20% of the thickest part of the layer.
- 20 7. The device of claim 1, wherein the graphitic barrier layer comprises at least one graphene monolayer.
8. An integrated circuit device, comprising:
an interlayer dielectric (ILD) feature;
an electrically conductive interconnect feature; and
25 a graphitic barrier layer positioned between the dielectric feature and the electrically conductive interconnect feature, wherein the graphitic barrier layer has a thickness that is substantially uniform, such that the thinnest part of the layer is within 35% of the thickest part of the layer.

9. The device of claim 8, wherein the thinnest part of the graphitic barrier layer is within 20% of the thickest part of the graphitic barrier layer.

10. The device of claim 8, wherein the graphitic barrier layer has a maximum thickness of less than 2 nanometers.

5 11. The device of claim 8, wherein the graphitic barrier layer has a maximum thickness of less than 1 nanometer.

12. The device of claim 8, wherein the graphitic barrier layer comprises at least 5% graphene by weight based on the weight of the graphitic barrier layer.

10 13. The device of claim 8, wherein the graphitic barrier layer comprises at least 25% graphene by weight based on the weight of the graphitic barrier layer.

14. The device of claim 8, wherein the graphitic barrier layer comprises at least one graphene monolayer.

15. A mobile computing device comprising the device of any one of claims 1-4 and 7-14.

15 16. A method of producing a graphitic barrier layer, the method comprising:
forming a dielectric feature;
applying barrier layer precursor materials to the dielectric feature;
depositing an electrically conductive feature over the barrier layer precursor materials; and
20 converting the barrier layer precursor materials to a graphitic barrier layer.

17. The method of claim 16, wherein the barrier layer precursor materials comprise self-assembling compounds.

18. The method of claim 16, wherein the barrier layer precursor materials comprise self-assembled monolayers.

25 19. The method of claim 16, wherein the barrier layer precursor materials comprise hydrocarbon-based self-assembled monolayers.

20. The method of claim 16, wherein converting the barrier layer precursor materials to a graphitic barrier layer is accomplished by subjecting the barrier layer precursor materials to thermal treatment.

21. The method of claim 16, wherein converting the barrier layer precursor materials
5 to a graphitic barrier layer occurs at a pressure of greater than 1 atm.

22. The method of claim 16, wherein applying the barrier layer precursor materials occurs in the liquid phase.

23. The method of claim 16, wherein applying the barrier layer precursor materials occurs in the vapor phase.

10 24. The method of claim 16, further comprising activating the barrier layer precursor materials with one or more catalysts.

25. An integrated circuit device produced by the method of any one of claims 16-24.

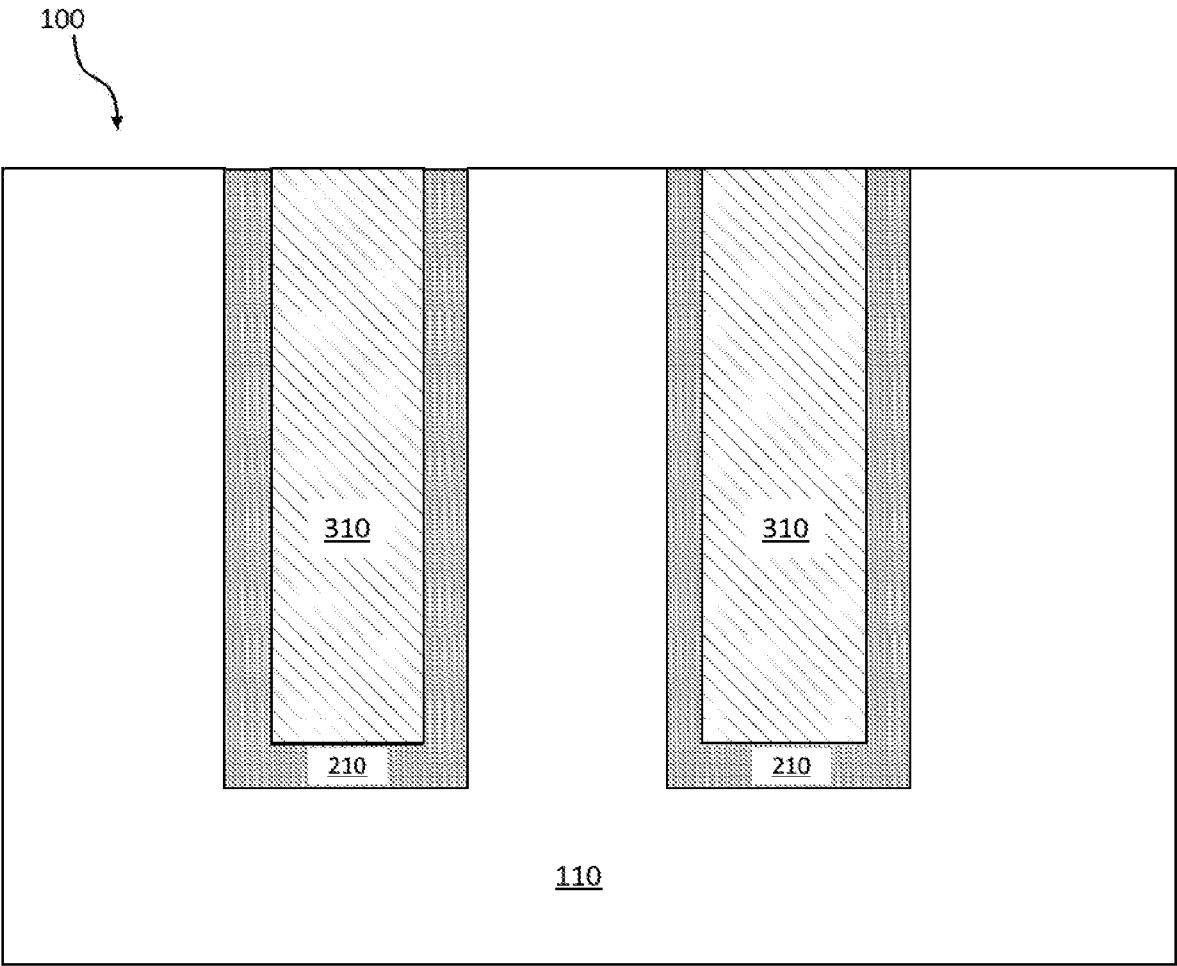


FIG 1

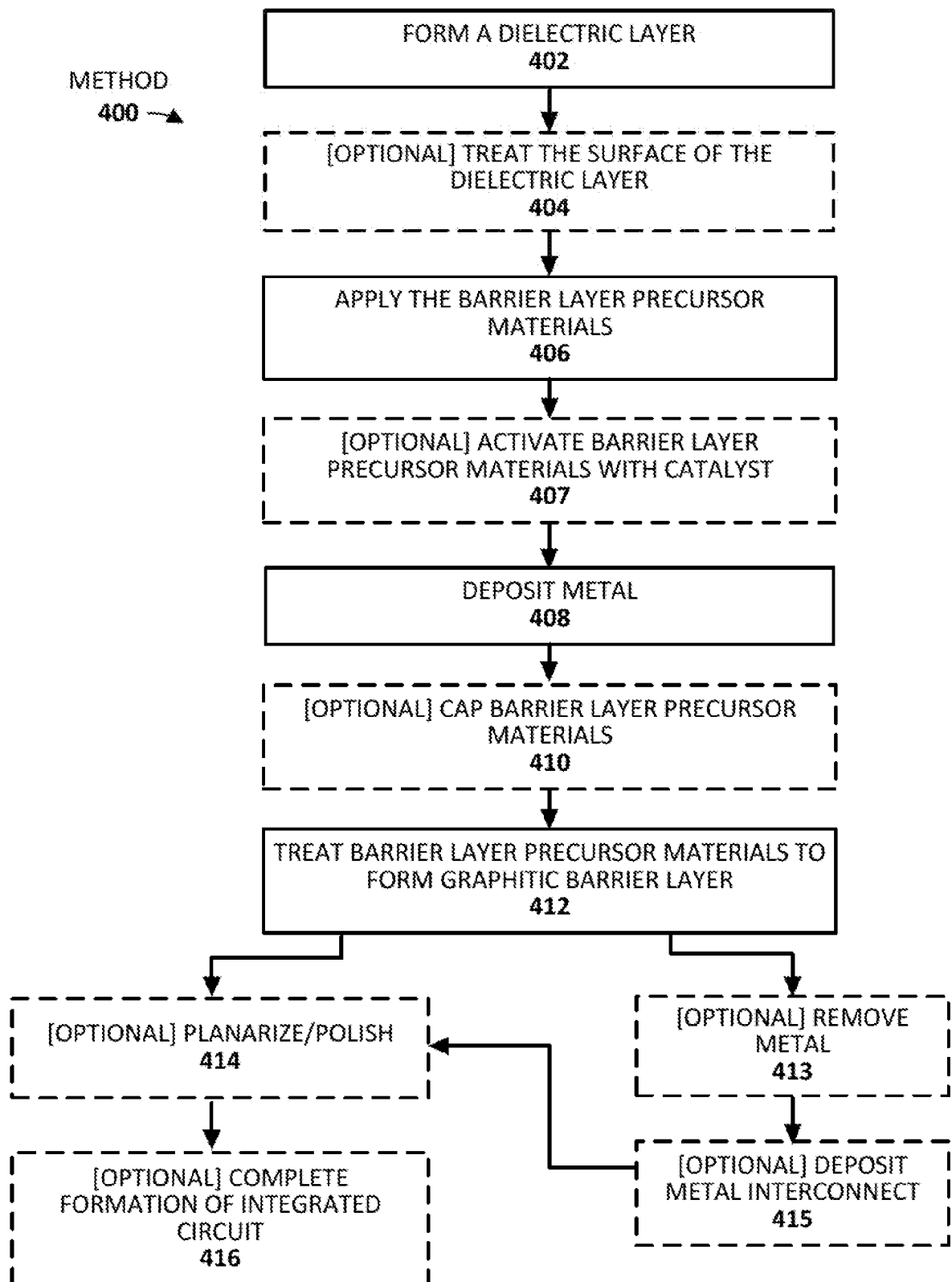


FIG 2

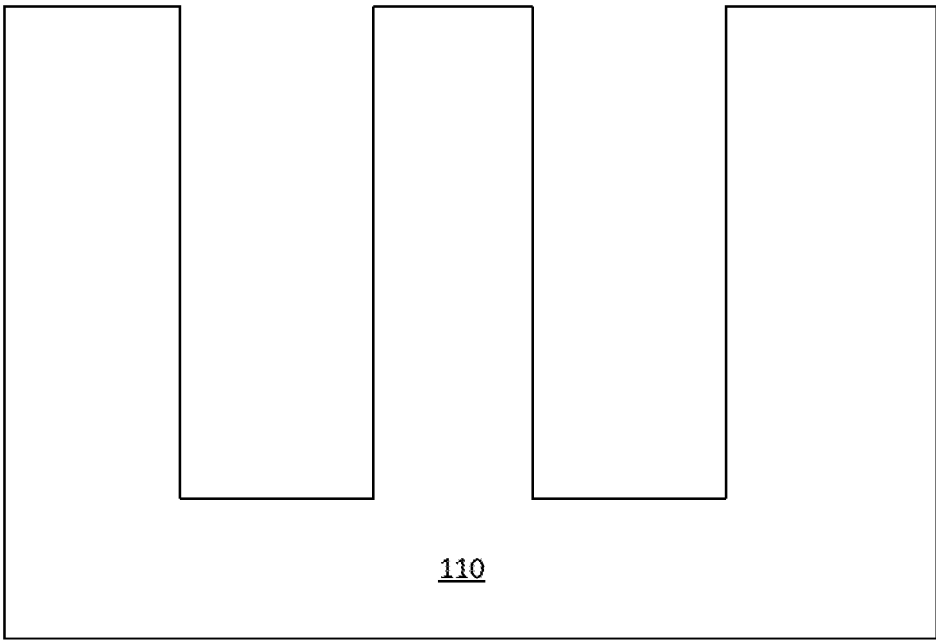


FIG 3A

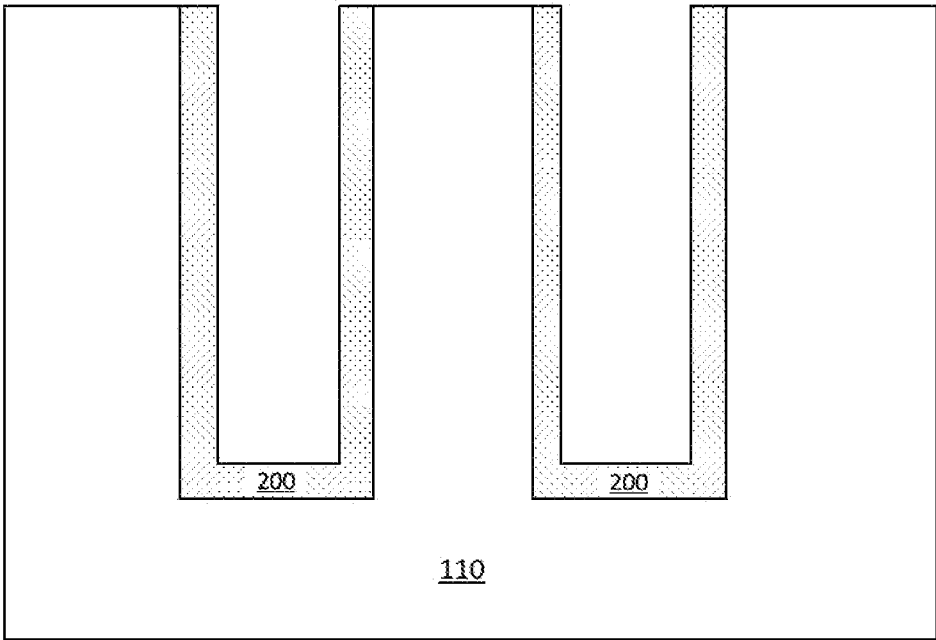


FIG 3B

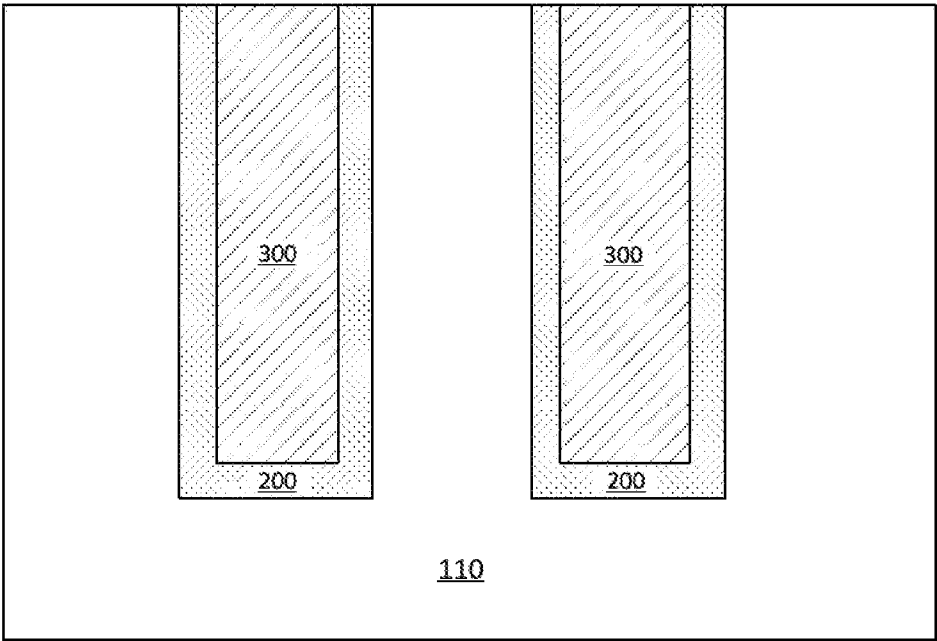


FIG 3C

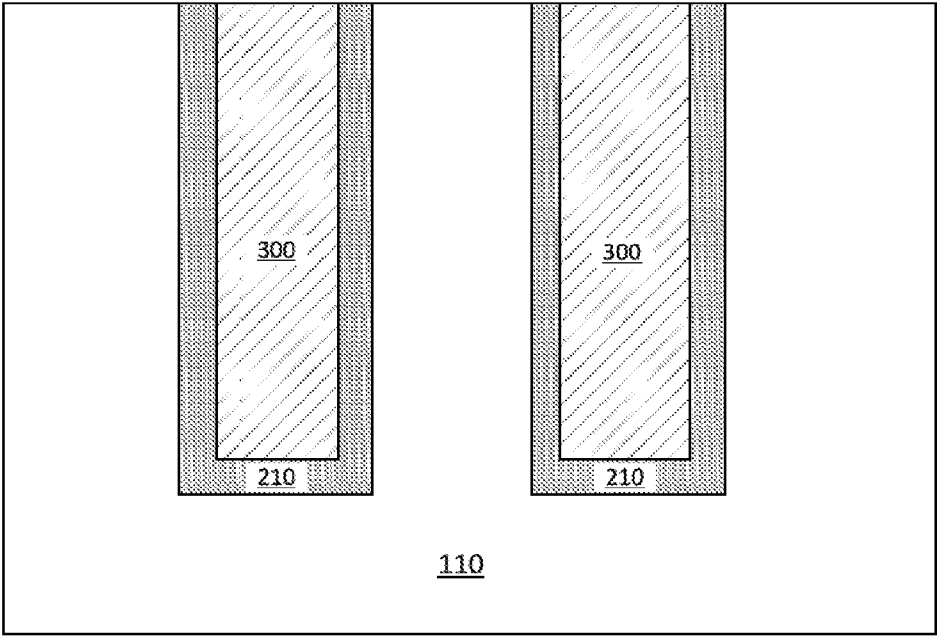


FIG 3D

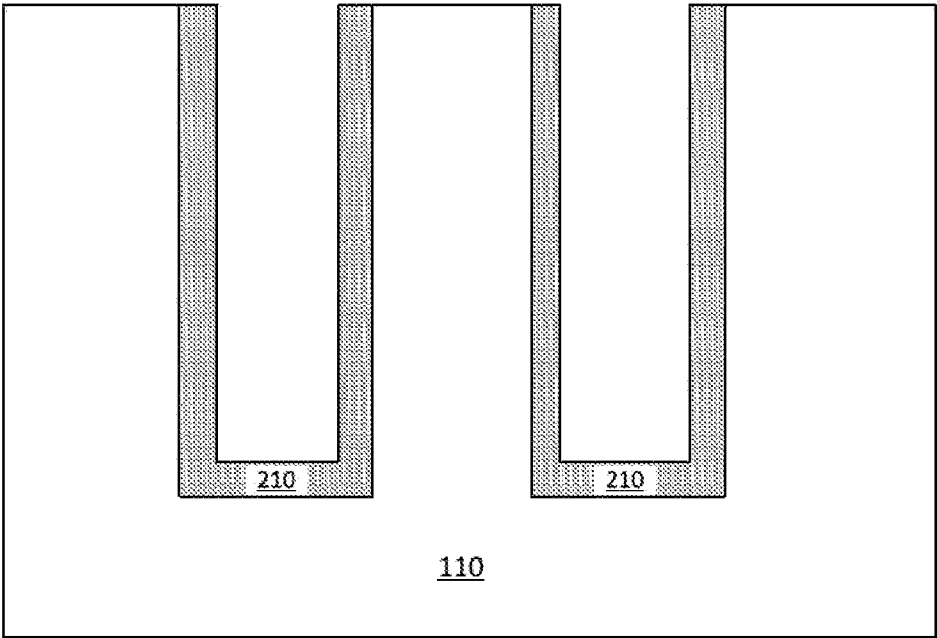


FIG 3E

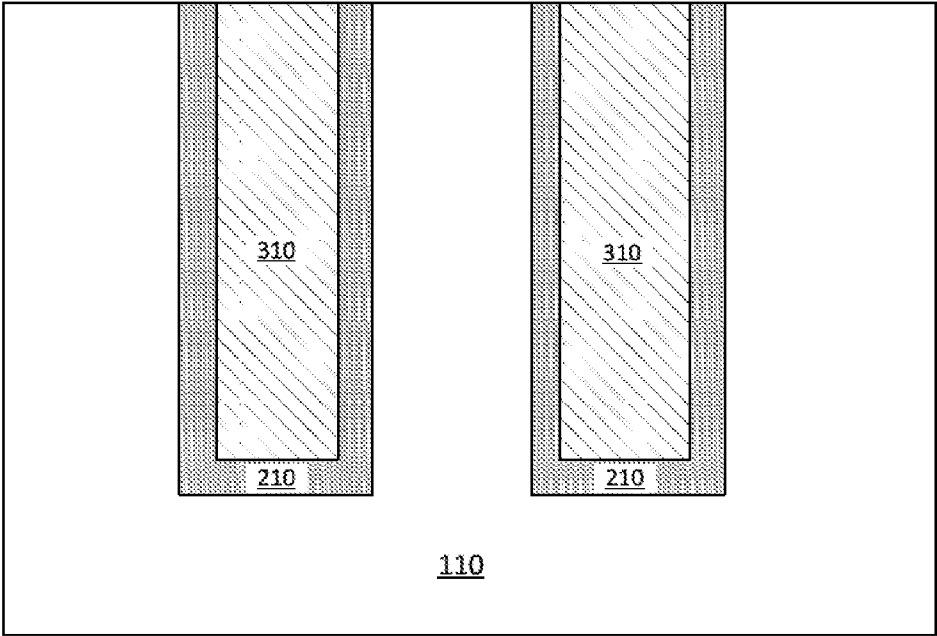


FIG 3F

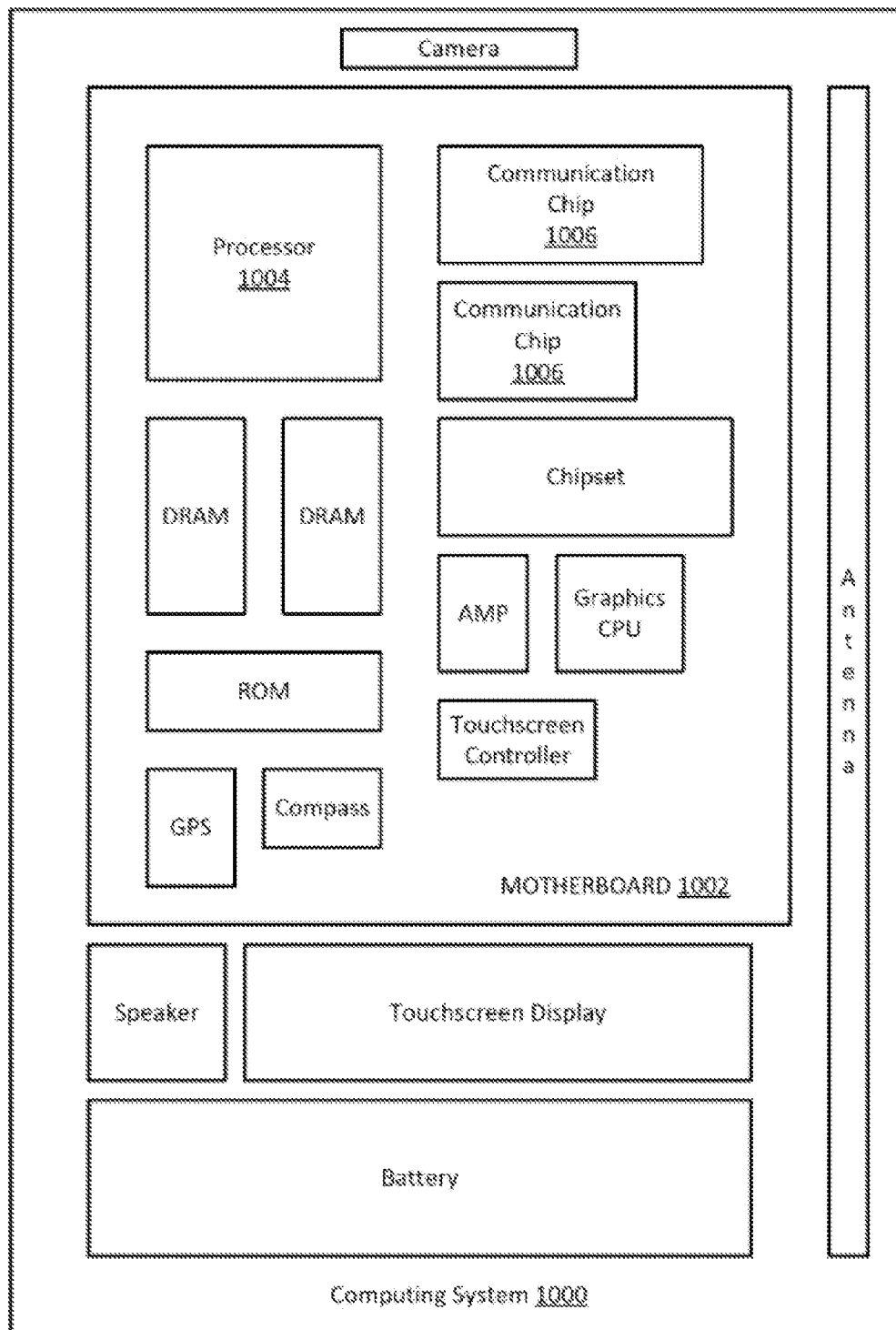


FIG 4

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/768(2006.01)i, H01L 21/31(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; H01L 23/535; H01L 21/4763; H01L 29/06; H01L 29/74; H01L 29/16; H01L 21/283; G11C 11/00; H01L 21/31

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: dielectric, layer, interconnect, graphene, barrier

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0106561 A1 (INTERMOLECULAR, INC.) 17 April 2014 See abstract, paragraphs [0053]-[0066] and figures 5-11.	1-16, 20, 22-25
Y		17-19, 21
Y	US 2013-0099195 A1 (MEMC ELECTRONIC MATERIALS, INC. et al.) 25 April 2013 See abstract, paragraphs [0035], [0040].	17-19
Y	US 2009-0257270 A1 (APRIL D. SCHRICKER et al.) 15 October 2009 See abstract, paragraphs [0027], [0032] and figure 1.	21
A	US 2012-0139114 A1 (JOHN HONGGUANG ZHANG et al.) 07 June 2012 See abstract, paragraphs [0011]-[0014] and figures 1A-2C.	1-25
A	US 2007-0018195 A1 (WALTER HARTNER et al.) 25 January 2007 See abstract, paragraphs [0065]-[0077] and figure 1.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 June 2016 (22.06.2016)

Date of mailing of the international search report

22 June 2016 (22.06.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/052147

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