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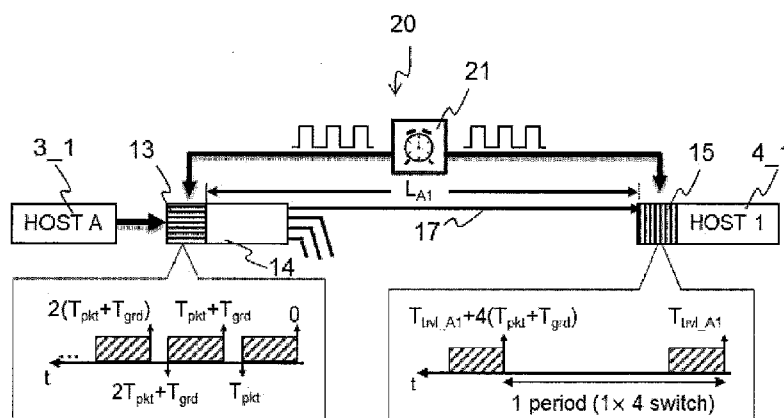
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(54) Title: SWITCHING SYSTEM, OPTICAL PACKET TRANSMISSION APPARATUS, AND METHOD OF GENERATING OPTICAL PACKET

[Fig. 5]



(57) Abstract: A switching system (10) according to this invention includes a plurality of optical transmitters (13) configured to convert an input electric packet into an optical packet and transmit the optical packet, a plurality of optical receivers (15) configured to receive the optical packet and convert the optical packet into an electric packet, an optical switch (14) arranged between the plurality of optical transmitters and the plurality of optical receivers and configured to transmit the optical packet input from the optical transmitter to any one of the plurality of optical receivers, and a clock unit (21) configured to transmit a clock signal having a clock phase to the optical transmitter and the optical receiver, wherein the clock phase of the optical transmitter is corrected based on a clock phase of the optical packet received by the optical receiver and the clock phase of the optical receiver. Accordingly, this invention can provide a switching system which suppresses collision between optical signals.

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Description

Title of Invention: SWITCHING SYSTEM, OPTICAL PACKET TRANSMISSION APPARATUS, AND METHOD OF GENERATING OPTICAL PACKET

Technical Field

[0001] The present invention relates to a switching system, an optical packet transmission apparatus, and a method of generating an optical packet, all of which perform switching while suppressing packet collision.

Background Art

[0002] In order to cope with a communication demand highly required in different application domains such as telephone communication and data communication, the bandwidth (bit/sec) of a transmission signal has been greatly increased. Since optical switching can perform switching without converting an optical signal into an electric signal, it can cope with an increase in bandwidth, that is, the communication amount.

[0003] In optical switching, optical signals simultaneously sent to the same transmission destination are affected by collision. In conventional electric signal switching, a mechanism for performing buffer processing of data to prevent signal collision is used.

Citation List

Patent Literature

[0004] PTL 1: Japanese Patent No. 3878112

Summary of Invention

Technical Problem

[0005] However, in optical switching, a mechanism for performing buffer processing of optical data to prevent optical signal collision has not been implemented yet. For this reason, a switching system including a mechanism for preventing optical signal collision in place of the mechanism for performing buffer processing is necessary.

Solution to Problem

[0006] In order to solve the above problem, a switching system according to the present invention includes a plurality of optical transmitters configured to convert an input electric packet into an optical packet and transmit the optical packet, a plurality of optical receivers configured to receive the optical packet and convert the optical packet into an electric packet, an optical switch arranged between the plurality of optical transmitters and the plurality of optical receivers and configured to transmit the optical packet input from the optical transmitter to any one of the plurality of optical receivers, and a clock unit configured to transmit a clock signal having a clock phase to the

optical transmitter and the optical receiver, wherein the clock phase of the optical transmitter is corrected based on a clock phase of the optical packet received by the optical receiver and the clock phase of the optical receiver.

[0007] In addition, an optical packet transmission apparatus according to the present invention is an optical packet transmitting apparatus that receives a second electric packet next to a first electric packet, converts the respective packets into optical packets, and transmits the optical packets to an optical receiver based on a clock signal, including an optical transmitter configured to receive the clock signal and store a clock phase of the clock signal, convert the first electric packet into a first optical packet, demultiplex the first optical packet by the number of optical receivers to which the first optical packets are transmitted, and transmit each of the demultiplexed first optical packets in the clock phase, receive, from the optical receiver, a phase difference between a clock phase of the demultiplexed first optical packet received by the optical receiver and a clock phase stored in the optical receiver, and convert the second electric packet into a second optical packet, demultiplex the second optical packet by the number of optical receivers to which the second packets are transmitted, and transmit each of the demultiplexed second optical packets in the phase-corrected clock phase, and an optical switch configured to assign time slots in the demultiplexed first optical packets and the demultiplexed second optical packets, and set guard times before and after a boundary of each of the time slots.

[0008] In addition, a method of generating an optical packet according to the present invention is a method of generating, based on a clock signal, an optical packet to be transmitted from an optical transmitter to an optical receiver via an optical switch, including a step of causing the optical transmitter to receive the clock signal and store a clock phase of the clock signal, a step of causing the optical transmitter to demultiplex the first optical packet and transmit each demultiplexed first optical packet in the clock phase, a step of causing the optical switch to assign time slots to the demultiplexed first optical packets, respectively, and transmit the demultiplexed first optical packets, a step of causing the optical receiver to measure a phase difference between a clock phase of each demultiplexed first optical packet and a clock phase stored in the optical receiver, a step of causing the optical receiver to transmit the phase difference to the optical transmitter, a step of causing the optical transmitter to correct a clock phase stored in the optical transmitter by using the phase difference, and a step of causing the optical transmitter to demultiplex the second optical packet and transmit each demultiplexed second optical packet in the corrected clock phase.

[0009] In addition, a method of generating an optical packet according to the present invention is a method of generating an optical packet to be transmitted to an optical receiver from an electric packet input to the optical transmitter by using the optical

transmitter and an optical switch, including a step of causing the optical transmitter to convert the electric packet into an optical packet, a step of causing the optical transmitter to demultiplex the optical packet by the number of optical receivers to which the optical packets are transmitted, a step of causing the optical switch to assign time slots to the demultiplexed optical packets, respectively, and a step of causing the optical switch to set guard times before and after a boundary of the time slots between the demultiplexed optical packets.

Advantageous Effects of Invention

[0010] According to the present invention, there are provided a high-speed lower power consumption switching apparatus and a switching method.

Brief Description of Drawings

[0011] [Fig.1]Fig. 1 is a block diagram showing the arrangement of a switching system according to the first embodiment of the present invention;
[Fig.2]Fig. 2 is a view for explaining the operation of the switching system according to the first embodiment of the present invention;
[Fig.3A]Fig. 3A is a view for explaining the operation of the switching system according to the first embodiment of the present invention;
[Fig.3B]Fig. 3B is a view for explaining the operation of the switching system according to the first embodiment of the present invention;
[Fig.3C]Fig. 3C is a view for explaining the operation of the switching system according to the first embodiment of the present invention;
[Fig.3D]Fig. 3D is a view for explaining the operation of the switching system according to the first embodiment of the present invention;
[Fig.4]Fig. 4 is a view for explaining the operation of the switching system according to a modification of the first embodiment of the present invention;
[Fig.5]Fig. 5 is a block diagram showing the arrangement of a switching system according to the second embodiment of the present invention;
[Fig.6]Fig. 6 is a view for explaining the operation of the switching system according to the second embodiment of the present invention;
[Fig.7]Fig. 7 is a flowchart showing a method of generating an optical packet in the switching system according to the second embodiment of the present invention;
[Fig.8]Fig. 8 is a view for explaining the operation of a switching system according to a modification of the second embodiment of the present invention;
[Fig.9]Fig. 9 is a block diagram showing the arrangement of a switching system according to the third embodiment of the present invention;
[Fig.10]Fig. 10 is a flowchart showing a method of generating optical packet in the switching system according to the third embodiment of the present invention; and

[Fig.11]Fig. 11 is a view for explaining the operation of the switching system according to the third embodiment of the present invention.

Description of Embodiments

[0012] (First Embodiment)

A switching system according to the first embodiment of the present invention will be described with reference to Figs. 1 to 4.

[0013] (Arrangement of Switching System)

As shown in Fig. 1, a switching system (packet switching system) 10 according to an embodiment sequentially includes input ports 11, input blocks 12, optical transmitters 13, an optical switch 14, optical receivers 15, and output ports 16. The optical switch 14 and the optical receiver 15 are connected to an optical fiber 17. In addition, an optical multiplexer is provided before in the former stage of the optical receiver 15. The multiplexer may multiplex and receive a plurality of optical signals (not shown).

[0014] The input block 12 is an electronic switching unit which is a low-radix switching block (chiplet).

[0015] The input ports 11 of the switching system 10 are branched into m groups, and each group is connected to the input block 12.

[0016] The input block 12 processes an input packet.

[0017] The optical transmitter 13 converts an electric signal output from the input block 12 into an optical signal and outputs the optical signal.

[0018] The optical switch 14 cross-connects the input block 12 and each group of the output port 16 based on an time slot operation (to be described later).

[0019] An optical signal output from the optical switch 14 propagates through the optical fiber 17 and is transmitted to the optical receiver 15.

[0020] The optical receiver 15 converts the optical signal output from the optical switch 14 into an electric signal.

[0021] The output ports 16 of the switching system 10 are divided into m virtual groups.

[0022] In the switching system 10, the same block is connected to different groups of the different output ports 16 in order, one at a time, and each connection takes place for a time slot (to be described later) where T is a duration of a packet input to the switching system 10.

[0023] Here, the time slot is $\Delta t = T/m$.

[0024] The same output port 16 of the input block 12 is always connected to the same output port 16 of the virtual group. In this case, both the ports have the same index inside the port groups.

[0025] (Operation of Switching System)

The operation of the switching apparatus (packet switch) 10 according to this em-

bodiment will be described with reference to Fig. 2.

[0026] Fig. 2 illustrates the basic operation of the switching system 10 which executes non-block processing using an example of a 4 x 4 switch. This switching system 10 is based on a time slot operation to be described below.

[0027] First, a packet is switched for each input group. In this case, arbitration is executed within the input packet of the same input group. Since this arbitration is executed for the small number of ports and a low communication amount, the operation can be executed fast without requiring a long time.

[0028] An electric packet 1 input to the switch has a bandwidth BW (bit/sec) and a duration T. The desired output port 16 to which the packet is transmitted is set.

[0029] In the switching system 10, a packet switching operation to any one of the four output ports 16 is complete within the time T. This is because if a time of T or longer is required for the switching of a single packet, the next input packet is blocked and a continuous switching delay is accumulated.

[0030] In order to match the input packet 1 with the time slot, the optical transmitter 13 compresses the input packet 1 by a factor (in this case, 4) equal in number to the number of ports (that is, the number of optical receivers to which packets are transmitted). That is, the duration of the input packet is divided by a factor equal in number of the number of ports and becomes $T/4$. In addition, the bandwidth is multiplied by the same factor and becomes $4BW$ in order to retain the packet data contents.

[0031] As described above, an optical input packet 2 is generated by satisfying the above conditions.

[0032] Next, the optical switch 14 distributes the respective optical input packets 2 to the desired output ports 16 using periodic time slots. In this case, the periodic operation of the switch is divided into four time slots.

[0033] The duration Δt of each time slot is $T/4$.

[0034] The distribution (switching) of the optical input packets 2 is repeatedly executed for each time slot in accordance with a sequence formed by steps S1 to S4 (to be described later).

[0035] Finally, the optical receiver 15 converts the packet into an electric packet, and the switching system 10 outputs the electric packet in a predetermined duration. In other words, the data rate of the signal output from the switching system 10 is equal to the data rate of the input signal.

[0036] In the packets arriving in different time slots whose time difference is reduced, the data rate is changed to the first data rate. This change is performed in the arrival order of packets. In addition, the priority of the change may be set by another arbitration.

[0037] The switching operation in the above optical switch 14 will be described with

reference to Figs. 3A to 3D. Figs. 3A to 3D show examples of a series of switching operations in steps S1 to S4, respectively.

- [0038] In the switching system 10, packets are input to four ports 11_1 to 11_4, respectively. The packet (packet C) input to the port 11_3 has the desired output port as a port 16_3 and has the highest priority.
- [0039] The packets (packets A and D) input to ports 11_1 and 11_4 have the desired ports as ports 16_2 and 16_1, respectively, and have the second highest priority.
- [0040] The packet (packet B) input to the port 11_2 has the desired output port as a port 16_4 and has the third highest priority.
- [0041] First, since the packet C has the highest priority, the packet C is transmitted to the output port 16_3 in a duration of the first time slot (step S1 and Fig. 3A).
- [0042] Since the packets A and D have the second highest priority, they are simultaneously transmitted to the output ports 16_2 and 16_1 in a duration of the second time slot (step S2 and Fig. 3B). In this case, since the packets A and D are transmitted to different output ports, no collision occurs.
- [0043] Next, since the packet (packet B) input to the port B has the third highest priority, it is transferred to the output port 16_4 in a duration of the third time slot (step S3 and Fig. 3C).
- [0044] Finally, since transmission of the packets A to D is complete in the previous step (step S3), switching is not executed in a duration of the fourth time slot (step S4 and Fig. 3D).
- [0045] Here, the durations of the first time slot, the second time slot, the third time slot, and the fourth time slot are shown by Δt_1 , Δt_2 , Δt_3 , and Δt_4 , respectively.
- [0046] As described above, if the operation cycle (the four steps) is complete, all the input packets are simultaneously switched to desired output ports by the non-blocking method.
- [0047] In this switching operation, in all the steps, as shown in Figs. 3A to 3D, the respective output ports 16 are connected to only one input port 11. In addition, the input port 11 is connected to the desired output port 16. In switching of the packet input to the input port 11, the packet is arranged in a correct (accurate) time slot (the divided duration).
- [0048] In addition, the optical receiver 15 in the switching system 10 can be operated in correspondence with this burst mode transmission.
- [0049] When the switching system 10 is formed by four 1 x 4 switching units corresponding to the different input ports 11, a high-speed 4 x 4 optical switch device can be easily implemented. In the 4 x 4 optical switch device, a time for making one switch form (for example, Fig. 3A) to transition to another switch form (for example, Fig. 3B) is very short as compared with the input packet duration.

- [0050] For example, if it is assumed that the transition time can be neglected, the transition time in an actually usable technique can be reduced to 10 psec and is very short as compared with 100 Gb/s Ethernet packet having a duration of, for example, 120 nsec.
- [0051] In addition, if a short guard time is set between the packets input to the same input port 11 to avoid the data loss between the switching operations, this guard time is less than 1/10 of the input packet duration. The transition time is short to fall within the guard time.
- [0052] (Effect)
- An effect of the switching system 10 according to this embodiment will be described below.
- [0053] In a normal electric switch, an input packet passes through an input port of the switch. The destination and the priority of the input packet are tested, and then a concentrated arbitration is performed. A packet to be transmitted first is determined from all the packets having the same output port as the destination.
- [0054] Execution of the concentrated arbitration process is complicated with an increase in the number of switch ports and the throughput. As a result, the communication latency and the power consumption increase.
- [0055] On the other hand, since switching system can be performed without executing the concentrated arbitration requiring a long time according to the switching apparatus (packet switch) of this embodiment, the communication latency and the power consumption can decrease.
- [0056] Since the optical switch is in charge of part of the switching processing, the switching capacity can be increased with the power consumption lower than that of an ASIC made of a CMOS transistor.
- [0057] In addition, since the chiplet is used for the input block 12, the area occupied by the input block 12 can be reduced. As a result, the entire area of the packet switch (chip) will not be increased even if an optical-electrical interface is mounted. Accordingly, the throughput (processing capacity) of the switch can be increased by mounting the optical-electrical interface without changing the chip area. In addition, by using the chiplet, the power consumption can be reduced.
- [0058] In addition, the contention between the ports of the same block can be prevented, and non-blocking processing can be executed.
- [0059] (First Modification)
- A switching system according to the first modification of the first embodiment of the present invention will be described with reference to Fig. 4. The arrangement of a switching system 10_2 according to this modification is the same as that of the first embodiment.
- [0060] (Operation of Switching System)

The operation of the switching system 10_2 according to this modification will be described below.

[0061] In the switching system 10_2, the packets (the packets A to D) are input to the four ports 11_1 to 11_4, respectively. The packets A to D have the same desired output port (16_2) and are assigned in the order of B, A, D, and C.

[0062] First, since the packet B has the highest priority, the packet B is transmitted to the output port 16_2 in the duration of the first time slot (step S1).

[0063] Next, since the packet A has the second highest priority, the packet A is transmitted to the output port 16_2 in the duration of the second time slot (step S2).

[0064] Next, since the packet D has the third highest priority, the packet D is transmitted to the output port 16_2 in the duration of the third time slot (step S3).

[0065] Finally, since the packet C has the fourth highest priority, the packet C is transmitted to the output port 16_2 in the duration of the fourth time slot (step S4).

[0066] As described above, if the operation cycle (the four steps) is complete, all the input packets are simultaneously switched to desired output ports by the non-blocking method. In this case, since the packets A to D are transmitted in the different time slots, no collision occurs.

[0067] As described above, in the switching system 10_2, all the input ports to be transmitted to the same output port are correctly (accurately) switched to this output port in the time T.

[0068] (Effect)

The switching system 10_2 according to this modification has the following effect in addition to the effect of the first embodiment.

[0069] When simultaneously transmitting a plurality of packets to the same destination in the conventional packet switch, parallel optical receivers equal in number of the number of packets are required.

[0070] In the switching system 10_2, the compact copies of the input packets are created at a high data rate, and the compact packets are demultiplexed and transmitted in short time slots. Transmission of the packets to the same destination can be executed within a short time using time interleaving as compared with the actual packet input interval.

[0071] According to the switching system of this modification, since the packets can be transmitted to the same output port without executing the concentrated arbitration requiring a long time, thereby reducing the communication latency and the power consumption.

[0072] (Second Embodiment)

A switching system according to the second embodiment of the present invention will be described with reference to Figs. 5 to 7.

[0073] (Arrangement of Switching System)

As shown in Fig. 5, a switching system 20 according to this embodiment includes an optical transmitter 13, an optical switch 14, an optical fiber 17, an optical receiver 15, and a clock unit 21. The basic arrangement of the switching system 20 except the clock unit 21 is the same as in the first embodiment.

[0074] A packet is input from a host A (3_1) to the optical transmitter 13, output from the optical receiver 15, and transmitted to a host 1 (4_1).

[0075] (Operation of Switching System)

The operation using a common clock signal in the switching system 20 according to this embodiment will be described with reference to Fig. 5.

[0076] In the switching system 20, the common clock signal is transmitted from the clock unit 21 to the optical transmitter 13 and the optical receiver 15. Alternatively, the common clock signal may be transmitted to the optical switch 14. In this case, the common clock signal to be transmitted includes a copy almost equivalent to the common clock signal. The copy almost equivalent to the common clock signal includes an equivalent copy and includes a range where the function of a clock signal (to be described later) in the switching system 20 can be executed.

[0077] A single host is connected to each switch port. For example, a 25-Gb/s packet generated by a source host is converted into a 100-Gb/s optical packet using the optical transmitter 13.

[0078] At the optical transmitter 13, a packet generated by the source host A (3_1) is demultiplexed by a guard time T_{grd} , and converted into two continuous packets. Then the packets are output.

[0079] If the time of the start end of the first packet in a duration T_{pkt} of the switched packet is given as zero, the terminal end of the first packet is T_{pkt} , and the time of the start end of the next packet is $T_{\text{pkt}} + T_{\text{grd}}$, and its terminal end is $2T_{\text{pkt}} + T_{\text{grd}}$.

[0080] For example, a guard time equivalent to 2% of the duration of the optical packet is set. The minimum value of T_{grd} will be described later.

[0081] If it is assumed that the duration of the switched packet, the guard time, and the number of switched packets are given as T_{pkt} , T_{grd} , and N , respectively, packets are received by the optical receiver 15 in a period N times ($T_{\text{pkt}} + T_{\text{grd}}$). For example, when receiving four switched packets, the period is four times ($T_{\text{pkt}} + T_{\text{grd}}$).

[0082] If the optical receiver 15 receives a packet data bit, a bit timing notification is requested. Conventionally, a process for detecting the accurate timing of the input bit and recovering the input packet clock on the reception side requires a long time as compared with the short duration of the assumed packet.

[0083] By sharing an optical clock between the optical transmitter 13 and the optical receiver 15, the process requiring a long time can be prevented.

[0084] Table 1 shows setting values in the switching system 20.

[0085] [Table 1]

Bandwidth of input packet	BW_{in}	25 Gb/s
Bandwidth of switched packet	BW_{sw}	100 Gb/s
Duration of switched packet	T_{pkt}	120 ns
Guard time (2%) of packet	T_{gtd}	2.4 ns
Link length between host A and host 1	L_{A1}	10 m
Travel time between host A and host 1	T_{trvl_A1}	50 ns

[0086] Fig. 6 shows the mode of clock phases in the switching system 20.

[0087] Even if the clock is generally shared, a clock phase 211 of the input packet does not match a phase 212 of the local copy of the clock shared on the reception side. A difference (mismatch) of the initial clock phase can be continuously corrected if the optical path between the optical transmitter 13 and the optical receiver 15 has a time invariant system.

[0088] Here, the difference of the clock phase is shown by $\Delta\phi$.

[0089] However, for example, if packets from the optical transmitter 13 can reach the same optical receiver 15 via unknown randomly selected optical paths, the optical paths between the optical transmitter 13 and the optical receiver 15 cannot be phase-adjusted because they do not have the time variant system.

[0090] In the switching system 20, the clock phase of the input packet can match the clock phase of the optical receiver 15 as the transmission destination (213 in Fig. 6) based on, for example, a phase cache method (K. A. Clark et.al, "Synchronous sub nanosecond clock and data recovery for optically switched data centers using clock phase caching," in Nature Electronics, vol.3, July 2020.)

[0091] Fig. 7 shows a flowchart of optical packet transmission/reception including generation of an optical packet using a clock signal in the switching system 20.

[0092] The clock signal is transmitted in advance between the optical transmitter 13 and the optical receiver 15, and a phase (clock phase) of the clock signal is cached (stored) (step S11).

[0093] First, the optical transmitter 13 demultiplexes the optical packet (the first optical packet) and transmits the demultiplexed optical packet (the first optical packet) to the optical switch 14 using the cached clock phase (step S12).

[0094] Next, the optical switch 14 assigns time slots to the respective demultiplexed optical packets (the first optical packets) and transmits these packets to the optical receiver 15 (step S13).

[0095] Next, the optical receiver 15 measures the phase difference between the clock phase

of the optical packet (the first optical packet) received from the optical switch 14 and the clock phase stored in the optical receiver 15 (step S14).

[0096] Next, the optical receiver 15 transmits the measured phase difference to the optical transmitter 13 (step S15).

[0097] Next, the optical transmitter 13 corrects and updates the cached clock phase using the received phase difference (step S16).

[0098] Next, the optical transmitter 13 transmits the next optical packet (the second optical packet) to the optical switch 14 using the updated cached clock phase (step S17).

[0099] Next, the optical switch 14 assigns the time slot to the optical packet (the second optical packet) and transmits it to the optical receiver 15 (step S18).

[0100] Finally, the optical receiver 15 receives the optical packet (the second optical packet). As a result, the phase difference becomes zero (step S19).

[0101] As described above, the optical transmitter 13 corrects the phase of the data transmitted to the predetermined optical receiver 15 by continuously using the cached clock phase. In this case, in the same optical transmitter 13, different phase correction values are used for the respective destinations.

[0102] According to this embodiment, by sharing the clock signal, the common time reference can be set so as to adjust the data communication in the set time slot without causing collision. In addition, the data in the burst mode can be received without requiring a long time to recover the clock data.

[0103] (Second Modification)

In a switching system 20_1 according to the second modification of this embodiment, a spatial optical fiber having a low temperature sensitivity is used as the optical fiber 17. Other arrangements are the same as in the second embodiment.

[0104] The optical fiber 17 is a commercially available optical fiber, covered with a predetermined coating, and has a low temperature sensitivity of 3.7 ps/km/k°. In addition, the length of the optical fiber 17 is about 10 m.

[0105] In the switching system 20_1, a variation in environmental temperature influences the refractive index of the optical fiber 17. In a packet to be transmitted, the already adjusted clock phase can change in the optical receiver 15 serving as the destination after the packet propagates through the fiber 17. As a result, a variation (fluctuation) occurs in a travel time of the packet between the hosts.

[0106] In the switching system 20_1, the validity of the value of the corrected cached phase will be examined. In this case, the frequency depends on a fiber length and a temperature variation pattern in the system environment.

[0107] As described above, the switching system 20_1 targets the mutual connection between the hosts arranged at a short distance of about 10 m. A 10-m long spatial

optical fiber having a low temperature sensitivity is used as the optical fiber 17 to suppress a phase change.

- [0108] In this optical fiber (a length of 10 m) 17, a change in travel time of the optical signal at a temperature change of 40°C is less than 1.5 psec. This value is less than 1/10 for a high bit rate (corresponding to T_{baud} of 20 ps) of 50 Gb/s. Since this value is a variation (fluctuation) of a very small single bit duration, the above value can be neglected.
- [0109] Accordingly, for example, if the clock phase is initially adjusted at the activation of the switching system, a long-time operation can be performed without requiring further correction.
- [0110] According to the switching system of this modification, the variation of the clock phase by the temperature change can be suppressed.
- [0111] (Third Modification)
- In a switching system 20_2 according to the third modification of this embodiment, as shown in Fig. 8, the end-to-end optical paths between pairs each formed by the optical transmitter 13 and the optical receiver 15 are made equal to each other. In other words, the lengths of the optical fibers 17 in all combinations each formed by a transmission-side host and a reception-side host (that is, the optical switch 14 and the optical receiver 15) are equal to each other. Other arrangements are the same as in the second embodiment.
- [0112] For example, if each of lengths L_{A1} , L_{A2} , L_{A3} , and L_{A4} of the fibers 17 connecting the host A (3_1) and hosts 1 to 4 (4_1 to 4_4) is about 10 m and includes an error of plus-minus 1 mm, the maximum value of the difference ($T_{\text{trvl_Ai}} - T_{\text{trvl_Aj}}$) of the travel times between the fibers (optical paths) 17 is 10 ps which is very small.
- [0113] In the switching system 20_2, the host unit is connected to the optical switching port and can be arranged regardless of the distance between the hosts.
- [0114] In the switching system 20_2 according to this modification, each time slot can be occupied by only a target packet without a wrong time slot state of another slot. Therefore, even if the host unit is arranged without any limitation, the appropriate operation of the switching system using the time slot can be ensured.
- [0115] According to the switching system of this modification, the host unit can be arranged without any limitation, and the switching system using the time slot can be appropriately operated.
- [0116] According to this modification, since the optical fibers 17 having the same length are connected to the adjacently arranged units, adjustment can be facilitated, and the optical fibers may be bundled as needed.

- [0117] The length of the optical fiber strand can be adjusted at a high resolution by another technique. In this case, if low cost and efficiency in the manufacture of the arranged optical fiber strand are taken into consideration, the resolution can be about plus-minus 1 mm.
- [0118] (Third Embodiment)
A switching system according to the third embodiment of the present invention will be described with reference to Figs. 9 to 11.
- [0119] (Arrangement of Switching System)
As shown in Fig. 9, a switching system 30 according to this embodiment sequentially includes optical transmitters 13, optical switches 14, optical fibers 17, an optical multiplexer 31, an optical receiver 15, and a clock unit 21. The basic arrangement of the switching system 30 except the clock unit 21 is the same as in the first embodiment.
- [0120] (Method of Generating Optical Packet)
A method of generating an optical packet in the switching system 30 according to this embodiment will be described below.
- [0121] Fig. 10 shows a flowchart of the method of generating the optical packet in the switching system 30.
- [0122] For example, as shown in Fig. 9, in the switching system 30, packets are transmitted from host A (3_1) and host D (3_4) to host 1 (4_1) as the destination host.
- [0123] A common clock signal (master) used here is assumed to have an actually used 840-MHz frequency (corresponding to the period of 1.2 nsec).
- [0124] For the packet to be transmitted from host A (3_1), a guard time T_{grd} is set before and after a boundary of the time slots between the packets in the optical switch 14 (to be described later). As a result, if the duration of the switched packet is given as T_{pkt} , and the time of the start end of the first packet is zero, the time of the start end of the next packet is $T_{\text{pkt}} + T_{\text{grd}}$, and the start end of the subsequent packet becomes twice ($T_{\text{pkt}} + T_{\text{grd}}$).
- [0125] Similarly, a packet is transmitted from host D (3_4).
- [0126] At this time, the phase of the common clock in the optical transmitter 13 of host A (3_1) is slightly different from the phase of the common clock of the optical transmitter 13 of host D (3_4).
- [0127] A value $\Delta T_{\text{AD_clock}}$ of this phase difference is about one clock period (1.2nsec) or less.
- [0128] The phase difference of one clock period or more can be perfectly easily detected and corrected (for example, by the time counter).
- [0129] Fig. 11 shows the mode of packet reception in the optical receiver 15 of host 1 (4_1).
- [0130] After the optical receiver 15 of host 1 (4_1) assigns the time slot for the reception (packet A) from host A (3_1), the time slot is assigned to the reception (packet D) from host D (3_4). Subsequently, the time slot is assigned to the reception (packet C) from

host C (3_3).

- [0131] After the packet A, signal-free guard times $T_{\text{grd_1}}$ and $T_{\text{grd_2}}$ are set. More specifically, $T_{\text{grd_1}}$ and $T_{\text{grd_2}}$ are set between the terminal end of the packet A and the start end of the packet D and between the terminal end of the packet D and the start end of the packet C before and after the boundaries (arrows indicated by the solid lines in Fig. 11) of the time slots. In other words, $T_{\text{grd_2}}$ is set at the start end of each packet, and $T_{\text{grd_1}}$ is set at the terminal end of each packet.
- [0132] If the clock phases of host A (3_1) and host D (3_4) perfectly match each other, the packet D (from host D) accurately reaches the light receiver 15 of host 1 (4_1) at the terminal end of guard time T_{grd} .
- [0133] However, since the phase difference generally occurs between the packet A and the packet D, the packet D reaches after the completion of $T_{\text{grd_1}}$ or before the completion of $T_{\text{grd_1}}$. Therefore, even if the packet D reaches as fast as possible, occurrence of the collision with the packet A must be prevented.
- [0134] If the phase clock in the optical transmitter 13 of host D (3_4) is earlier than the phase clock in the optical transmitter 13 of host A (3_1) at the perfectly common clock period, the packet D reaches as fast as possible.
- [0135] The time difference ΔT_{AD} between the terminal end of the packet A and the start end of the packet D is represented by the sum of the differences $\Delta T_{\text{AD_trvl}}$ and $\Delta T_{\text{AD_clock}}$ of the travel times of two packets A and D. In this case, the difference between the travel times of the two packets must also be considered. However, along with the adjustment of all the optical paths, the maximum difference of the travel times can almost be neglected (10ps or less). Therefore, ΔT_{AD} is almost equal to $\Delta T_{\text{AD_clock}}$.
- [0136] If at least the guide time $T_{\text{grd_2}}$ between the packet A and the packet D, that is, $T_{\text{grd_2}}$ at the start end of the packet D is selected to satisfy a condition exceeding the duration of the common clock period, the packet D does not reach within the time slot assigned to the packet A, so that no collision occurs between the packet A and the packet D.
- [0137] If the start end of the packet D falls within $T_{\text{grd_2}}$ even if the packet D reaches earlier, no collision occurs between the packet A and the packet D (a rectangle D1 indicated by a dotted line in Fig. 11).
- [0138] In addition, similarly, collision with the packet C must be prevented even if the packet D reaches as fast as possible. If at least guard time $T_{\text{grd_1}}$ between the packet D and the packet C, that is, if $T_{\text{grd_1}}$ at the terminal end of the packet D is selected to satisfy a condition exceeding the duration of the common clock period, the packet D does not reach within the time slot assigned to the packet C, so collision between the packet D and the packet C does not occur.
- [0139] If the terminal end of the packet D falls within $T_{\text{grd_1}}$ even if the packet D reaches

with a delay, no collision occurs between the packet D and the packet C (a rectangle D2 indicated by a dotted line in Fig. 11).

[0140] As described above, by setting the guard times between the packets to exceed the common clock phase differences between the packets, collision can be prevented between different packets.

[0141] According to this embodiment, by sharing the clock signal and setting the guard time, occurrence of the collision can further be suppressed, and the packet can be switched and transmitted/received.

[0142] According to this embodiment, another method using a burst mode receiver (S. Ibrahim et. al, "Hybrid Optoelectronic Router for Future Optical Packet-Switched Networks", Optoelectronics-Advanced Device Structures, 2017) to receive an input data packet in a burst mode without wasting a long time to execute recovery of the clock data may be used. In this case, the optical clock pulse is generated in synchronism with the input packet in the burst mode. This optical clock is used in an operation of a light-triggered specially designed serial/parallel conversion device.

[0143] According to this embodiment of the present invention, a demultiplexing clock signal is transmitted together with the data signal and may be used on the reception side. By maintaining synchronization between the clock signal and the data signal up to the reception side, the input data can be received fast without requiring an additional process of recovering the clock data.

[0144] The embodiments of the present invention illustrate examples of the structure, size, material, and the like of each constituent component in the arrangements of the switching system and the optical packet transmission apparatus and the method of generating the optical packet. However, the present invention is not limited to this. Any example can be employed as far as the functions of the switching system and the optical packet transmission apparatus and the method of generating the optical packet are enhanced to obtain the same effect as described above.

Industrial Applicability

[0145] The present invention is related to the switching system, the optical packet transmission apparatus, and the method of generating the optical packet and is also applicable to a telephone communication system and a data communication system.

Reference Signs List

[0146] 10: switching system
13: optical transmitter
14: optical switch
15: optical receiver
21: clock unit

Claims

- [Claim 1] A switching system comprising:
a plurality of optical transmitters configured to convert an input electric packet into an optical packet and transmit the optical packet;
a plurality of optical receivers configured to receive the optical packet and convert the optical packet into an electric packet;
an optical switch arranged between the plurality of optical transmitters and the plurality of optical receivers and configured to transmit the optical packet input from the optical transmitter to any one of the plurality of optical receivers; and
a clock unit configured to transmit a clock signal having a clock phase to the optical transmitter and the optical receiver,
wherein the clock phase of the optical transmitter is corrected based on a clock phase of the optical packet received by the optical receiver and the clock phase of the optical receiver.
- [Claim 2] The switching system according to claim 1, further comprising an optical fiber configured to connect the optical switch and the optical transmitter,
wherein the optical fiber has a low temperature sensitivity.
- [Claim 3] The switching system according to claim 1, further comprising a plurality of optical fibers configured to connect the optical switch and the optical transmitter,
wherein the plurality of optical fibers are made to equal to each other.
- [Claim 4] The switching system according to claim 1, wherein
the optical transmitter demultiplexes the optical packet in a number equal to the number of optical receivers to which the optical packets are transmitted, and
the optical switch transmits the demultiplexed optical packets in time slots respectively assigned to the demultiplexed optical packets.
- [Claim 5] The switching system according to claim 4, wherein the optical switch sets guard times before and after a boundary of the time slot.
- [Claim 6] An optical packet transmitting apparatus that receives a second electric packet next to a first electric packet, converts the respective packets into optical packets, and transmits the optical packets to an optical receiver based on a clock signal, comprising:
an optical transmitter configured to
receive the clock signal and store a clock phase of the clock signal,

convert the first electric packet into a first optical packet, demultiplex the first optical packet by the number of optical receivers to which the first optical packets are transmitted, and transmit each of the demultiplexed first optical packets in the clock phase,
 receive, from the optical receiver, a phase difference between a clock phase of the demultiplexed first optical packet received by the optical receiver and a clock phase stored in the optical receiver, and
 convert the second electric packet into a second optical packet, demultiplex the second optical packet by the number of optical receivers to which the second packets are transmitted, and transmit each of the demultiplexed second optical packets in the phase-corrected clock phase; and
 an optical switch configured to
 assign time slots in the demultiplexed first optical packets and the demultiplexed second optical packets, and set guard times before and after a boundary of each of the time slots.

[Claim 7]

A method of generating, based on a clock signal, an optical packet to be transmitted from an optical transmitter to an optical receiver via an optical switch, comprising:
 a step of causing the optical transmitter and the optical receiver to receive the clock signal and store a clock phase of the clock signal;
 a step of causing the optical transmitter to demultiplex the first optical packet and transmit each demultiplexed first optical packet in the clock phase;
 a step of causing the optical switch to assign time slots to the demultiplexed first optical packets, respectively, and transmit the demultiplexed first optical packets;
 a step of causing the optical receiver to measure a phase difference between a clock phase of each demultiplexed first optical packet and a clock phase stored in the optical receiver;
 a step of causing the optical receiver to transmit the phase difference to the optical transmitter;
 a step of causing the optical transmitter to correct a clock phase stored in the optical transmitter by using the phase difference; and
 a step of causing the optical transmitter to demultiplex the second optical packet and transmit each demultiplexed second optical packet in the corrected clock phase.

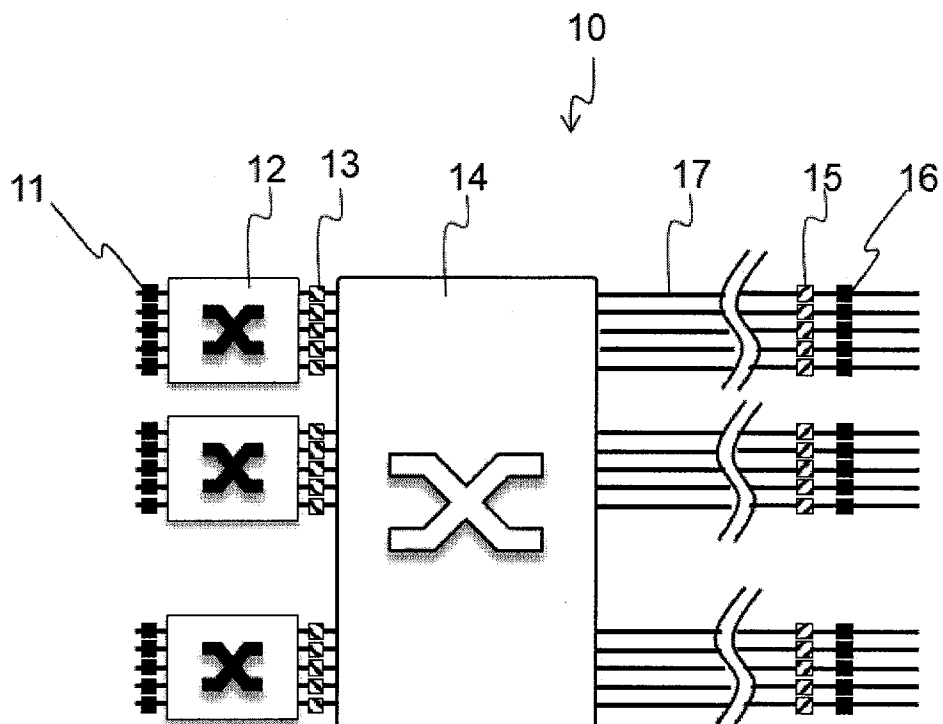
[Claim 8]

A method of generating an optical packet to be transmitted to an optical

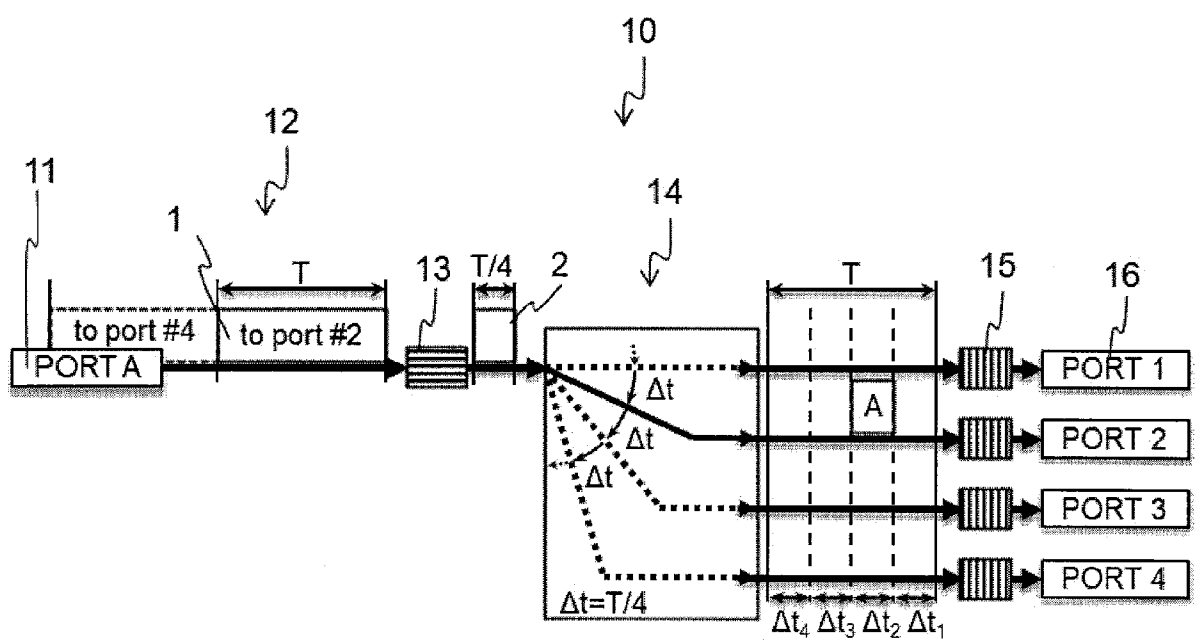
receiver from an electric packet input to the optical transmitter by using the optical transmitter and an optical switch, comprising:

- a step of causing the optical transmitter to convert the electric packet into an optical packet;
- a step of causing the optical transmitter to demultiplex the optical packet by the number of optical receivers to which the optical packets are transmitted;
- a step of causing the optical switch to assign time slots to the demultiplexed optical packets, respectively; and
- a step of causing the optical switch to set guard times before and after a boundary of the time slots between the demultiplexed optical packets.

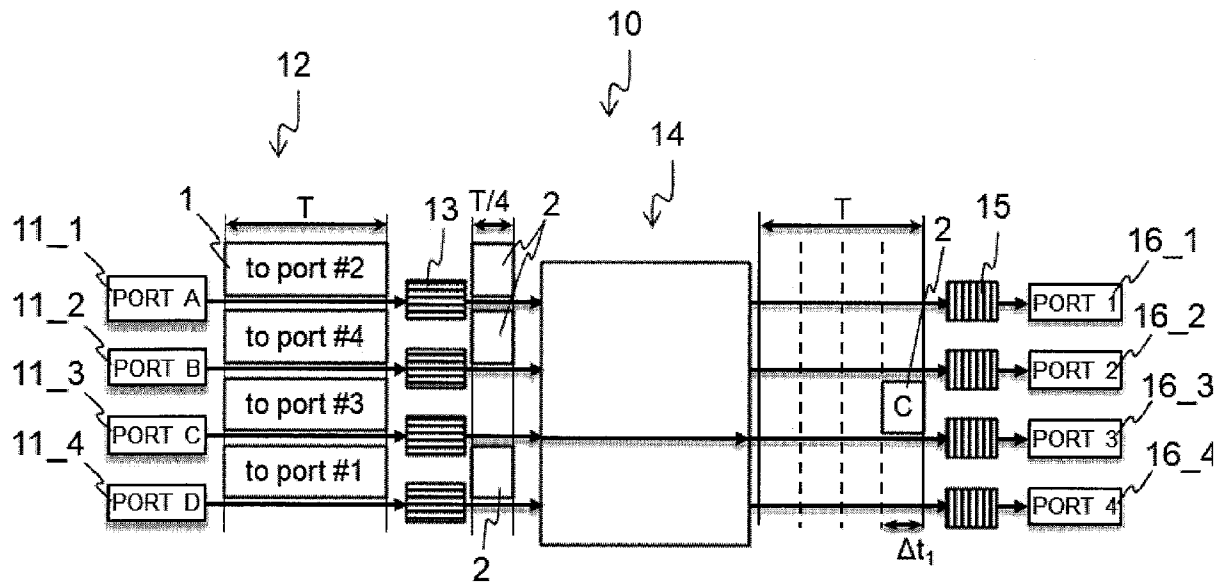
[Fig. 1]



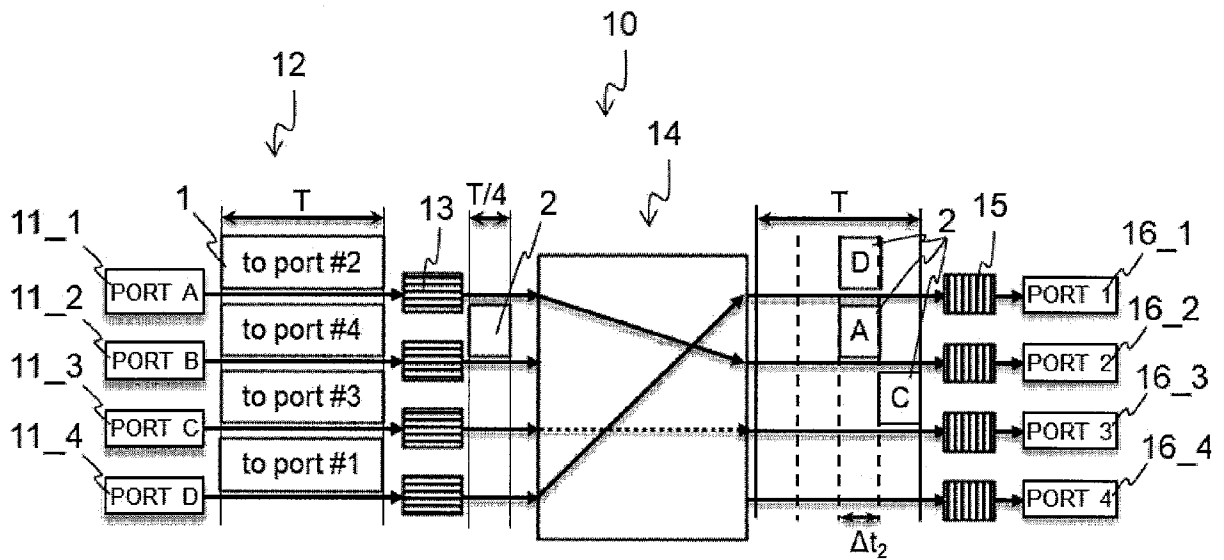
[Fig. 2]



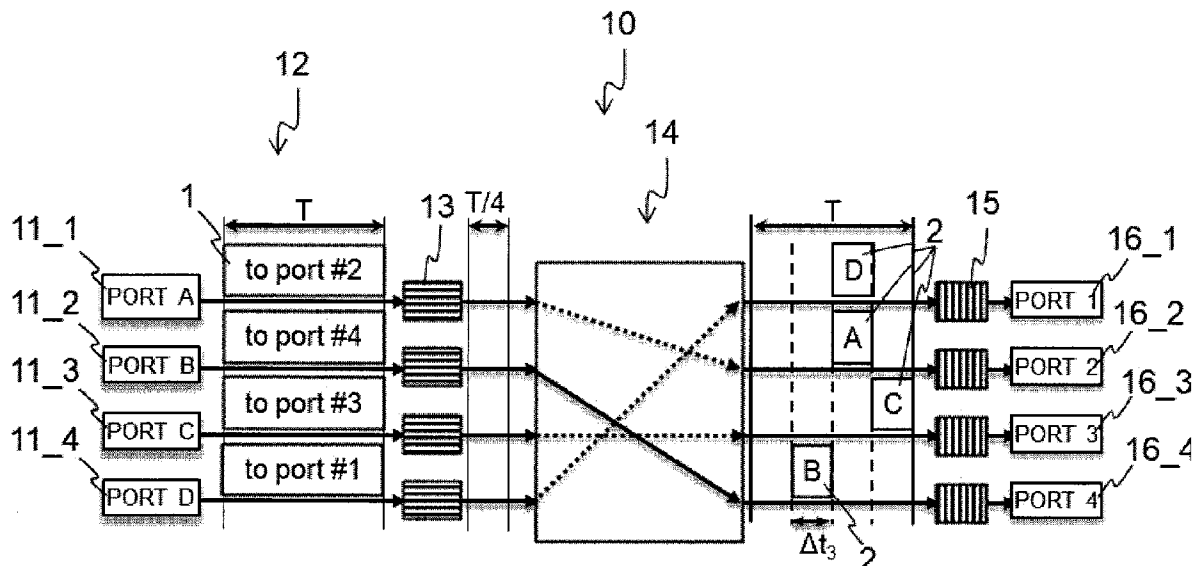
[Fig. 3A]



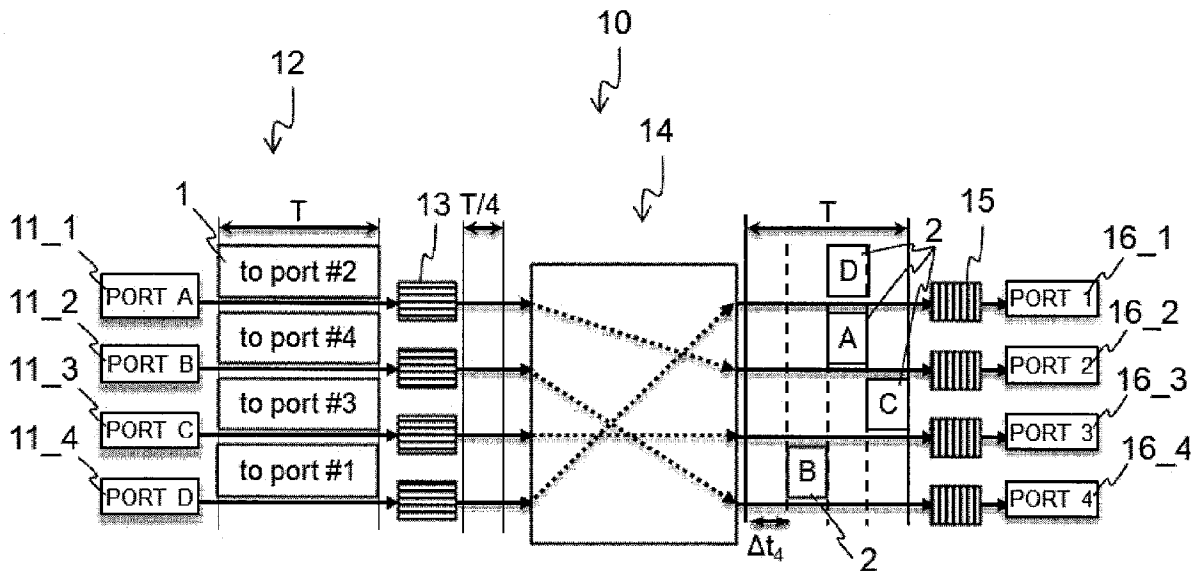
[Fig. 3B]



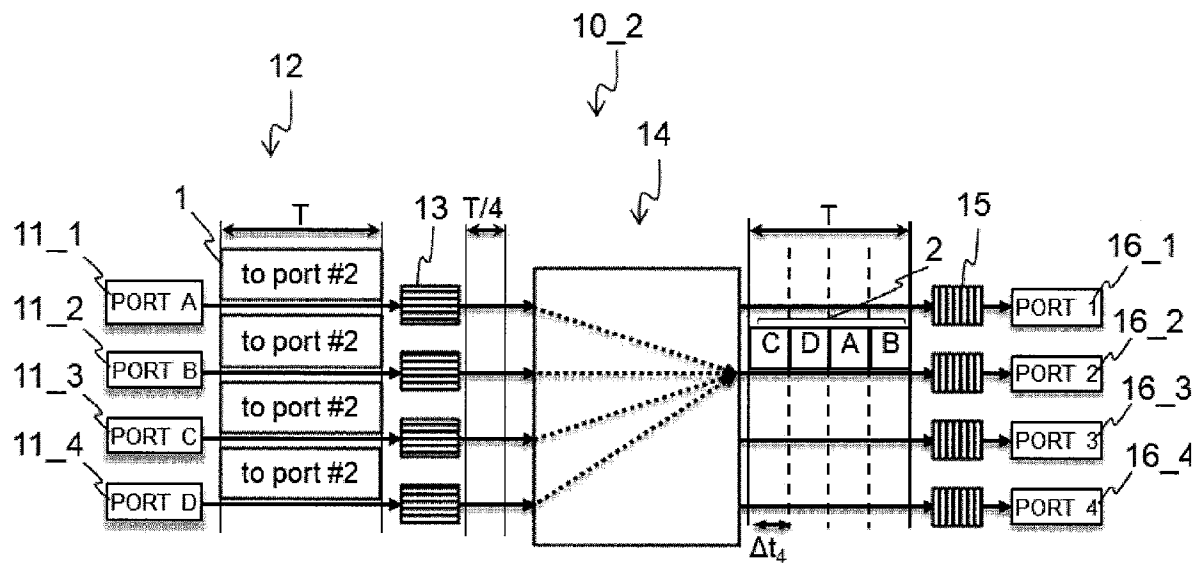
[Fig. 3C]



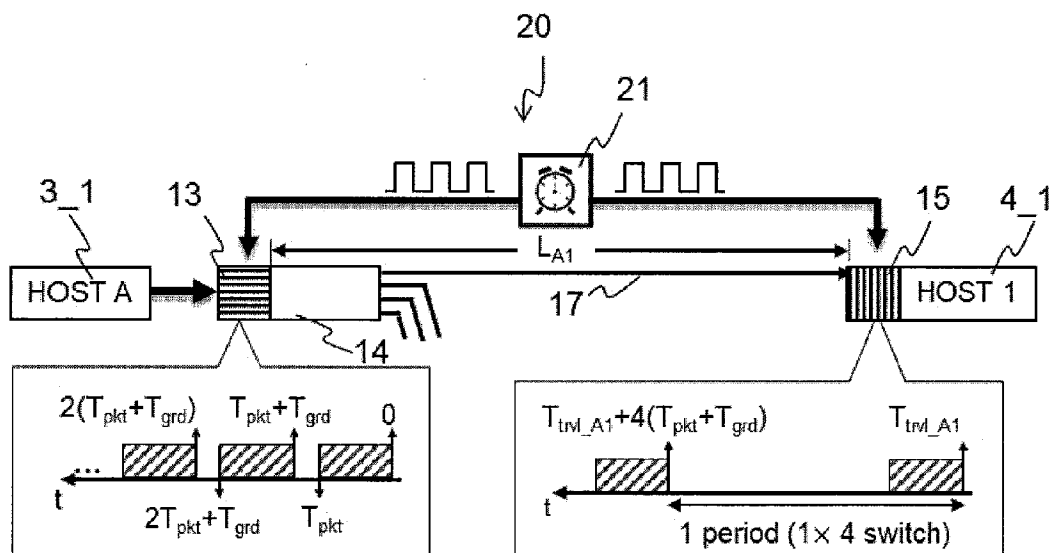
[Fig. 3D]



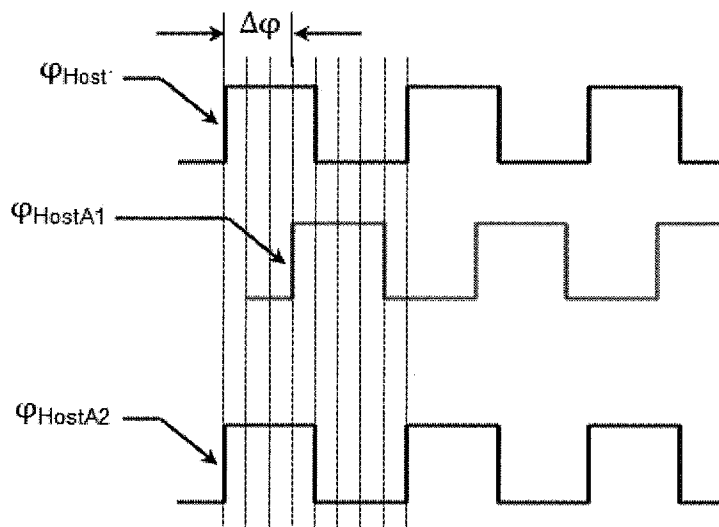
[Fig. 4]



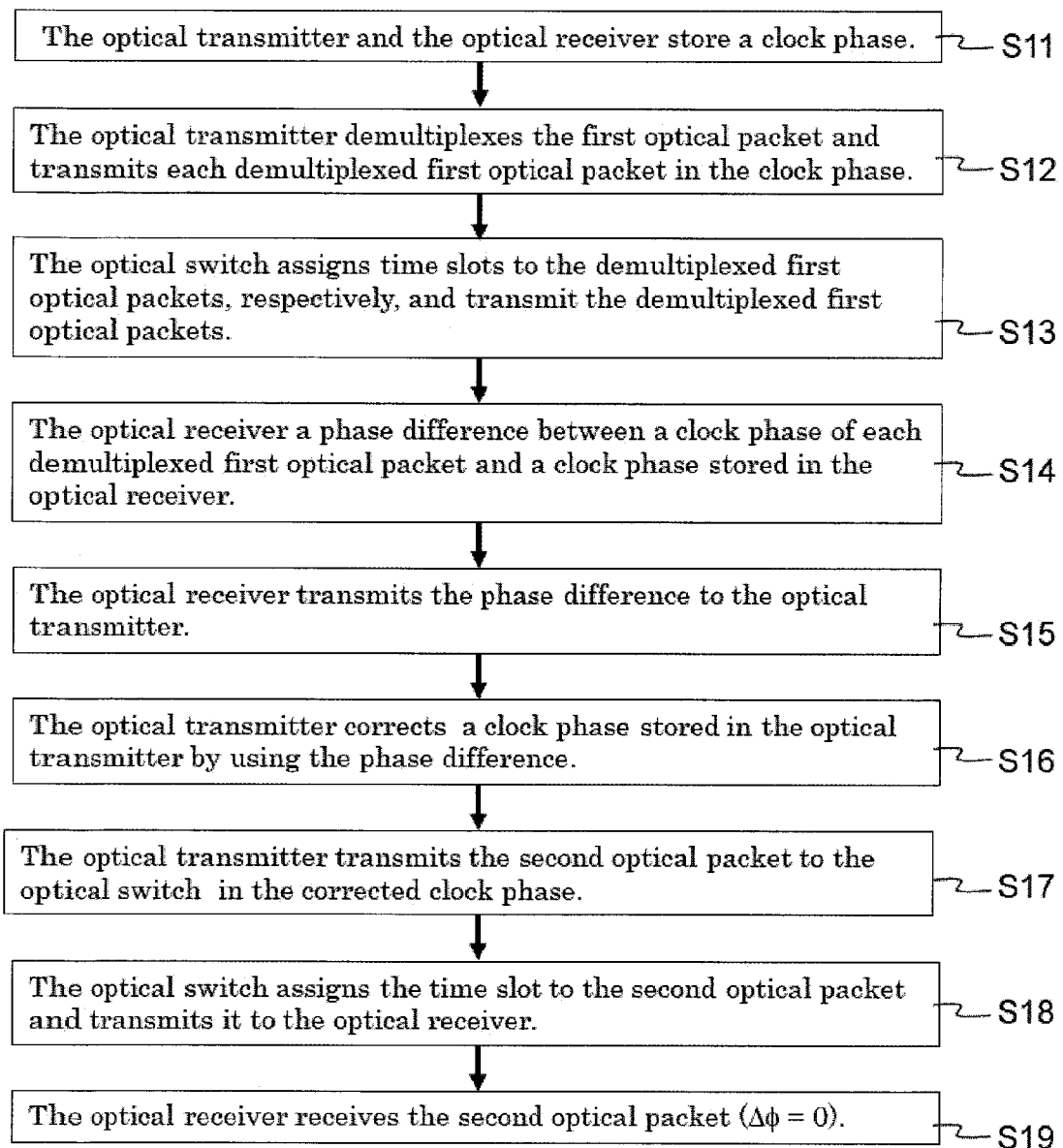
[Fig. 5]



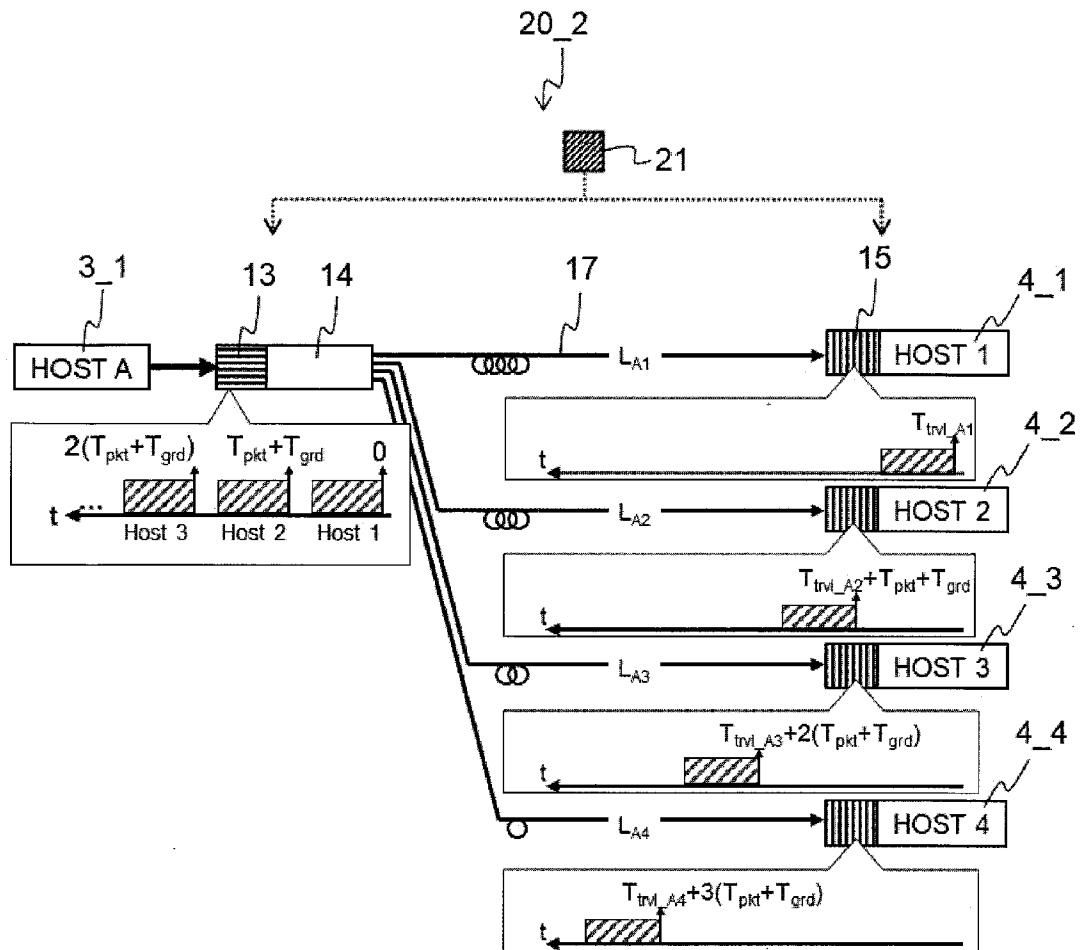
[Fig. 6]

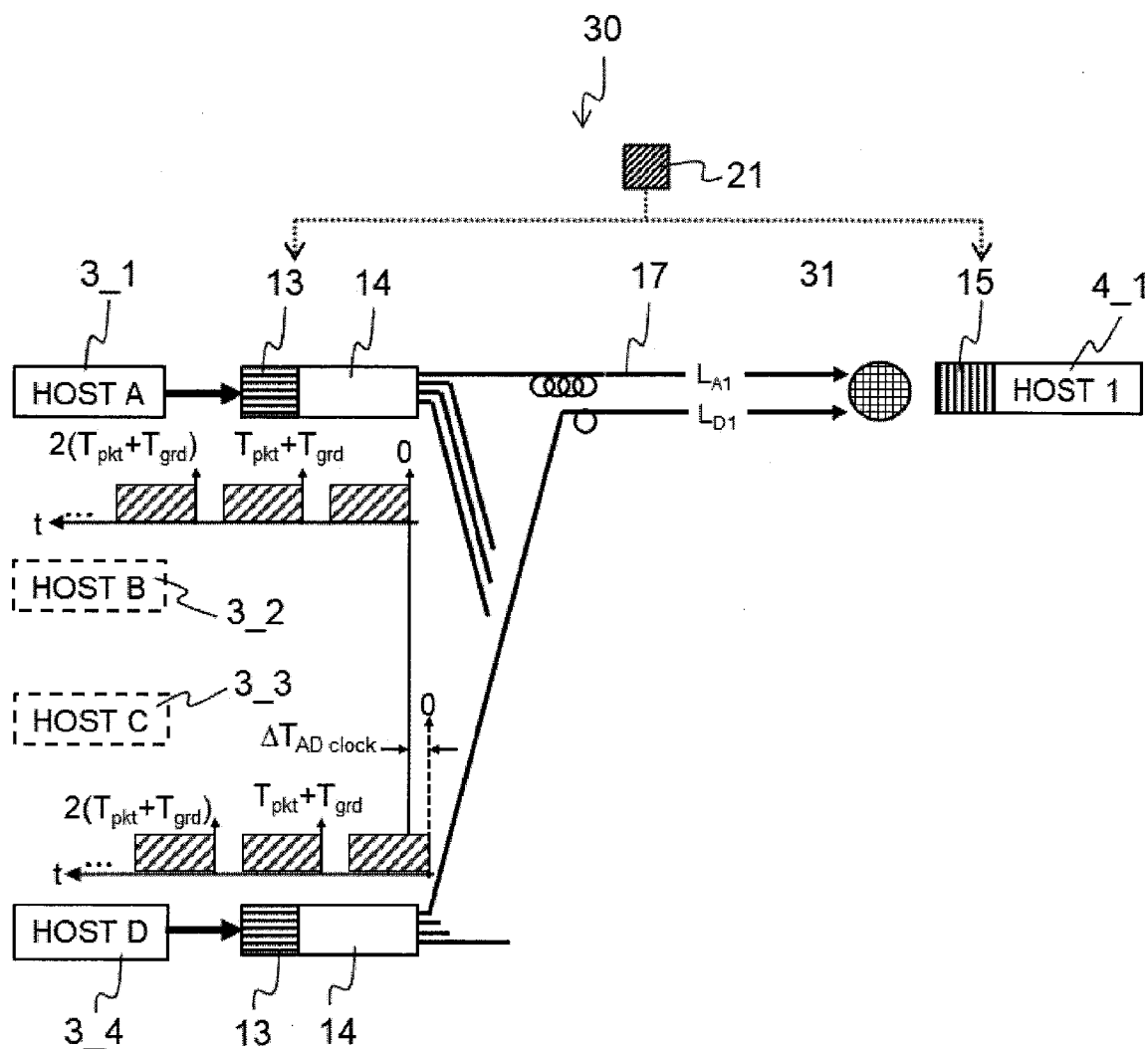
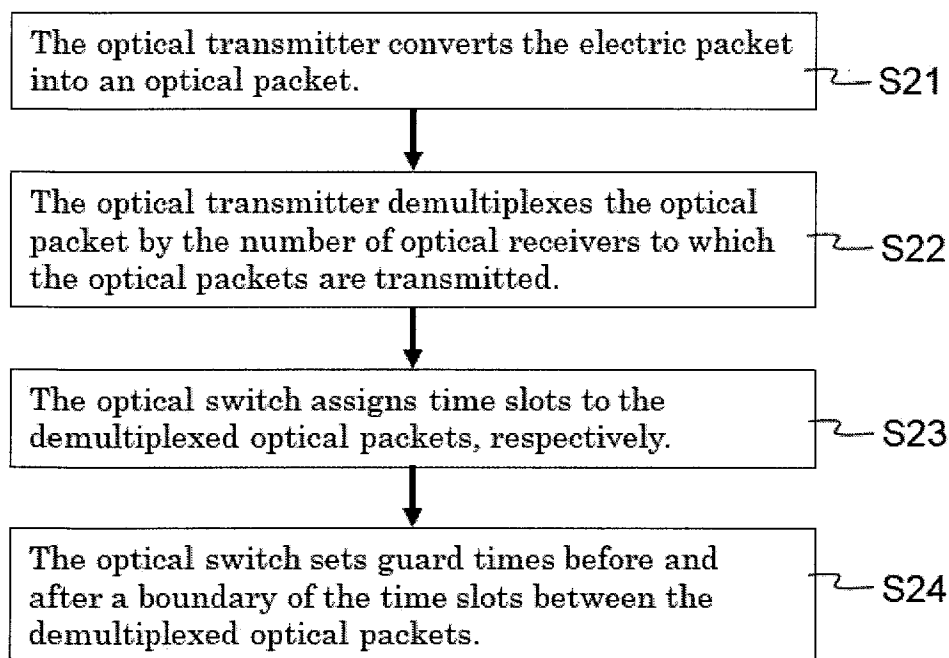


[Fig. 7]

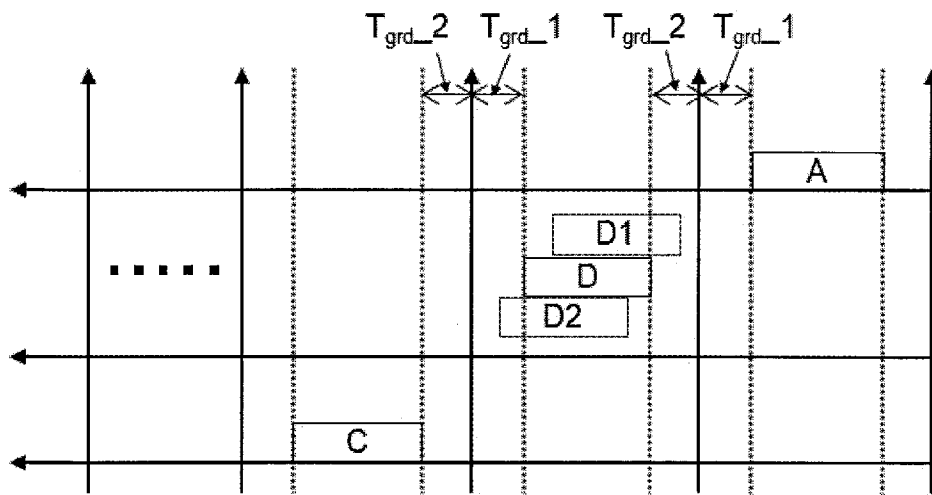


[Fig. 8]





[Fig. 11]



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2022/031219

A. CLASSIFICATION OF SUBJECT MATTER**H04L 49/112**(2022.01)i

FI: H04L49/112

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L49/112

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996

Published unexamined utility model applications of Japan 1971-2022

Registered utility model specifications of Japan 1996-2022

Published registered utility model applications of Japan 1994-2022

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 10-243017 A (NEC CORP) 11 September 1998 (1998-09-11) whole document	1-8
A	JP 2011-19122 A (OKI ELECTRIC INDUSTRY CO LTD) 27 January 2011 (2011-01-27) whole document	1-8
A	US 6441935 B1 (NEC CORPORATION) 27 August 2002 (2002-08-27) whole document	1-8



Further documents are listed in the continuation of Box C.



See patent family annex.

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“O” document referring to an oral disclosure, use, exhibition or other means

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/JP2022/031219

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
JP	10-243017	A	11 September 1998	(Family: none)	
JP	2011-19122	A	27 January 2011	(Family: none)	
US	6441935	B1	27 August 2002	JP 11-177624 A	
				whole document	
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				US 2002/0131120 A1	
				EP 923263 A2	