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(54) Current amplifier and data bus circuit

(57) There is provided a current amplifier and a data bus circuit using such a current amplifier capable of reducing input impedance with a smaller circuit area than the conventional so that high-speed operation of the data bus lines can be realized without a remarkable increase of the circuit area. The current amplifier includes first and second field effect transistors N11, N12 respectively provided between a pair of input terminals I, Ib and a first potential supply terminal Vcc, and third and fourth field effect transistors N13, N14 for supplying output power to a pair of output terminals O, Ob. The gate of the third field effect transistor is connected to the first input terminal and to the source of the first field effect transistor the gate of which is connected to the drain of the third field effect transistor, whereas the gate of the fourth field effect transistor is connected to the second input terminal and to the source of the second field effect transistor the gate of which is connected to the drain of the fourth field effect transistor.

EP 0 753 858 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 96 30 5041

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 468 861 A (FUJITSU) * page 3, column 2, line 36 - page 5, column 5, line 26; figure 2 * ---	1-4	G11C7/00
A	US 5 353 249 A (ITANO) * column 1, line 25 - column 2, line 39; figure 1 * ---	7	
A	US 5 365 488 A (Y. MATSUSHITA) * column 3, line 3 - column 3, line 44; figure 1 * -----	15	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G11C
H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 January 1998	Degraeve, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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