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(54) Title of the Invention: **Ohmic contacts in semiconductor devices**
Abstract Title: **A high-electron-mobility transistor having ohmic contacts**

(57) A semiconductor arrangement comprising: a substrate 801; a dielectric layer 806, 807; a semiconductor layer disposed between the substrate 801 and the dielectric layer 806, 807; one or more trenches formed in the dielectric layer 806, 807; one or more ohmic metal contacts 808 located in said one or more trenches; and a metallic connector layer. The semiconductor arrangement may be a high electron mobility transistor (HEMT). The metal contacts 808 may comprise a first metal alloy, with the metal connector comprising a second metal alloy. The first metal alloy and the second metal alloy may consist of the same component metals in different ratios. The metal contacts may be cylindrical, triangular, rectangular or obround. The HEMT may be manufactured by filling the trench with a different ratios of a first and second metal in different regions of the trench to form a metal stack 809, 810, 811. The metals may then be annealed to form an alloy.

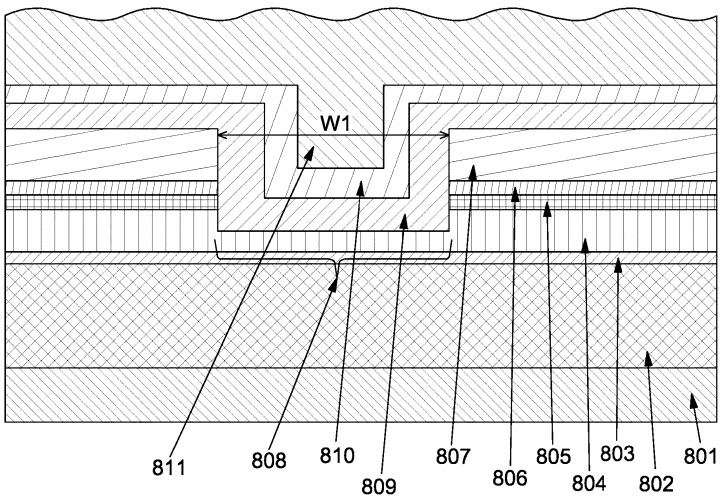

Figure 8

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

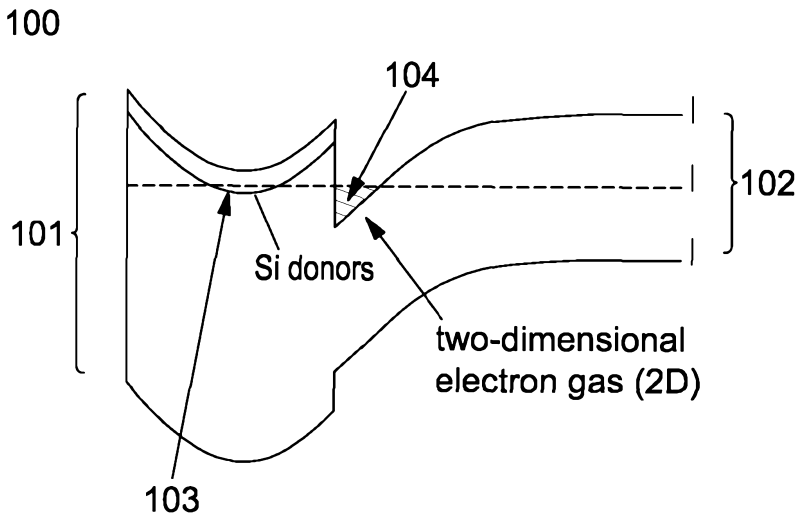


Figure 1a

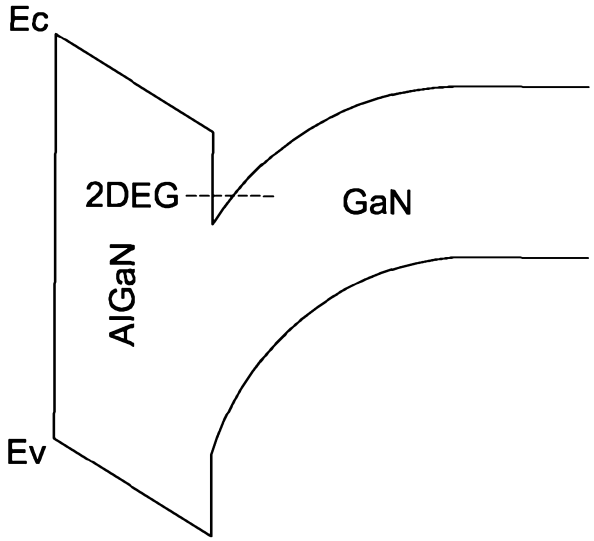


Figure 1b

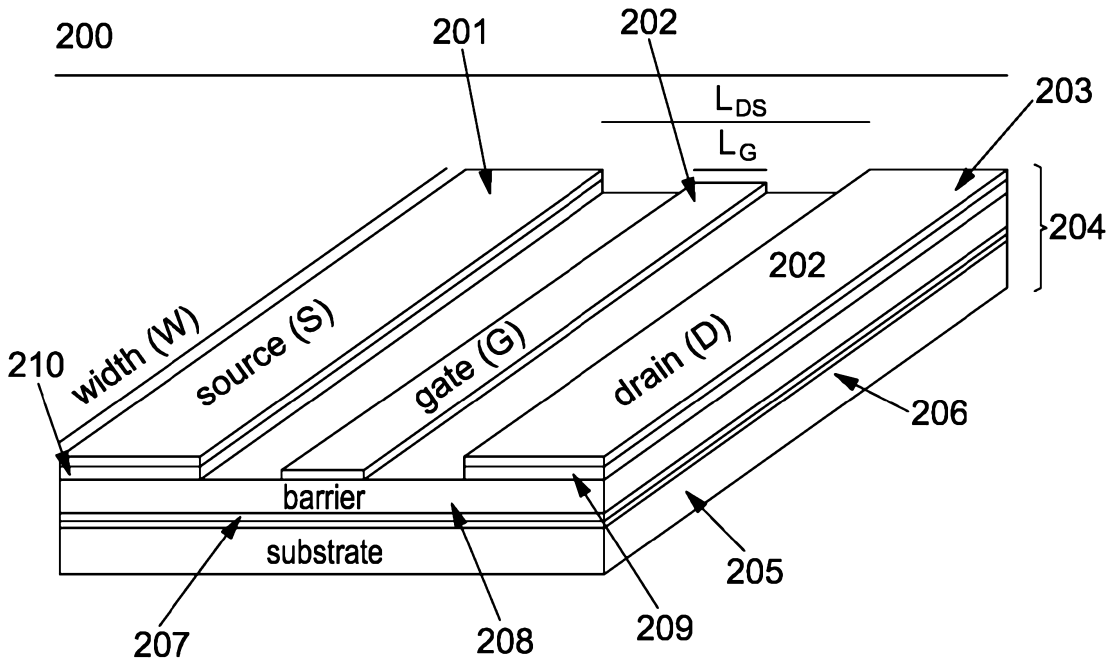


Figure 2

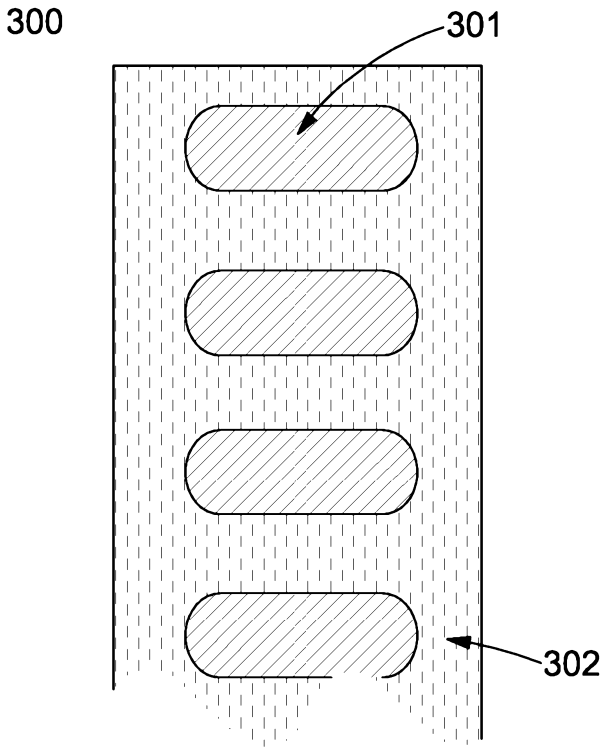


Figure 3

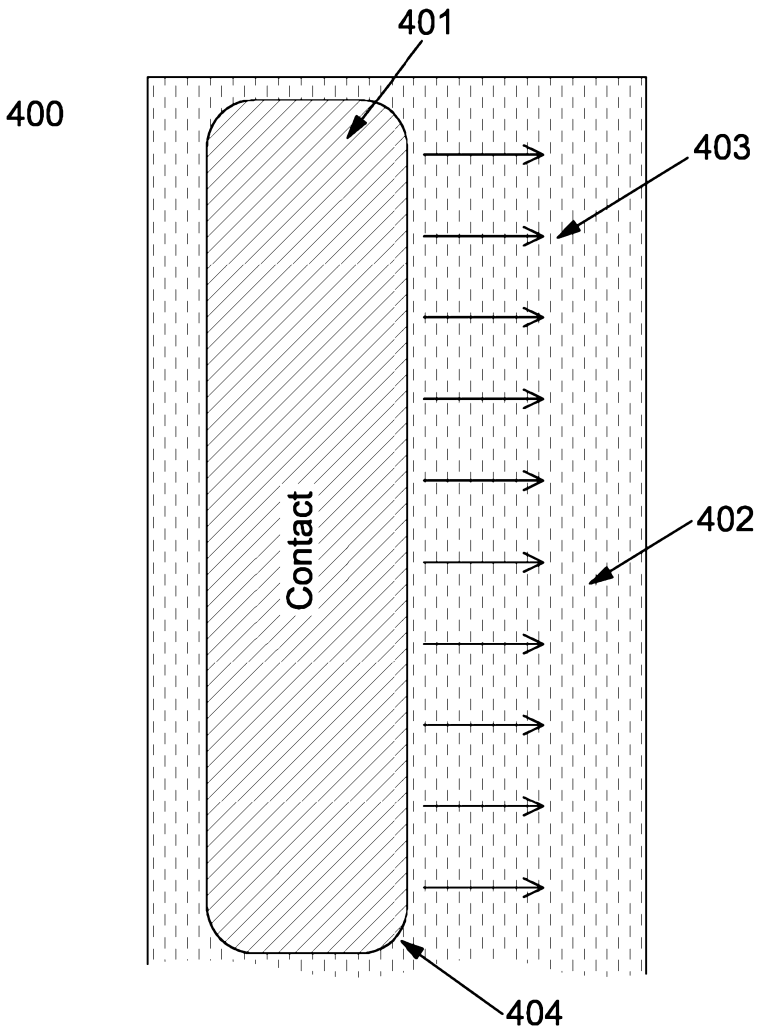


Figure 4

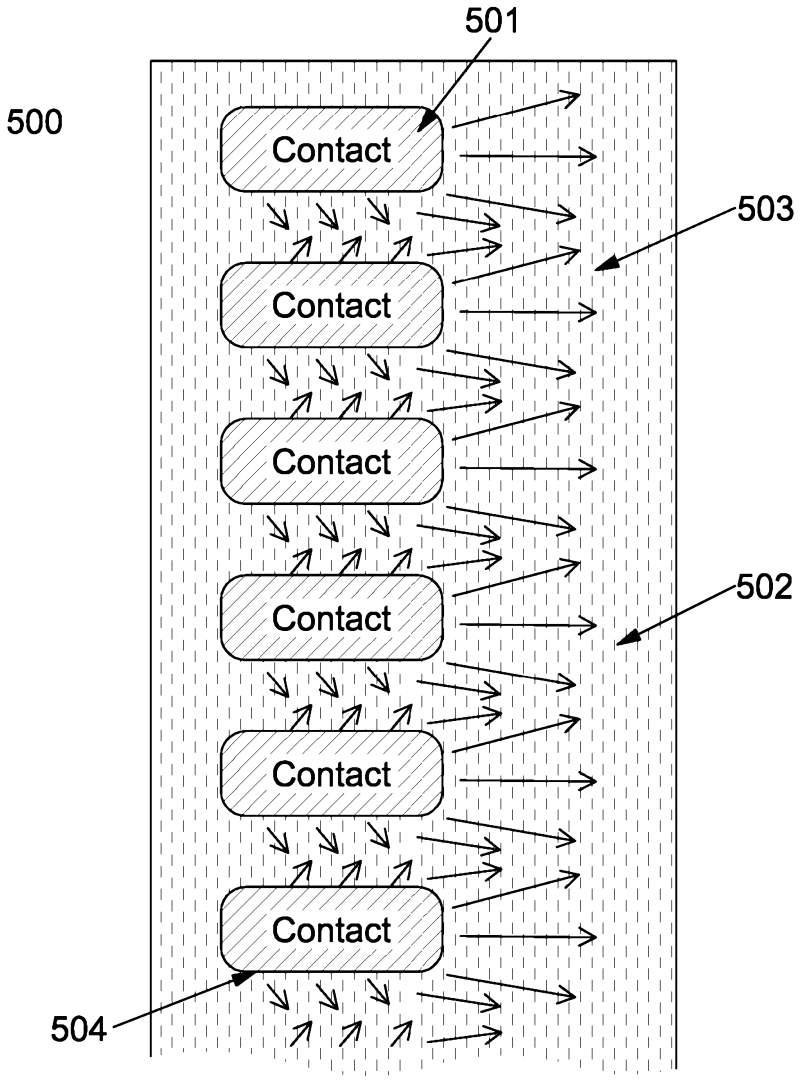


Figure 5

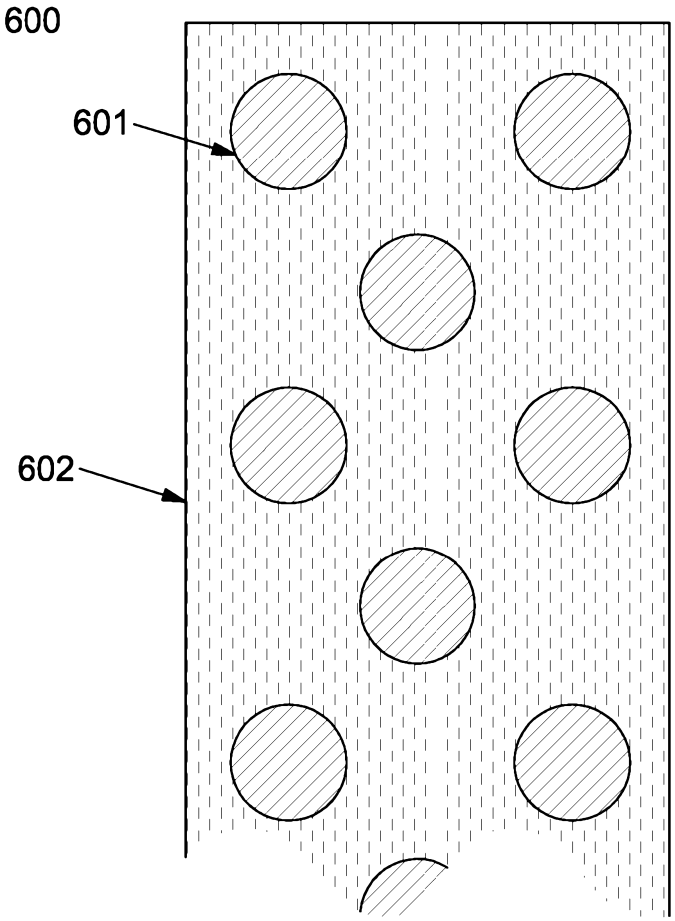


Figure 6

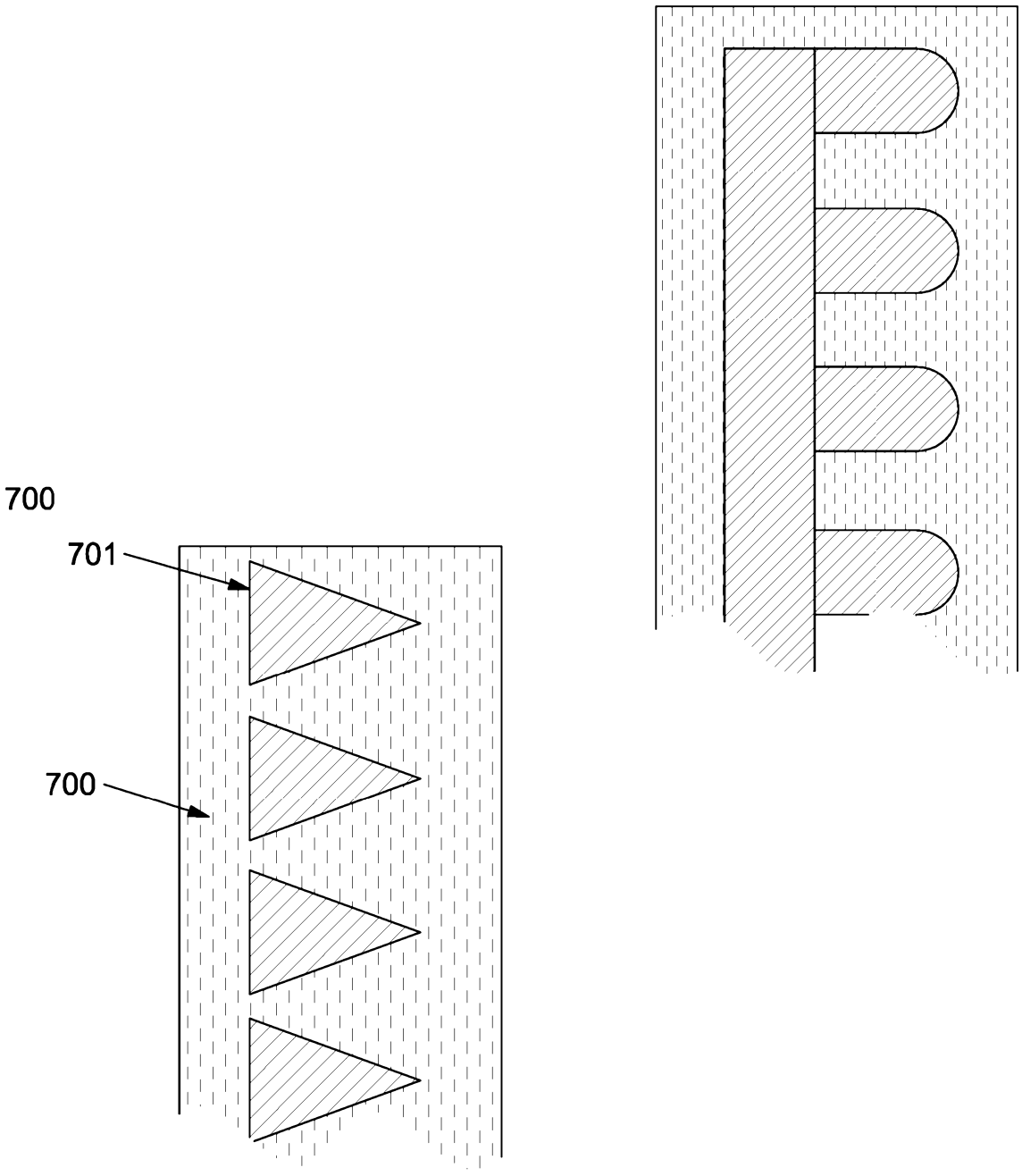


Figure 7

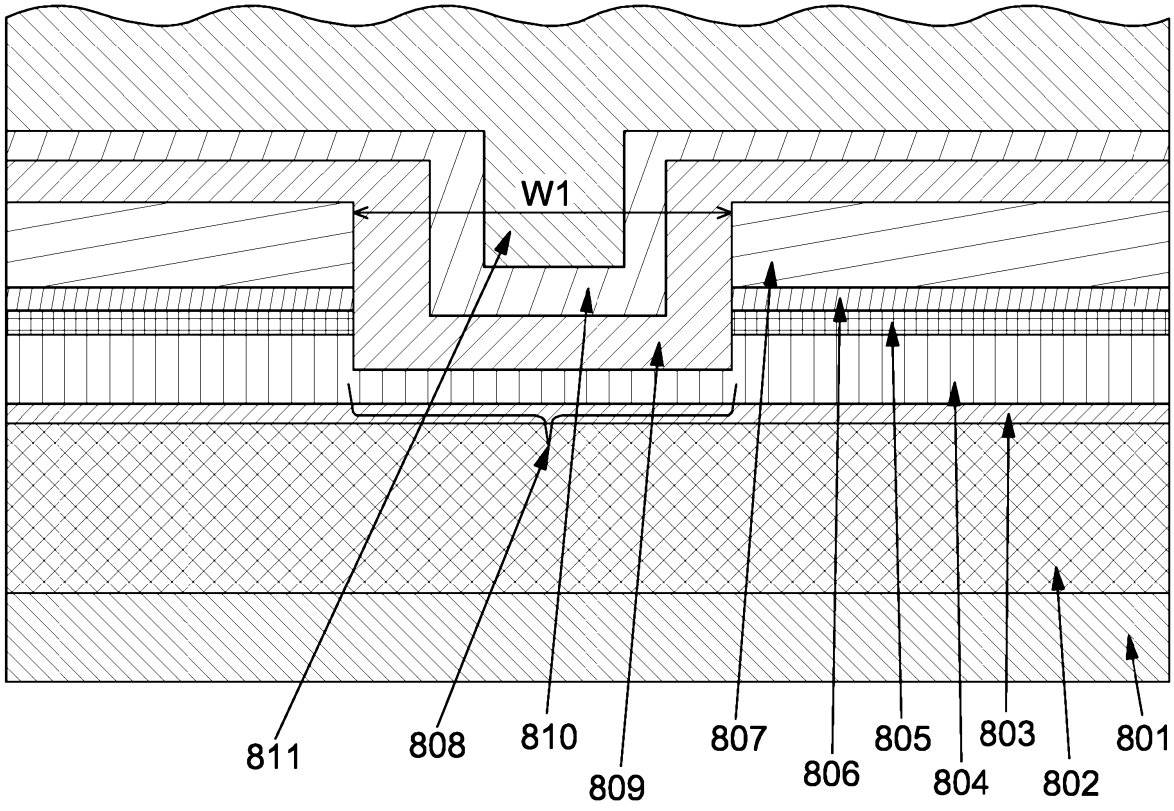
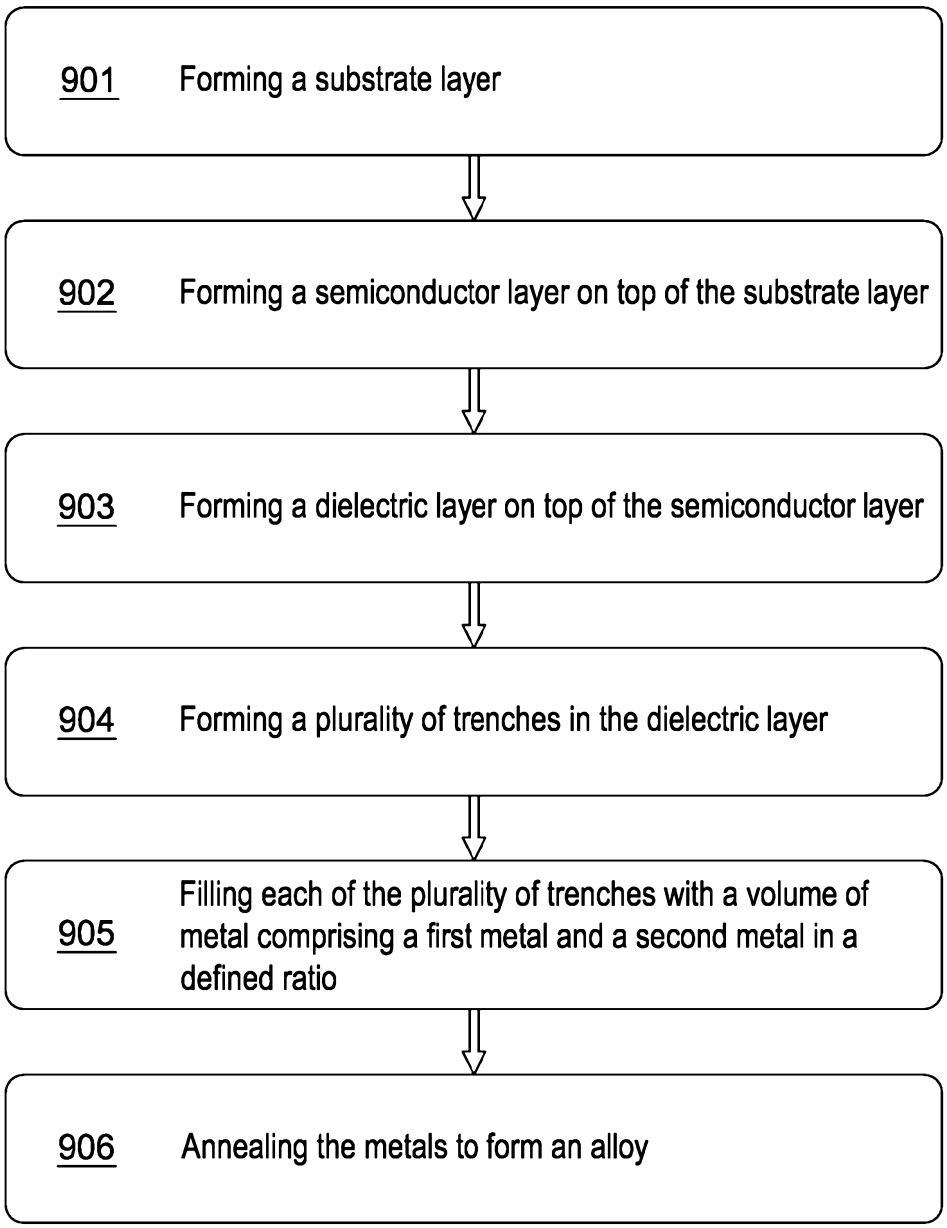


Figure 8



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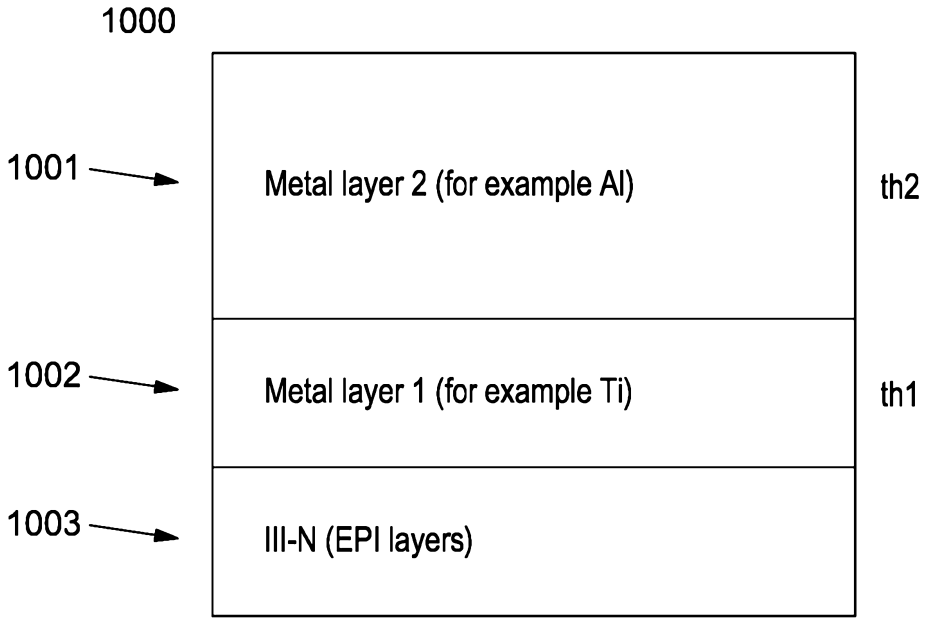

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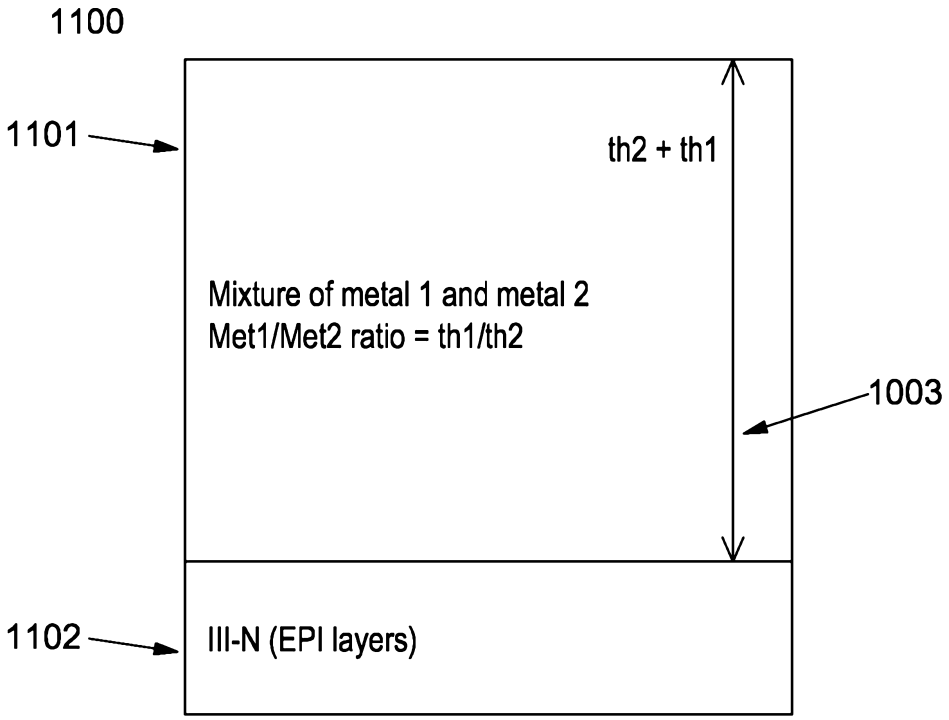

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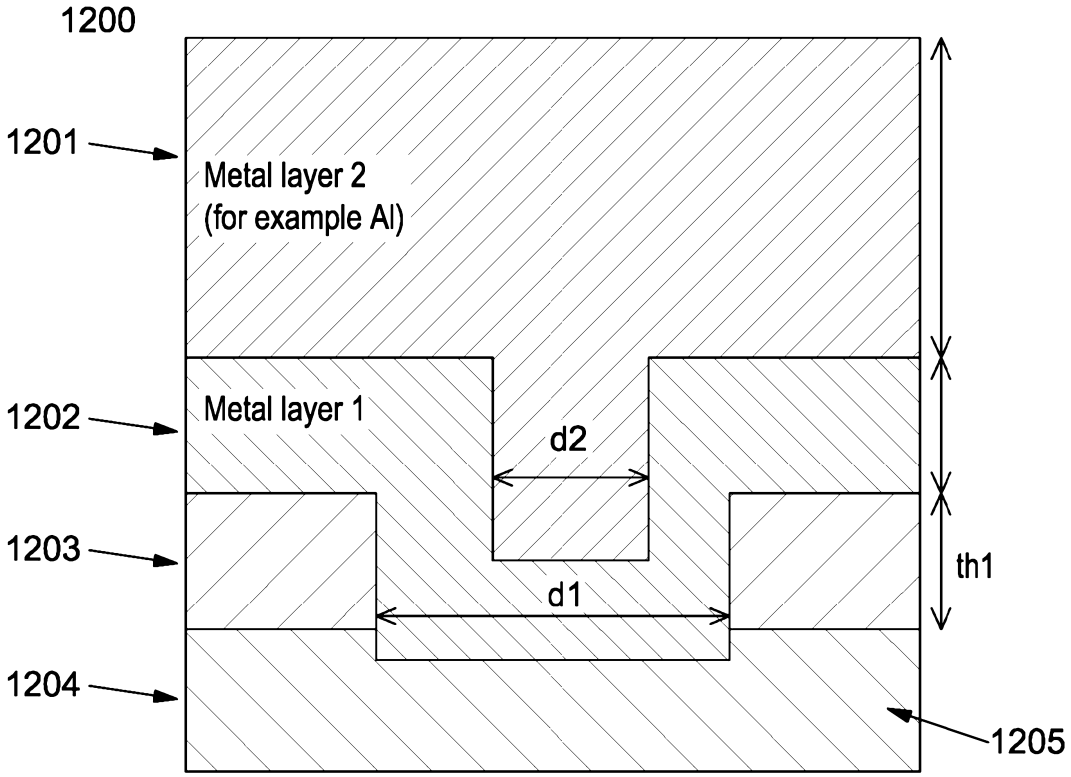


Figure 12

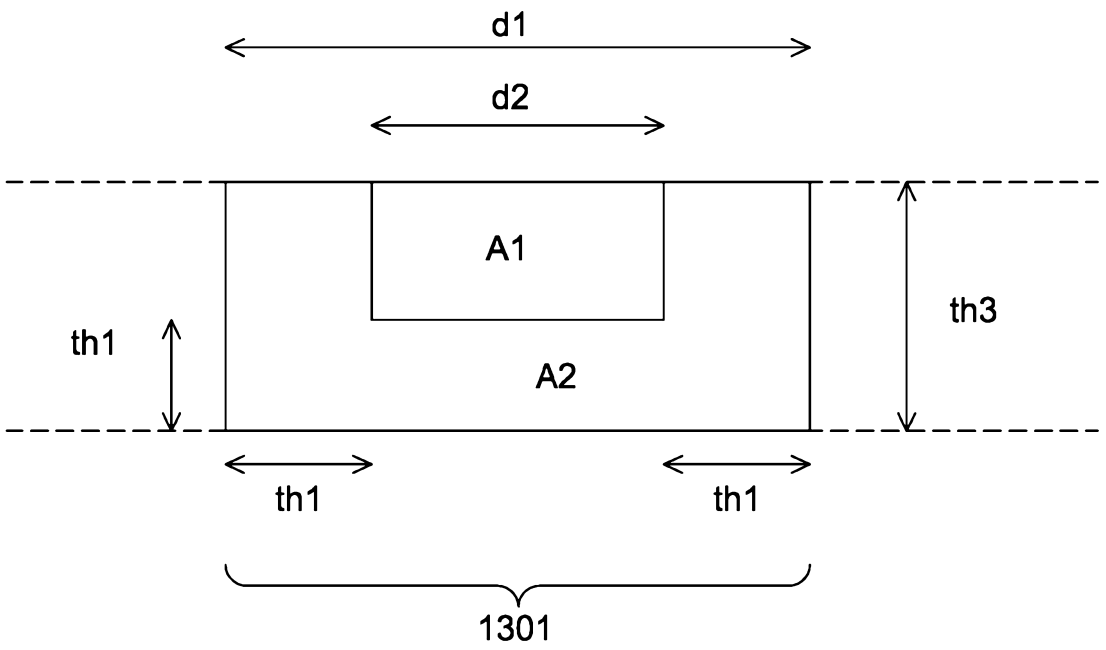
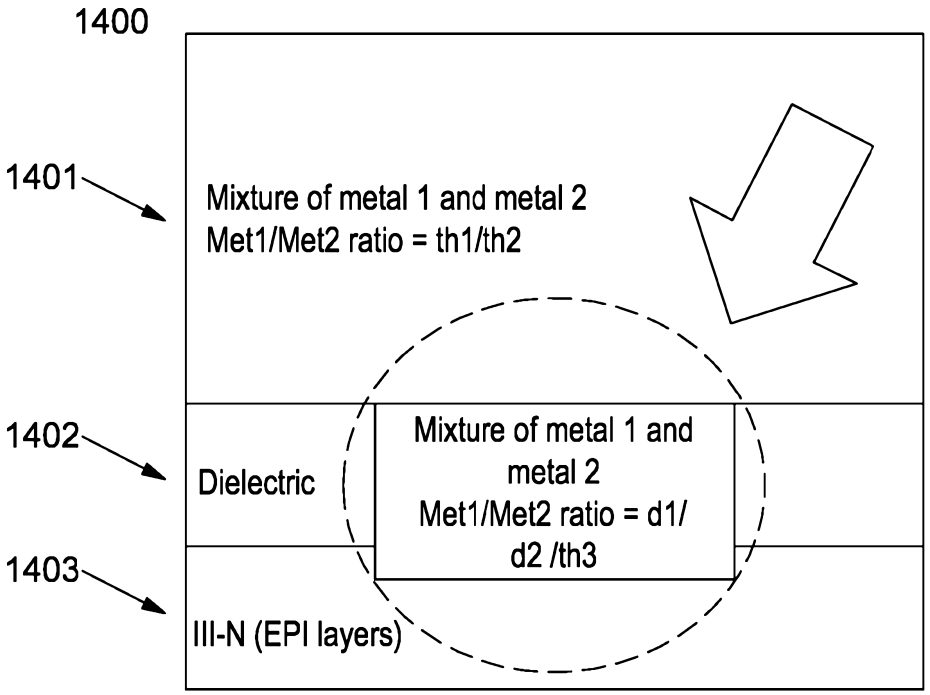


Figure 13



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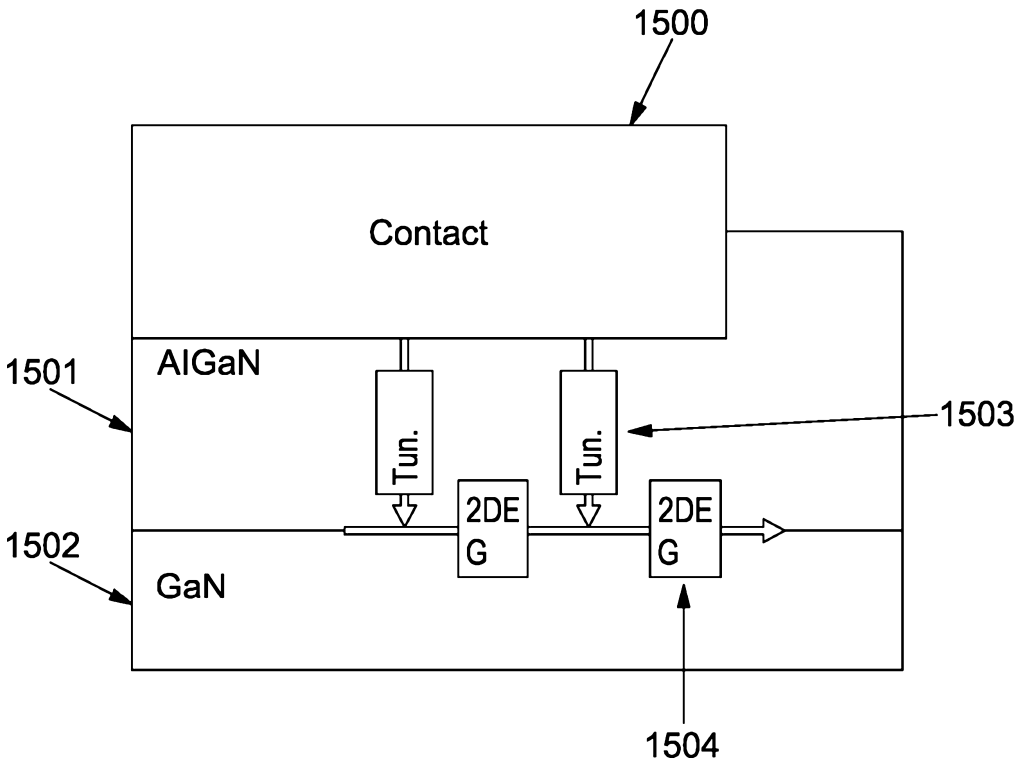

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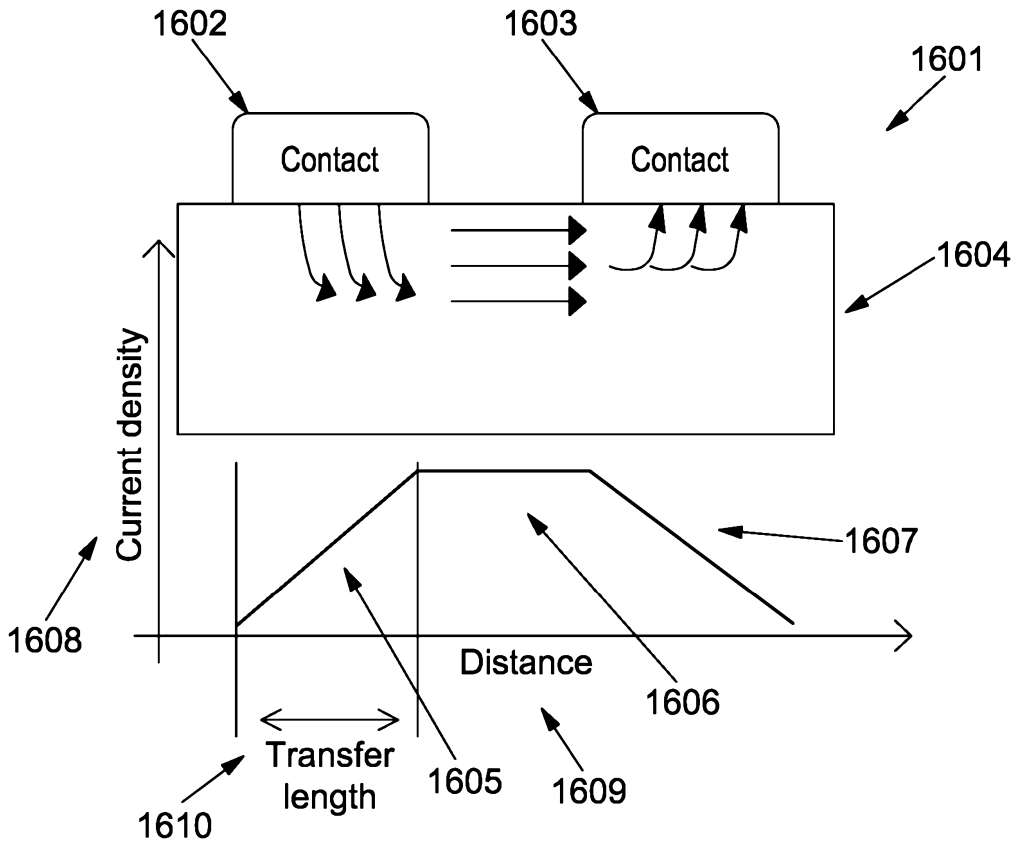

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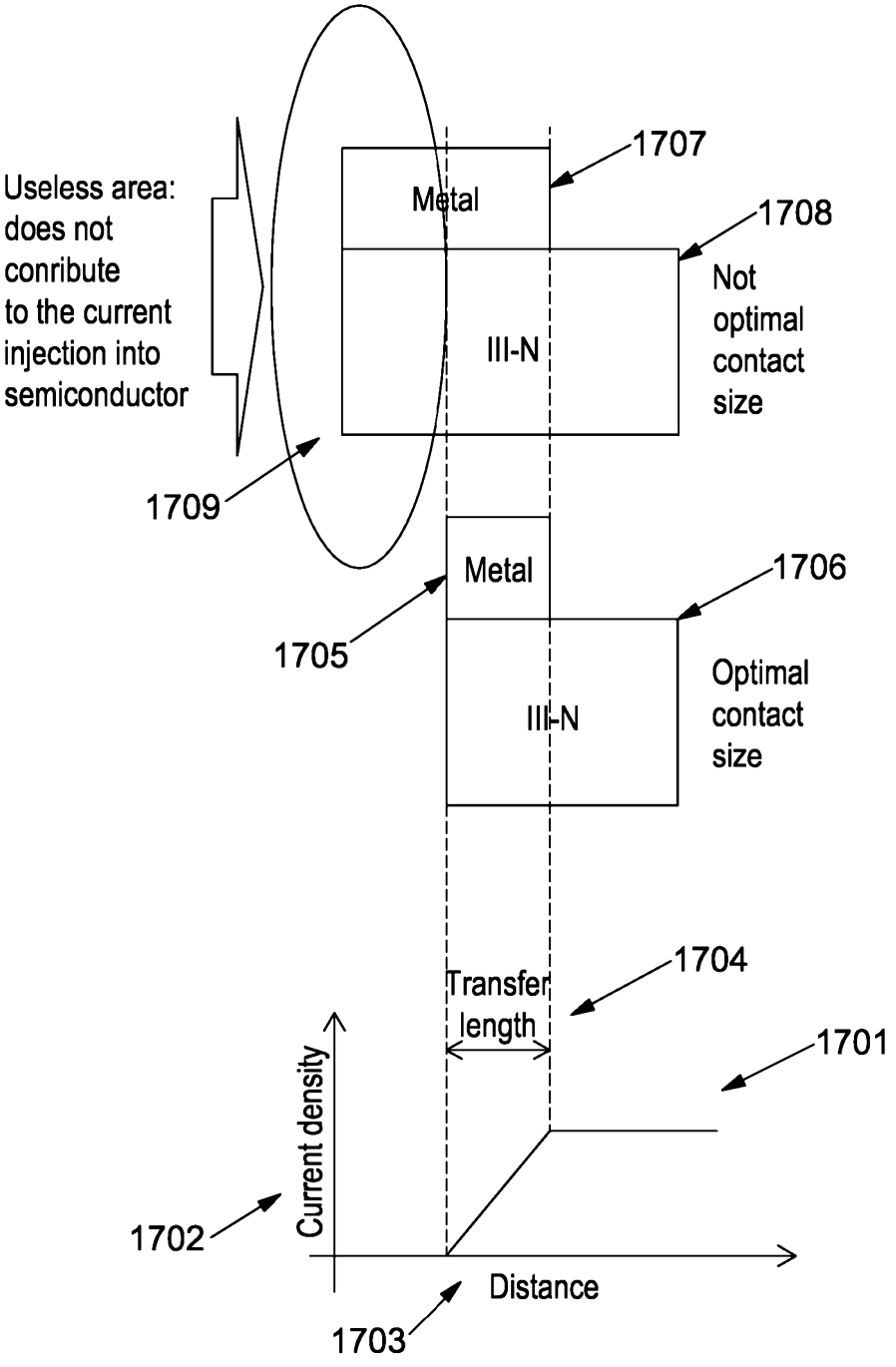


Figure 17

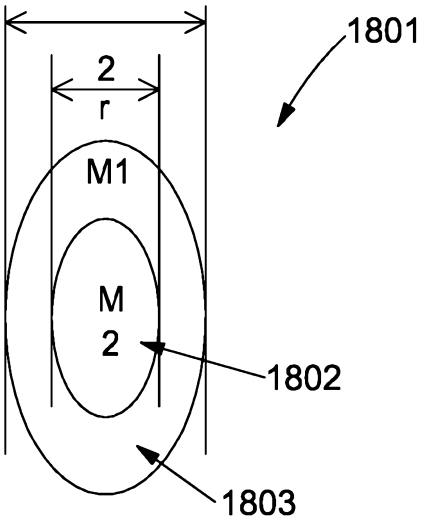


Figure 18a

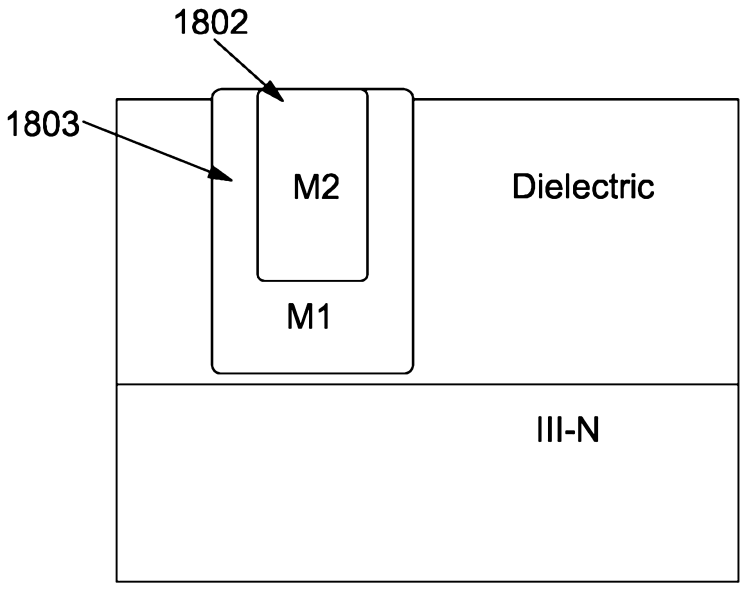


Figure 18b

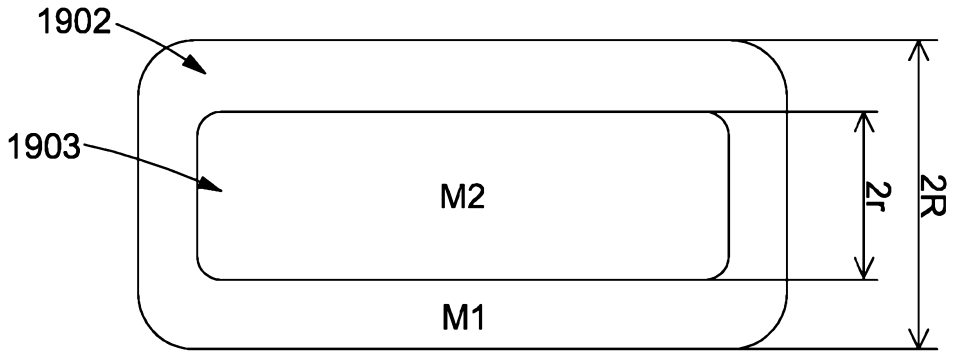


Figure 19a

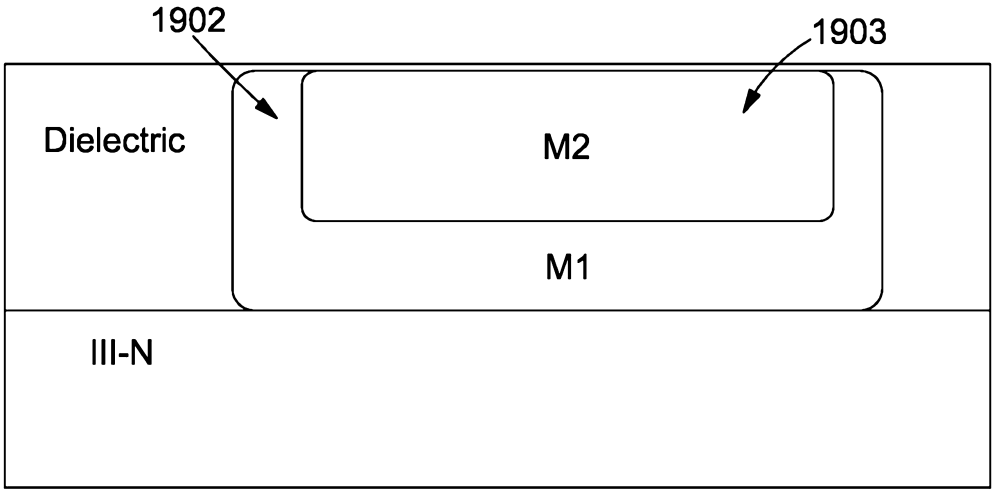


Figure 19b

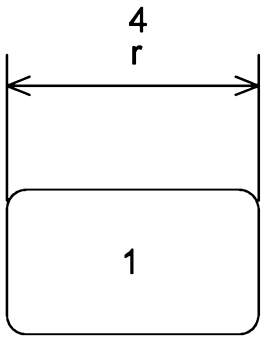
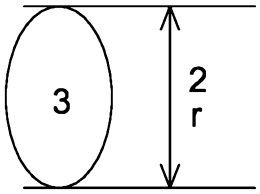


Figure 20a



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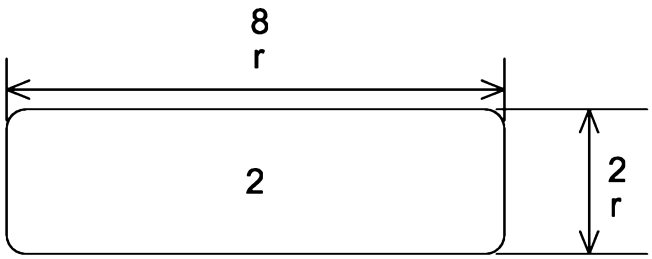

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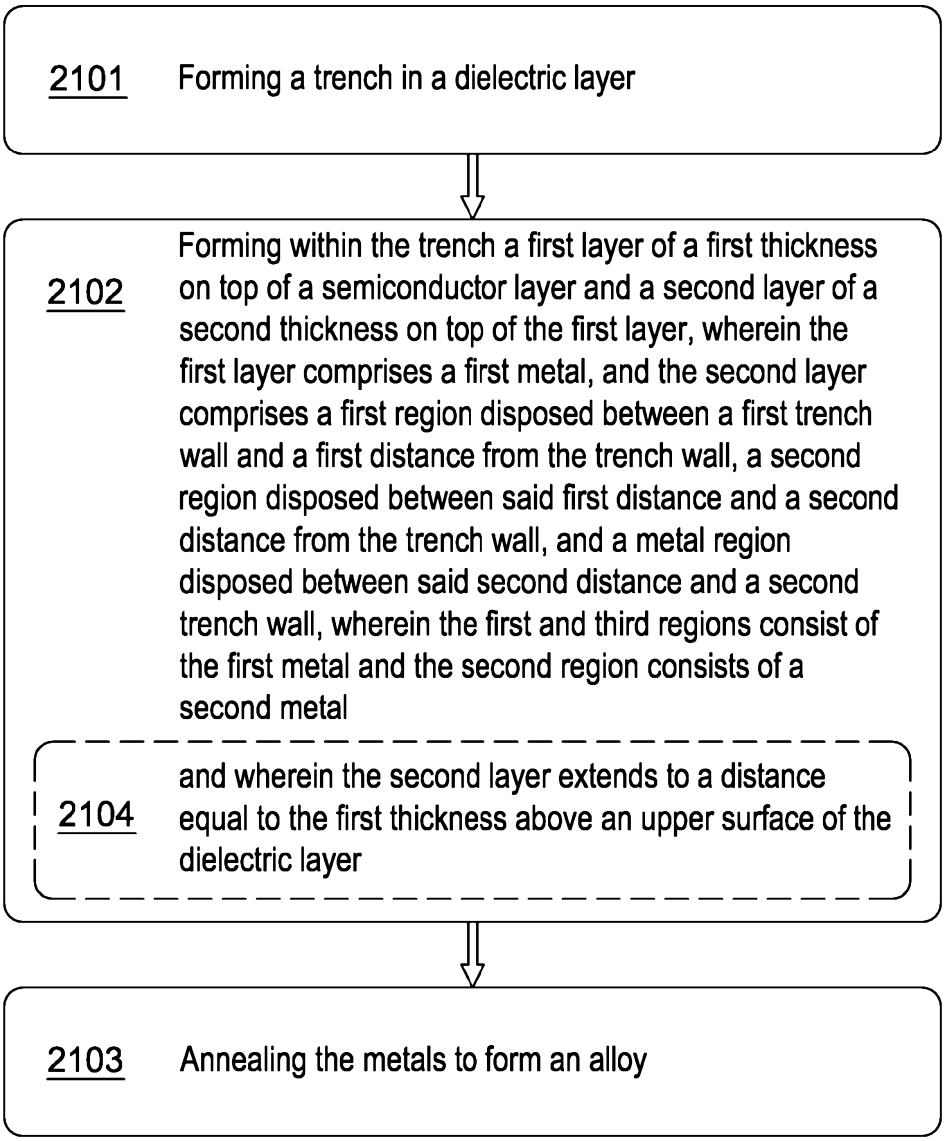

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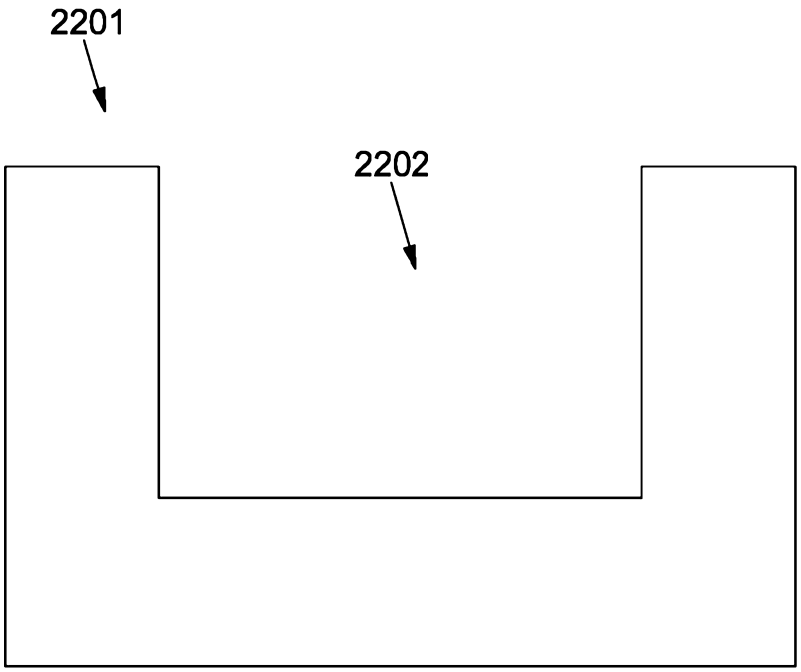


Figure 22

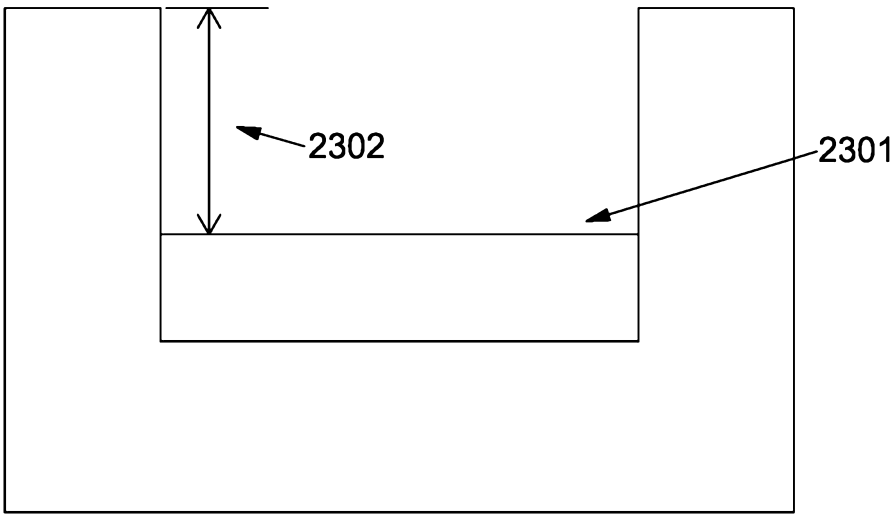


Figure 23

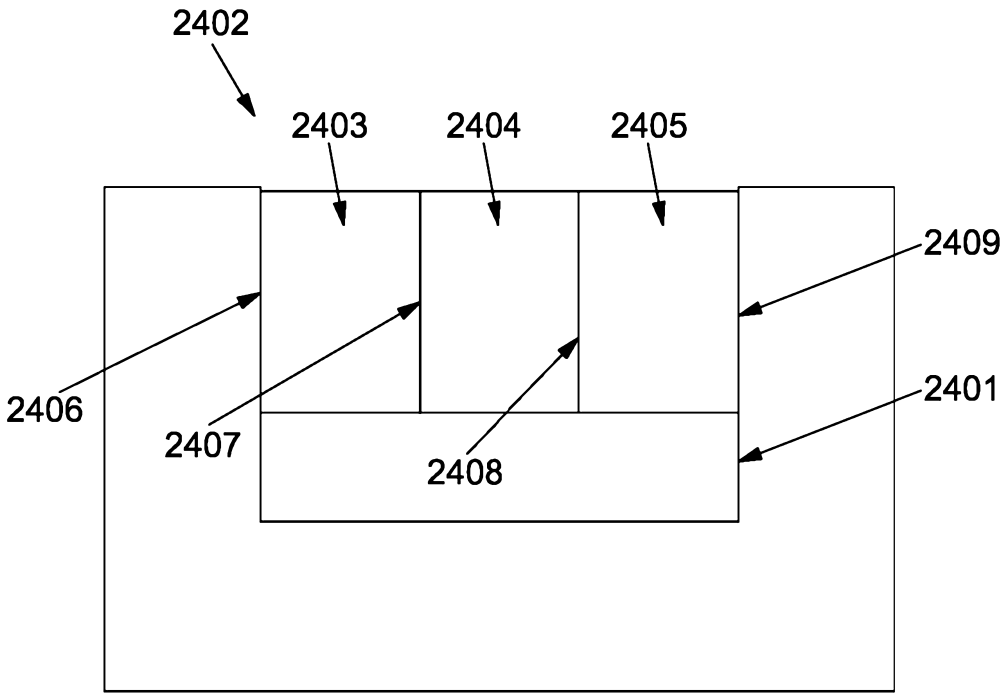


Figure 24

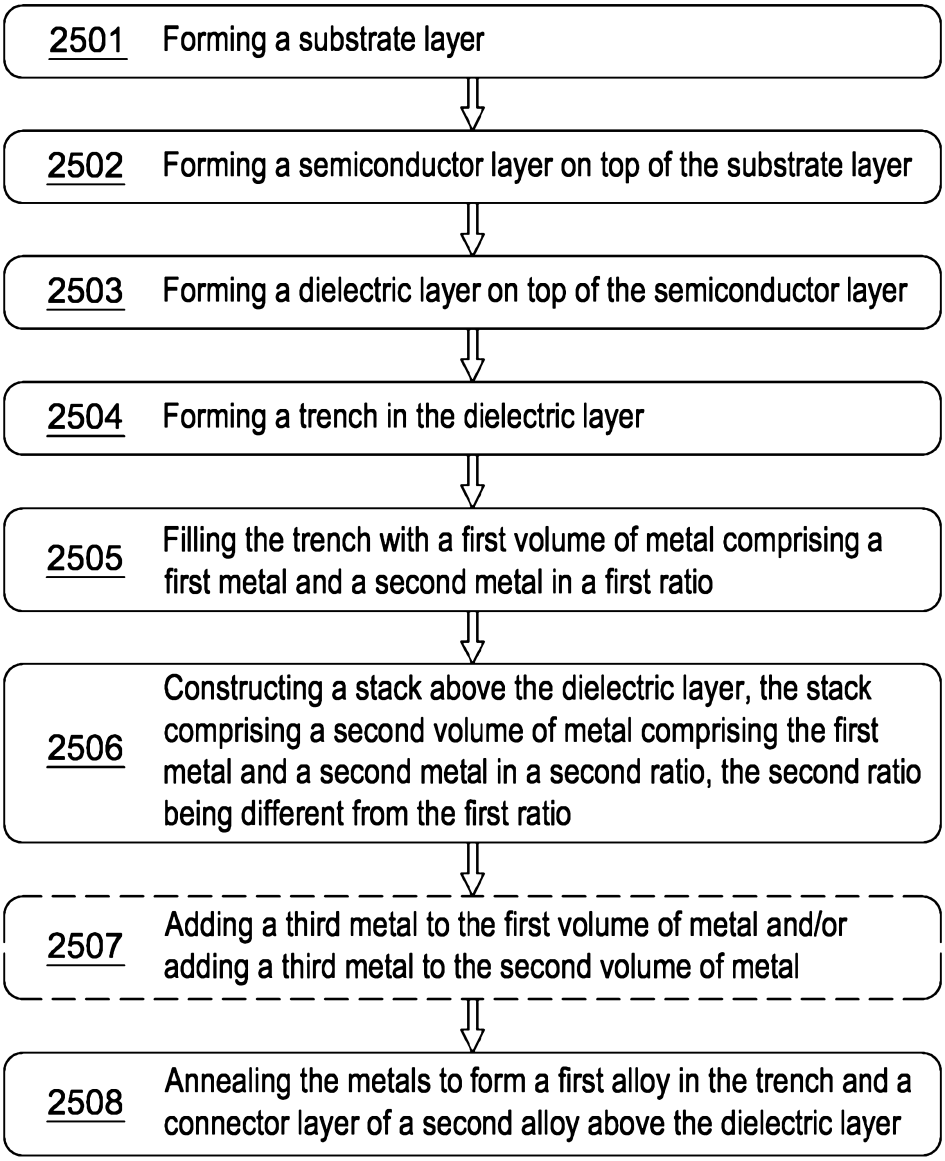


Figure 25

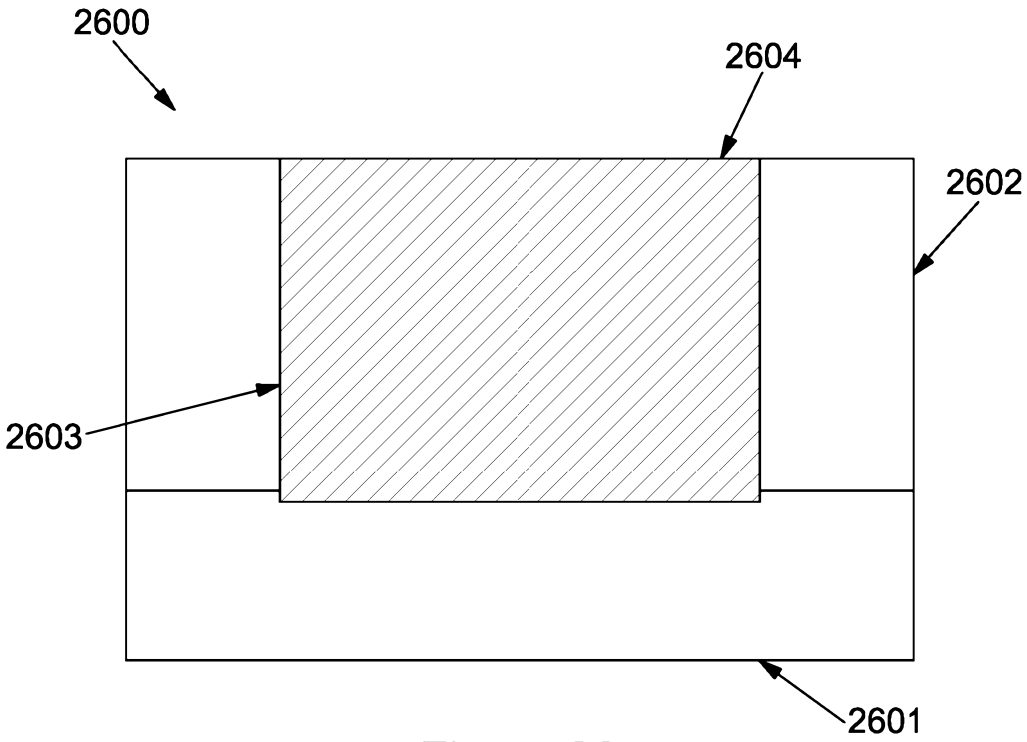
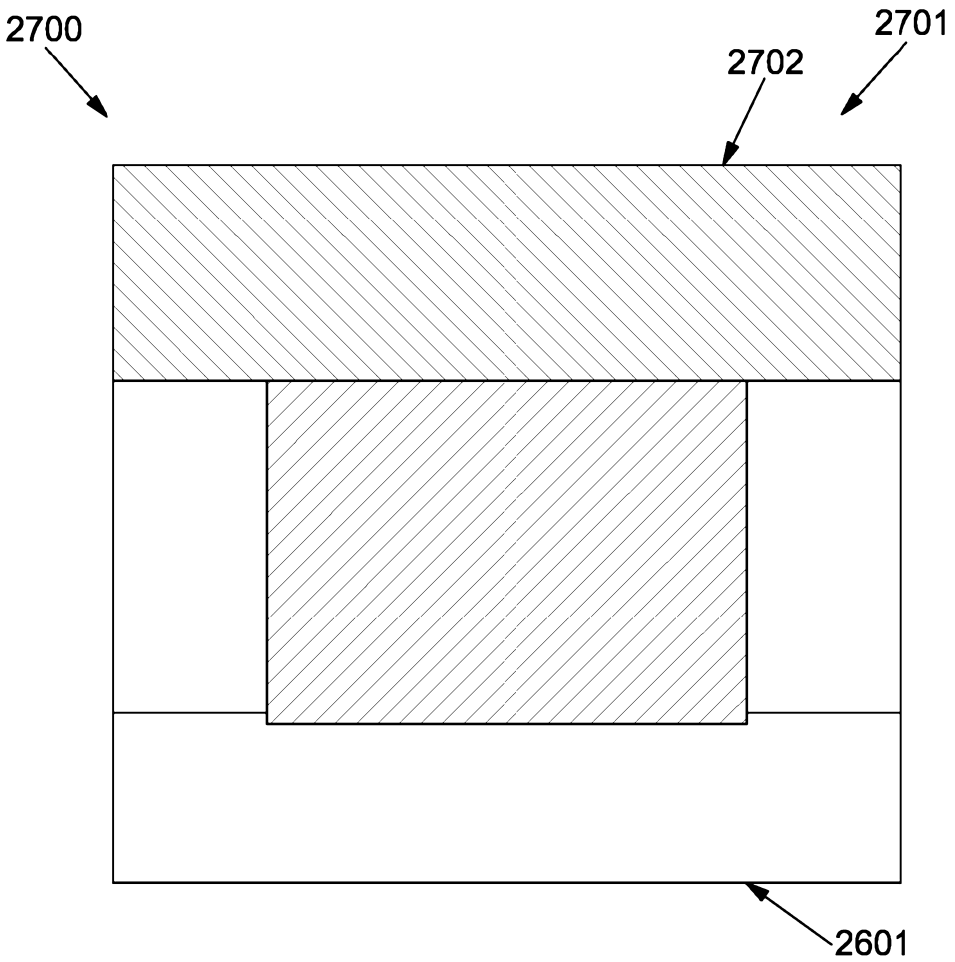


Figure 26



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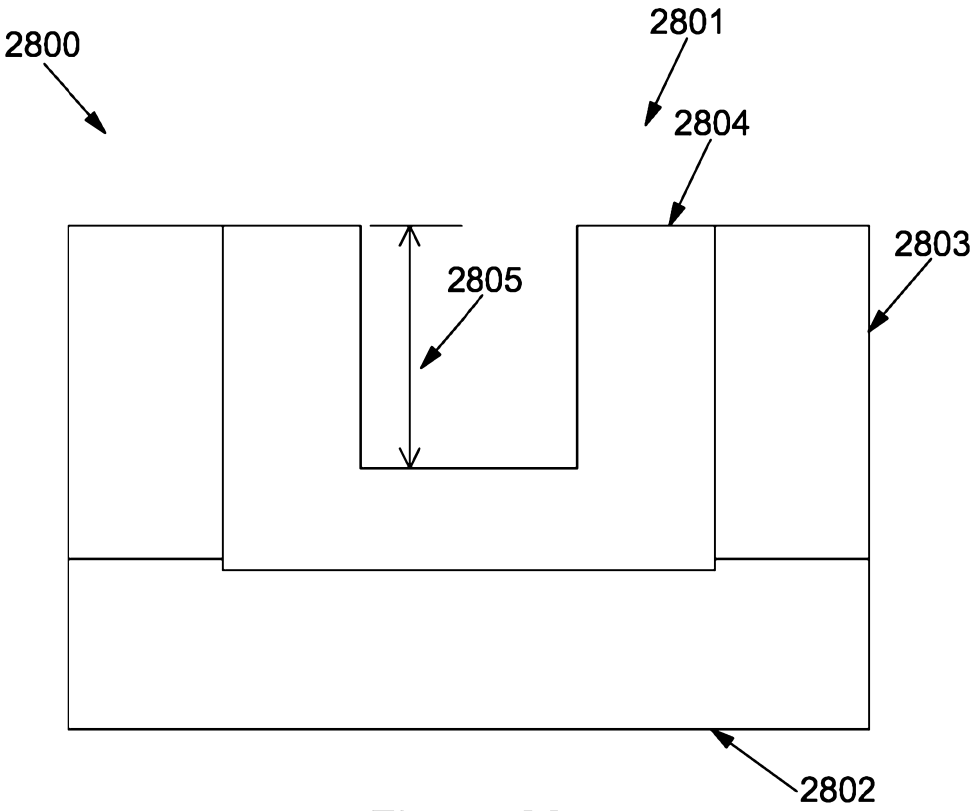

Figure 28

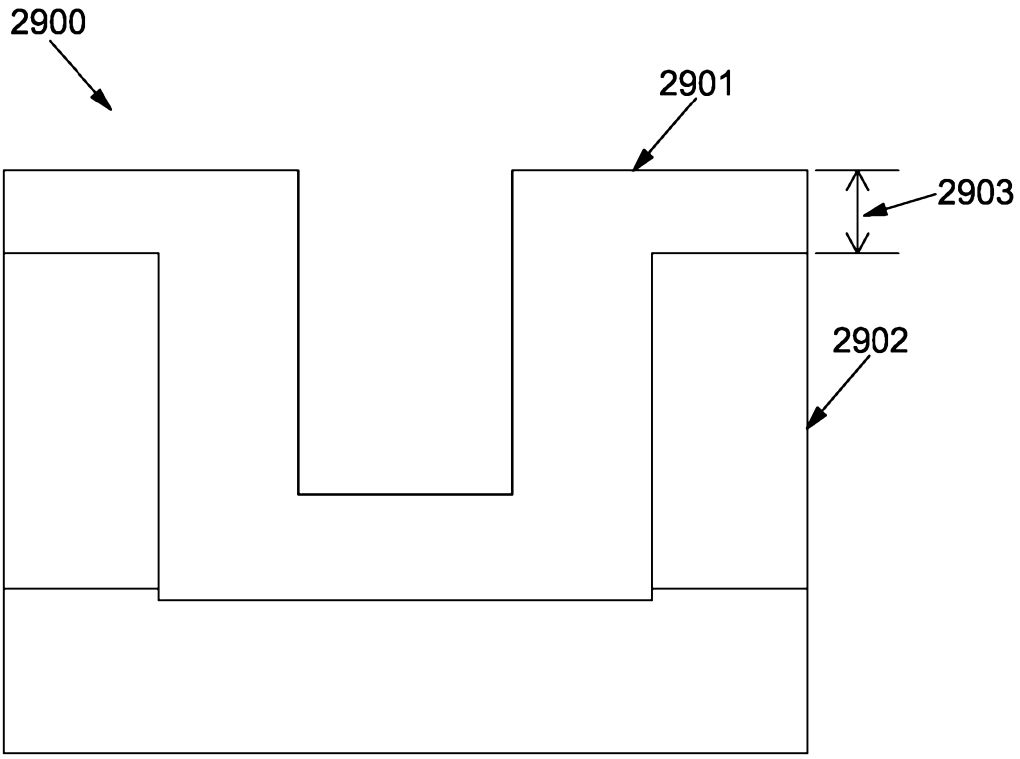

Figure 29

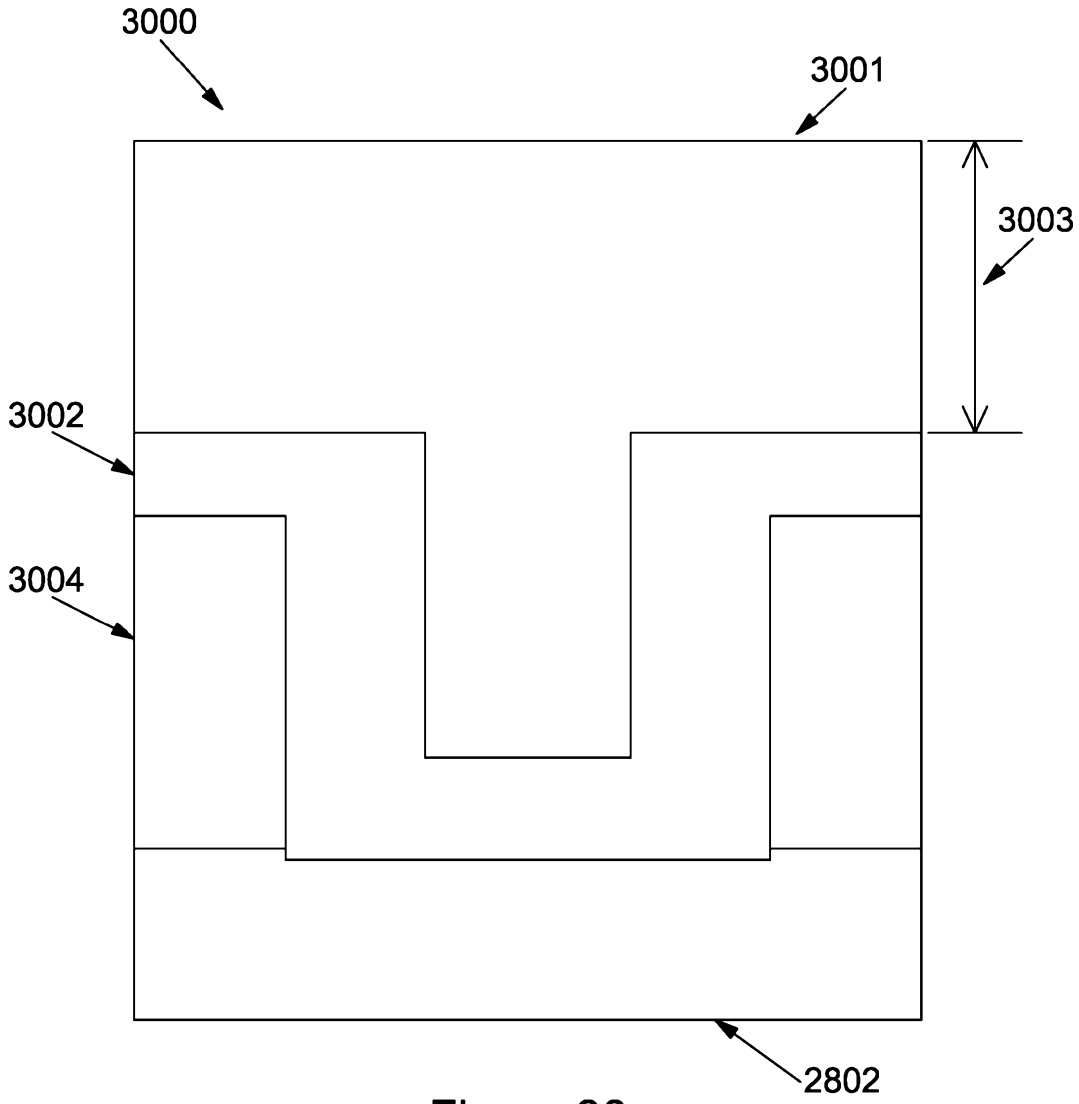

Figure 30

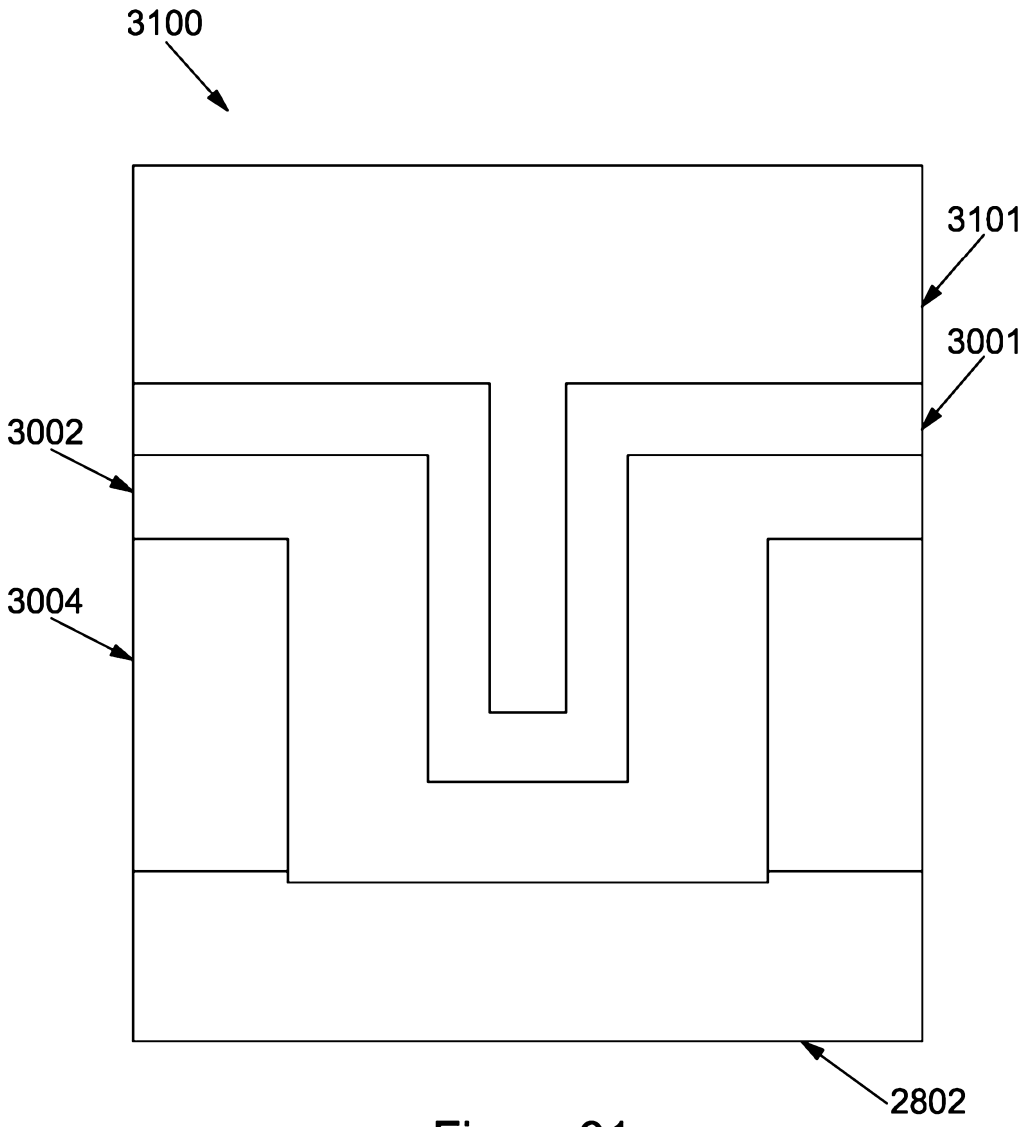

Figure 31

Ohmic contacts in semiconductor devices

Field of disclosure

The invention relates to ohmic contacts in semiconductor devices.

Background

A high-electron-mobility transistor (HEMT) is a field-effect transistor incorporating a junction between two materials with different band gaps and lattice constants as the channel instead of a doped region. Such a junction is known as a hetero-junction. Thanks to the spontaneous polarization jump and/or piezoelectric field induced by crystal strain at the hetero-junction, a potential distortion occurs which forms a channel. In the case that the potential distortion is sufficient to form localization potential, the electrons are accumulated at the hetero-junction interface. These electrons form a layer known as a two dimensional electron gas. Within this region the electrons are able to move freely because there are no intentionally introduced doping or other scattering centers with which electrons will collide with significant impact into mobility and the mobility of the electrons in the gas is very high. In a GaN HEMT, doping is usually not used, and instead electrons are attributed to the states at the barrier surface.

A bias applied to the gate formed as a Schottky barrier diode is used to modulate the number of electrons in the channel formed from the 2D electron gas and in turn this controls the conductivity of the device. This can be compared to the more traditional types of FET where the width of the channel is changed by the gate bias. Figure 1a is an energy momentum diagram 100 of a typical GaAs based HEMT. There is illustrated a larger bandgap semiconductor 101, a smaller bandgap semiconductor 102, donors 103 and electron gas 104. Figure 1b shows a band diagram of a GaN HEMT.

Figure 2 is a perspective view of an arrangement of a typical HEMT 200. There is a source 201, gate 202 and drain 203 as in any field effect transistor. The body 204 of the device comprises a substrate 205, a two-dimensional electron gas (2DEG) 206, a spacer 207, a barrier layer 208 and capping layers 209, 210.

Although they give good performance, the manufacture of HEMTs, and particularly the provision of low resistance ohmic contacts, is challenging. The channel layer, which enables the formation of the 2DEG, lies typically in the region of 1 to 50 nm below the

surface of the barrier layer. This distance is too high to provide tunnelling carrier transport via an isolated barrier layer placed between the ohmic contact metal and channels. Special treatment is required involving creating a recess in the barrier layer and/or high temperature annealing. During annealing a chemical reaction between ohmic metal stack and semiconductor takes place providing low resistance ohmic contact. In order to implement such an approach, well-defined metals stacks thicknesses have to be controlled to provide a correct metal alloy, so that during annealing the required chemical reaction occurs. It limits freedom for designing the Front End of Line (FEOL) and Back End of Line (BEOL).

Summary

The invention provides semiconductor arrangements and methods of fabricating such, as set out in the accompanying claims.

Preferred embodiments will now be described, by way of example only, with reference to the accompanying figures.

Brief description of figures

Figure 1a is an energy momentum diagram illustrating the bandgaps of an HEMT according to the prior art;

Figure 1b is a band diagram of a GaN HEMT;

Figure 2 is a cross-sectional view of a High Electron Mobility Transistor according to the prior art;

Figure 3 is a plan view of a fragmented ohmic contact according to an embodiment;

Figure 4 is a plan view of the current flow from a conventional ohmic contact according to the prior art;

Figure 5 is a plan view of the current flow from a fragmented ohmic contact according to an embodiment;

Figure 6 is a plan view of a fragmented ohmic contact according to an embodiment;

Figure 7 is a plan view of a fragmented ohmic contact according to an embodiment;

Figure 8 is a cross sectional view of an ohmic contact embedded into the body of a semiconductor device according to an embodiment;

Figure 9 is a flow chart of a method of constructing a semiconductor arrangement according to an embodiment;

Figure 10 is a cross sectional view of a metal stack for use in the manufacture of an ohmic contact according to the prior art;

Figure 11 is a cross sectional view of the stack of Figure 9 after annealing;

Figure 12 is a cross sectional view of a metal stack for use according to an embodiment;

Figure 13 is a cross sectional view of the trench of Figure 12;

Figure 14 is a cross sectional view of the embodiment of Figure 12 after the annealing process is completed;

Figure 15 is a cross sectional view of a contact, showing the relevant resistances;

Figure 16 is a graphical illustration of the current density against length in such an arrangement;

Figure 17 is a cross sectional representation of two ohmic contacts of different size

Figure 18(a) is a plan view of a cylindrical ohmic contact fragment;

Figure 18(b) is a cross sectional view of the same embodiment ;

Figure 19(a) is a plan view of an ohmic contact fragment according to another embodiment;

Figure 19(b) is a cross sectional view of the embodiment of Figure 19(a);

Figure 20(a) is a plan view of an ohmic contact with an obround shape;

Figure 20(b) is a plan view of an ohmic contact with an elliptic shape;

Figure 20(c) is a plan view of an ohmic contact with an obround shape with a greater length to width ratio than the embodiment of Figure 20(a);

Figure 21 is a flow chart showing the steps of manufacturing an ohmic contact in a semiconductor section according to an embodiment;

Figure 22 is a cross section of a semiconductor section illustrating the result of a first step of a method according to an embodiment;

Figure 23 is a cross section of a semiconductor section illustrating the result of a second step of a method according to an embodiment;

Figure 24 is a cross section of a semiconductor section illustrating the result of a third step of a method according to an embodiment;

Figure 25 is a flow chart illustrating a method of constructing an ohmic contact in a semiconductor section according to another embodiment of the invention;

Figure 26 is a cross sectional view of a semiconductor section illustrating the result of a first step of a method according to an embodiment;

Figure 27 is a cross sectional view of a semiconductor section illustrating the result of a second step of a method according to an embodiment;

Figure 28 is a cross sectional view of a semiconductor section illustrating the result of a first step of a method according to an embodiment;

Figure 29 is a cross sectional view of a semiconductor section illustrating the result of a second step of a method according to an embodiment;

Figure 30 is a cross sectional view of a semiconductor section illustrating the result of a third step of a method according to an embodiment; and

Figure 31 is a cross sectional view of a semiconductor section at a stage before annealing according to another embodiment of the invention.

Detailed description

Embodiments will now be described more fully hereinafter with reference to the accompanying drawings, in which certain embodiments are shown. However, other embodiments in many different forms are possible within the scope of the present disclosure. Rather, the following embodiments are provided by way of example so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to those skilled in the art.

The present disclosure provides an improved ohmic contact and method of manufacture. The structure of the contact is based on the recognition that for an effective ohmic contact, the key parameter is not the area of the contact, but the perimeter which is in contact with the semiconductor with lateral topology of the devices. To take advantage of this phenomenon, an ohmic contact is provided that is fragmented into multiple sections, thus increasing the perimeter for a given area of contact. Figure 3 is a plan view of a fragmented ohmic contact according to an embodiment. The fragmented ohmic contact structure 300 comprises a plurality of metallic contacts 301 located within a semiconductor layer 302. In an embodiment, all of the contacts are connected to a single external electrode, which provides a terminal to the semiconductor device. In an embodiment the arrangement illustrated in Figure 3 is the terminal of a transistor, i.e. one of the gate, source or drain. An advantage of the fragmentation of the ohmic contact can be seen by comparison of the current flow from a conventional ohmic contact with that provided by a contact according to the present disclosure. Figure 4 is a plan view showing the current flow from a conventional ohmic contact. Figure 4 illustrates a single ohmic contact 401, conventionally arranged as a single block within the active region of the semiconductor device 402. The current 403 flows from the perimeter 404 of the contact. Figure 5 is a plan view showing the improved efficiency of the fragmented contact, and shows the current flow from a

fragmented ohmic contact according to an embodiment of the present disclosure. Figure 5 illustrates the current flows 503 from the ohmic contact fragments 501 into the active region 502, due to the increase in the perimeter 504. By fragmenting the ohmic contact, an increase in the perimeter for a given overall area of contact is possible.

Other configurations for the fragmented ohmic contact are possible. Figures 6 and 7 are plan views of alternative embodiments. Figure 6 illustrates an arrangement comprising ohmic contact fragments 601 with substantially circular shapes. Figure 7 illustrates an arrangement comprising ohmic contact fragments 701 with substantially triangular shapes. The person skilled in the art will recognise that a very large number of such arrangements are possible which fall within the scope of the invention. The invention is not limited to any one arrangement of contact fragments.

Figure 8 is a cross-sectional view of a single ohmic contact fragment located within a semiconductor device, according to an embodiment. Figure 8 illustrates the layers of the device, which comprise a substrate 801 and buffer 802. On top of the buffer is the spacer layer 803 (optional) and a barrier layer 804. In embodiments, there are also a number of optional layers, such as a cap layer 805, and one or more dielectric layers 806, 807. In an embodiment, the ohmic contact 808 comprises a metal stack with three metal layers 809, 810, 811. In an embodiment, the buffer layer comprises a stack of (Al)GaN layers with varied Al composition. In another embodiment, the buffer layer comprises InGaN with varied In composition. In yet another embodiment, the buffer layer comprises GaN. In an embodiment, the barrier layer comprises AlGaN. In an embodiment, at least one dielectric layers comprises SiN or SiO_2. The person skilled in the art will appreciate that any suitable semiconductor or dielectric material may be selected for each of the layers, and that the invention is not limited to any particular material or combination of materials.

In the embodiment illustrated in Figure 8, the metal stack comprises three metal layers. In another embodiment, two metal layers are used. The person skilled in the art will appreciate that other arrangements are possible and that the invention is not limited to any particular arrangement of the metal stack.

The process of creating the fragmented ohmic contact comprises forming trenches for filling with a metal stack. In an embodiment, the trenches are formed by etching the one or more dielectric layers, the cap layer (if present), and the barrier layer.

Figure 9 is a flow chart illustrating the steps of a method of constructing a semiconductor arrangement as described herein. The method comprises forming a substrate layer (901), forming a semiconductor layer on top of the substrate layer (902), forming a dielectric layer on top of the semiconductor layer (903), and forming a plurality of trenches in the dielectric layer (904). The plurality of trenches may also be formed in the semiconductor layer. The method further comprises filling each of the plurality of trenches with a volume of metal comprising a first metal and a second metal in a defined ratio (905), and annealing the metals to form an alloy (906).

Each of the plurality of trenches formed in step (904) may be a trench as illustrated in Figure 8. The plurality of trenches may after the step of annealing (906) form the fragmented contacts 301, 501, 601 and 701 shown in Figures 3 and 5 to 7. Figure 10 is a cross-sectional view of a metal stack for use in the manufacture of an ohmic contact according to the prior art. The stack consists of two metal layers, 1001, 1002 located on an EPI layer (typically III-N) 1003. Figure 11 is a cross-sectional view of the stack of Figure10 after annealing. The composition of the metal alloy will be defined by the relative thicknesses of the metal layers 1001 and 1002 according to the following formula:

Mixture of metal 1 and metal 2: $Met1/Met\ 2 = th1/th2$ Equation 1

In this equation th1 and th2 are the thicknesses of the metal layers 1002 and 1001 respectively, and Met1/Met2 is the ratio of the two metals in these layers.

Figure 12 is a cross-sectional view of a metal stack for use according to an embodiment. As in the conventional arrangement, there are two metals 1201, 1202 in the stack. However, in the embodiment of Figure 12, there is an additional dielectric layer 1203. There is a trench 1205 etched into the EPI layer 1204, which is filled with metal.

The process for constructing the ohmic contact is based on the following assumptions:

1) Metal diffusion is very small.
2) Metal deposition is conformal.
3) The metals get mixed completely within the trench.

The very low level of metal diffusion allows the composition in the trench to be different from that in the stack above the dielectric layer. The metal deposition being conformal

means that the thickness of the metal layer 1 is constant along the dielectric and in the trench (thickness th1 in Figures 12 and 13). This latter assumption means that a simple derivation of a formula for the alloy ratio in the trench is possible. The ratio is given by the cross sectional areas of the respective metal components.

The contact illustrated in Figure 12 may be formed by the method illustrated in Figure 9. The EPI layers 1204, the dielectric layer 1203, the trench 1205 and the metal layers 1202 and 1201 may be formed in steps (902), (903), (904) and (905) respectively.

Figure 13 is a cross section of the trench 1301 of Figure 12. Area A1 is the cross sectional area of the section consisting of metal 1 and A2 is the cross sectional area of the section consisting of metal 2. Area A1 is given by:

$$A1 = (th3 - th1) \times (d1 - d2) \qquad \text{Equation 2}$$

$$A2 = (th3 \times d1) - (th3 - th1) \times (d1 - d2) \qquad \text{Equation 3}$$

The ratio of the areas and hence the ratio of the metals is therefore given by:

$$\text{Metal2/Metal 1} = (th3 - th1) \times (d1 - d2)/((th3 \times d1) - (th3 - th1) \times (d1 - d2)) \qquad \text{Equation 4}$$

D2 is given by:

$$d2 = (d1 - 2 \times th1) \qquad \text{Equation 5}$$

Hence the metal ratio of the alloy in the trench is given by:

$$\text{Metal2/Metal 1} = (th3 - th1) \times (d1 - d1 - 2 \times th1)/((th3 \times d1) - (th3 - th1) \times (d1 - d1 - 2 \times th1)) \qquad \text{Equation 6}$$

Hence the ratio of the metals is determined by the thickness of the dielectric, the width of the trench and the thickness of the layer comprising metal 1.

Figure 14 is a cross-sectional view 1400 of the embodiment of Figure 12 after the annealing process is completed. In the region 1401 above the dielectric 1402, the composition of the alloy is the same as in the conventional process. However, within the trenches, the composition is different.

The transfer length is the average length that a carrier travels within the semiconductor under the contact before it flows into the contact. In a bulk semiconductor, the transfer length depends on the vertical resistance between the contact and the semiconductor and the resistance of the semiconductor under the contact.

Figures 15 and 16 show a contact in a GaN HEMT, in which the the AlGaN barrier is not completely etched. In this case, the transfer length depends on the vertical resistance of the AlGaN barrier (1501) between contact (1500) and the 2DEG (located at the 1502/1501 interface) and the 2DEG lateral resistance.

Figure 15 is a cross-sectional view of a contact, showing the relevant resistances. A metallic contact 1500 is located on top of a first semiconductor layer 1501, which in an embodiment is Aluminium Gallium Nitride, which in turn is located on top of a second semiconductor layer 1502, which in an embodiment is (Al)GaN. The person skilled in the art will appreciate that other semiconductors may be used and the invention is not limited to particular materials for either layer. The vertical resistance 1503 and the semiconductor or 2DEG resistance 1504 are shown in Figure 15. If the semiconductor or 2DEG resistance is much higher than the vertical resistance then the transfer length is very short. Conversely, a contact with a vertical resistance much higher than the semiconductor or 2DEG resistance would result in a very long transfer length.

Figure 16 is a graphical illustration of the current density against length in such an arrangement. Above the graph is a cross section of a typical semiconductor device 1601, comprising contacts 1602, 1603 and a semiconductor section 1604. Current movement from the first contact to the semiconductor 1605, within the semiconductor 1606 and from the semiconductor to the second contact 1607, are illustrated. In the graph below, current density 1608 is plotted against distance 1609, with the transfer length 1610 indicated. The optimal contact size in approximately the same as the transfer length. This enables the area of the contact to be used most efficiently.

Figure 17 is a cross sectional representation of two ohmic contacts of different size, illustrating optimal contact size. For reference, a graphical representation 1701 of current density 1702 against distance 1703 is provided, which shows the transfer length 1704. Two contacts, the first contact 1705, located on a semiconductor section 1706, and a second contact 1707, located on a semiconductor section 1708, are illustrated. The first contact 1705 is of optimal size, being approximately the size of the transfer length. That is, at least one dimension of the ohmic contact 1705 is

substantially equal to the transfer length 1704. For example, said dimension may be within 10% of the transfer length 1704, or preferably within 5% of the transfer length 1704. The second contact 1707 is larger than the transfer length, and therefore has a useless section 1708, which does not contribute to current injection into the semiconductor.

A further degree of design freedom is the shape of the contacts. Figure 18(a) is a plan view of a cylindrical ohmic contact fragment 1801. Figure 18(b) is a cross sectional view of the same embodiment. The radius of the cylinder should be approximately equal to the transfer length. Figures 18(a) and (b) illustrates the pre-annealing arrangements of the first metal M1 1802 and the second metal M2 1803 which are the constituent metals of the alloy to be formed by annealing. Figure 19(a) is a plan view of an ohmic contact fragment according to another embodiment. In the embodiment of Figure 19(a), the ohmic contact has an obround surface. Figure 19(b) is a cross sectional view of the embodiment of Figure 19(a). Figures 19(a) and (b) illustrates the pre-annealing arrangements of the first metal M1 1902 and the second metal M2 1903 which are the constituent metals of the alloy to be formed by annealing. The embodiments of Figures 18 and 19 comprise an ohmic contact fragments shaped as right circular cylinder and an obround respectively. However, the person skilled in the art would appreciate that there are a very large number of possible alternative shapes that could be used, such as a cuboid, a triangular based section etc.

Since the current density under the contact area decreases away from the edge of the contact, it is beneficial to have the shape with the higher perimeter/area ratio. Figures 20(a), 20(b) and 20(c) are plan views of ohmic contacts with different shapes, illustrating this principle. Figure 20(a) illustrates a contact with an obround shape. The ratio of the perimeter to area is approximately:

Perimeter to area ratio = $3/(2*r)$ Equation 7

Figure 20(b) illustrates a contact with a circular shape. The ratio of the perimeter to area is approximately:

Perimeter to area ratio = $5/(4*r)$ Equation 8

Figure 20(c) illustrates a contact with an obround shape, but with a greater length to width ratio than the embodiment of Figure 20(a). The ratio of the perimeter to area is approximately:

Perimeter to area ratio = 2/r Equation 9

The optimal shape of contact for creating an alloy with the desired local metal composition may be however different to the shape required to provide the optimal perimeter to area ratio. Hence there is a trade-off for each combination of metal stack, between the requirements for annealing condition, EPI material, device design and other parameters in order to produce the optimal shape for providing the best ohmic contact performance.

Figure 21 is a flow chart showing the steps of manufacturing an ohmic contact in a semiconductor section. The section may comprise one or more layers, such as a dielectric layer, a buffer layer, and a barrier layer. The person skilled in the art will appreciate that the method is applicable to different types of semiconductor sections and that the invention is not limited to any particular arrangement of layers. The method comprising the steps of forming a trench in a dielectric layer (and optionally in a semiconductor layer) (2101), forming within the trench a first layer of a first thickness on top of a semiconductor layer and a second layer of a second thickness on top of the first layer, wherein the first layer comprises a first metal, and the second layer comprises a first region disposed between a first trench wall and a first distance from the trench wall, a second region disposed between said first distance and a second distance from the trench wall, and a metal region disposed between said second distance and a second trench wall, wherein the first and third regions consist of the first metal and the second region consists of a second metal (2102). Optionally, the first and second layers are formed so that the second layer extends to a distance equal to the first thickness above an upper surface of the dielectric layer (2104). The method further comprises annealing the metals to form an alloy (2103).

The stages of the construction of the ohmic contact are illustrated in Figures 22 to 24. Figure 22 is a cross section of a semiconductor section 2201 illustrating the result of the first step (2001) of the method according to an embodiment. A trench 2202 has been formed in the section 2201. Figure 23 is a cross section of the semiconductor section after the second stage (2002) has been completed. A first metal layer 2301 has been formed in the trench to a first depth 2302. The first metal layer comprises a first metal. In an embodiment, the first metal is titanium However, the person skilled in the art will appreciate that a wide range of metals are suitable and the invention is not limited to any one metal. A wide range of options is provided in Tables 1 and 2.

Figure 24 is a cross sectional view of the semiconductor section after the completion of the third stage (2004) of the method according to an embodiment. Above the first metal layer 2401, a second metal layer 2402 has been formed. This second layer comprises three regions. The first region 2403 comprises the first metal, the second region 2404 comprises the second metal (e.g. Aluminium) and the third region 2405 comprises the first metal. The first region extends from a first side 2406 of the trench to a first distance 2407. The second region extends from the first distance 2407 to a second distance 2408. The third region extends from the second distance 2408 to a second side of the trench 2409, the second side being opposite to the first side. Although shown as separate steps in Figures 22 to 24, the regions 2403 and 2405 are generally formed at the same time as the first metal layer 2401.

Table 1 shows a selection of possible metal stacks which may be formed and the associated contact resistances that can be expected. The skilled person will appreciate that the invention is not limited to this selection of alloys. Table 2 shows another selection of possible metal stacks to form ohmic metal on AlGaN without the use of gold (Au).

Table 1 Ohmic contacts to AlGaN/GaN heterostructures

Metal Layers (nm)	d_{AlGaN} (nm)	χ_{AL} (%)	Annealing conditions	ρ (Ωcm^2)
Ti/Al (30/71 nm)	33 nm	15%	950 ºC for 20 s in N_2	2.2×10^{-5}
Ti/Al (30/71 nm)	33 nm	15%	950 ºC for 20 s in N_2 (with pre-annealing)	3.2×10^{-6}
Ti/Al (20/150 nm)	34 nm	22%	950 ºC for 10 min in N_2	5×10^{-5}
Ti/Al (20/150 nm)	34 nm	22%	950 ºC for 10 min in N_2 (with implantation)	5×10^{-6}
Ti/Ta/Al (thickness N.A.)	16 nm	35%	950 ºC for 4 min in N_2	5.1×10^{-4}
Ta/Ti/Al (thickness N.A.)	10 nm	33%	950 ºC for 4 min in N_2	5.3×10^{-7}
Ti/Al/Ni/Au (15/220/40/50 nm)	30 nm	24%	800 ºC for 60 s in Ar	2.8×10^{-6}

Ti/Al/Ni/Au (30/180/40/150 nm)	18 nm	25%	900 ºC for 30 s in N_2	7.3×10^{-7}
Ti/Al/Pt/Au (15/85/50/50 nm)	7.5 nm	30%	850 ºC for 60 s in N_2	2.2×10^{-6}
V/Al/Pt/Au (15/85/50/50 nm)	7.5 nm	30%	850 ºC for 60 s in N_2	1.0×10^{-5}
Ti/Al/Pt/Au (20/100/40/80 nm)	40 nm	30%	850 ºC for 45 s in N_2	2×10^{-5}
Ti/Al/Pt/W/Ti/Au (20/100/40/50/80 nm)	40 nm	30%	850 ºC for 45 s in N_2	1.6×10^{-5}
Ti/Al/Pt/WSi/Ti/Au (20/100/40/50/80 nm)	40 nm	30%	850 ºC for 45 s in N_2	1.0×10^{-5}
Ti/Al/Ir/Au (30/200/50/20 nm)	40 nm	30%	850 ºC for 30 s in N_2	4.6×10^{-5}
Ti/Al/Nb/Au (15/60/35/50 nm)	35 nm	30%	850 ºC for 100 s in N_2	5×10^{-6}
Ti/Al/Mo/Au (15/60/35/50 nm)	25 nm	20%	800 ºC in N_2	3×10^{-6}
Mo/Al/Mo/Au (15/60/35/50 nm)	25 nm	20%	650 ºC in N_2	9×10^{-7}
V/Al/Mo/Au (15/60/35/50 nm)	25 nm	20%	700 ºC in N_2	2.7×10^{-6}
Ti/Al (30/120 nm)	27 nm	25%	500 ºC in N_2	4.7×10^{-5}
Ti/Al/Ni/Au (30/120/40/50 nm)	27 nm	25%	700 ºC in N_2	6.5×10^{-6}
Ta/Ti/Al/Ni/Au (10/30/120/40/50 nm)	27 nm	25%	700 ºC in N_2	7.5×10^{-7}
Ti/Al/Mo/Au (15/60/35/50 nm)	21.5 nm	30%	800 ºC for 30 s in N_2	2.96×10^{-7}
Ta/Al/Mo/Au (15/60/35/50 nm)	21.5 nm	30%	800 ºC for 30 s in N_2	1.09×10^{-6}
Ti/Al/Mo/Au (15/60/35/50 nm)	24 nm	30%	750 ºC for 30 s in N_2	1.0×10^{-6}

Ti/Al/Pt/Au (15/60/35/50 nm)	24 nm	30%	750 ºC for 30 s in N_2	1.5×10^{-6}
Ti/Al/Ir/Au (15/60/35/50 nm)	24 nm	30%	750 ºC for 30 s in N_2	2.8×10^{-6}
Ti/Al/Ni/Au (15/60/35/50 nm)	24 nm	30%	750 ºC for 30 s in N_2	1.5×10^{-6}
Ti/Al/Ta/Au (15/60/35/50 nm)	24 nm	30%	850 ºC for 30 s in N_2	4.5×10^{-6}
Ti/Al/Nb/Au (15/60/35/50 nm)	24 nm	30%	850 ºC for 30 s in N_2	3.5×10^{-6}
Ti/Al/Ti/Au (15/60/35/50 nm)	24 nm	30%	950 ºC for 30 s in N_2	3.5×10^{-6}
Ti/Al/Mo/Au (15/60/35/50 nm)	21 nm	28%	850 ºC for 30 s in N_2	2.96×10^{-7}
Nb/Ti/Al/Ni/Au (10/20/100/40/50 nm)	32 nm	25%	850 ºC for 35 s in N_2	1.5×10^{-5}
Nb/Ti/Al/Ni/Au (20/20/100/40/50 nm)	32 nm	25%	850 ºC for 35 s in N_2	3.7×10^{-6}
Ti/Al/Ti/Au (20/80/40/100 nm)	23 nm	30%	850 ºC for 30 s in N_2	6.50×10^{-6}
Ti/Al/Ni/Au (20/80/40/100 nm)	23 nm	30%	850 ºC for 30 s in N_2	2.50×10^{-6}
Ti/Al/Ta/Au (20/80/40/100 nm)	23 nm	30%	850 ºC for 30 s in N_2 (with 50 nm SiN encapsulation layer)	7.27×10^{-7}
Ti/Al/Ni/Au (20/180/55/45 nm)	22 nm	21.5%	870 ºC for 50 s in N_2	2.13×10^{-4}
Ti/Al/Ni/Au (20/120/55/45 nm)	22 nm	21.5%	870 ºC for 50 s in N_2	9.7×10^{-7}
Ti/Al/Ni/Au (15/200/50/50 nm)	50 nm	22%	850 ºC for 60 s in Ar	7.0×10^{-5}

Table 2 Au-free Ohmic contacts to AlGaN/GaN heterostructures

Metal Layers (nm)	d_{AlGaN} (nm)	χ_{AL} (%)	Annealing conditions	Contact resistance, R_C (Ωmm)
Ta/Al/Ta (10/280/20 nm)	22 nm	14%	550 ºC for 60 s in N_2	0.06
Ta/Al/Ta (10/280/20 nm)	25 nm	25%	600 ºC for 60 s in N_2	0.28
Ti/Al/Ti/TiN (thickness N.A.)	10 nm	25%	550 ºC for 90 s in N_2	1.25
Ta/Al (70/200 nm)	25 nm	25%	700 ºC for 60 s in Ar	36.3
Ti/Al (70/200 nm)	25 nm	25%	500 ºC for 60 s in Ar	1.8
Ta/Si/Ti/Al/Ni/Ta (5/5/20/120/40/30 nm)	18 nm	26%	850 ºC for 30 s in N_2	0.22
Ti/Al/W (60/100730 nm)	17.5 nm	26%	870 ºC for 30 s in N_2	0.49
Ti/Al/W (20/100/20 nm)	10 nm	25%	600 ºC for 60 s in N_2	0.65
Ti/Al/TiN (0.02x/x/60 nm)	15 nm	20%	550 ºC for 90 s in N_2	0.62
Ti/Al/TiN (0.10x/x/60 nm)	15 nm	20%	550 ºC for 90 s in N_2	1.63
Ti/Al/TiN (0.20x/x/60 nm)	15 nm	20%	550 ºC for 90 s in N_2	2.00

Figure 25 is a flow chart illustrating a method of constructing an ohmic contact in a semiconductor section according to another embodiment of the invention. The method comprises forming a substrate layer (2501), forming a semiconductor layer on top of the substrate layer (2502), forming a dielectric layer on top of the semiconductor layer (2503), and forming a trench in the dielectric layer (2504). The method further comprises filling the trench with a first volume of metal comprising a first metal and a second metal in a first ratio (2505), constructing a stack above the dielectric layer, the stack comprising a second volume of metal comprising the first metal and a second

metal in a second ratio, the second ratio being different from the first ratio (2506), and then annealing the metals to form a first alloy in the trench and a connector layer of a second alloy above the dielectric layer (2508).

The method may optionally comprise adding a third metal to the first volume of metal and/or adding a third metal to the second volume of metal (2507).

The stages constructing of the ohmic contact are illustrated in Figures 26 and 27. Figure 26 shows a cross sectional view of a semiconductor section 2600 with a semiconductor layer 2601, a dielectric layer 2602, and a trench 2603 in the semiconductor layer 2601 and the dielectric layer 2602. Figure 26 shows the semiconductor section in a stage after the step (2505) of filling the trench 2601 with a first volume of metal 2604 comprising a first metal and a second metal.

Figure 27 shows the semiconductor section 2700 at a stage after the step (2506) of constructing a stack 2701 comprising a second volume of metal 2702 comprising the first metal and the second metal.

Figure 28 is a cross sectional view of a semiconductor section 2800 in a stage of a method according to an embodiment. The trench 2801 in the semiconductor layer 2802 and the dielectric layer 2803 is filled with a first metal 2804 to a first depth 2805. That is, the first volume of metal (in the trench 2801) has been partially filled with the first metal 2804 as part of the fifth step (2505). A third volume inside the trench 2801 remains unfilled.

Figure 29 shows a cross sectional view of the semiconductor section 2900 in a subsequent stage. A layer of the first metal 2901 is deposited on the dielectric layer 2902. The metal layer has a thickness 2903 above the dielectric layer 2902. That is, the second volume of metal (above the dielectric layer 2502) is partially filled with the first metal 2901 as part of the sixth step (2506).

Figure 30 shows a cross sectional view of the semiconductor section 3000 after completing a further stage. A second metal layer 3001 is deposited on top of the first metal layer 3002 as part of the fifth (2505) and sixth (2506) steps of the method. The second metal layer 3001 has a thickness 3003 above the first metal layer 3002. The first volume of metal is filled with the first metal and the second metal in the trench, wherein the second metal fills the third volume (contained within the first volume). The second volume of metal comprises the first metal layer 3002 and the second metal

layer 3001 above the dielectric layer 3004. After depositing the second metal layer 3001, the metals are annealed to form an alloy (2507).

Figure 31 shows a cross sectional view of the semiconductor section 3100 constructed according to the method illustrated in Figure 25. The figure shows the stage directly preceding the step of annealing (2507). A third metal 3101 has been added to the first volume of metal and to the second volume of metal in the optional step (2507). Hence, Figures 30 and 31 show to alternative embodiments of filling (2505) the first metal volume and constructing (2506) the stack comprising the second metal volume according the method illustrated in Figure 25.The present disclosure has mainly been described above with reference to a few embodiments. However, as is readily appreciated by a person skilled in the art, other embodiments than the ones disclosed above are equally possible within the scope of the present disclosure, as defined by the appended claims.

CLAIMS:

1. A semiconductor arrangement comprising:
a substrate;
a dielectric layer;
a semiconductor layer disposed between the substrate and the dielectric layer;
a plurality of trenches formed in the dielectric layer;
a plurality of metal contacts located in said plurality of trenches; and
a metallic connector layer electrically connecting said metal contacts.

2. A semiconductor arrangement according to claim 1, wherein said plurality of trenches are formed in the dielectric layer and the semiconductor layer.

3. A semiconductor arrangement according to claim 1 or 2, wherein at least one dimension of at least one of said metal contacts is substantially equal to a transfer length of an interface between the metal contact and said semiconductor layer.

4. A semiconductor arrangement according to any preceding claim, wherein said metal contacts comprise a first metal alloy.

5. A semiconductor arrangement according to claim 4, wherein the metallic connector layer comprises a second metal alloy.

6. A semiconductor arrangement according to claim 5, wherein the first metal alloy and the second metal alloy consist of the same component metals in different ratios.

7. A semiconductor arrangement according to any preceding claim, wherein the metal contacts are cylindrical.

8. A semiconductor arrangement according to any one of claims 1 to 6, wherein the metal contacts have a triangular profile.

9. A semiconductor arrangement according to any one of claims 1 to 6, wherein the metal contacts have a rectangular profile.

10. A semiconductor arrangement according to any one of claims 1 to 6, wherein the metal contacts have an obround profile.

11. A semiconductor arrangement according to any preceding claim, wherein said metal contacts are ohmic metal fragments.

12. A semiconductor device comprising a semiconductor arrangement according to any preceding claim.

13. A transistor comprising a semiconductor arrangement according to any one of claims 1 to 11.

14. A High Electron Mobility Transistor, HEMT, comprising a semiconductor arrangement according to any one of claims 1 to 12.

15. A method of constructing a semiconductor arrangement according to any of claims 1 to 14, the method comprising:

forming a substrate layer;

forming a semiconductor layer on top of the substrate layer;

forming a dielectric layer on top of the semiconductor layer;

forming a plurality of trenches in the dielectric layer;

filling each of the plurality of trenches with a volume of metal comprising a first metal and a second metal in a defined ratio; and

annealing the metals to form an alloy.

16. A method to claim 15, wherein said step of forming a plurality of trenches in the dielectric layer further comprises forming said trenches in the semiconductor layer.

17. A semiconductor arrangement comprising:

a substrate layer, a semiconductor layer, a dielectric layer, and a connector layer, wherein the layers are disposed in the order: the substrate layer, the semiconductor layer, the dielectric layer, and the connector layer;

a trench formed in the dielectric layer; and

a metal contact located in said trench electrically connecting the connector layer and the semiconductor layer,

wherein the connector layer comprises a first metal alloy, and the metal contact comprises a second metal alloy,

and wherein the first metal alloy and the second metal alloy comprise a first metal and a second metal in different ratios.

18. A semiconductor arrangement according to claim 17, wherein said trench is formed in the dielectric layer and the semiconductor layer.

19. A method of manufacturing a semiconductor arrangement, the arrangement comprising a substrate layer, a semiconductor layer, a dielectric layer, and a connector layer, wherein the layers are disposed in the order: the substrate layer, the semiconductor layer, the dielectric layer, and the connector layer, the method comprising:

forming a trench in the dielectric layer;

forming within the trench a first layer of a first thickness on top of the semiconductor layer and a second layer of a second thickness on top of the first layer,

wherein the first layer comprises a first metal, and the second layer comprises a first region disposed between a first trench wall and a first distance from the trench wall, a second region disposed between said first distance and a second distance from the trench wall, and a metal region disposed between said second distance and a second trench wall, wherein the first and third regions consist of the first metal and the second region consists of a second metal; and

annealing the first and second metals to form an alloy.

20. A method according to claim 19, wherein said step of forming a trench in the dielectric layer further comprises forming said trench in the semiconductor layer.

21. A method according to claim 19 or 20, wherein the first thickness, the first distance and the second distance are equal.

22. A method according to any one of claim 19 to 21, wherein the second layer extends to a distance equal to the first thickness above an upper surface of the dielectric layer.

23. A method of manufacturing a semiconductor arrangement, the method comprising:

forming a substrate layer;

forming a semiconductor layer on top of the substrate layer;

forming a dielectric layer on top of the semiconductor layer;

forming a trench in the dielectric layer;

filling the trench with a first volume of metal comprising a first metal and a second metal in a first ratio;

constructing a stack above the dielectric layer, the stack comprising a second volume of metal comprising the first metal and a second metal in a second ratio, the second ratio being different from the first ratio; and

annealing the metals to form a first alloy in the trench and a connector layer of a second alloy above the dielectric layer.

24. A method according to claim 23, wherein said step of forming a trench in the dielectric layer further comprises forming said trench in the semiconductor layer.

25. A method according to claim 23 or 24, wherein filling the trench with a first volume of metal comprises depositing a first layer of a first thickness comprising the first metal along a base of the trench, along a first wall of the trench, and along a second wall of the trench.

26. A method according to claim 25, wherein the filling further comprises filling a remaining unfilled volume with a third volume of metal comprising the second metal.

27. A method according to any of claims 23 to 26, further comprising adding a third metal to the first volume of metal.

28. A method according to any of claims 23 to 27, further comprising adding a third metal to the second volume of metal.

Amendmewnts to the claims have been filed as follows:

CLAIMS:

1. A semiconductor arrangement comprising:
a substrate;
a dielectric layer;
a semiconductor layer disposed between the substrate and the dielectric layer;
an ohmic contact comprising a plurality of metal contact fragments located in a plurality of trenches formed in said dielectric layer; and
a metallic connector layer electrically connecting said metal contact fragments,
wherein said ohmic contact electrically connects said metallic connector layer to said semiconductor layer.

2. A semiconductor arrangement according to claim 1, wherein said plurality of trenches are formed in the dielectric layer and in the semiconductor layer.

3. A semiconductor arrangement according to claim 1 or 2, wherein a dimension of at least one of said metal contact fragments is substantially equal to a transfer length of an interface between the metal contact fragments and said semiconductor layer.

4. A semiconductor arrangement according to claim 3, wherein said dimension is within 10% of the transfer length.

5. A semiconductor arrangement according to claim 3 or 4, wherein said dimension is a length of the fragments in a lateral direction parallel to a current traveling to or from the ohmic contact when in use.

6. A semiconductor arrangement according to any preceding claim, wherein said metal contact fragments are arranged in a single row perpendicular to a direction of current travelling to or from the ohmic contact when in use.

7. A semiconductor arrangement according to any one of claims 1 to 5, wherein said metal contact fragments are arranged in multiple rows perpendicular to a direction of current travelling to or from the ohmic contact when in use.

8. A semiconductor arrangement according to any preceding claim, wherein said metal contact fragments comprise a first metal alloy.

9. A semiconductor arrangement according to claim 8, wherein the metallic connector layer comprises a second metal alloy.

10. A semiconductor arrangement according to claim 9, wherein the first metal alloy and the second metal alloy consist of the same component metals in different ratios.

11. A semiconductor arrangement according to any preceding claim, wherein the metal contacts are cylindrical.

12. A semiconductor arrangement according to any one of claims 1 to 10, wherein the metal contacts have a triangular profile.

13. A semiconductor arrangement according to any one of claims 1 to 10, wherein the metal contacts have a rectangular profile.

14. A semiconductor arrangement according to any one of claims 1 to 10, wherein the metal contacts have an obround profile.

15. A semiconductor device comprising a semiconductor arrangement according to any preceding claim.

16. A transistor comprising a semiconductor arrangement according to any one of claims 1 to 14.

17. A High Electron Mobility Transistor, HEMT, comprising a semiconductor arrangement according to any one of claims 1 to 14.

18. A method of constructing a semiconductor arrangement according to any of claims 1 to 14, the method comprising:

forming a substrate layer;

forming a semiconductor layer on top of the substrate layer;

forming a dielectric layer on top of the semiconductor layer;

forming a plurality of trenches in the dielectric layer;

forming an ohmic contact comprising a plurality of metal contact fragments located in said trenches; and

forming a metallic connector layer electrically connecting said metal contact fragments, wherein said ohmic contact electrically connects said metallic connector layer to said semiconductor layer.

19. A method according to claim 18, wherein said step of forming the plurality of trenches further comprises forming said trenches in the semiconductor layer.

20. A method according to claim 18 or 19, wherein said step of forming said trenches comprises forming a trench having a dimension that is substantially equal to a transfer length of an interface between the metal contact fragments and said semiconductor layer in the constructed semiconductor arrangement.

21. A method according to claim 20, wherein said dimension is within 10% of the transfer length.

22. A method according to claim 20 or 21, wherein said dimension is a length of the fragments in a lateral direction parallel to a current traveling to or from the ohmic contact in the constructed semiconductor arrangement when in use.

23. A method according to any one of claims 18 to 22, wherein said step of forming said trenches comprises forming said trenches in a single row perpendicular to a direction of current travelling to or from the ohmic contact in the constructed semiconductor arrangement when in use.

24. A method according to any one of claims 18 to 22, wherein said step of forming said trenches comprises forming said trenches in multiple rows perpendicular to a direction of current travelling to or from the ohmic contact in the constructed semiconductor arrangement when in use.

25. A method according to any one of claim 18 to 24, wherein said step of forming an ohmic contact and said step of forming a metal connector layer are performed in the same step and said same step comprises:

depositing a first metal in the trenches to form a first metal layer having a first thickness;

depositing a second metal in the trenches to form a second metal layer having a second thickness; and

annealing to form a first metal alloy in the trenches and a second metal alloy above the trenches, wherein the first and second metal alloys comprise the first and second metal in different ratios.

26. A method according to any one of claims 18 to 25, wherein said step of forming said trenches comprises forming cylindrical trenches.

27. A method according to any one of claims 18 to 25, wherein said step of forming said trenches comprises forming trenches having a triangular profile.

28. A method according to any one of claims 18 to 25, wherein said step of forming said trenches comprises forming trenches having a rectangular profile.

29. A method according to any one of claims 18 to 25, wherein said step of forming said trenches comprises forming trenches having an obround profile.

Intellectual Property Office

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Claims searched:	1-28	**Date of search:**	2 July 2018

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1, 2, 4-20 and 23-28	WO 2016/157371 A1 (RENESAS ELECTRONICS CORP) see whole document, especially table 2 page 20, page 29, pages 42-44 and figures 13 and 27.
X	1, 2, 4-20 and 23-28	EP2905811 A1 (RENESAS ELECTRONICS CORP) see whole document, especially figures 6 and 37, [0066-0069] and [0109].
X	1, 2, 4-20 and 23-28	US 2017/294530 A1 (MOENS et.al) see whole document, especially figure 4 and [0053].
X	1, 2, 4-20 and 23-28	US 2011/260174 A1 (HEBERT FRANCOIS) see whole document, especially figures 1D and 4D, [0033-0037], [0052] and [0078].

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EPODOC, WPI, Patent Fulltext

International Classification:

Subclass	Subgroup	Valid From
H01L	0029/423	01/01/2006
H01L	0029/778	01/01/2006