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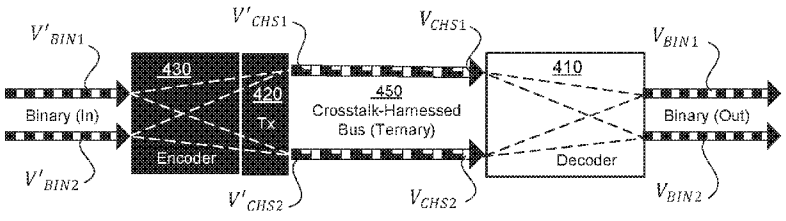


FIG. 4A

(57) Abstract: A logic-based decoder recovers binary data from ternary Crosstalk-Harnessed Signaling (CHS) streams with lower part cost, complexity and power consumption than analog/digital converter (ADC)-based CHS decoders. The decoders use inverters, latches, gates, latching circuits, and one comparator per bit pair to carry out the decoding calculations to produce a reconstructed binary signal with very low crosstalk noise that is largely insensitive to routing density. System-on-chip, multi-chip package, printed circuit board, and wired network applications are discussed.

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LOGIC-BASED DECODER FOR CROSSTALK-HARNESSED SIGNALING

FIELD

[0001] Related fields include signal integrity in digital communication and more particularly reducing signal degradation from crosstalk as signaling speeds and routing densities increase.

BACKGROUND

[0002] Modern computing devices incorporate a growing number of components into progressively smaller device housings. As device sizes decrease, the data buses between components must be routed more densely. When increased routing density is combined with increased bandwidth demand, noise from crosstalk between signal lines of the data bus, particularly differential signal lines, becomes a limiting factor in bus performance. In some scenarios, crosstalk noise may limit the data rate at which a data bus can successfully transfer data between components.

[0003] One way of reducing crosstalk in a data bus is to increase the signal line spacing, which limits the degree of miniaturization that can be achieved. Adding an extra layer and moving some of the interconnects to that extra layer may reduce crosstalk while allowing more miniaturization. However, this approach may be costly. Some crosstalk noise may be equalized at the receiver, but the components may be costly and power-consuming.

[0004] Many of the new miniature devices are intended for mobile use; thus power conservation (e.g., battery life) joins high bandwidth and small size as a top priority. Thus, a need exists for an effective solution that reduces crosstalk in small and miniature-sized devices. The present disclosure addresses this need.

BRIEF DESCRIPTION OF DRAWINGS

[0005] FIGs. 1A-1C are dimensioned drawings of differential signal-line pairs and reproductions of corresponding eye diagrams for binary and CHS signaling.

[0006] FIG. 2 illustrates ternary CHS-encoded signals and corresponding decoded binary signals.

[0007] FIG. 3 is a flowchart of a process for reading incoming ternary CHS bit pairs and decoding them to recover the original binary bit pairs.

[0008] FIGs. 4A and 4B illustrate a ternary CHS link and a decoder logic circuit with an OR gate.

[0009] FIG. 5 is a schematic diagram of a logic-based decoder using an AND gate.

[0010] FIG. 6 illustrates some comparative data for logic-based decoders, other decoders, and other link types.

[0011] FIG. 7 is a schematic of four logic-based decoders coupled in parallel.

[0012] FIG. 8 is a block diagram of an example of a computing system with a signaling module that reduces crosstalk.

DETAILED DESCRIPTION

[0013] Crosstalk-harnessed signaling (CHS) removes a fundamental limitation of high-speed digital bus design by eliminating or significantly reducing the effects of crosstalk noise between differential pairs of lines. Each of the components connected by a data bus may include an Input/Output (I/O) transmitter with an encoding block and an I/O receiver with a decoding block. The encoded, non-binary CHS signal spreads the information from each binary bit across multiple signal lines in such a way that any crosstalk that may occur will effectively become part of the signal. The binary data recovered during the decode process shows little or no negative effects of crosstalk compared to data sent over the same type of line in its binary form. More detailed explanation of CHS encoding may be found in co-owned U.S. Pat. App. Pub. Nos.

US2014/0181348 A1 and US2014/0181358 A1, which are incorporated herein by reference in their entirety.

[0014] Opportunities remain to reduce cost, complexity and power consumption in CHS links.

[0015] The following terms shall have the following meanings for purposes of this document:

[0016] Connected: in direct physical or electrical contact with each other.

[0017] Coupled: co-operating or interacting with each other whether or not in direct physical or electrical contact with each other.

[0018] CHS techniques provide significant increases in both routing density and bus speeds for packages, printed circuit boards (PCBs), multi-chip modules (MCMs) and multi-chip packages (MCPs). Increasing the routing density and bus speed enables more functionality to fit in a smaller package volume, facilitating continued scaling of computer performance.

[0019] Some existing CHS receivers use analog to digital converters (ADCs) to sample the encoded CHS data stream during the decoding process. ADCs consume an amount of power consistent with their performing hundreds of comparator operations per signal. ADCs are designed for faithful reproduction of analog signals with potentially wide dynamic or frequency ranges. CHS encoded signals are more complex than binary signals, but they are nevertheless digital; some embodiments only use a small fraction of the ADC's capabilities. Therefore, simpler components that consume less power than an ADC may nevertheless produce satisfactory results in a CHS decoder.

[0020] A low-power logic-based CHS decoder uses logic circuits to "deduce" the original binary bit values by sampling the encoded signal at strategic levels and applying inverse mathematical processes derived from the known encoding equations to recover the binary signal. Additionally, instead of the 4-bit "nibble" processing that may be used in embodiments of the ADC-based decoders, the logic-based decoders may use a 2-bit decoding process. Parallel processing with

multiple decoders is possible with either solution; processing a byte at a time could be achieved with four logic-based decoders alternatively to two ADC-based decoders.

[0021] FIGs. 1A-1C are dimensioned drawings of differential signal-line pairs and reproductions of corresponding eye diagrams for binary and CHS signaling. Traditional binary crosstalk-limited buses comprising microstrip traces were routed at different trace spacings for a length of 127mm (5 inches) and a data rate of 8 Gb/s. In FIGs. 1A-1C, trace width "w" for traces 103.1, 103.2, 113.1, 113.2, 123.1 and 123.2 is about 0.1mm (4 mils). Thickness "d" of a substrate (e.g., a composite PCB substrate with optional grounding planes 102, 112, 122) may also be about 0.1mm (4 mils).

[0022] In FIG. 1A, spacing S1 between traces 103.1 and 103.2 is 0.4mm (16 mils). Both the binary-transmission eye diagram 104 and the CHS-encoded-transmission eye diagram 105 are open, but diagram 105 is more open than diagram 104, suggesting that even at this wide trace spacing, CHS transmission will have a lower bit-error rate than binary transmission.

[0023] In FIG. 1B, spacing S2 between traces 113.1 and 113.2 is 0.3mm (12 mils). The binary-transmission eye diagram 114 is only barely open. However, the CHS-encoded-transmission eye diagram 115 is, to the unaided eye, visually identical to diagram 105 (see FIG. 1A), suggesting that the bit-error rate has not increased or, conservatively, may have increased by less than a few percent.

[0024] In FIG. 1C, spacing S3 between traces 123.1 and 123.2 is 0.1mm (4 mils). The binary-transmission eye diagram 124 is closed, suggesting a bit-error rate that may be unacceptable. However, the CHS-encoded-transmission eye diagram 125 is, to the unaided eye, visually identical to diagram 105 (see FIG. 1A), suggesting that the bit-error rate has not increased or, conservatively, may have increased by less than a few percent.

[0025] As the trace spacing was reduced from 0.4mm (16 mils) to 0.1mm (4 mils), the binary-transmission eye diagram completely closes, indicating that this bus may produce an unacceptably high bit-error rate. By contrast, the CHS eye diagrams are wide open and almost independent of the trace spacing at this scale. For this reason, CHS holds promise for implementing denser routings in crosstalk-limited high-speed architectures with other materials and dimensions as well.

[0026] FIG. 2 illustrates ternary CHS-encoded signals and corresponding decoded binary signals. Ternary (3-level) CHS operates on pairs of bits, unlike quaternary (4-level) CHS which operates on "nibbles" (groups of 4 bits). For simplicity, these examples involve ternary CHS, but they do not preclude logic-based decoders being adapted for quaternary or higher-order CHS.

[0027] CHS bit pairs 201, 202, 203, and 204 demonstrate that a ternary CHS bit may have one of three voltage levels: a minimum, a maximum, and an intermediate. In some embodiments, the intermediate may be halfway between the minimum and the maximum.

[0028] As shown by the encoding eqn. 270.1, the vector V'_{CHS} representing the CHS bit pair exiting the transmitter is a product of the vector V'_{BIN} representing the binary bit pair entering the decoder, a weighted matrix W (which is a 2x2 matrix in the case of ternary CHS) and a normalizing factor of 1/2. In some embodiments, a multiplier M may be applied to the CHS signal before transmission to limit the excursion from minimum to maximum to a desirable range. In some embodiments, an offset $\mathbf{V}_{offset}$ may be added to the (multiplied, if applicable) CHS signal before transmission to force all three levels to have the same polarity (e.g., $\mathbf{V}_{offset}$ may raise the minimum to >=0 to make all levels positive or $\mathbf{V}_{offset}$ may lower the maximum to <=0 to make all levels negative). As a non-limiting example, a multiplier M and and/or an offset $\mathbf{V}_{offset}$ may be used to cause the CHS signal to be within a range from 0 to 1V. $\mathbf{V}_{offset}$ may be, for

example, a value between 0V and 1V, such as 0.5V (e.g., $\mathbf{V}_{offset}$ = [$\mathbf{V}_{offset1}$ = $\mathbf{V}_{offset2}$] = [0.5V 0V]). If the encoded CHS signal is transmitted "as-is," M=1 and $\mathbf{V}_{offset}$= 0.

[0029] The other encoding eqn. 270.2, is an expanded version of encoding eqn. 270.1 to explicitly show how each bit value in the vector V'_{CHS} depends on both bit values in the vector V'_{BIN}. These 2-to-2 (or, more generally, many-to-many) relationships in CHS encoding produce non-binary bit streams that are virtually immune to crosstalk that may occur between neighboring differential signal lines.

[0030] Binary bit pairs 211, 212, 213 and 214 are recovered from CHS bit pairs 201, 202, 203 and 204 respectively by reversing the encoding process: subtracting V_{offset}, multiplying by 2, optionally dividing by M and multiplying the CHS bit values by using a digital decoder that can be expressed using decoding eqns. 280 and 290: simple thresholding expressions involving sums. Threshold voltage V_{ref} may be between the CHS ternary intermediate and maximum levels. Any of a range of V_{ref} values between those two levels may work, which may lend flexibility to the design of logic-based encoders.

[0031] FIG. 3 is a flowchart of a process for reading incoming ternary CHS bit pairs and decoding them to recover the original binary bit pairs. This process is set up to perform multiple operations in parallel as one possible way to optimize processing speed. Other orders of the pictured steps and the addition of intermediate steps between the pictured steps, may also be incorporated within this disclosure.

[0032] For this process, V_{ref} and V_{offset} may be stored constants.

[0033] At step 301, the decoder detects incoming CHS signals from the receiver. At step 302, the decoder reads/measures V_{CHS1}. At step 303, the decoder reads/measures V_{CHS2}. In some embodiments, two different sensors in the decoder may be deployed to read/measure V_{CHS1} and V_{CHS2} in parallel. At decision 310, if $V_{CHSI} > V_{ref}$, the decoder sets V_{BIN1} = 1 at step 311. If not,

the decoder goes to decision 320. At decision 320, if $V_{CHS2} > V_{ref}$, the decoder sets $V_{BIN1} = 1$ at step 311. If not, the decoder sets $V_{BIN1} = 0$ at step 322. At decision 330, if $V_{CHS2} > V_{CHS1}$, the decoder sets $V_{BIN2} = 1$ at step 331. If not, the decoder sets $V_{BIN2} = 0$ at step 332. The decoder outputs V_{BIN1} and V_{BIN2} at step 339 and returns to step 301 to detect the next CHS bit pair.

[0034] One aspect of the process that this type of chart clarifies is that there are at least two different options for logic hardware to perform the two comparisons that determine the value of V_{BIN1} based on the value of V_{ref}. In FIG. 3, $V_{BIN1} = 1$ if decision 310 = "yes" or alternatively if decision 320 = "yes." On the other hand, $V_{BIN1} = 0$ if decision 310 = "no" and if decision 320 also = "no." Therefore, some embodiments of the logic circuit of the logic-based decoder for ternary CHS signals may include an OR gate and some embodiments may include an AND gate.

[0035] FIGs. 4A and 4B illustrate a ternary CHS link and a decoder logic circuit with an OR gate.

[0036] In FIG.4A, a first pair of binary signals V'_{BIN1} and V'_{BIN2} enter an encoder 430 before being transmitted. Encoder 430 uses aspects of both of the binary signals V'_{BIN1} and V'_{BIN2} to construct each of a first pair of CHS ternary signals. The ternary signals are input to digital transmitter 420, which sends them into a first end of crosstalk-harnessed bus 450 as V'_{CHS1} and V'_{CHS2}. For example, crosstalk-harnessed bus 450 may include a differential pair of signal lines carrying V'_{CHS1} and V'_{CHS2}.

[0037] At a second end of the crosstalk-harnessed bus 450, CHS ternary output signals V_{CHS1} and V_{CHS2} are received by digital receiver 410. V_{CHS1} and V_{CHS2} are essentially the inputs V'_{CHS1} and V'_{CHS2} convolved with the impulse response of crosstalk-harnessed bus 450. In the digital decoder 410, V_{CHS1} and V_{CHS2} are used as inputs to decoder 410 and the decoder 410 recovers binary signals V_{BIN1} and V_{BIN2}. V_{BIN1} and V_{BIN2} are preferably a very close match for V'_{BIN1} and V'_{BIN2}, with any artifacts added by encoding, transmission and decoding being too minor to affect

the bit error rate. Digital decoder 410 uses aspects of both of the CHS ternary signals V_{CHS1} and V_{CHS2} to recover each of the pair of binary signals V_{BIN1} and V_{BIN2}.

[0038] FIG. 4B illustrates more details of digital decoder 410 shown in FIG. 4A. Ternary signals V_{CHS1} and V_{CHS2} exit the crosstalk-harnessed bus 450, so that the logic deriving V_{BIN2} (bottom section of decoder logic circuit 410) and the logic deriving V_{BIN1} (top section of decoder logic circuit 410) have parallel access to V_{CHS1} and V_{CHS2}.

[0039] V_{BIN2} may be recovered by applying the decoding eqn. 290, which involves comparing V_{CHS1} and V_{CHS2}. If $V_{CHS2} > (V_{CHS1})$, then $V_{BIN2} = 1$; otherwise $V_{BIN2} = 0$. Comparator 406, connected the digital or sampled output of V_{CHS1} and V_{CHS2} sends comparison results to latching circuit 409.2, which outputs V_{BIN2}.

[0040] V_{BIN1} may be recovered by applying the decoding eqn. 280, which assigns a value of 1 to V_{BIN1} if either one of two conditions is fulfilled. Latch 405.1, which receives input from a digital or sampled output of V_{CHS1} and V_{CHS2}, has a threshold voltage V_{ref} (e.g., 0.6V or elsewhere in the range between 0.55V and 0.95V). Latch 405.2 receives input from a branch of splitter 403.2, has a threshold voltage V_{ref} that is the same as, or very close e.g. within +/- 20% of, the V_{ref} of latch 405.1. Latches 405.1 and 405.2 each produce a digital output of 1 if the input voltage exceeds V_{ref}; OR gate 408 produce a digital output of 1 if the input from either of the latches = 1.

[0041] The latches and the OR gate consume very little power; while the comparator is the dominant power consumers in the decoder logic circuit of FIG. 4B. This circuit uses only one comparator per bit pair -- much less than, for example, a 6-bit ADC exercising as many as 63 comparators per bit.

[0042] Logic-based decoder 410 also includes latching circuits 409.1 and 409.2, one per bit, first clock sample signal 404 and second clock sample signal 414 to keep the bits synchronized. However, none of these consume as much power as an ADC converter.

[0043] In some embodiments, clock sample 404 may be a rising-edge sample and clock sample 414 may be a falling-edge sample, of the same clock, such as a system clock. Clock sample 404 latches incoming data to the inputs of decoder 410, whereas clock sample 414 latches outgoing data to the outputs of decoder 410.

[0044] FIG. 5 is a schematic diagram of a logic-based decoder 510 using an AND gate. The Eqn. 290, the decoding equation for V_{BIN2}, is the same for this circuit as it was for the circuit of FIG. 4B. The bottom part of the circuit, which produces the V_{BIN2} result, is also unchanged from FIG. 4B. In FIG. 5, input V_{CHS2} goes into two branches. One of the branches goes to comparator 506 where its signal is compared with the V_{CHS1} signal. The comparison results are sent to latching circuit 509.2, which yields the recovered V_{BIN2} value.

[0045] Eqn, 580 is the decoding equation for V_{BIN1}. It produces the same decoding results as eqn. 280 (see FIGs. 2 and 4B), but expresses the conditions in terms of "and" instead of "or" based on the threshold voltage V_{ref}. When the possible results are limited to 0 or 1, as they may be when reconstructing binary bit-values, "Result = 1 if A is above the threshold and B is above the threshold otherwise Result = 0." However, such alternate expressions may indicate alternatives in component choices for a logic circuit, depending on which expression is implemented in the hardware.

[0046] Latch 505.1, which receives a signal V_{CHS1}, feeds its output into AND gate 518. Latch 505.2, which receives a signal from V_{CHS2}, feeds its output into AND gate 518. The output of AND gate 518 is sent to latching circuit 509.1, which produces the binary bit value V_{BIN1}.

[0047] Another dissimilarity between this circuit and that of FIG. 4B, besides the type of gate, is the threshold voltage V_{ref} for latches 505.1 and 505.2. To test the "less than or equal to" expressions of eqn. 580, V_{ref} is chosen to be in a voltage range between the minimum and intermediate values

of V_{CHS1} and V_{CHS2}. For example, if the minimum is 0 V and the intermediate value is 0.5 V, V_{ref} may be in a range between 0.05 V and 0.45 V, for instance 0.3 V.

[0048] FIG. 6 illustrates some comparative data for logic-based decoders, other decoders, and other link types. The data most relevant to this disclosure is the power consumed by receivers, which include decoders (illustrated as the white sections of the stacked columns). The logic-based decoder (CHS-->logic) has low receiver power consumption 601.1. Termination does not seem to change the receiver power consumption 601.2 of the logic-based decoder. The terminated CHS --> 2-bit ADC decoder has receiver power consumption 602 comparable to logic-based decoder consumption values 601.1 and 601.2. The terminated CHS --> 2-bit ADC decoder consumes about the same amount of power 602 as the logic-based decoder. By contrast, the 6-bit ADC decoder consumes power 612, about 3-4x more than the logic-based decoder. A binary low-power PCIe receiver without encoding or decoding consumes about 8x the power of the logic-based decoder.

[0049] FIG. 7 is a schematic of four logic-based decoders coupled in parallel. With each of the decoders decoding a bit pair at a time, this parallel 4-decoder arrangement may decode a byte (4 bit pairs) of ternary CHS data at a time. All of the decoders are synchronized to the same clock-H sample 704 and clock-L sample 714.

[0050] FIG. 8 is a block diagram of an example of a computing system with a signaling module that reduces crosstalk. The computing system may be, for example, a mobile phone, laptop computer, Ultrabook, desktop computer, server or tablet computer, among others. The computing system may include a processor 802 that is adapted to execute stored instructions, as well as a memory device 804 that stores instructions that are executable by the processor 802. The processor 802 can be a single core processor, a multi-core processor, a computing cluster or any number of other configurations. The processor 802 may be implemented as Complex Instruction Set

Computer (CISC) or Reduced Instruction Set Computer (RISC) processors, x86 Instruction set compatible processors, multi-core or any other microprocessor or central processing unit (CPU). In some embodiments, the processor 802 includes dual-core processor(s), dual-core mobile processor(s) or the like.

[0051] The memory device 804 can include random access memory (e.g., SRAM, DRAM, zero capacitor RAM, SONOS, eDRAM, EDO RAM, DDR RAM, RRAM, PRAM, etc.), read only memory (e.g., Mask ROM, PROM, EPROM, EEPROM, etc.), flash memory or any other suitable memory systems. The memory device 804 can be used to store computer-readable instructions that, when executed by the processor, direct the processor to perform various operations in accordance with embodiments described herein.

[0052] The computing system may also include a graphics processor 806 that processes computer generated graphics. The graphics processor 806 is configured to process memory related to the generation of graphics to be sent to a display (not shown). The display may be a built-in component of the computing system externally connected to the computing system. The computing system can also include an I/O hub 808 used to connect and control additional I/O devices (not shown), such as network interface controllers, memory storage devices, user input devices, among others. The I/O devices coupled to the I/O hub 808 may be built-in components of the computing system or may be devices that are externally connected to the computing system.

[0053] The computing system may also include a memory controller hub 810 that handles communications between the processor 802, memory 804, graphics processor 806 and I/O hub 810. Communications between the various components of the computing system can be performed over various data buses. For example, the graphics processor 806 can be coupled to the memory controller 810 through a graphics bus 816. The memory 804 can be coupled to the

memory controller 810 through a memory bus 814. The data bus between the processor 802 and the memory controller 810 may be referred to as the front side bus 812. The data bus between the memory controller 810 and the I/O hub may be referred to as the internal bus 818. Memory controller may include a memory element (not shown).

[0054] In some embodiments, the processor 802, graphics processor 806, memory device 804, memory controller 810 and I/O hub 808 may be separate integrated circuit chips coupled to a mother board. In some embodiments, one or more of the processor 802, the graphics processor 806, the memory device 804, the memory controller 810 and the I/O hub 808 may be included in a multi-chip module (MCM), multi-chip package (MCP) or system-on-a-chip (SOC). Depending on the design considerations of a particular implementation, the signal lines of the one or more of the buses 812, 814, 816, 818 may disposed, at least in part, on one or more circuit boards.

[0055] The computing system also includes signaling modules 820 that facilitate digital communications between the components coupled to the respective bus. Each signaling module 820 receives digital data and generates signals that propagate on the signal lines of the various buses. As explained further below, the signals are encoded by a transmitting signaling module and decoded by a receiving signaling module in a way that reduces the effects of crosstalk between the signal lines of the data bus. A respective signaling module 820 may be coupled to or included in, any component of the computing device 800 that transmits data over a data bus that uses differential communications. For example, signaling modules may be included in the processor 802, graphics processor 806, memory device 804, memory controller 810 and I/O hub 808, among others.

[0056] The block diagram of FIG. 8 is not intended to indicate that computing systems must include all of the components shown. Rather, the computing system can include fewer or additional components not illustrated in FIG. 8. Furthermore, the components may be coupled to one

another according to any suitable system architecture, including the system architecture shown in FIG. 8 or any other suitable system architecture that uses a data bus to facilitate communications between components. For example, embodiments of the present techniques can also be implemented any suitable electronic device, including ultra-compact form factor devices, such as System-On-a-Chip (SOC) arrangements in which all the components are formed on a single integrated chip and multi-chip modules where some of the components may be on different chips mounted on a PCB or other substrate. Signal lines may include stripline, microstrip, PCIe or any other suitable type. The buses 812-818 in FIG. 8 could also be any electrical cable inside or outside of a computer that carries digital information from one point to another. For example, embodiments of logic-based CHS decoders may be used for connecting disk drives or other peripherals, as well as networked desktop computers.

[0057] These low-power CHS decoders are expected to significantly reduce the negative impact of crosstalk noise in high-speed buses. For example, some embodiments may:

(1) Facilitate major increases in microstrip bus speed and routing density by mitigating or obviating the historical crosstalk-noise penalty.

(2) Decrease bill-of-materials (BOM) cost by tolerating higher routing density and thereby opening up design options such as smaller packages and fewer interconnect layers.

(3) Increase the maximum computational capability possible in a small volume chassis by supporting increased routing density.

(4) Accelerate commercialization emerging package technologies with finer I/O lines

[0058] In summary, passive test board measurements and simulations have both demonstrated that CHS mitigates or eliminates the increases in crosstalk noise associated with binary signaling at high bandwidth and high routing density. The logic-based CHS decoders described herein support high-density routing of high-speed signals with low power consumption without

sacrificing performance. This technology has the potential to reduce system costs by reducing PCB, package or cable layers; reducing board areas and I/O counts; and creating opportunities to use smaller connectors.

[0059] The method allows for significant increases in both routing density and bus speeds on packages, printed circuit boards (PCBs), multi-chip modules (MCMs) and multi-chip packages.

[0060] *Examples*

[0061] Example 1 includes a computing system comprising a memory controller and a first communication link between the memory controller and at least one peripheral device. The communication link carries a crosstalk-harnessed signal (CHS). The CHS is a multi-level non-binary signal in one or more embodiments. The CHS is decoded to a binary signal by arithmetic logic coupled to a receiver. The arithmetic logic is to decode the CHS by sampling an encoded signal and recovering the binary signal based on the sampling.

[0062] In Example 2, the computing system in Example 1, can further comprise a processor, memory, and an input/output (I/O) hub. In addition, a second communication link between the memory controller and the memory; a third communication link between the memory controller and the I/O hub; and a fourth communication link between the memory controller and a graphics processor. The at least one of the second communication link, the third communication link, or the fourth communication link carries and additional CHS.

[0063] In Example 3, the computing system in Example 2, wherein the processor, the graphics processor, the memory, the I/O hub, the memory controller, the first communication link, the second communication link, the third communication link, and the fourth communication link are formed on a single integrated chip.

[0064] In Example 4, the computing system in Example 2, wherein at least one of the processor, the graphics processor, the memory, the I/O hub, or the memory controller is formed on a different

chip than at least a different one of the processor, the graphics processor, the memory, the I/O hub or the memory controller.

[0065] In Example 5, the computing system in Example 2, wherein at least one of the second communication link, the third communication link, or the fourth communication link that carries the additional CHS is formed as a conductive trace on a printed circuit board.

[0066] In Example 6, the computing system in Example 2, wherein at least one of the second communication link, the third communication link, or the fourth communication link that carries the additional CHS is formed as a cable-connecting separate device.

[0067] In Example 7, the computing system in Example 2, wherein the arithmetic logic employs a 2-bit decoding process.

[0068] In Example 8, the computing system in claim 1, wherein the first communication link carries a pair of crosstalk-harnessed signals and wherein the pair of crosstalk-harnessed signals is decoded to a pair of binary signals by the arithmetic logic, the arithmetic logic to decode the CHS by sampling the encoded signal and recovering at least one of the pairs of binary signals by using aspects of the pair of crosstalk-harnessed signals by comparing a first set of voltages associated with a first CHS of the pair of crosstalk-harnessed signals with a second set of voltages associated with a second CHS of the pair of crosstalk-harnessed signals or by comparing the first set of voltages and the second set of voltages with a reference voltage.

[0069] Example 9 includes a link comprising a crosstalk-harnessed bus having a first differential pair of signal lines. The link further comprises a digital transmitter coupled to a first end of the crosstalk-harnessed bus; a digital receiver coupled to a second end of the crosstalk-harnessed bus; and an encoder coupled to an input of the digital transmitter. The encoder comprises arithmetic logic to convert a pair of binary signals to a first pair of ternary signals based on a product of a first voltage vector (V'_{BIN}) representing a binary bit, a weighted matrix, a

normalizing factor, and a multiplier. The link further comprises a first decoder logic circuit coupled to an output of the first differential pair of signal lines through the digital receiver.

[0070] In Example 10, the link in Example 9, wherein the digital transmitter is to transmit the first pair of ternary signals and the digital receiver is to receive the first pair of ternary signals.

[0071] In Example 11, the link in Example 9, wherein the first decoder logic circuit comprises a pair of latches, a comparator, and a gate.

[0072] In Example 12, the link in Example 9 further comprising at least a second pair of ternary signals transmitted in a second pair of differential signal lines; and at least a second decoder logic circuit coupled to the additional pair of differential signal lines through the digital receiver; wherein the first decoder logic circuit and the second decoder logic circuit work in parallel to convert the first pair of ternary signals and the second pair of ternary signals, respectively, to binary signals.

[0073] In Example 13, the link of Example 9 further comprising adding an offset to the product of the first voltage vector.

[0074] Example 14 includes a decoder comprising a first input for a first multi-level CHS and a second input for a second multi-level CHS. The decoder further comprises a first latch and a second latch having identical reference voltages; a comparator; and a gate coupled to an output of the first latch and an output of the second latch. Furthermore, the decoder comprises a first latching circuit coupled to an output of the gate and a second latching circuit coupled to an output of the comparator. Additionally, the decoder comprises a first clock sample signal coupled to the first latch, the second latch and the comparator and a second clock sample signal coupled to the first latching circuit and the second latching circuit.

[0075] In Example 15, the decoder in Example 14, wherein the first latching circuit and the second latching circuit are to produce binary output signals from inputs from the first multi-level CHS

and the second multi-level CHS at the first latch, the second latch, and the comparator. The first multi-level CHS and the second multi-level CHS each comprises three or more voltage levels which have an identical polarity.

[0076] In Example 16, the decoder in Example 14, wherein one of the first clock sample signal and the second clock sample signal comprise at least one of a clock-high signal or a clock-low signal.

[0077] In Example 17, the decoder in Example 14, wherein the first clock sample signal and the second clock sample signal originate in at least one of a single clock or a system clock.

[0078] In Example 18, the decoder in Example 14, wherein the identical reference voltages are between 0V and 1V.

[0079] In Example 19, the decoder in Example 14, wherein the decoder comprises arithmetic logic to detect an incoming CHS from a receiver, wherein the logic comprises: logic to read a first ternary voltage vector (V_{CHS1}); logic to read a second ternary voltage vector (V_{CHS2}); logic to compute a sum of V_{CHS1} and an offset constant (V_{offset}); logic to set a first voltage vector (V_{BIN1}) to 1 if the sum is greater than a reference constant (V_{ref}); logic to set a second voltage vector (V_{BIN2}) to 1 if $V_{CHS2} > (V_{CHS1})$ or set to 0 otherwise; logic to set V_{BIN1} to 1 if $V_{CHS2} > V_{ref}$ or set to 0 if the sum is not greater than V_{ref},, and logic to output V_{BIN1} and V_{BIN2}.

[0080] In Example 20, the decoder in Example 14, wherein the decoder is an analog/digital converter-based decoder.

[0081] The preceding Description and accompanying Drawings describe examples of embodiments in some detail to aid understanding. However, the scope of protection may also include equivalents, permutations and combinations that are not explicitly described herein. Only the claims appended here (along with those of parent, child or divisional patents, if any) define the limits of the protected intellectual-property rights.

CLAIMS

We claim:

1. A computing system, comprising:

a memory controller;

a first communication link between the memory controller and at least one peripheral device,

wherein the first communication link carries a crosstalk-harnessed signal (CHS),

wherein the CHS is a multi-level non-binary signal, and

wherein the CHS is decoded to a binary signal by arithmetic logic coupled to a receiver, the arithmetic logic to decode the CHS by sampling an encoded signal and recovering the binary signal based on the sampling.

2. The computing system of claim 1 further comprising a processor, a memory, and an input/output (I/O) hub;

a second communication link between the memory controller and the memory;

a third communication link between the memory controller and the I/O hub; and

a fourth communication link between the memory controller and a graphics processor,

wherein at least one of the second communication link, the third communication link, or the fourth communication link carries an additional CHS.

3. The computing system of claim 2, wherein the processor, the graphics processor, the memory, the I/O hub, the memory controller, the first communication link, the second communication link, the third communication link, and the fourth communication link are formed on a single integrated chip.

4. The computing system of claim 2, wherein at least one of the processor, the graphics processor, the memory, the I/O hub, or the memory controller is formed on a different chip than at least a different one of the processor, the graphics processor, the memory, the I/O hub or the memory controller.

5. The computing system of claim 2, wherein at least one of the second communication link, the third communication link, or the fourth communication link that carries the additional CHS is formed as a conductive trace on a printed circuit board.

6. The computing system of claim 2, wherein at least one of the second communication link, the third communication link, or the fourth communication link that carries the additional CHS is formed as a cable-connecting separate device.

7. The computing system of claim 1, wherein the arithmetic logic employs a 2-bit decoding process.

8. The computing system of claim 1, wherein the first communication link carries a pair of crosstalk-harnessed signals and wherein the pair of crosstalk-harnessed signals is decoded to a pair of binary signals by the arithmetic logic, the arithmetic logic to decode the pair of crosstalk-harnessed signals by sampling the encoded signal and recovering at least one of the binary signals by using aspects of the pair of crosstalk-harnessed signals by comparing a first set of voltages associated with a first CHS of the pair of crosstalk-harnessed signals with a second set of voltages associated with a second CHS of the pair of crosstalk-harnessed signals or by comparing the first set of voltages and the second set of voltages with a reference voltage.

9. A link, comprising:

a crosstalk-harnessed bus having a first differential pair of signal lines;

a digital transmitter coupled to a first end of the crosstalk-harnessed bus;

a digital receiver coupled to a second end of the crosstalk-harnessed bus;

an encoder coupled to an input of the digital transmitter,

wherein the encoder comprises arithmetic logic to convert a pair of binary signals to a first pair of ternary signals based on a product of a first voltage vector (V'_{BIN}) representing a binary bit, a weighted matrix, a normalizing factor, and a multiplier; and

a first decoder logic circuit coupled to an output of the first differential pair of signal lines through the digital receiver.

10. The link of claim 9, wherein the digital transmitter is to transmit the first pair of ternary signals and the digital receiver is to receive the first pair of ternary signals.

11. The link of claim 9, wherein the first decoder logic circuit comprises a pair of latches, a comparator, and a gate.

12. The link of claim 9, further comprising at least a second pair of ternary signals transmitted in a second pair of differential signal lines; and

at least a second decoder logic circuit coupled to the additional pair of differential signal lines through the digital receiver;

wherein the first decoder logic circuit and the second decoder logic circuit work in parallel to convert the first pair of ternary signals and the second pair of ternary signals, respectively, to binary signals.

13. The link of claim 9 further comprising adding an offset to the product of the first voltage vector.

14. A decoder, comprising:

a first input for a first multi-level crosstalk-harnessed signal (CHS) and a second input for a second multi-level CHS;

a first latch and a second latch having identical reference voltages;

a comparator to compare the first multi-level CHS and the second multi-level CHS;

a gate coupled to an output of the first latch and an output of the second latch;

a first latching circuit coupled to an output of the gate;

a second latching circuit coupled to an output of the comparator;

a first clock sample signal coupled to the first latch, the second latch and the comparator; and

a second clock sample signal coupled to the first latching circuit and the second latching circuit.

15. The decoder of claim 14, wherein the first latching circuit and the second latching circuit are to produce binary output signals from inputs from the first multi-level CHS and the second multi-level CHS at the first latch, the second latch, and the comparator, wherein the first multi-level CHS and the second multi-level CHS each comprise three or more voltage levels which have an identical polarity.

16. The decoder of claim 14, wherein one of the first clock sample signal and the second clock sample signal comprise at least one of a clock-high signal or a clock-low signal.

17. The decoder of claim 14, wherein the first clock sample signal and the second clock sample signal originate in at least one of a single clock or a system clock.

18. The decoder of claim 14, wherein the identical reference voltages are between 0V and 1V.

19. The decoder of claim 14, wherein the decoder comprises arithmetic logic to detect the first multi-level CHS or the second multi-level CHS from a receiver, wherein the logic comprises:

logic to read a first ternary voltage vector (V_{CHS1});

logic to read a second ternary voltage vector (V_{CHS2});

logic to compute a sum of V_{CHS1} and an offset constant (V_{offset});

logic to set a first voltage vector (V_{BIN1}) to 1 if the sum is greater than a reference constant (V_{ref});

logic to set a second voltage vector (V_{BIN2}) to 1 if $V_{CHS2} > (V_{CHS1})$ or set to 0 otherwise;

logic to set V_{BIN1} to 1 if $V_{CHS2} > V_{ref}$ or set to 0 if the sum is not greater than $V_{ref,}$, and

logic to output V_{BIN1} and V_{BIN2}.

20. The decoder of claim 14, wherein the decoder is an analog/digital converter-based decoder.

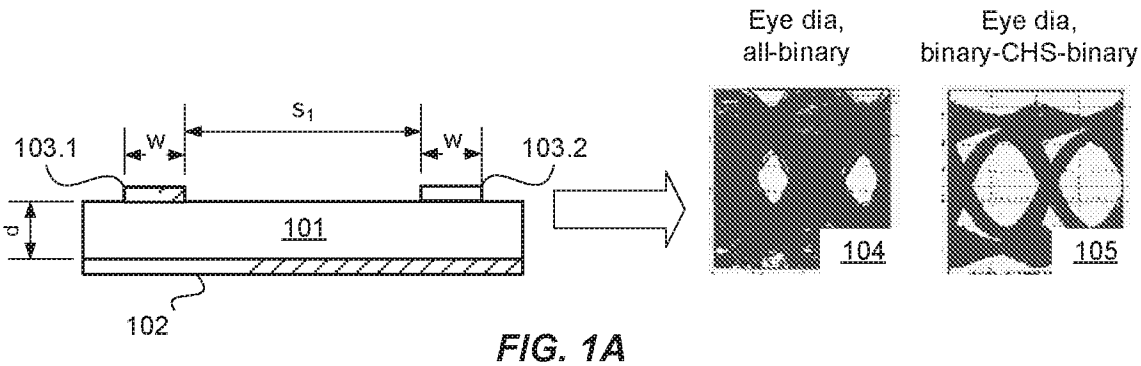


FIG. 1A

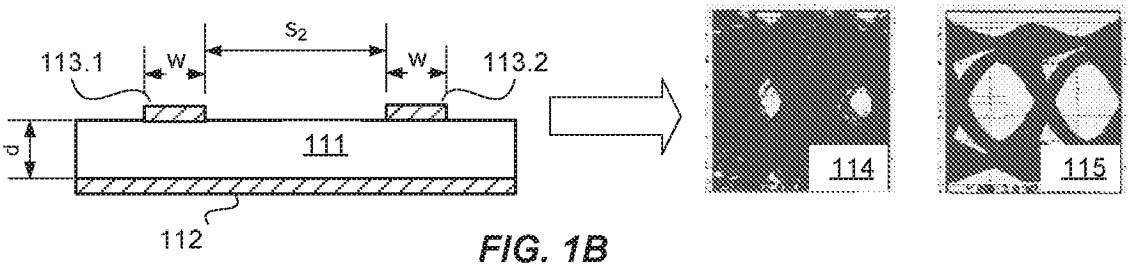


FIG. 1B

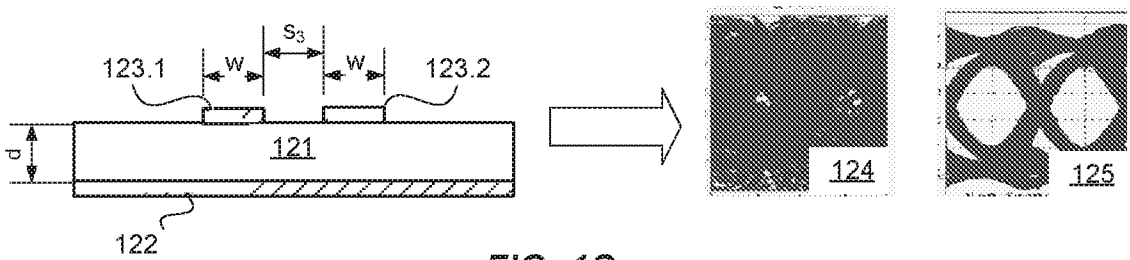


FIG. 1C

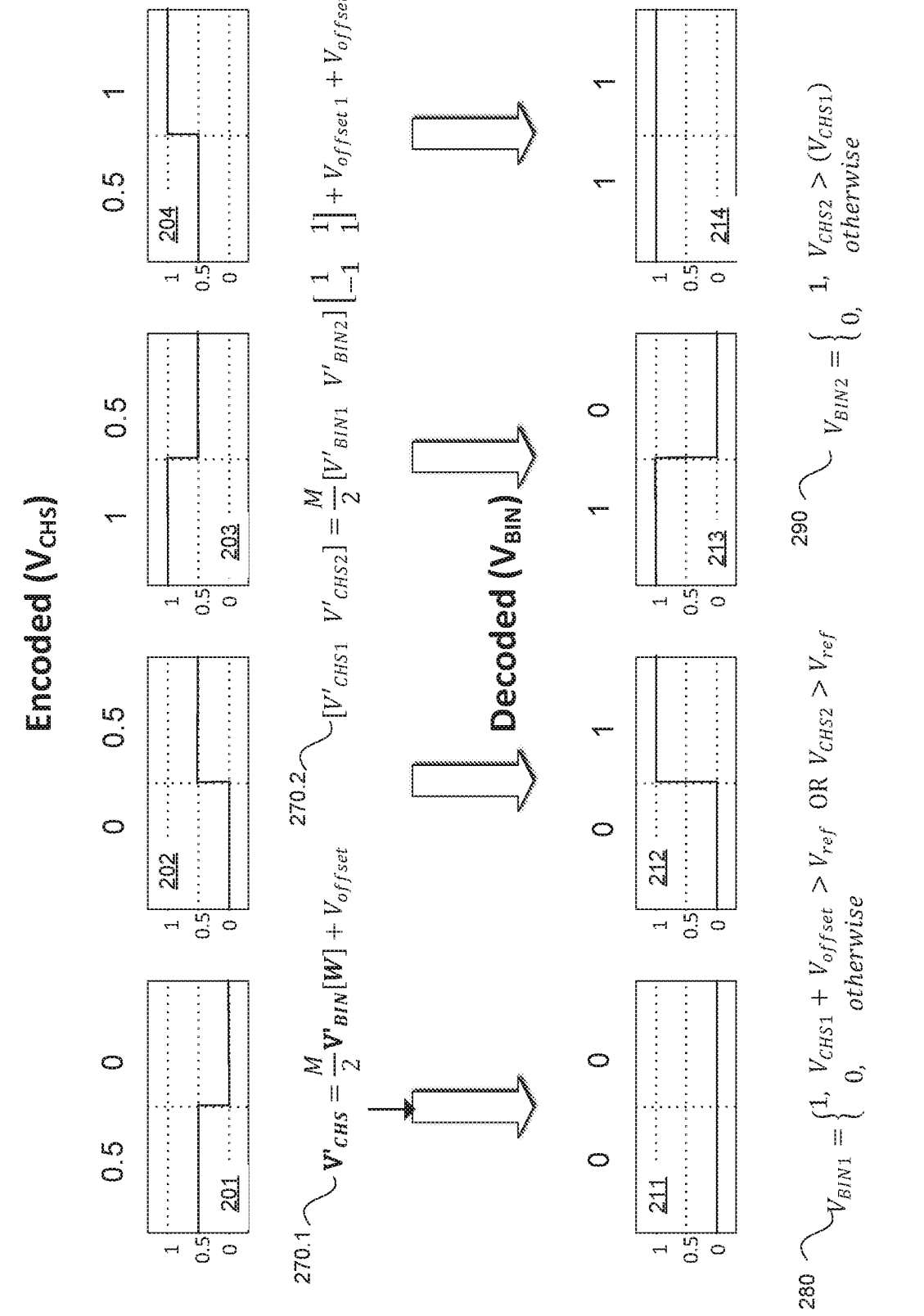

Encoded (V_{CHS})
0.5 0
0 0.5
1 0.5
0.5 1
201
202
203
204
270.1
$\mathbf{V'_{CHS}} = \frac{M}{2}\mathbf{V'_{BIN}}[\mathbf{W}] + V_{offset}$
270.2
$[V'_{CHS1} \quad V'_{CHS2}] = \frac{M}{2}[V'_{BIN1} \quad V'_{BIN2}] \begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} + V_{offset\,1} + V_{offset\,2}$
Decoded (V_{BIN})
0 0
0 1
1 0
1 1
211
212
213
214
280
$V_{BIN1} = \begin{cases} 1, & V_{CHS1} + V_{offset} > V_{ref} \text{ OR } V_{CHS2} > V_{ref} \\ 0, & otherwise \end{cases}$
290
$V_{BIN2} = \begin{cases} 1, & V_{CHS2} > (V_{CHS1}) \\ 0, & otherwise \end{cases}$

FIG. 2

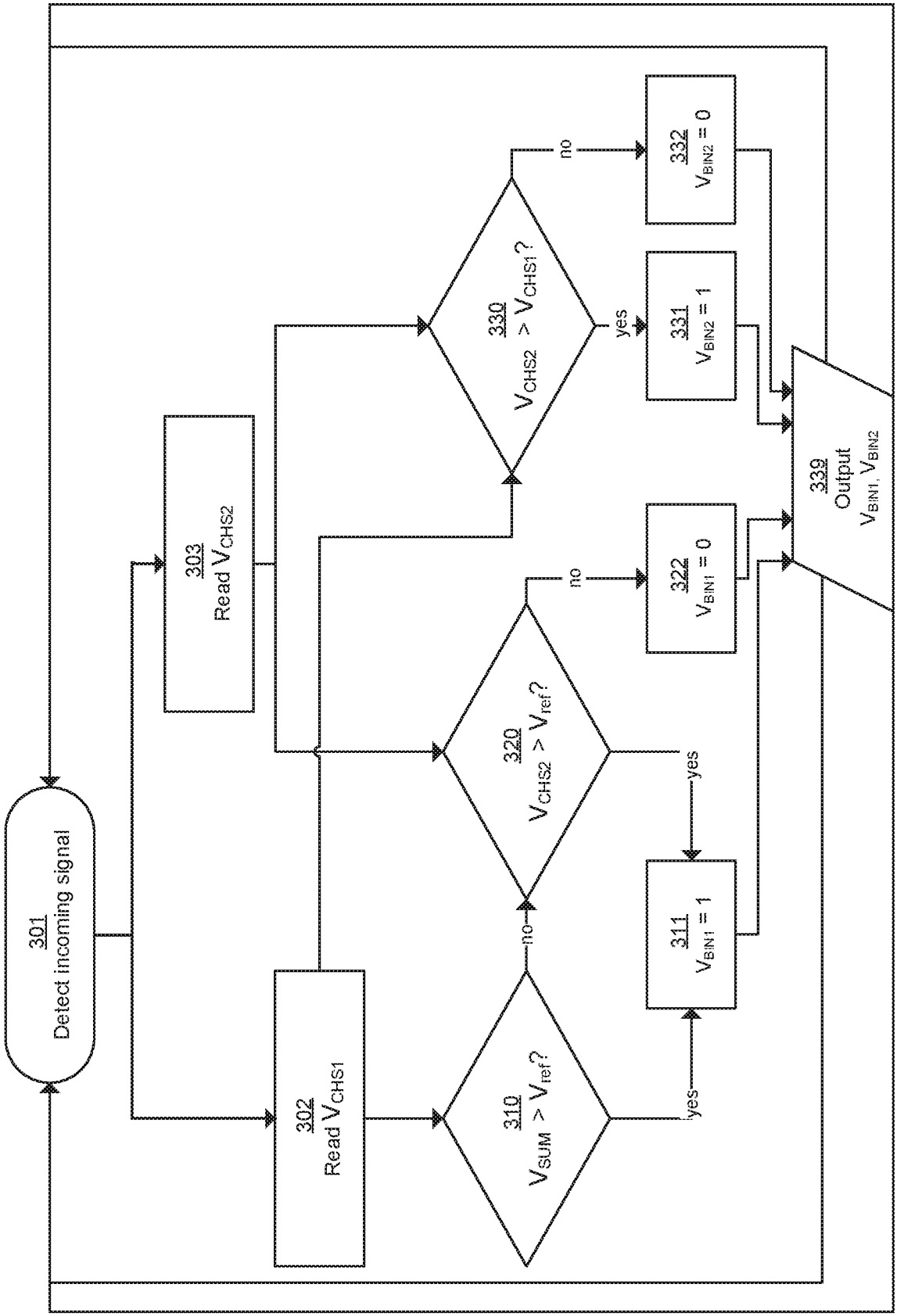

301
Detect incoming signal
302
Read V_{CHS1}
303
Read V_{CHS2}
310
$V_{SUM} > V_{ref}$?
311
$V_{BIN1} = 1$
320
$V_{CHS2} > V_{ref}$?
322
$V_{BIN1} = 0$
330
$V_{CHS2} > V_{CHS1}$?
331
$V_{BIN2} = 1$
332
$V_{BIN2} = 0$
339
Output
V_{BIN1}, V_{BIN2}
yes
no
yes
no
yes
no

FIG. 3

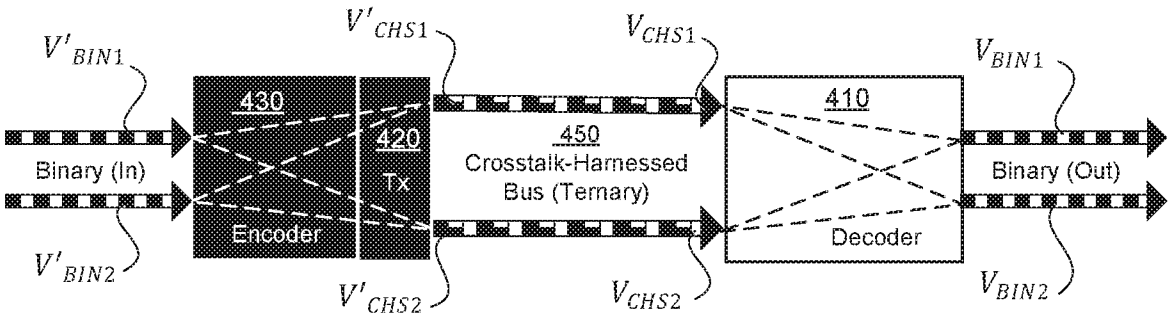
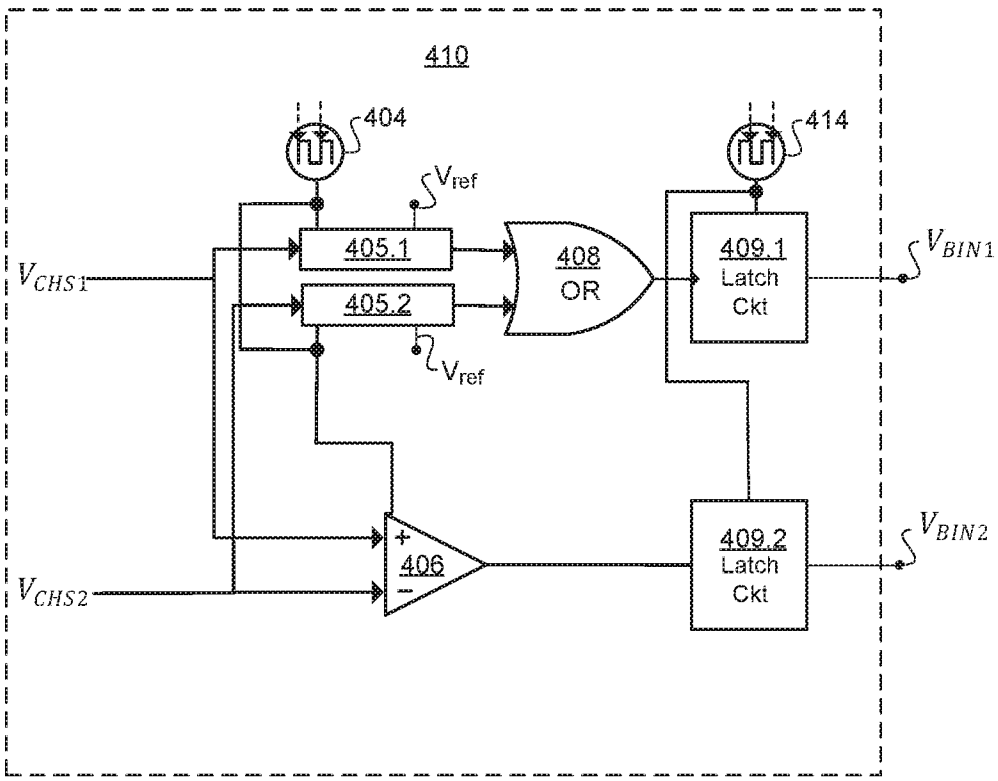


FIG. 4A

280 $V_{BIN1} = \begin{cases} 1, & V_{CHS1} > V_{ref} \text{ OR } V_{CHS2} > V_{ref} \\ 0, & otherwise \end{cases}$

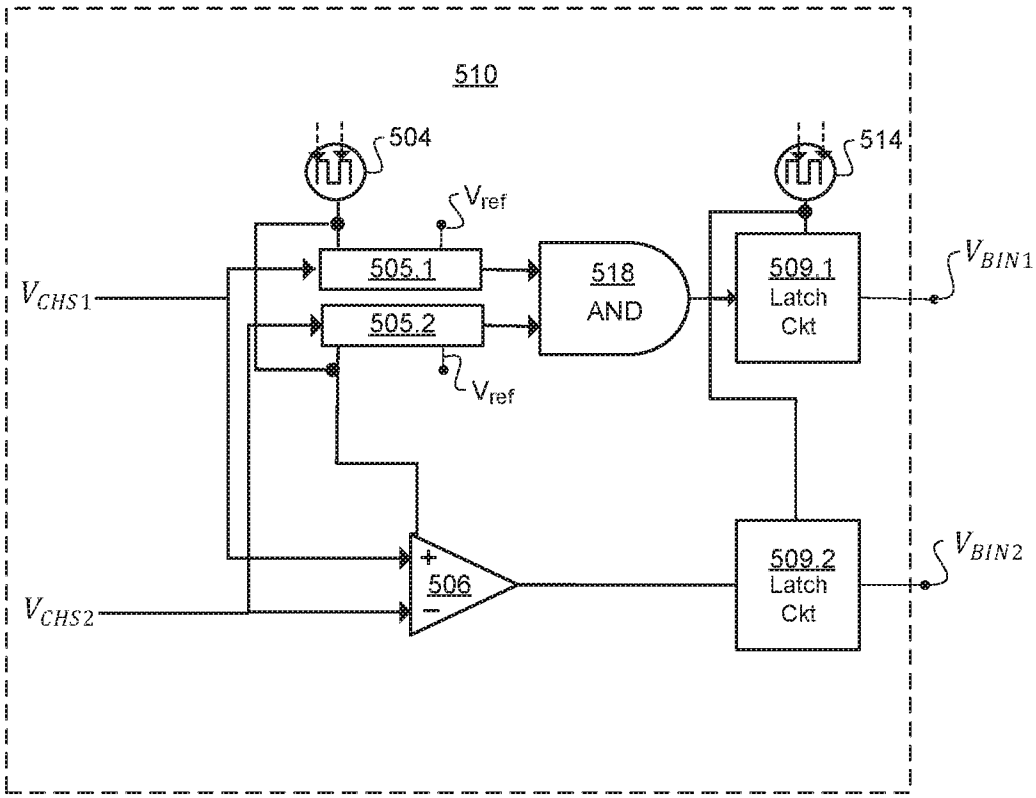


290 $V_{BIN2} = \begin{cases} 1, & V_{CHS2} > (V_{CHS1}) \\ 0, & otherwise \end{cases}$

FIG. 4B

580

$$V_{BIN1} = \begin{cases} 0, & V_{CHS1} \leq V_{ref} \text{ AND } V_{CHS2} \leq V_{ref} \\ 1, & otherwise \end{cases}$$



290

$$V_{BIN2} = \begin{cases} 1, & V_{CHS2} > V_{CHS1} \\ 0, & otherwise \end{cases}$$

FIG. 5

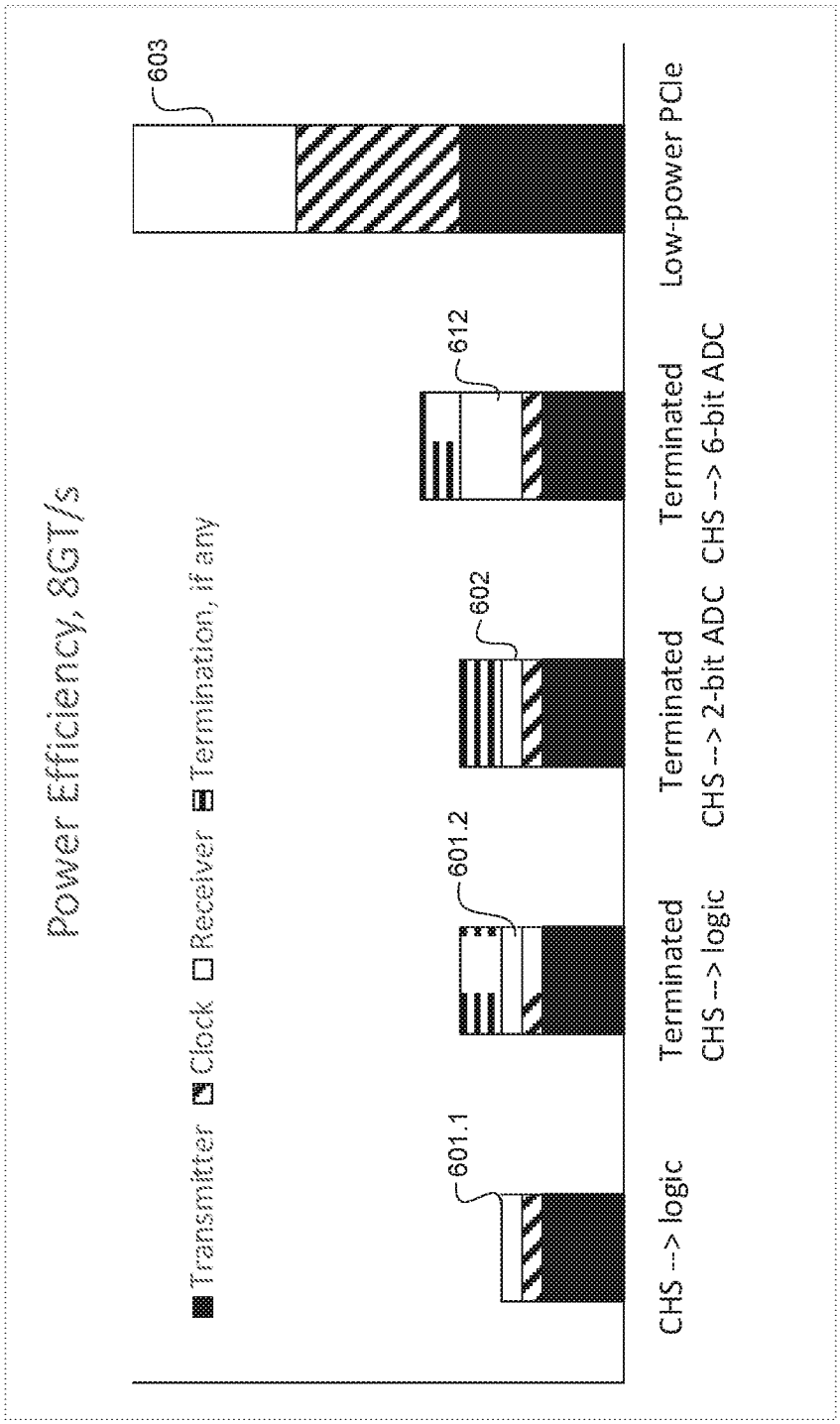

Power Efficiency, 8GT/s
Transmitter
Clock
Receiver
Termination, if any
603
612
602
601.2
601.1
CHS --> logic
Terminated
CHS --> logic
Terminated
CHS --> 2-bit ADC
Terminated
CHS --> 6-bit ADC
Low-power PCIe

FIG. 6

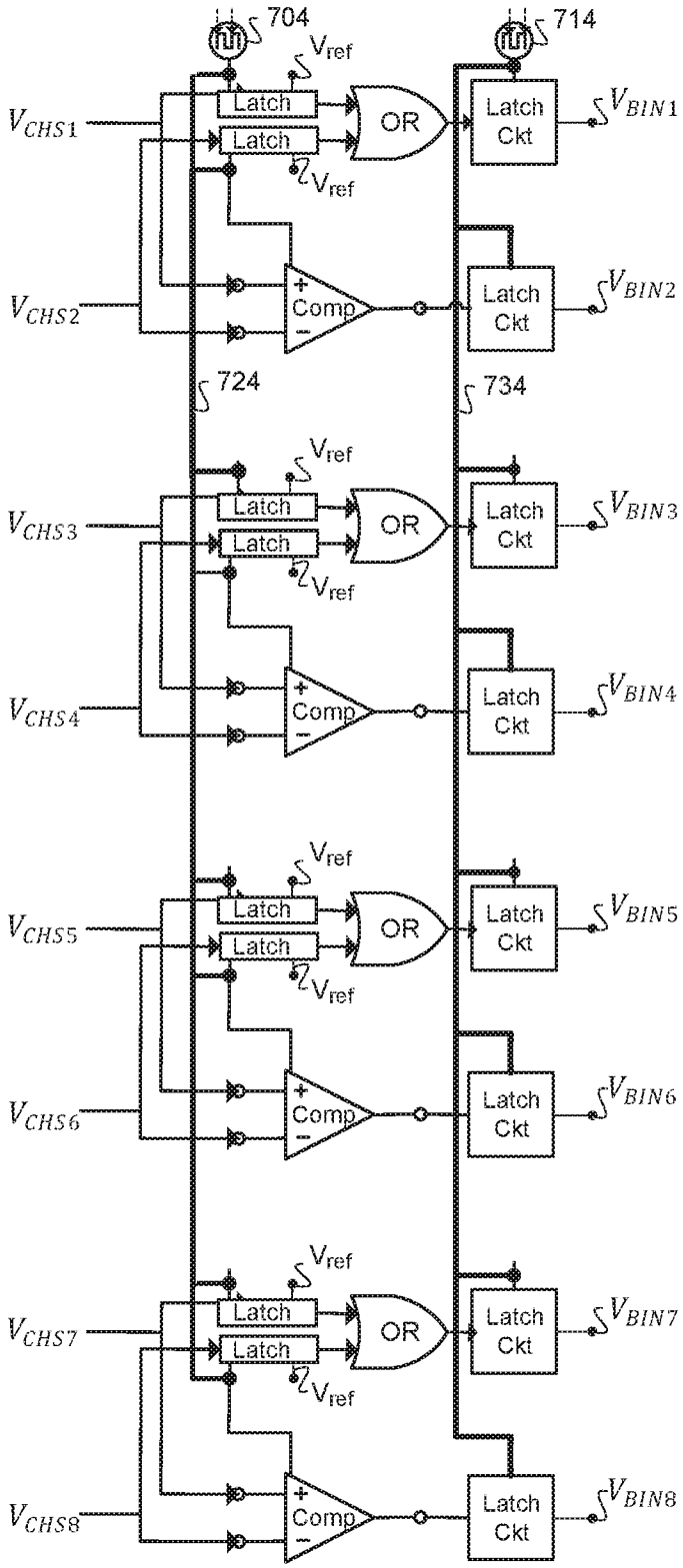

704
714
Vref
Latch
Latch
OR
Latch Ckt
V_{BIN1}
V_{CHS1}
Comp
V_{CHS2}
V_{BIN2}
724
734
V_{CHS3}
V_{BIN3}
V_{CHS4}
V_{BIN4}
V_{CHS5}
V_{BIN5}
V_{CHS6}
V_{BIN6}
V_{CHS7}
V_{BIN7}
V_{CHS8}
V_{BIN8}

FIG. 7

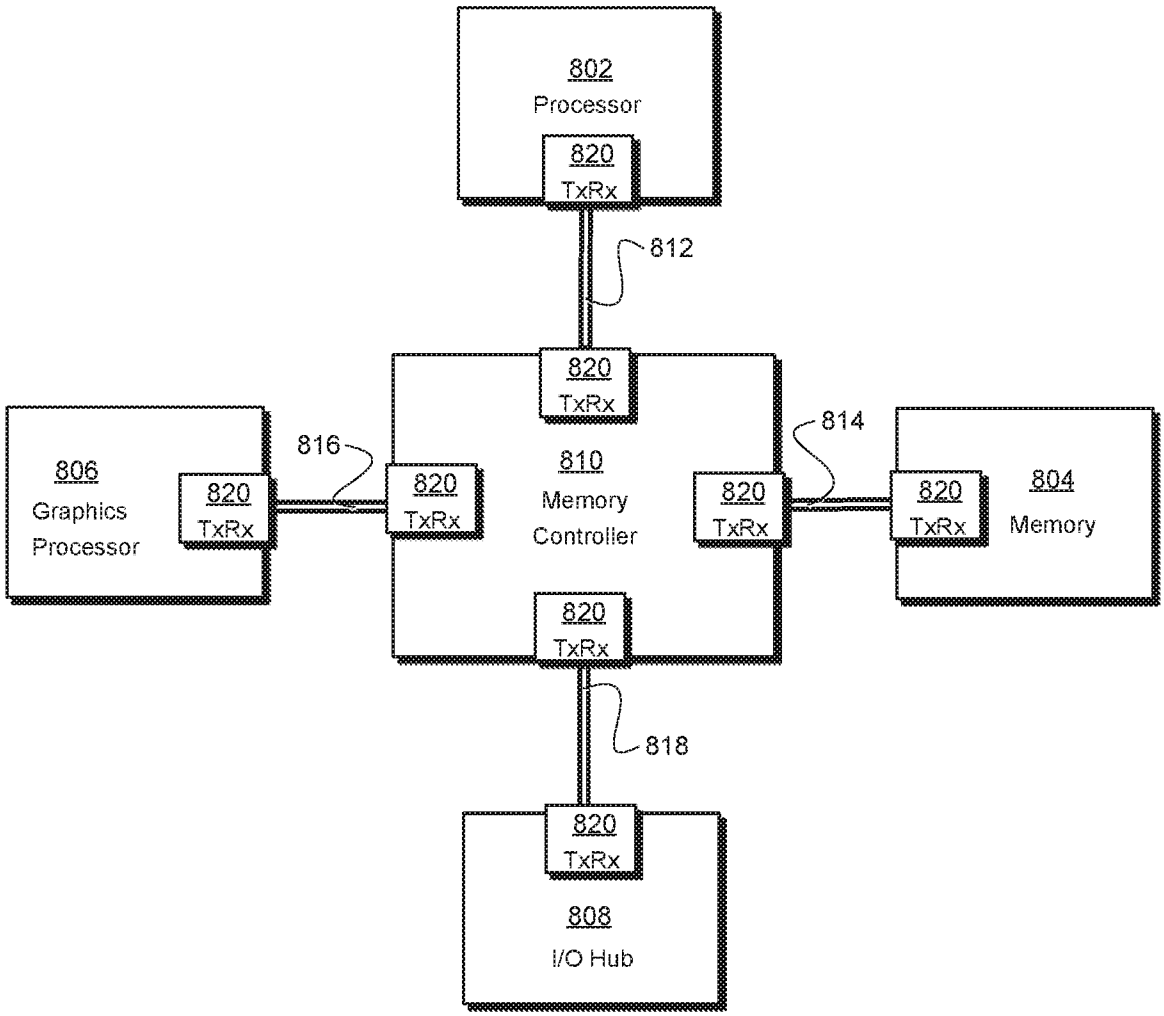

802
Processor
820
TxRx
812
820
TxRx
816
814
806
Graphics
Processor
820
TxRx
820
TxRx
810
Memory
Controller
820
TxRx
820
TxRx
804
Memory
820
TxRx
818
820
TxRx
808
I/O Hub

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US16/67502

A. CLASSIFICATION OF SUBJECT MATTER
IPC - H04B 3/487; H01B 11/04; G06F 15/17 (2017.01)
CPC - H01B 11/04; H05K 1/0212; G06F 3/122; H04B 3/32; H04M 3/34; G06F 17/5068; G11C 5/04; G11C 5/063; G06F 15/17

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/0181348 A1 (OLUWAFEMI, O et al.) 26 June 2014; Abstract; paragraphs [0018], [0025], [0030], [0042].	1-8
A	US 2014/0355407 A1 (CRONIE, H) 4 December 2014; entire document.	1-8
A	US 2010/0254467 A1 (BRAUN, M et al.) 7 October 2010; entire document.	1-8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 April 2017 (13.04.2017)	03 MAY 2017
Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US16/67502

-***-Continued from Box III-***-

The special technical features of Group I include at least a memory controller; a first communication link between the memory controller and at least one peripheral device; a multi-level non-binary signal; and sampling an encoded signal and recovering the binary signal based on the sampling., which are not present in Groups II-III.

The special technical features of Group II include at least a crosstalk-harnessed bus having a first differential pair of signal lines; a digital transmitter coupled to a first end of the crosstalk-harnessed bus; a digital receiver coupled to a second end of the crosstalk-harnessed bus; an encoder coupled to an input of the digital transmitter, wherein the encoder comprises arithmetic logic to convert a pair of binary signals to a first pair of ternary signals based on a product of a first voltage vector (V'.sub.BIN.) representing a binary bit, a weighted matrix, a normalizing factor, and a multiplier, which are not present in Groups I and III.

The special technical features of Group III include at least a comparator to compare the first multi-level CBS and the second multi-level CHS; a gate coupled to an output of the first latch and an output of the second latch; a first latching circuit coupled to an output of the gate; a second latching circuit coupled to an output of the comparator; a first clock sample signal coupled to the first latch, the second latch and the comparator; and a second clock sample signal coupled to the first latching circuit and the second latching circuit, which are not present in Groups I-II.

The common technical features shared by Groups I-III are a decoder; and a crosstalk-harnessed signal. However, these common features are previously disclosed by US 2014/0181348 A1 to OLUWAFEMI et al. (hereinafter "Oluwafemi"). Oluwafemi discloses a decoder (decoder 212; Fig. 2 and para [0024]-[0027]); and a crosstalk-harnessed signal (data transmitted (signal) over bus 200 in such a way that negative effects of crosstalk are removed (crosstalk-harnessed) and signal quality is enhanced; para [0023]).

Since the common technical features are previously disclosed by the Oluwafemi reference, these common features are not special and so Groups I-III lack unity.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US16/67502

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-8 are directed towards a computing system.
Group II: Claims 9-13 are directed towards a link.
Group III: Claims 14-20 are directed towards a decoder.

The inventions listed as Groups I-III do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

***see extra sheet ***

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-8

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.