



- (51) **International Patent Classification:**
H01L 27/115 (2006.01) *H01L 21/8247* (2006.01)
- (21) **International Application Number:**
PCT/US2012/044077
- (22) **International Filing Date:**
25 June 2012 (25.06.2012)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
61/500,547 23 June 2011 (23.06.2011) US
13/529,985 21 June 2012 (21.06.2012) US
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(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report (Rule 48.2(g))

(54) **Title:** MEMORY ARRAY ARCHITECTURE WITH TWO-TERMINAL MEMORY CELLS

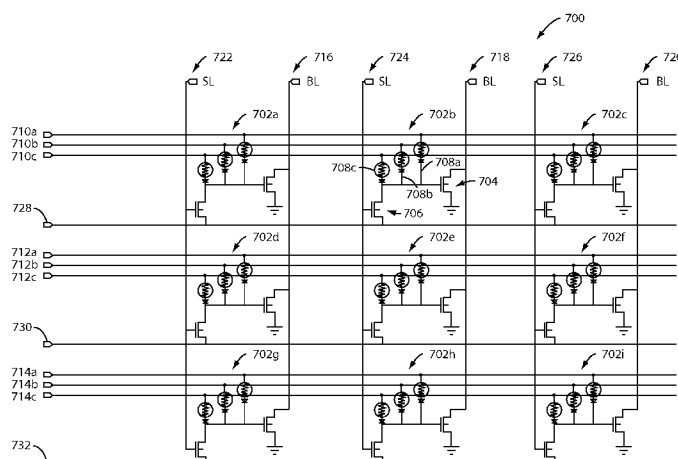


FIG. 7

(57) **Abstract:** A non-volatile memory device includes a word line extending along a first direction; a bit line extending along a second direction; a memory unit having a read transistor coupled to the bit line, at least one two-terminal memory cell, and a select transistor, the two-terminal memory cell having a first end coupled to the word line and a second end coupled to a gate of the read transistor. The second end of the two-terminal memory cell is coupled to a common node shared by a drain of the select transistor and the gate of the read transistor.

MEMORY ARRAY ARCHITECTURE WITH TWO-TERMINAL MEMORY CELLS

BACKGROUND

[0001] The present invention relates to a memory array architecture including two-terminal memory cells, e.g., resistive memory cells.

[0002] A resistive random-access memory (RRAM) is a type of a resistive memory and has generated significant interest recently as a potential candidate for ultra-high density non-volatile information storage. A typical RRAM device has an insulator layer provided between a pair of electrodes and exhibits electrical pulse induced hysteretic resistance switching effects.

[0003] The resistance switching has been explained by the formation of conductive filaments inside the insulator layer due to Joule heating and electrochemical processes in binary oxides (e.g. NiO and TiO₂) or redox processes for ionic conductors including oxides, chalcogenides, and polymers. The resistance switching has also been explained by field assisted diffusion of ions in TiO₂ and amorphous silicon (a-Si) films.

[0004] In the case of a-Si structures, electric field-induced diffusion of metal ions into the silicon leads to the formation of conductive filaments that reduce the resistance of the a-Si structure. These filaments remain after a biasing (or program) voltage is removed, thereby giving the device its non-volatile characteristic, and they can be removed by reverse flow of the ions back toward the metal electrode under the motive force of a reverse polarity applied voltage.

[0005] Resistive devices based on the a-Si structure, particularly, that formed on polysilicon, typically exhibit good endurance or life cycle. However, the endurance of the resistive device can be shortened if an excessive bias voltage is applied to the device during repeated write and erase cycles in part due to Joule heating and movements of an unnecessarily large number of metal ions in the a-Si structure. Furthermore, in general, RRAM device yield is affected by an electroforming process during which a major part of a conducting path is formed inside a switching medium by applying a larger voltage (or current) signal to the device.

BRIEF SUMMARY OF THE INVENTION

[0006] The present invention relates to a memory array architecture including two-terminal memory cells, e.g., resistive memory cells. The memory array includes a plurality of memory units, each including a program/erase transistor, a read transistor, and at least one two-terminal memory cell such as RRAM.

[0007] In one embodiment, a non-volatile memory device includes a word line extending along a first direction; a bit line extending along a second direction; and a memory unit having a read transistor coupled to the bit line, at least one two-terminal memory cell, and a select transistor, the two-terminal memory cell having a first end coupled to the word line and a second end coupled to a gate electrode of the read transistor.

[0008] In another embodiment, a non-volatile memory device includes a plurality of memory units arranged in an array of rows and columns, the each memory unit having a plurality of resistive memory cells, each resistive memory cell having a first end and a second end. A plurality of word lines extends along a first direction and having a first group of word lines associated with a first row of memory units, a second group of word lines associated with a second row of memory units, and a third group of word lines associated with a third row of memory units. A plurality of bit lines extends along a second direction and having a first bit line associated with a first column of memory units, a second bit line associated with a second column of memory units, and a third bit line associated with a third column of memory units. A plurality of read transistors is provided, each read transistor being associated with one of the memory units and having a drain electrode coupled to one of the bit lines. A plurality of select transistors is provided, each select transistor being associated with one of the memory units. A plurality of select lines have a first select line coupled to gate electrodes of the select transistors associated with the first column of memory units, a second select line coupled to gate electrodes of the select transistors associated the second column of memory units, and a third select line coupled to gate electrodes of the select transistors associated with the third column of memory units. A plurality of source lines have a first source line coupled to source electrodes of select transistors associated with the first row of memory units, a second source line coupled to source electrodes of select transistors associated with the second row of memory units, and a third source line coupled to source electrodes of select transistors associated with the third row of memory units. The first terminals of the resistive memory cells are coupled to the corresponding word lines and the second terminals of the resistive memory cells are coupled to corresponding common nodes,

each common node being shared by the drain electrode of one of the select transistor and the gate electrode of the corresponding read transistor.

[0009] In another embodiment, a memory unit of a memory device includes a plurality of resistive memory cells; a select transistor having a drain electrode coupled to a common node, a gate electrode coupled to a select line, and a source electrode coupled to a source line; and a read transistor having a drain electrode coupled to a bit line and a gate electrode coupled to the common node. Each resistive memory cell has a first end coupled to a word line and a second end coupled to the common node, and a switching medium provided between the first and second ends.

[0010] In yet another embodiment, a method for programming a memory device includes providing a memory unit having a plurality of resistive memory cells, a select transistor having a drain electrode coupled to a common node, a gate electrode coupled to a select line, and a source electrode coupled to a source line, a read transistor having a drain electrode coupled to a bit line and a gate electrode coupled to the common node, wherein each resistive memory cell has a first end coupled to a word line and a second end coupled to the common node, and a switching medium provided between the first and second ends. The method further includes selecting at least one resistive memory cell; and applying a first potential to the word line associated with the selected memory cell with respect to the common node.

[0011] In yet another embodiment, the first potential is a positive potential. The method further includes applying the program voltage to the word line associated with the selected memory cell; and applying a select voltage to the gate electrode of the select transistor to turn on the select transistor.

[0012] In yet another embodiment, the first potential corresponds to a read voltage sufficient to cause electrical current to flow through the selected resistive memory cell if the selected resistive memory cell is in a low resistive state, the read voltage not being sufficient to change a resistive state of the selected memory cell.

[0013] In yet another embodiment, the first potential is a negative potential. The method further includes applying an erase voltage to the source line; applying about 0 volt to the word line associated with the selected memory cell; and applying a select voltage to the gate electrode of the select transistor to turn on the select transistor.

[0014] The details of one or more embodiments are set forth in the accompanying drawings and the description below. Other features, objects, and advantages will be apparent from the description and drawings, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Exemplary embodiments will hereinafter be described in conjunction with the appended drawings, wherein like designations denote like elements, and wherein:

[0016] FIG. 1 illustrates a non-volatile memory device including a bottom electrode, a switching medium, and a top electrode according an embodiment of the present invention;

[0017] FIG. 2A illustrates resistance switching characteristics of the device according to an embodiment of the present invention;

[0018] FIG. 2B illustrates resistance switching characteristics of the device according to an embodiment of the present invention;

[0019] FIG. 3A illustrates a two-terminal device that is placed in an ON state by applying a program voltage V_{pth} to the top electrode;

[0020] FIG. 3B illustrates a two-terminal device that is placed in an OFF state by applying an erase voltage V_{eth} to the top electrode.

[0021] FIG. 4 illustrates a non-crystalline or amorphous silicon (a-Si) based crossbar memory array according to an embodiment of the present invention.

[0022] FIG. 5 illustrates a block diagram of a non-volatile memory device according to an embodiment of the present invention.

[0023] FIG. 6 illustrates a memory array including a plurality of memory units according to an embodiment of the present invention.

[0024] FIG. 7 illustrates a memory array including a plurality of memory units where each memory unit includes a read transistor, a plurality of resistive memory cells, and a select transistor according to an embodiment of the present invention.

[0025] FIG 8 illustrates a program operation of a memory device according to an embodiment of the present invention.

[0026] FIG 9 illustrates a bit erase operation of a memory device according to an embodiment of the present invention.

[0027] FIG 10 illustrates a page erase operation of a memory device according to an embodiment of the present invention.

[0028] FIG 11 illustrates a read operation of a memory device according to an embodiment of the present invention.

[0029] FIG 12 illustrates a read operation of a memory device according to another embodiment of the present invention.

[0030] FIG 13 illustrates a read operation of a memory device according to another embodiment of the present invention.

[0031] FIG 14 illustrates a bit line sensing operation according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0032] The present invention relates to a memory array architecture including two-terminal memory cells, e.g., resistive memory cells. The memory array includes a plurality of memory units, each including a program/erase transistor, a read transistor, and at least one two-terminal memory cell. The two-terminal memory cells include RRAM, phase-change memory, magnetoresistive random access memory (MRAM), spin-transfer torque RAM (STT-RAM), and the like.

[0033] FIG. 1 illustrates a non-volatile memory device 100 including a bottom electrode 102, a switching medium 104, and a top electrode 106 according an embodiment of the present invention. The switching medium 104 exhibits a resistance that can be selectively set to various values, and reset, using appropriate control circuitry. The device 100 is a two-terminal resistive memory device, e.g., a resistive random-access memory (RRAM), in the present embodiment. As will be appreciated by one skilled in art, the device 100 may also be used as other types of devices such as a programmable variable capacitor.

[0034] The resistive memory device is a two-terminal device having a switching medium provided between top and bottom electrodes. The resistance of the switching medium can be controlled by applying an electrical signal to the electrodes. The electrical signal may be current-based or voltage-based. As used herein, the term “RRAM” or “resistive memory device” or “resistive memory cell” refers to a memory device that uses a switching medium whose resistance can be controlled by applying an electrical signal without ferroelectricity, magnetization and phase change of the switching medium.

[0035] In the present embodiment, the device 100 is an amorphous-silicon-based resistive memory device and uses amorphous silicon (a-Si) as the switching medium 104. The resistance of the switching medium 104 changes according to formation or retrieval of a conductive filament inside the a-Si switching medium 104 according to a voltage applied. The top electrode 106 is a conductive layer containing silver (Ag) and acts as a source of filament-forming ions in the a-Si switching medium 104. Although silver is used in the present embodiment, it will be understood that the top electrode 106 can be formed from various other suitable metals, such as gold (Au), nickel (Ni), aluminum (Al), chromium (Cr), iron (Fe), manganese (Mn), tungsten (W), vanadium (V), and cobalt (Co). The bottom electrode 102 is a boron-doped or other p-type polysilicon electrode that is in contact with a lower end face of the a-Si switching medium 104.

[0036] FIG. 2A illustrates resistance switching characteristics of the device 100 according to an embodiment of the present invention. The switching medium 104 displays a bipolar switching mechanism. The resistance of the switching medium 104 changes depending on the polarity and magnitude of a current signal applied to the switching medium 104 via the top and bottom electrodes 106 and 102. The device 100 is changed into an ON-state (low resistance state) when a positive voltage equal to or greater than a program threshold voltage (or program voltage) V_{pth} is applied. In an embodiment, the program voltage ranges between 1 volt to 5 volts depending on the materials used for the switching medium 104 and the top electrode 106. The device 100 is switched back to an OFF-state (high resistance state) when a negative voltage equal to or greater than an erase threshold voltage (or erase voltage) V_{eth} is applied. In an embodiment, the erase voltage ranges from -1 volts to -5 volts. The device state is not affected if the voltage applied is between the two threshold voltages V_{pth} and V_{eth} , which enables a low-voltage, read process. Once the device 100 is set to a specific resistance state, the device 100 retains information for a certain period (or retention time) without electrical power.

[0037] FIG. 2A illustrates non-rectifying switching characteristics of the device 100 according to an embodiment of the present invention. Electrical current flows from the top electrode 106 to the bottom electrode 102 when the top electrode 106 is applied with a positive potential with respect to the bottom electrode 102. On the other hand, the current flows in a reverse direction if the top electrode 106 is applied with a negative potential with respect to the bottom electrode 102.

[0038] FIG. 2B, on the other hand, illustrates rectifying switching characteristics of the device 100 according to another embodiment of the present invention. Electrical current flows from the top electrode 106 to the bottom electrode 102 when the top electrode 106 is applied with a positive potential with respect to the bottom electrode 102, but the current does not flow in the reverse direction even if the top electrode 106 is applied with a negative potential with respect to the bottom electrode 102. Under this embodiment, the device 100 exhibits a diode-like behavior and can be represented with an equivalent circuit including a resistor connected in series with a diode. The device 100 can be controlled to exhibit either rectifying or non-rectifying characteristics by controlling the amount of current flowing through the device as will be explained in more detail later.

[0039] FIGs. 3A and 3B illustrate a switching mechanism of the device 100 during the ON and OFF states according to an embodiment of the present invention. The switching in the a-Si switching medium 104 is based on formation and retrieval of a conductive filament or a plurality of filaments in a filament region in the a-Si switching medium 104 according to the program and erase voltages applied to the electrodes 102 and 106 of the device 100.

[0040] FIG. 3A illustrates the device 100 that is placed in the ON state (or programmed state) by applying the program voltage V_{pth} to the top electrode 106. The switching medium 104 made of a-Si is provided between the bottom electrode 102 and the top electrode 106. An upper portion of the switching medium 104 includes a metallic region (or conductive path) 302 that extends from the top electrode 106 to about 10 nm above the bottom electrode 102. The metallic region 302 is formed during an electroforming process when a slightly larger voltage than a subsequent switching voltage, e.g., 1 ~ 5 V, is applied to the top electrode 106. This large voltage causes the electric field induced diffusion of the metal ions from the top electrode 106 toward the bottom electrode 102, thereby forming a continuous conductive path 303. A lower portion of the switching medium 104 defines a filament region 304 wherein a filament 305 is formed when the program voltage V_{pth} is applied after the electroforming process. The regions 303 and 305 can be also formed together during the electroforming process. The filament 305 includes a series of metal particles that are trapped in defect sites in the lower portion of the switching medium 104 when the program voltage V_{pth} applied provides sufficient activation energy to push a number of metal ions from the metallic region 302 toward the bottom electrode 102.

[0041] The filament 305 is believed to be comprised of a collection of metal particles that are separated from each other by the non-conducting switching medium and does not define a continuous conductive path, unlike the path 303 in the metallic region 302. The filament 305 extends about 2-10 nm depending on implementation. The conduction mechanism in the ON state is electrons tunneling through the metal particles in the filament 305. The device resistance is dominated by the tunneling resistance between a metal particle 306 and the bottom electrode 102. The metal particle 306 is a metal particle in the filament region 304 that is closest to the bottom electrode 102 and is the last metal particle in the filament region 304 in the ON state.

[0042] FIG. 3B illustrates the device 100 that is placed in an OFF state (or erased state) by applying the erase voltage V_{eth} to the top electrode 106. The erase voltage V_{eth} exerts a sufficient electromagnetic force to dislodge the metal particles trapped in the defect sites of the a-Si and retrieves at least part of the filament 305 from the filament region 304. A metal particle 308 that is closest to the bottom electrode 102 in the OFF state is separated from the bottom electrode 102 by a distance greater than the metal particle 306 during the ON state. This increased distance between the metal particle 308 and the bottom electrode 102 places the device 100 in a high resistance state compared to the ON state. In an embodiment, a resistance ratio between the ON/OFF states ranges from $10E3$ to $10E7$. The device 100 behaves like a resistor in the ON state and a capacitor in the OFF state. That is, the switching medium 104 does not conduct current in any meaningful amount and behaves basically as a dielectric in the OFF state. In an implementation, the resistance is $10E5$ Ohm in the ON state and $10E10$ Ohm in the OFF state. In another implementation, the resistance is $10E4$ Ohm in the ON state and $10E9$ Ohm in the OFF state. In yet another implementation, the resistance is at least $10E7$ Ohm in the OFF state.

[0043] Referring back to FIGs. 2A and 2B, the device 100 can be controlled to exhibit a diode-like behavior by controlling the amount of current flowing through the device 100. If the amount of current flowing through the device 100 is less than a threshold amount, the device 100 exhibits a diode-like behavior, thereby preventing a reverse current flow from the bottom electrode 102 to the top electrode 106. In an embodiment, the threshold current is $10 \mu A$ so that the device 100 exhibits non-rectifying characteristics (see FIG. 2A) if the amount of current is $10 \mu A$ or more and rectifying characteristics (see FIG. 2B) if the amount of current is less than $10 \mu A$. The threshold current varies according to the device implementation, e.g., the materials used and the size of the device 100.

[0044] It is believed that a negative potential applied to the bottom electrode 102 causes the metal particle 306 closest to the bottom electrode 102 (see FIG. 3A) to shift slightly upward without dislodging it from the filament region 304. The resulting increased distance between the metal particle 306 and the bottom electrode 102 increases the resistance and prevents the current from flowing from the bottom electrode 102 to the metal particle 306. If the current, however, is equal to or greater than the threshold level, the large current bursts through the metal particle 306 from the bottom electrode 102.

[0045] FIG. 4 illustrates a non-crystalline or a-Si based crossbar memory array 400 according to an embodiment of the present invention. The crossbar memory array 400 includes a parallel array of bottom electrodes 402 extending along a first direction. In an embodiment, the bottom electrodes 402 include a bottom metal (not shown) and a p-type polysilicon (not shown) formed on the bottom metal. The bottom electrodes 402 are nanoscale in the present embodiment. For example, the bottom electrodes 402 have a width of about 40 nm and a pitch of about 60 nm.

[0046] A parallel array of top electrodes 404 extends along a second direction to intersect the bottom electrodes 402. The top electrodes 404 include metals capable of supplying filament-forming ions such as silver (Ag), gold (Au), nickel (Ni), aluminum (Al), chromium (Cr), iron (Fe), manganese (Mn), tungsten (W), vanadium (V) and cobalt (Co). In an embodiment, the top electrodes 404 and the bottom electrodes 402 are orthogonal to each other. The top electrodes 404 are nanowires having a width of about 60 nm and a pitch of about 150 nm.

[0047] Each intersection 406 of the two arrays 402 and 404 defines a two-terminal resistive memory cell 408. The memory cell 408 at each intersection 406 includes two electrodes 402 and 404 separated by a switching layer 410. The switching layer or structure can have a width substantially the same as or narrower than that of the bottom electrode 402. In some embodiments, each memory cell in a crossbar memory array can store a single bit. In other embodiments, the memory cells exhibit multi-level resistance thereby allowing storage of a plurality of bits at each cell.

[0048] In the present embodiment, the switching layer 410 includes amorphous silicon or other non-crystalline silicon. As used herein, the term “amorphous silicon” refers to silicon material that is in substantially amorphous phase and may include small grains of crystalline

silicon. As used herein, the term “non-crystalline silicon” refers to amorphous silicon or amorphous polysilicon that exhibits controllable resistance, a combination thereof, or the like.

[0049] The crossbar memory array as described above may be fabricated on a silicon substrate in an embodiment. In another embodiment, III-V type semiconductor compounds (such as gallium arsenide (GaAs), gallium nitride (GaN), boron nitride (BN), etc.) or II-VI type semiconductor compounds (such as cadmium selenide, zinc telluride, etc.) may also be used as the substrate.

[0050] FIG. 5 illustrates a block diagram of a non-volatile solid state resistive switching device 500 according to an embodiment of the present invention. The device 500 includes a memory array 502 including a plurality of memory units. Each memory unit includes a plurality of resistive memory cells. In the present embodiment, the resistive memory cells are in a NOR configuration where each resistive memory cell can be accessed independently from other resistive memory cells in the same memory unit. In other embodiment, the resistive memory cells may be in a NAND, crossbar, or other configuration. A row decoder 504 receives the address of a resistive memory cell to be operated on and selects a word line associated with the resistive memory cell. A column decoder 506 receives the address of the resistive memory cell for an operation and selects a bit line associated with the resistive memory cell. A select line decoder 508 receives the address of the resistive memory cell and selects a select line associated with a memory unit including the resistive memory cell. A source switch 510 applies a voltage suitable for an operation to be performed on a source line of the memory unit. A sense amplifier 512 senses the current flowing through the bit line selected to determine whether or not a selected resistive memory cell of the memory unit has been programmed or erased. An output buffer 514 receives data sensed by the sense amplifier 512 and outputs the data to a data bus according to an output enable signal.

[0051] FIG. 6 illustrates a memory array 600 including a plurality of memory units 602 according to an embodiment of the present invention. Each memory unit 602 is uniquely identified by a word line 606, a bit line 608, and a select line 610. A source line 612 provides voltages suitable for performing a given operation. The source line 612 is not needed to identify the memory unit 602 in the present embodiment. In other embodiment, the source line 612 may be used to identify a specific memory unit 602.

[0052] Each memory unit 602 includes at least one resistive memory cells (See FIG. 7) for storing information. The resistive memory cell stores one or more bits depending on

implementation. Each resistive memory cell is coupled to the word line 606. Although only one word line 606 is illustrated for each memory unit 602 in Fig. 6, any number of word lines may be provided for the memory unit 602 according to implementation. In an embodiment, each memory unit 602 has twelve (12) resistive memory cells and twelve (12) word lines associated thereto. In another embodiment, each memory unit 602 has thirty-two (32) resistive memory cells and thirty-two (32) word lines associated thereto. In yet another embodiment, each memory unit 602 has sixty-four (64) resistive memory cells and sixty-four (64) word lines associated thereto.

[0053] FIG. 7 illustrates a memory array 700 including a plurality of memory units 702a-702i that are arranged an array of rows and columns according to an embodiment of the present invention. Each memory unit includes a read transistor 704, a program/erase transistor 706 (also referred to as a “select transistor”), and a plurality of resistive memory cells 708a, 708b, and 708c for storing data. Since data are stored in the resistive memory cells, the read transistor 704 is not required to be scaled down to a nano scale in order to provide the requisite device density, unlike those memory devices that use transistors to store data, e.g., Flash and DRAM memory devices.

[0054] A gate electrode of the read transistor 704 and a drain electrode of the program/erase transistor 706 share a common node. Bottom electrodes of the resistive memory cells 708a, 708b, and 708c are coupled to this common node connecting the gate electrode of the read transistor 704 and the drain electrode of the program/erase transistor 706. Each resistive memory cell in a memory unit may be programmed, erased, or read independently from other memory cells in the same memory unit. For illustrative convenience, only three resistive memory cells 708a, 708b, and 708c are shown for each memory unit, but their number can vary according to implementation.

[0055] In the present embodiment, the resistive memory cells 708a, 708b, and 708c are operated to exhibit diode-like characteristics so that an electrical current flows from the top electrode (e.g., the word line) to the bottom electrode (e.g., the common node connected to the gate electrode of the read transistor). Each resistive memory cell, therefore, exhibits characteristics of a resistor connected in series with a diode. This unidirectional current flow prevents problems associated with a sneak-path current without using an external diode that would require greater device fabrication complexity and larger device real estate.

[0056] Referring back to FIG. 7, the memory array 700 has word lines that are grouped according to the rows of memory units. A plurality of first word lines 710a, 710b, and 710c are associated with the memory units 702a, 702b, and 702c in a first row. Each of the first word lines is connected to the top electrode of one of memory cells of each memory unit in the first row. For example, the first word lines 710a, 710b, and 710c are connected to the resistive memory cells 708a, 708b, and 708c of the memory unit 702b, respectively. A plurality of second word lines 712a, 712b, and 712c are associated with the memory units 702d, 702e, and 702f in a second row. Each of the second word lines is connected to the top electrode of one of memory cells of each memory unit in the second row. A plurality of third word lines 714a, 714b, and 714c are associated with the memory units 702g, 702h, and 702i in a third row. Each of the third word lines is connected to the top electrode of one of memory cells of each memory unit in the third row.

[0057] In an embodiment, each group of word lines has the same number of word lines as the number of memory cells in a memory unit. For example, each group of word lines may have eight (8) word lines, sixteen (16) word lines, thirty-two (32) word lines, or sixty-four (64) word lines according to the number of memory cells provided in each memory unit. Depending on implementation, a page of data may be defined by each word line, each memory unit, or each row of memory units.

[0058] A first bit line 716 is connected to drains of read transistors of the memory units 702a, 702d, and 702g in a first column. A second bit line 718 is connected to drains of read transistors of the memory units 702b, 702e, and 702h in a second column. A third bit line 720 is connected to drains of read transistors of the memory units 702c, 702f, and 702i in a third column.

[0059] A first select line 722 is connected to gates of program/erase transistors of the memory units 702a, 702d, and 702g in a first column. A second select line 724 is connected to gates of program/erase transistors of the memory units 702b, 702e, and 702h in a second column. A third select line 726 is connected to gates of program/erase transistors of the memory units 702c, 702f, and 702i in a third column. In the present embodiment, a memory unit is selected for an operation by selecting a word line, a bit line, and a select line associated thereto.

[0060] A first source line 728 is connected to sources of program/erase transistors of the memory units 702a, 702b, and 702c in the first row. A second source line 730 is connected

to sources of program/erase transistors of the memory units 702d, 702e, and 702f in the second row. A third source line 732 is connected to sources of program/erase transistors of the memory units 702g, 702h, and 702i in the third row. In the present embodiment, the source lines provide appropriate voltages to the program/erase transistors according to an operation to be performed on a selected resistive memory cell. In an embodiment, each memory unit is associated with at least one word line, a bit line, and a select line. In an embodiment, each memory unit has eight (8) memory cells and is associated with eight (8) word lines. In another embodiment, each memory unit has sixteen (16) memory cells and is associated with sixteen (16) word lines. In another embodiment, each memory unit has thirty-two (32) memory cells and is associated with thirty-two (32) word lines.

[0061] In operations, a resistive memory cell is operated, e.g., programmed, erased, or read, by applying predetermined voltages to word lines, bit lines, select lines, and source lines of the memory array 700 according to an operation to be performed. The memory array 700 reads fast since the resistive memory cells are provided between the word lines and the gate of the read transistor instead of in the path of the bit lines. Below is an operation table according to an embodiment of the present invention.

Table 1

Operation	WL Selected	WL Unselected	Source Line	Select Line	BL Selected
Program	~3V (pulse)	1.5V or Float	0V	3V	Float or 0V
Erase	0V	Float or 4V	4V	4V	Float or 0V
Read	~1.5V (pulse)	Float or 0V	0V	0V or Vref	Sense current or voltage

[0062] The memory unit 702b is taken as an example, and the resistive memory cell 708a in the memory unit 702b is selected for programming. A select voltage is applied to the select line 724 and thus to the gate of the program transistor (or select transistor) 706. The channel region of the program transistor 706 becomes conductive. A first voltage (or the program voltage V_{pth}) is applied to the word line 710a connected to the resistive memory cell 708a by providing a potential difference between the word line 710a and the source line

728 connected to the source of the program transistor 706. A second voltage is applied to the word lines 710b and 710c that are connected to the unselected memory cells 708b and 708c.

[0063] In an embodiment, to program a cell, the first voltage of about 3 volts is applied to the word line 710a while the source line 728 is grounded. In another embodiment, the first voltage of about 1 volt is applied to the word line 710a while the source line 728 is grounded. The first voltage may be applied as voltage pulses. The second voltage having amplitude of no more than about half of that of the first voltage is applied to the word lines 710b and 710c. Alternatively, word lines associated with the unselected resistive memory cells can be maintained at float depending on the implementation. For amorphous silicon as the resistive switching material, the first voltage can range from about 0.5 volt to about 5 volts depending on the device dimension and process conditions of the amorphous silicon material, among others.

[0064] To erase a programmed cell, an erase voltage V_{eth} having a polarity opposite to that of the program voltage V_{pth} is applied to programmed cell. The erase voltage V_{eth} has amplitude that is about the same as or slightly greater than the program voltage V_{pth} .

[0065] The resistive memory cell 708a is taken as an example again. The erase voltage V_{eth} (e.g., 4 volts) is applied between the source line 728 and the word line 710a by applying a positive voltage to the source line 728 while the word line 710a is maintained at about 0 volt. The select voltage is applied to the select line 724 to turn on the program transistor 706.

[0066] In an embodiment, the read transistor 704 is kept turned off during the program or erase operation since the bit line is used to read data. Bit line 718 is maintained at float or 0 volt.

[0067] A read operation is performed to determine a state of a resistive memory cell. The bit line 718 is used to measure the current flow through the selected resistive memory cell 708a. The resistance state of the selected memory cell 708a is determined based on this current flow amount.

[0068] During read operation, a read voltage is applied to the word line 710a to provide a potential difference between the word line 710a and the source line 728. In an embodiment, the read voltage has amplitude that is about half of that of the program voltage V_{pth} in order to prevent the read voltage from disturbing the resistive state of the memory cell being read. In an embodiment, the read voltage is 0.5 to 1.5 volt and is applied as voltage pulses. A

voltage (e.g., 0.5 volt) is applied to the word lines 710b and 710c, which are associated with the unselected cells 708b and 708c. The voltage applied to the word lines 710b and 710c may vary according to implementation.

[0069] FIG. 8 illustrates a program operation of a memory device according to an embodiment of the present invention. Since memory cells are interconnected extensively, a leakage current can affect neighboring cells during a program, erase, or read operation. Accordingly, in an embodiment, a precharge operation is performed on the resistive memory cells before the program operation is performed. The precharge operation causes first and second terminals of each of the resistive memory cells in the same row to have substantially the same potential before the program operation. For example, if the resistive memory cell 708a in the memory unit 702b is selected for the programming, a precharge operation is performed to cause the first and second terminals of the resistive memory cells 708a, 708b, and 708c in the memory unit 702b to have a zero potential difference. The precharge operation includes applying a precharge voltage V_{pc} (or a first precharge voltage) to a selected word line WL_{sel} , e.g., the word line 710a associated with the selected resistive memory cell 708a. The precharge voltage V_{pc} is also applied to unselected word lines WL_{unsel} , e.g., the word lines 710b and 710c, that are in the same word line group and are associated with the memory units in the first row. Additionally, the precharge voltage V_{pc} (or second precharge voltage) is applied to the source line 728. In an embodiment, the first precharge voltage applied to the word lines WL_{sel} and WL_{unsel} and the second precharge voltage applied to the source line 728 are substantially the same. In other embodiments, the first and second precharge voltages may be different.

[0070] During the precharge operation, the second word lines 712a-712c and the third word lines 714a-714c that are associated with the memory units in the second row and the third row, respectively, are maintained at zero volt or float. The precharge voltage V_{pc} has an amplitude that is less than the program voltage V_{pth} so as not unintentionally program the memory cells during the precharge operation. In an embodiment, the amplitude of precharge voltage V_{pc} is no more than about half of that of the program voltage. A voltage V_{select} is applied to the select line 724 to turn on the program transistor 706 when the precharge voltage V_{pc} is applied to the word lines 710a, 710b, and 710c and the source line 728. As a result, the resistive memory cells 708a, 708b, and 708c in the memory unit 702b are at a precharged state.

[0071] Thereafter, the program voltage V_{pth} is applied to the word line 710a connected to the memory cell 708a in order to program it. The precharge voltage V_{pc} is no longer applied to the source line 728 and a voltage level of the source line 728 is reduced to a zero volt. The precharge voltage V_{pc} as is continued to be applied to the word lines 710b and 710c of the unselected resistive memory cells 708b and 708c. This precharge voltage V_{pc} (or inhibit voltage) is applied to inhibit the memory cells 708b and 708c from unintentionally be programmed by the program voltage V_{pth} applied to the selected resistive memory cell 708a.

[0072] FIG. 9 illustrates a bit erase operation of a memory device according to an embodiment of the present invention. The resistive memory cell 708a is taken as an example of a programmed cell. An erase voltage V_{eth} is applied to the source line 728 while a zero volt is applied to a selected word line WL_{sel} , e.g., the word line 710a associated with the selected resistive memory cell 708a. A select voltage V_{select} applied to the select line 724 to turn on the program transistor 706. The negative potential difference between the word line 710a and the source line 728 cause the memory cell 710a to be erased, i.e., placed at a high resistive state. A voltage, e.g., about $V_{eth}/2$, is applied to unselected word lines WL_{unsel} , i.e., the word lines 710b and 710c associated with the unselected cells 708b and 708c to prevent the unselected resistive memory cells 708b and 708c from being erased unintentionally. In an embodiment, the select voltage V_{select} is applied as voltage pulses.

[0073] FIG 10 illustrates a page erase operation of a memory device according to another embodiment of the present invention. The erase operation may be performed on a single cell, for example, the resistive memory cell 708a, as described above with reference to FIG. 9 or on a plurality of selected cells in a same row or a page, as illustrated in FIG. 10. In the present embodiment, the page is defined as all the memory cells of the memory units in the same row.

[0074] In a page erase operation, all the memory cells in the memory units 702a, 702b, and 702c are erased at the same time. A zero volt is applied to all the word lines WL_{sel} in the same row, i.e., the first word lines 710a, 710b, and 710c. A source voltage equivalent to the erase voltage V_{eth} is applied to the source line 728. A select voltage V_{select} is applied to the select lines 722, 724, and 726, in order to turn on the program/erase transistors of the memory units 702a, 702b, and 702c. All the memory cells of the memory units in the same row are erased at the same time since all of them are applied with the erase voltage. At this time, a

zero voltage is applied to the bit lines 716, 718, and 720. Alternatively, the bit lines 716, 718, and 720 may be maintained at float.

[0075] In an embodiment, a page may be defined as all the memory cells of a single memory unit. The page erase operation is performed in a similar manner as in figure 10, one difference being that the select voltage V_{select} is only applied to the select line associated with the memory unit to be erased. In another embodiment, a page is defined as all the memory cells connected to the same word line. The page erase operation can be performed in a similar manner as in figure 10, one difference being that the unselected word lines (e.g., 710b and 710c) of the same group are applied with an inhibit voltage, e.g., 1.5 volt, to prevent the memory cells connected to these unselected word lines from being erased.

[0076] FIGs. 11, 12, and 13 illustrate various ways to implement a read operation to determine the bit value of a resistive memory cell according to embodiments of the present invention. As memory cells in a memory array are interconnected using a bottom electrode and a top electrode as illustrated in FIG. 4, a read voltage applied to a selected cell should not inadvertently erase or program the memory cells. The read operation may be implemented with or without pre-charging the selected word lines or the selected source line. In the examples herein, the memory cell 708a of the memory unit 702b is assumed to have been selected for the read operation (see figure 7).

[0077] In an embodiment, no precharge voltage is applied before the read operation is performed on the memory cell 708a (see figure 11). A voltage V_1 , which is no more than the read voltage V_{read} , is applied to word lines WL_{unsel} , i.e., the word lines 710b and 710c, associated with the unselected memory cells 708b and 708c in the memory unit 702b. A read voltage V_{read} is applied to a selected word line WL_{sel} , i.e., the word line 710a, connected to the selected memory cell 708a while maintaining the source line 728 at a zero volt to. The read voltage V_{read} is selected to have amplitude (e.g., 0.5-1.5 volt) that would not inadvertently program or erase the resistive memory cell 708a. In an embodiment, the amplitude of the read voltage V_{read} is no more than half of that of the program voltage V_{pth} .

[0078] The potential difference caused by the read voltage V_{read} between the word line 710a and the source line 728 causes a current to flow through the selected memory cell 708a if it is in a programmed state (or low resistance state). This current (or the read voltage), in turn, turns on the read transistor 704 and causes current to flow through the read transistor 704, which would be sensed by a load or a sense circuitry (not shown) coupled to the bit line

718. The sense circuitry may be a current sensor or a voltage sensor according to implementation.

[0079] On the other hand, if the memory cell 708a is in an erased state (or high resistance state), little or no current would flow through the memory cell 708a even if the read voltage V_{read} is applied to the word line 710a. The read transistor 704 would remain turned off and the sense circuitry would not sense a necessary amount of current flow.

[0080] FIG. 12 illustrates a read operation according to another embodiment of the present invention. A reference voltage V_{ref} is applied to the select line 724 allowing the program transistor 706 to be conductive during a read operation (see figure 12). A read voltage V_{read} is applied to the word line 710a connected to the selected memory cell 708a. The source line 728 is applied a 0 volt. The potential difference between the word line 710a and the source line 728 causes current to flow through the memory cell 708a if it is in a programmed state. This current (or the read voltage), in turn, turns on the read transistor 704 and causes current to flow through the read transistor 704, which would be sensed by a load or a sense circuitry (not shown) coupled to the bit line 718. The sense circuitry may be a current sensor or a voltage sensor according to implementation.

[0081] FIG. 13 illustrates a read operation according to yet another embodiment of the present invention. The precharge operation is performed before the read operation. The precharge voltage V_{pc} is applied to a word line WL_{sel} , i.e., the word line 710a, for the select memory cell 708a and word lines WL_{unsel} , i.e., 710b and 710c, for the unselected memory cells in the memory unit 702b. The precharge voltage V_{pc} is also applied to the source line 728. A first select voltage V_{select} is applied to the select line 724 to turn on the program transistor 706. The memory cells 708a, 708b, and 708c in the memory unit 702b are thereby placed in a precharged state. The select voltage V_{select} is set to zero from the select line 724 to turn off the program transistor 706. A read voltage V_{read} is applied to word line 710a, and the source line 728 is applied with a zero volt. The potential difference between the word line 710a and the source line 728 would cause a current to flow if the memory cell 708a is in a programmed state. This current (or the read voltage), would increase the gate voltage of the read transistor 704, thereby turning on the read transistor 704 and causing current to flow through the read transistor 704, which would be sensed by a load or a sense circuitry (not shown) coupled to the bit line 718. The sense circuitry may be a current sensor or a voltage sensor according to implementation.

[0082] In an embodiment, a resistance state or a bit value of the selected memory cell, i.e., the resistive memory cell 708a, is determined by comparing the read current to a reference current. As noted, the memory cell can be characterized by an off-state resistance of a giga-ohm (10^9) range which corresponds to an off-state current of a nano-ampere (10^{-9}) range and an on-state resistance of a mega-ohm (10^6) range which corresponds to an on-state current of micro-ampere (10^{-6}) range.

[0083] The program, erase, and read operations described above are performed by applying appropriate voltages to word lines, bit lines, select lines, and source lines according to an operation to be performed. Below is an operation table showing the voltages applied to the word lines, bit lines, select lines, and source lines with respect to the operation to be performed according to embodiments of the present invention.

Table 2

Operation		WL 1 (e.g., 710a) Selected	WL 2, 3 (e.g., 710b, 710c)	WLs in different WL groups (e.g., 712a-c, 714a-c)	Select line	Source line	BL Selected	BL Unselected
Program	Precharge	1.5V	1.5V	0V	3V (pulse)	1.5V	0V	0V
	Program cell 708a on 702b	3V	1.5V	0V	3V (pulse)	0V	0V	0V
	Inhibit cells on 702b	3V	1.5V	0V	0V	0V	0V	0V
Erase a bit		0V	1.5V	0V	4V (pulse)	3V	0V	0V
Erase a page		0V	0V	0V	4V (pulse)	3V	0V	0V
Read option 1 No precharge		0.5V to 1.5V	0.5V	0V	0V	0V	Sense Current	X
Read option 2 No precharge		0.5V to 1.5V	0.5V	0V	Vref~0.8V	0V	Sense Current	X
Read option 3	Precharge	0.5V	0.5V	0V	3V	0.5V	1V	X
	Read	0.5V to 1.5V	0.5V	0V	0V	0V	Sense Voltage drop	X

[0084] FIG 14 illustrates a bit line sensing operation according to an embodiment of the present invention. In this embodiment, the resistance state of the memory device is determined by sensing the time elapsed for a voltage of the bit line 718 to drop to a predetermined value V_p . A memory cell in a low resistance state would take a first time period, e.g., t_1 , for the voltage drop. On the other hand, a memory cell in a high resistance state would take a second time period, e.g., t_2 , that is longer than the first time period for the voltage drop. The high resistance state can also be determined if the voltage drop does not occur at or after the time period t_2 .

[0085] A number of embodiments have been described. It will be understood that various modifications may be made without departing from the spirit and scope of the present invention. For example, the memory units may be provided with two-terminal memory cells other than resistive memory cells, e.g., phase-change memory (PCRAM), magnetoresistive

random access memory (MRAM), and spin-transfer torque RAM (STT-RAM). The scope of the present invention should be defined using the appended claims.

WHAT IS CLAIMED IS:

1. A non-volatile memory device, comprising:
a word line extending along a first direction;
a bit line extending along a second direction; and
a memory unit having a read transistor coupled to the bit line, at least one two-terminal memory cell, and a select transistor, the two-terminal memory cell having a first end coupled to the word line and a second end coupled to a gate electrode of the read transistor.
2. The device of claim 1, wherein the second end of the two-terminal memory cell is coupled to a common node shared by a drain electrode of the select transistor and the gate electrode of the read transistor.
3. The device of claim 2, wherein the device has a plurality of word lines, and wherein the memory unit has a plurality of two-terminal memory cells, each two-terminal memory cell having a first end coupled to one of the word lines and a second end coupled to the common node.
4. The device of claim 3, further comprising:
a source line coupled to a source electrode of the select transistor; and
a select line coupled to a gate electrode of the select transistor.
5. The device of claim 4, further comprising:
a plurality of word lines, the word line being one of the plurality of word lines, wherein the plurality of word lines have a first group of word lines, a second group of word lines, and a third group of word lines;
a plurality of memory units, the memory unit being one of the plurality of memory units, wherein the plurality of memory units have a first row of memory units, a second row of memory units, and a third row of memory units, and
wherein the first group of word lines is associated with the first row of memory units, the second group of word lines is associated with the second row of memory units, and the third group of word lines is associated with the third row of memory units.
6. The device of claim 5, wherein each memory unit includes a plurality of two-terminal memory cells, each memory cell in each memory unit having one end connected to one of the word lines and the other end connected to the common node.

7. The device of claim 6, wherein the two-terminal memory cells in each memory unit are configured to be accessed independently from other two-terminal memory cells in the same memory unit.

8. The device of claim 7, wherein each two-terminal memory cell includes a top electrode, a switching medium, and a bottom electrode, wherein the top electrode includes silver, the switching medium includes amorphous silicon, and the bottom electrode includes polysilicon.

9. The device of claim 8, wherein the two-terminal memory cell is a resistive memory cell configured to have a high resistance state and a low resistance state.

10. The device of claim 1, wherein the two-terminal memory cell includes one selected from the group consisting of: a resistive memory cell, a phase-change memory (PCRAM) cell, a magnetoresistive random access memory (MRAM) cell, and a spin-transfer torque RAM (STT-RAM) cell.

11. The device of claim 1, further comprising:
a source line coupled to a source electrode of the select transistor; and
a select line coupled to a gate electrode of the select transistor,
wherein the second end of the two-terminal memory cell is coupled to a common node shared by a drain electrode of the select transistor and the gate electrode of the read transistor,

wherein the device has a plurality of word lines, and wherein the memory unit has a plurality of two-terminal memory cells, each two-terminal memory cell having a first end coupled to one of the word lines and a second end coupled to the common node, and

wherein each two-terminal memory cell includes a switching medium provided between the first and second ends, wherein the first end includes silver, the switching medium includes amorphous silicon, and the second end includes poly silicon.

12. A non-volatile memory device, comprising:
a plurality of memory units arranged in an array of rows and columns, the each memory unit having a plurality of resistive memory cells, each resistive memory cell having a first end and a second end;

a plurality of word lines extending along a first direction and having a first group of word lines associated with a first row of memory units, a second group of word lines associated with a second row of memory units, and a third group of word lines associated with a third row of memory units;

a plurality of bit lines extending along a second direction and having a first bit line associated with a first column of memory units, a second bit line associated with a second column of memory units, and a third bit line associated with a third column of memory units;

a plurality of read transistors, each read transistor being associated with one of the memory units and having a drain electrode coupled to one of the bit lines;

a plurality of select transistors, each select transistor being associated with one of the memory units;

a plurality of select lines having a first select line coupled to gate electrodes of the select transistors associated with the first column of memory units, a second select line coupled to gate electrodes of the select transistors associated the second column of memory units, and a third select line coupled to gate electrodes of the select transistors associated with the third column of memory units;

a plurality of source lines having a first source line coupled to source electrodes of select transistors associated with the first row of memory units, a second source line coupled to source electrodes of select transistors associated with the second row of memory units, and a third source line coupled to source electrodes of select transistors associated with the third row of memory units; and

wherein the first terminals of the resistive memory cells are coupled to the corresponding word lines and the second terminals of the resistive memory cells are coupled to corresponding common nodes, each common node being shared by the drain electrode of one of the select transistor and the gate electrode of the corresponding read transistor.

13. The device of claim 12, wherein each memory unit includes at least eight resistive memory cells.

14. The device of claim 12, wherein each of the resistive memory cells is configured to have at least a high resistance state and a low resistance state.

15. The device of claim 12, wherein the first group of word lines, the second group word lines, and the third group of word lines each has the same number of word lines as the number of resistive memory cells in each memory unit.

16. The device of claim 12, wherein the source lines extend along the first direction, and the select lines extend along the second direction.

17. The device of claim 16, wherein each memory unit is provided within a space defined by a corresponding group of word lines, a corresponding source line, a corresponding select line, and a corresponding bit line.

18. The device of claim 16, wherein the resistive memory cells in each memory unit are configured to be accessed independently from other resistive memory cells in the same memory unit.

19. The device of claim 18, wherein each resistive memory cell includes a switching medium provided between the first and second terminals, and
wherein the first terminal includes silver, the switching medium includes amorphous silicon, and the second terminal includes polysilicon.

20. A memory unit of a memory device, the memory unit comprising:
a plurality of resistive memory cells;
a select transistor having a drain electrode coupled to a common node, a gate electrode coupled to a select line, and a source electrode coupled to a source line;
a read transistor having a drain electrode coupled to a bit line and a gate electrode coupled to the common node, and
wherein each resistive memory cell has a first end coupled to a word line and a second end coupled to the common node, and a switching medium provided between the first and second ends.

21. The memory unit of claim 20, wherein each resistive memory cell is configured to be accessed independently from other resistive memory cells of the memory unit.

22. The memory unit of claim 21, wherein the memory unit is provided as part of an array of memory units arranged in rows and columns in the memory device.

23. The memory unit of claim 22, wherein the first terminal includes silver, the switching medium includes amorphous silicon, and the second terminal includes poly silicon.

24. A method for operating a memory device, the method comprising:
providing a memory unit having
a plurality of resistive memory cells,
a select transistor having a drain electrode coupled
to a common node, a gate electrode coupled to a select line, and a
source electrode coupled to a source line,
a read transistor having a drain electrode coupled to
a bit line and a gate electrode coupled to the common node,
wherein each resistive memory cell has a first end coupled to a
word line and a second end coupled to the common node, and
a switching medium provided between the first and
second ends;
selecting at least one resistive memory cell from the plurality of the resistive
memory cells; and
applying a first potential to the word line associated with the selected memory
cell with respect to the common node.

25. The method of claim 24, wherein the first potential is a positive
potential.

26. The method of claim 25, wherein the first potential corresponds to a
program voltage that is sufficient to change a resistive state of the selected memory cell.

27. The method of claim 26, further comprising:
applying the program voltage to the word line associated with the selected
memory cell; and
applying a select voltage to the gate electrode of the select transistor to turn on
the select transistor.

28. The method of claim 27, wherein the programming voltage is provided
in a form of one or more voltage pulses.

29. The method of claim 27, wherein the first potential is no more than 3 volts.

30. The method of claim 27, further comprising:
applying a first precharge voltage to a plurality of word lines associated with the memory units, the plurality of word lines including the word line associated with the selected memory cell;
applying the select voltage to the gate electrode of the select transistor; and
applying a second precharge voltage to the source line.

31. The method of claim 30, wherein the first precharge and the second precharge voltages are about 1.5 volt.

32. The method of claim 30, further comprising:
lowering a potential of the source line with respect to the ground to a second potential by stop applying the second precharge to the source line during a program operation; and
increasing a potential of the word line associated with the selected memory cell with respect to the common node to a third potential during the program operation.

33. The method of claim 32, wherein the second potential is no more than 1.5 volt, and the third potential is about 3 volts.

34. The method of claim 33, wherein the first potential is substantially the same as the third potential.

35. The method of claim 24, wherein the first potential corresponds to a read voltage sufficient to cause electrical current to flow through the selected resistive memory cell if the selected resistive memory cell is in a low resistive state, the read voltage not being sufficient to change a resistive state of the selected memory cell.

36. The method of claim 35, wherein the electrical current flowing through the select resistive memory cell increases a voltage being applied to the gate electrode of the read transistor, thereby turning on the read transistor and causing electrical current to flow through the read transistor.

37. The method of claim 36, the selected resistive memory cell is determined to be in a programmed state or an erased state according to a potential drop of the bit line coupled to the read transistor.

38. The method of claim 35, wherein the read voltage is no more than 1.5 volt.

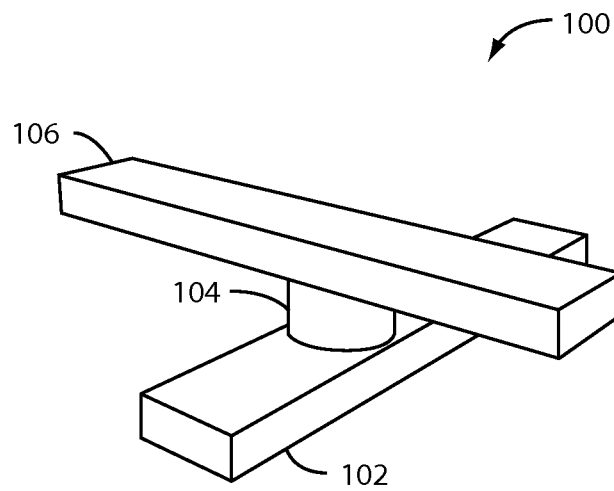
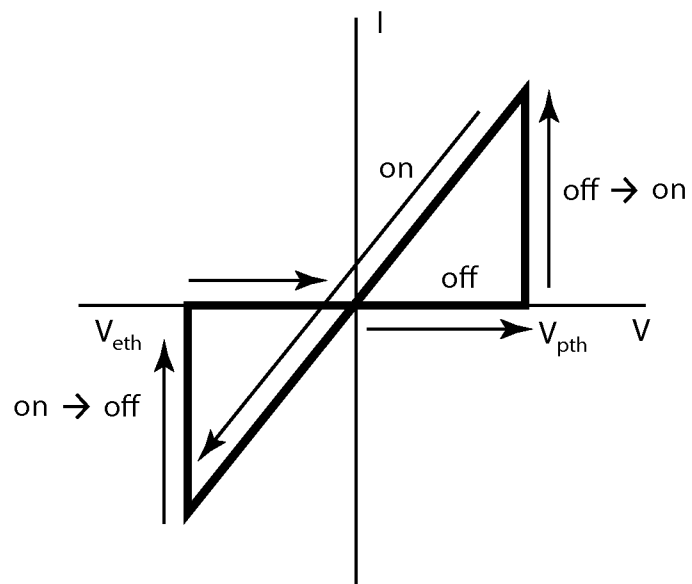
39. The method of claim 24, wherein the first potential is a negative potential.

40. The method of claim 39, further comprising:
applying an erase voltage to the source line;
applying about 0 volt to the word line associated with the selected memory cell; and
applying a select voltage to the gate electrode of the select transistor to turn on the select transistor.

41. The method of claim 40, wherein about 0 volt is applied to a plurality of word lines associated with the memory units so that all the resistive memory cells in the memory unit are erased together, the plurality of word lines including the word line associated with the selected memory cell.

42. The method of claim 40, wherein an inhibit voltage is applied to a plurality of word lines associated with the memory units so that only the selected memory cell is erased in the memory unit, the plurality of word lines including the word line associated with the selected memory cell.

43. The method of claim 40, wherein the erase voltage is applied in a form of one or more voltage pulses.

**FIG. 1****FIG. 2A**

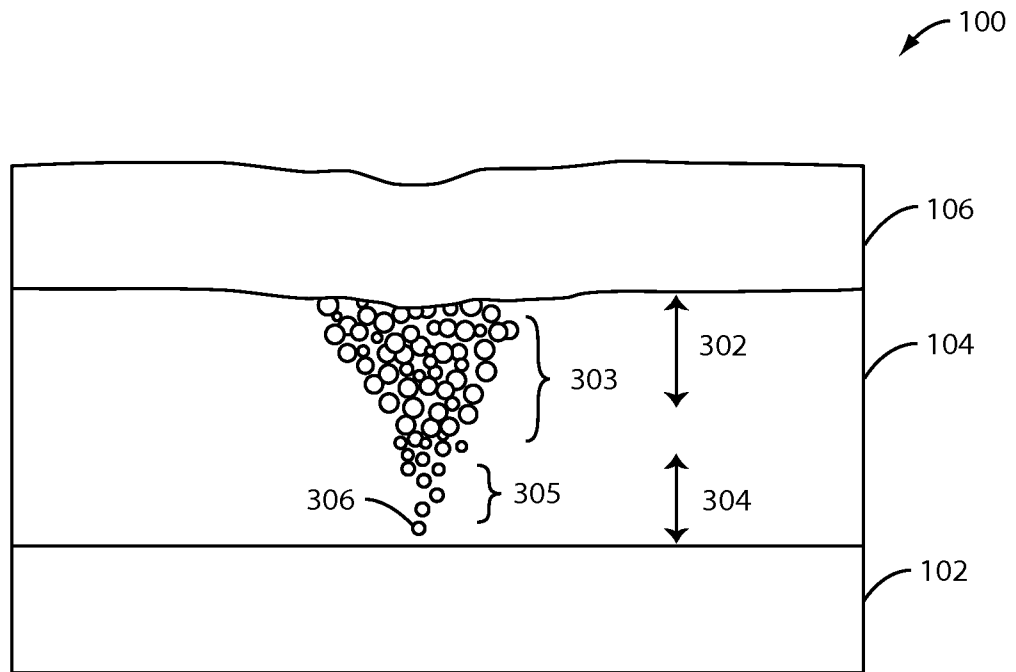


FIG. 3A

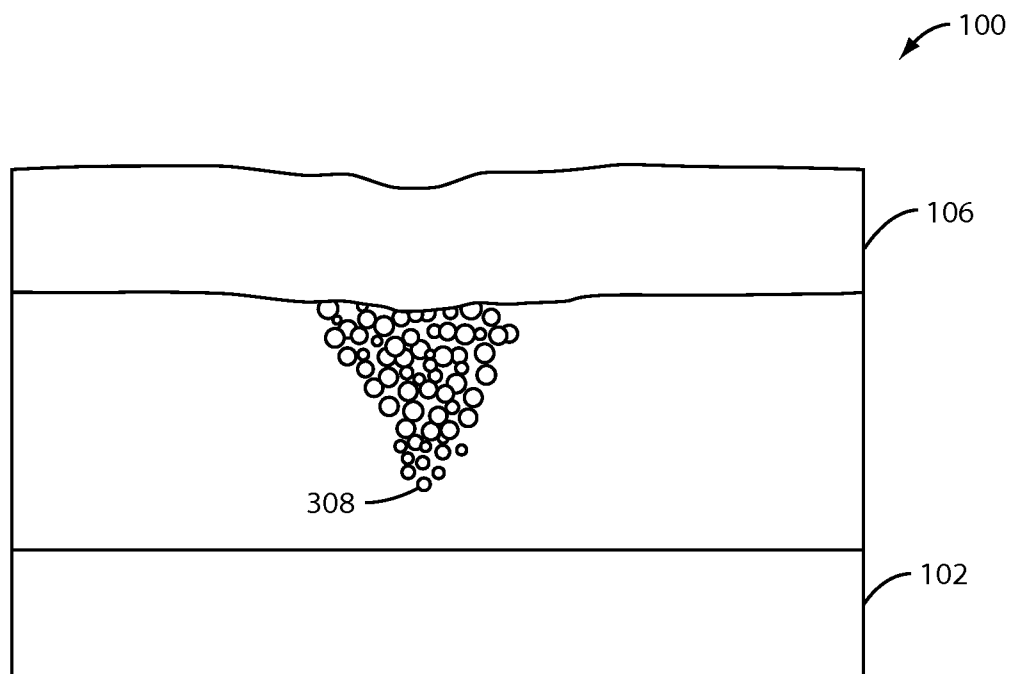
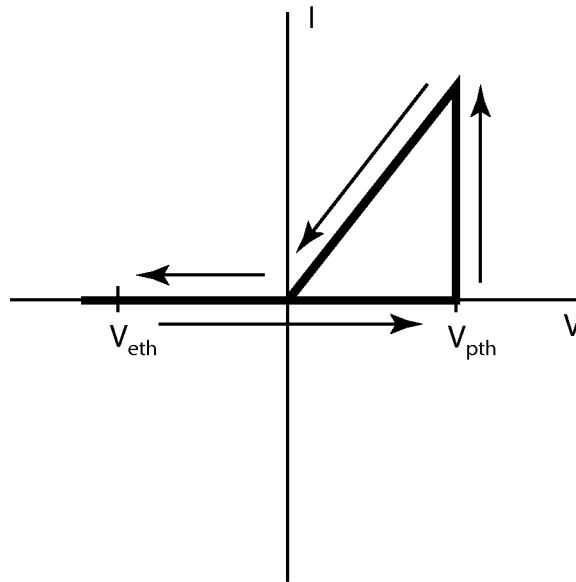
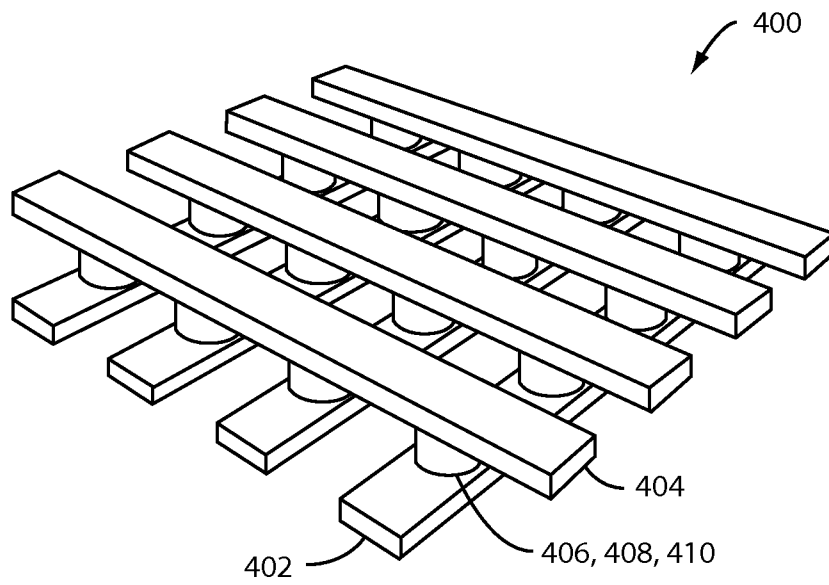
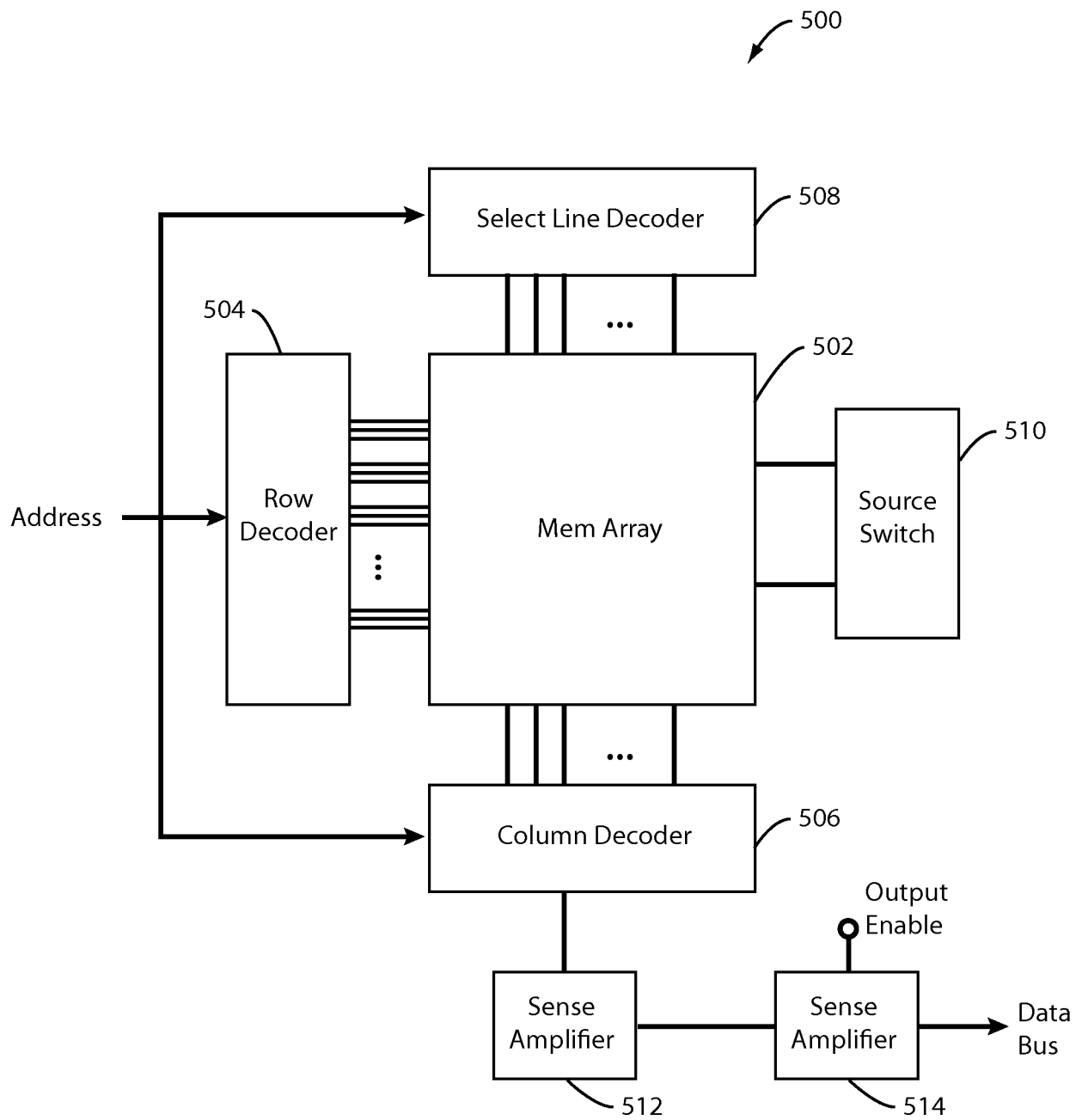


FIG. 3B

**FIG. 2B****FIG. 4**

**FIG. 5**

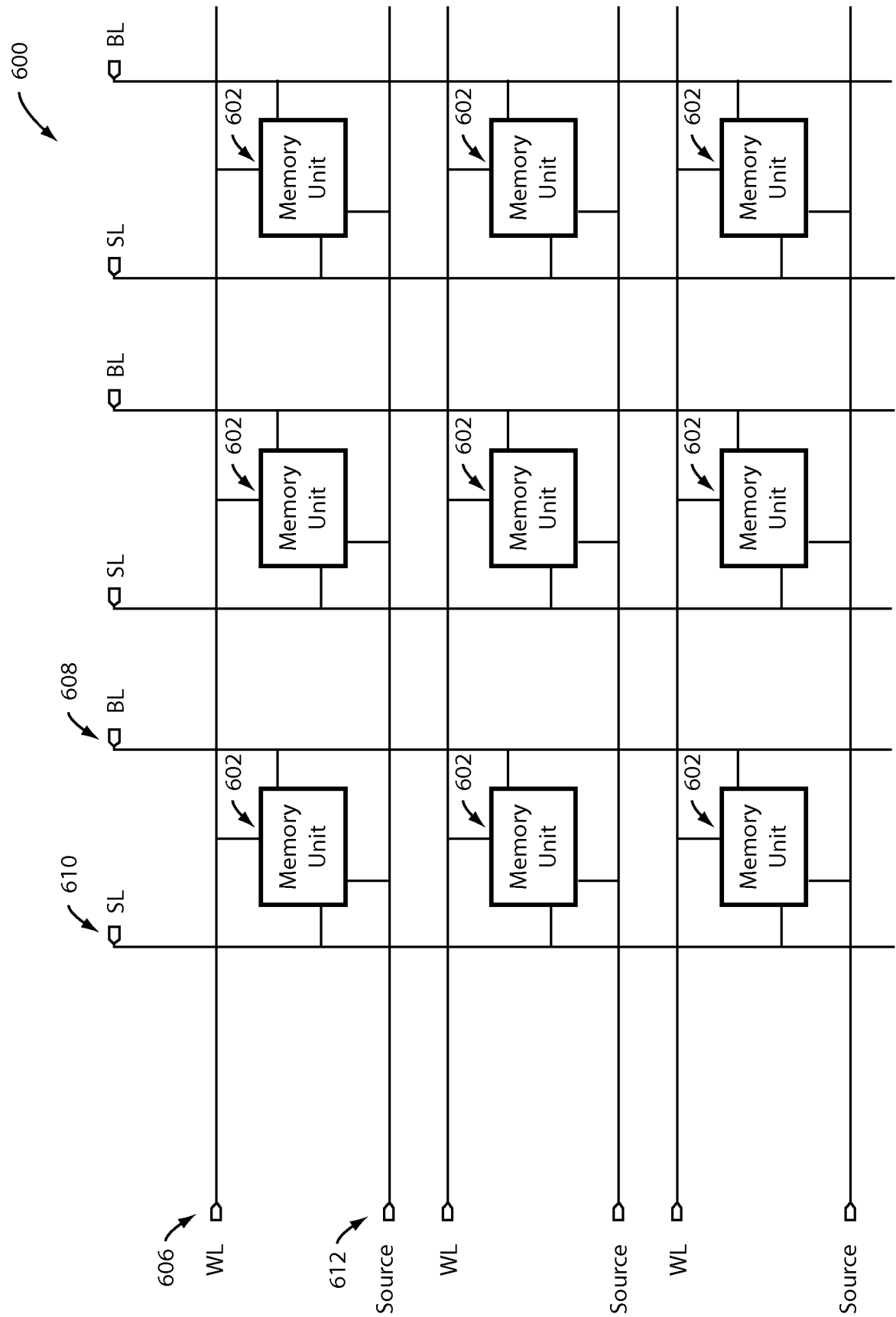


FIG. 6

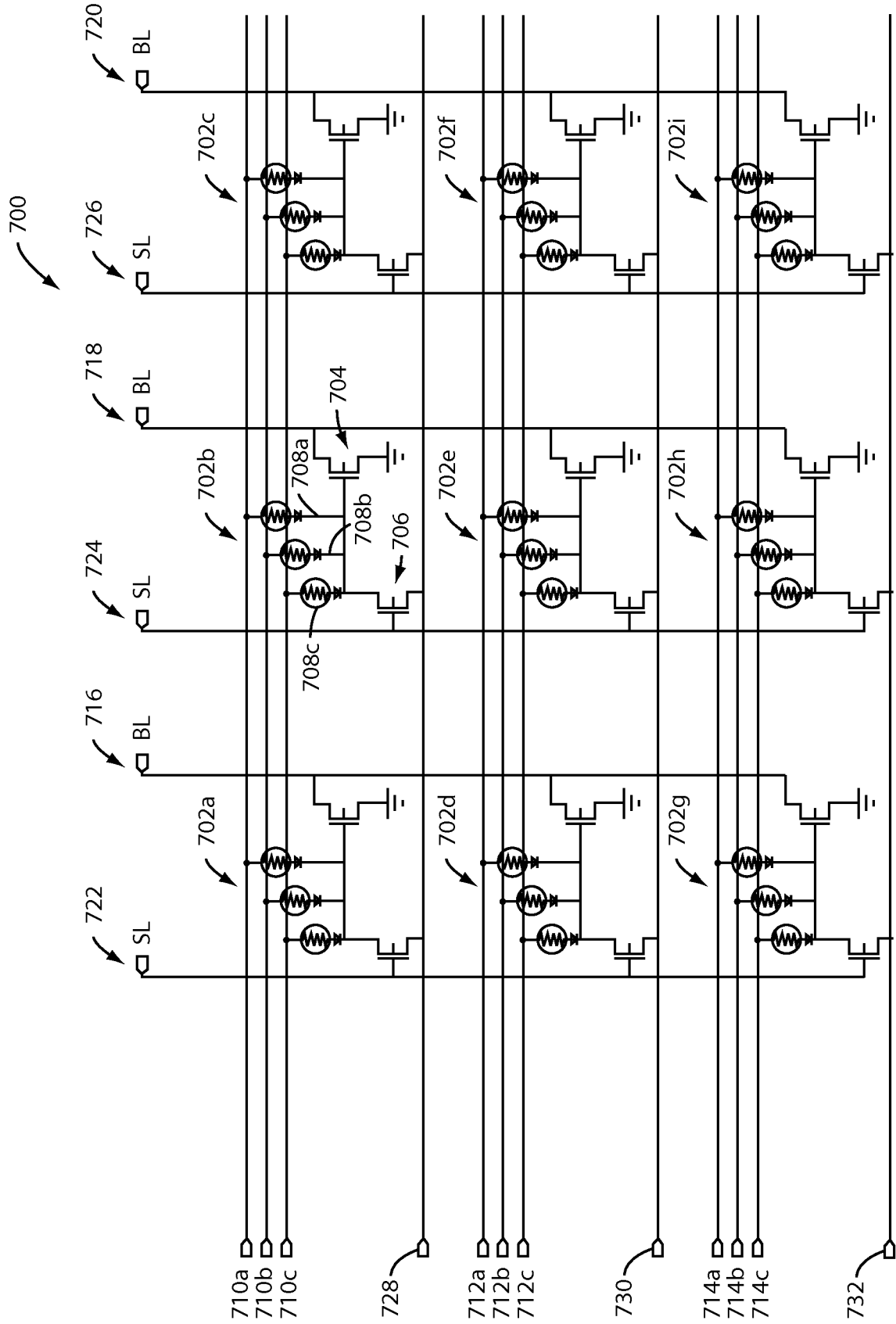


FIG. 7

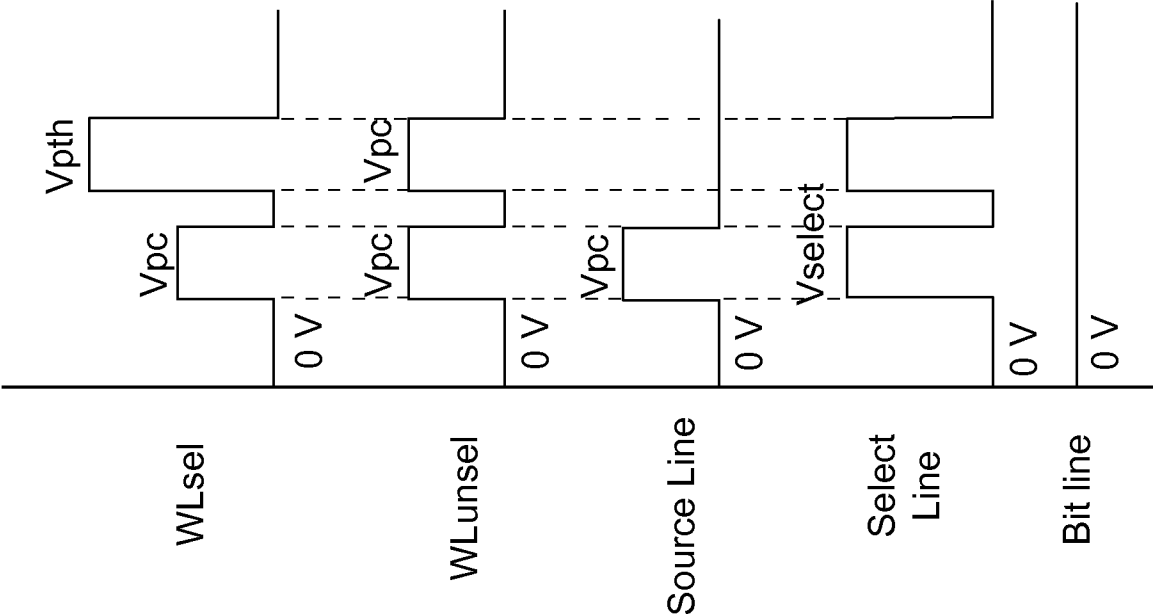


FIG. 8

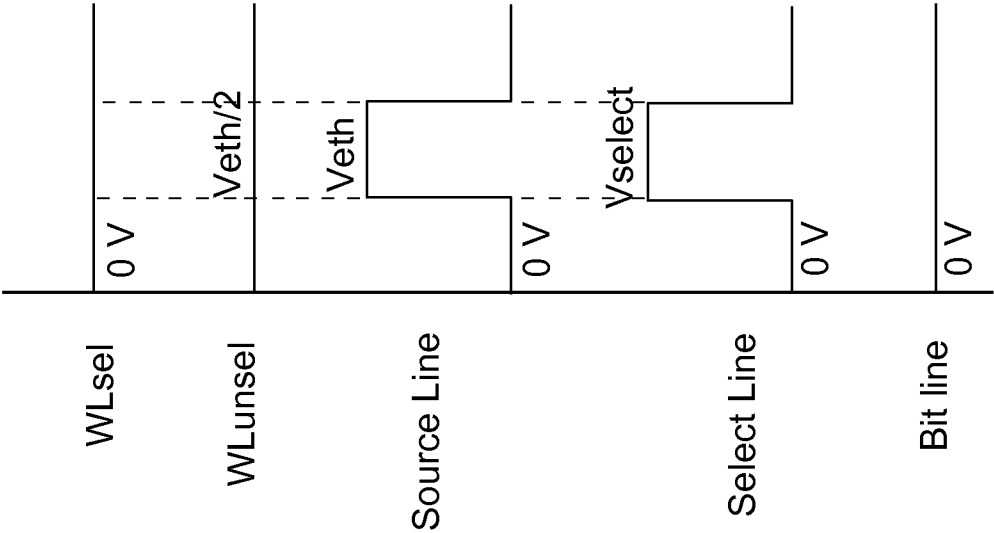


FIG. 9

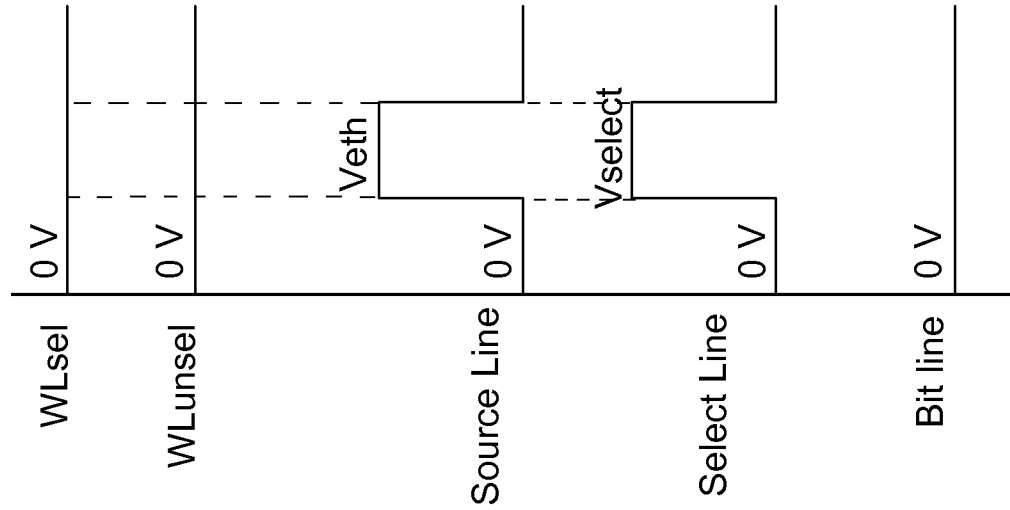


FIG. 10

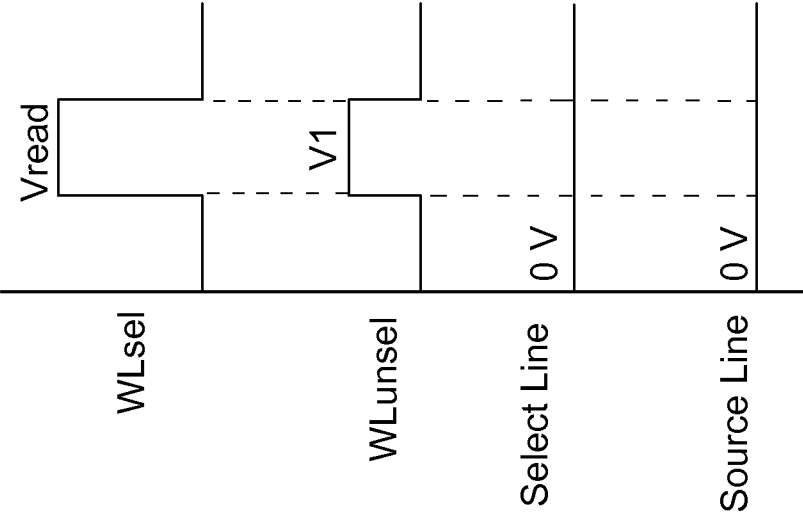


FIG. 11

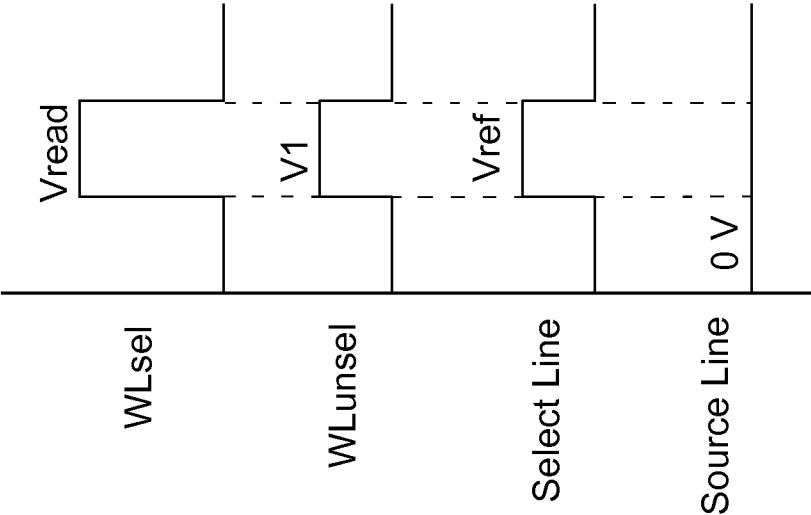


FIG. 12

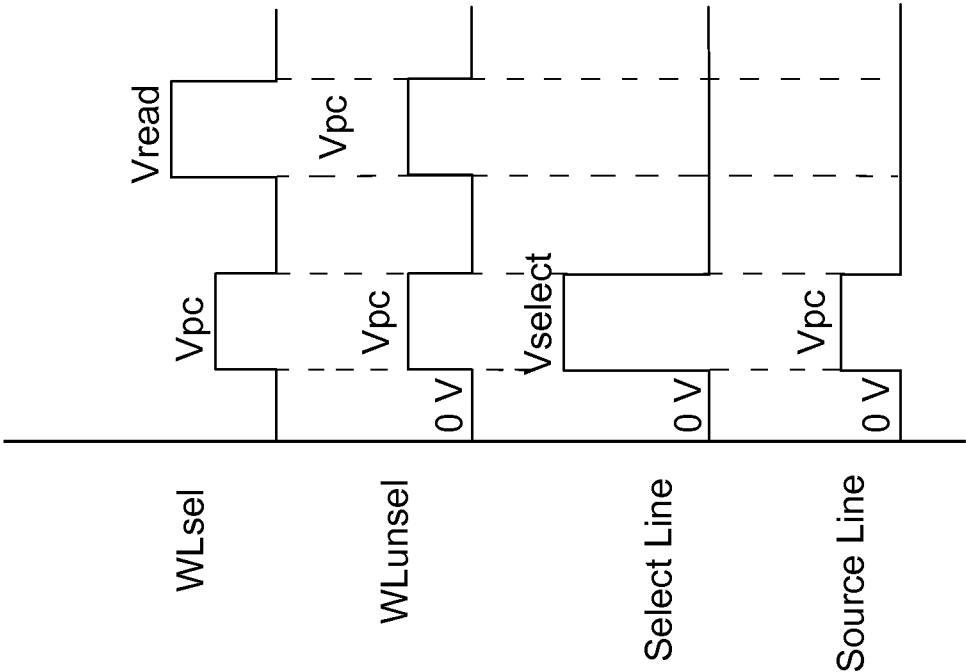
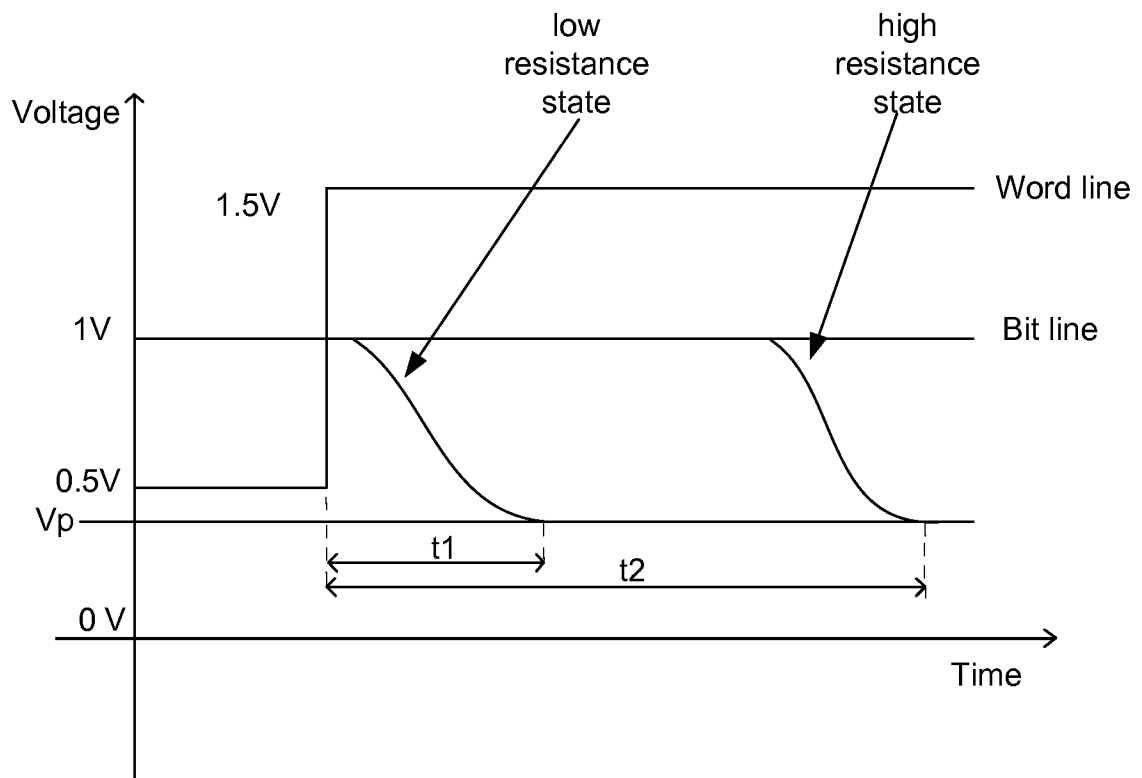


FIG. 13

**FIG. 14**