

[54] COIN OPERATED TELEPHONE SET
EMPLOYING ELECTRONIC TOTALIZER

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abandoned.

[52] U.S. Cl. 235/92 CN, 179/6.3 R, 235/92 R,
235/92 TE

[51] Int. Cl. G06m 3/10

[58] Field of Search 235/92 TE, 92 CN;
179/6.3 R

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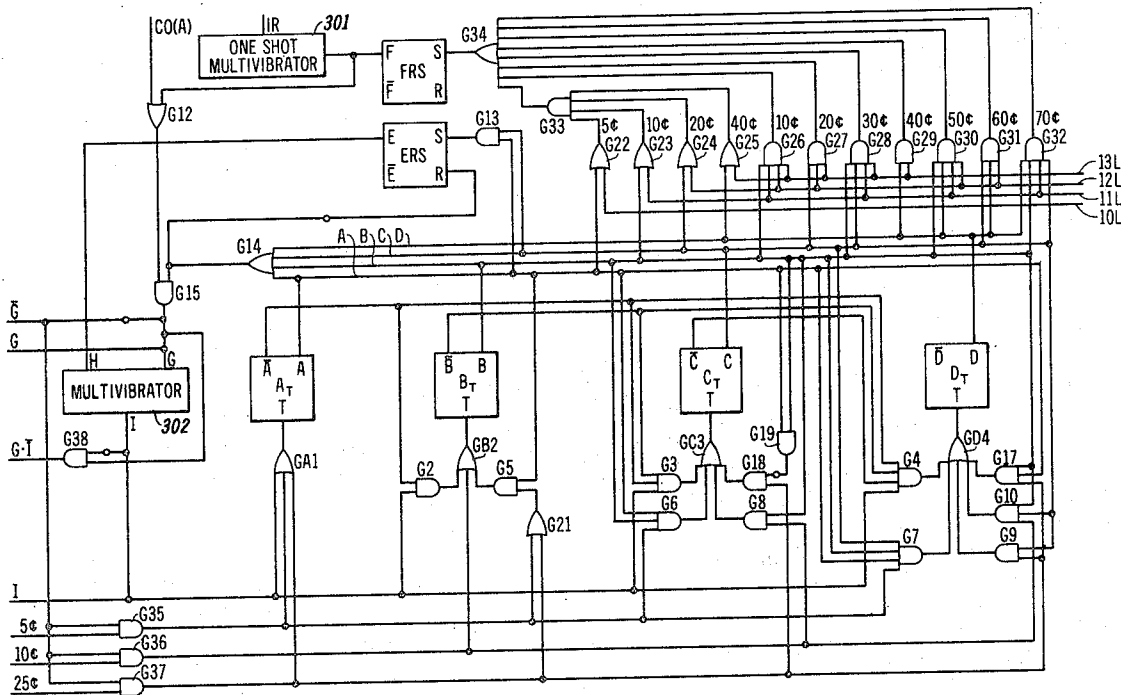
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[57] ABSTRACT

An electronic totalizer for coin operated apparatus combines a plurality of flip-flop logic stages into a ripple counter arrangement that is gated to count-up on coin deposits and to count-down when the coin deposit signal is generated. A variable speed multivibrator controls the coin deposit signals. In a coin telephone embodiment the totalizer is employed in combination with a signal oscillator and additional logic circuitry.

4 Claims, 14 Drawing Figures



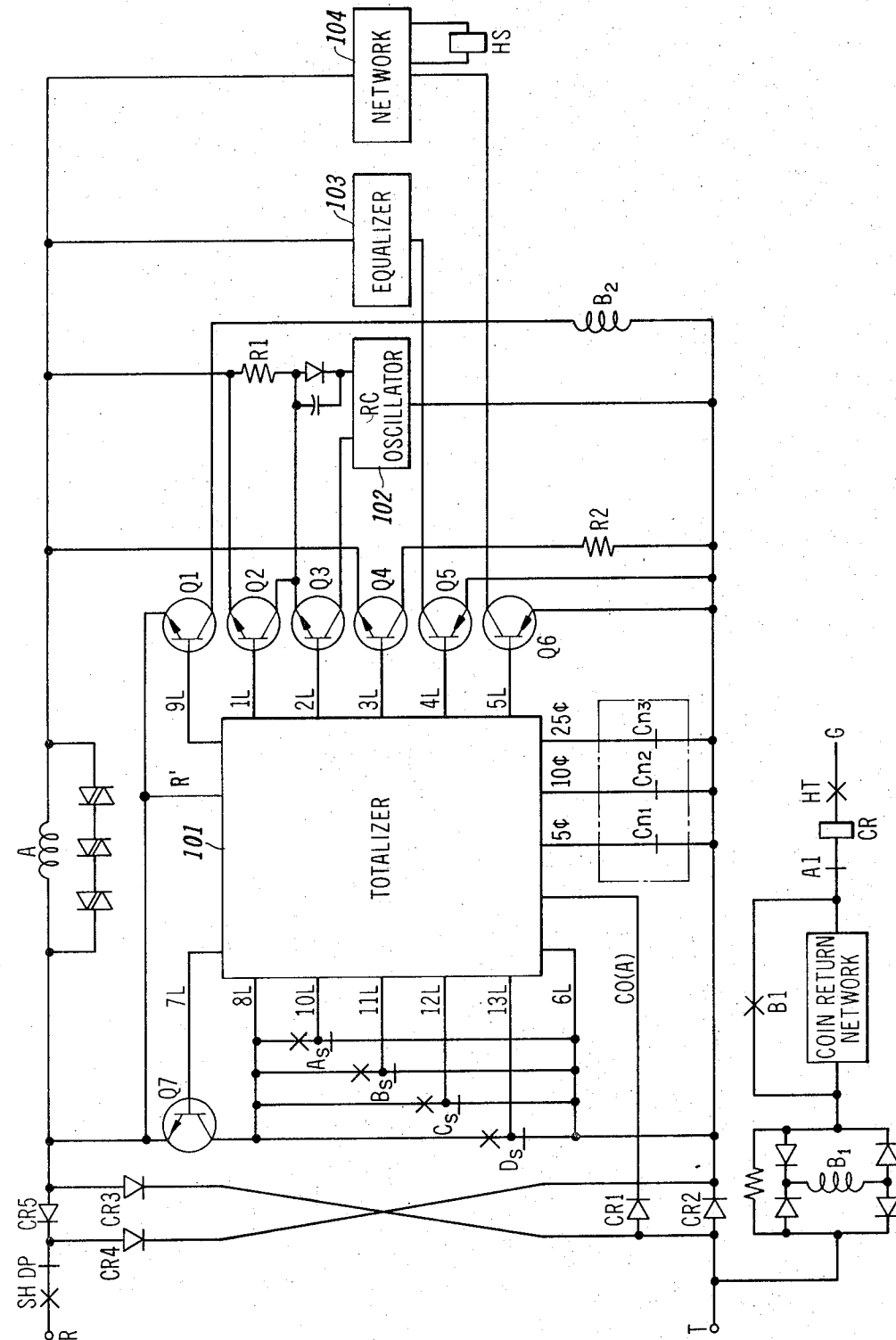
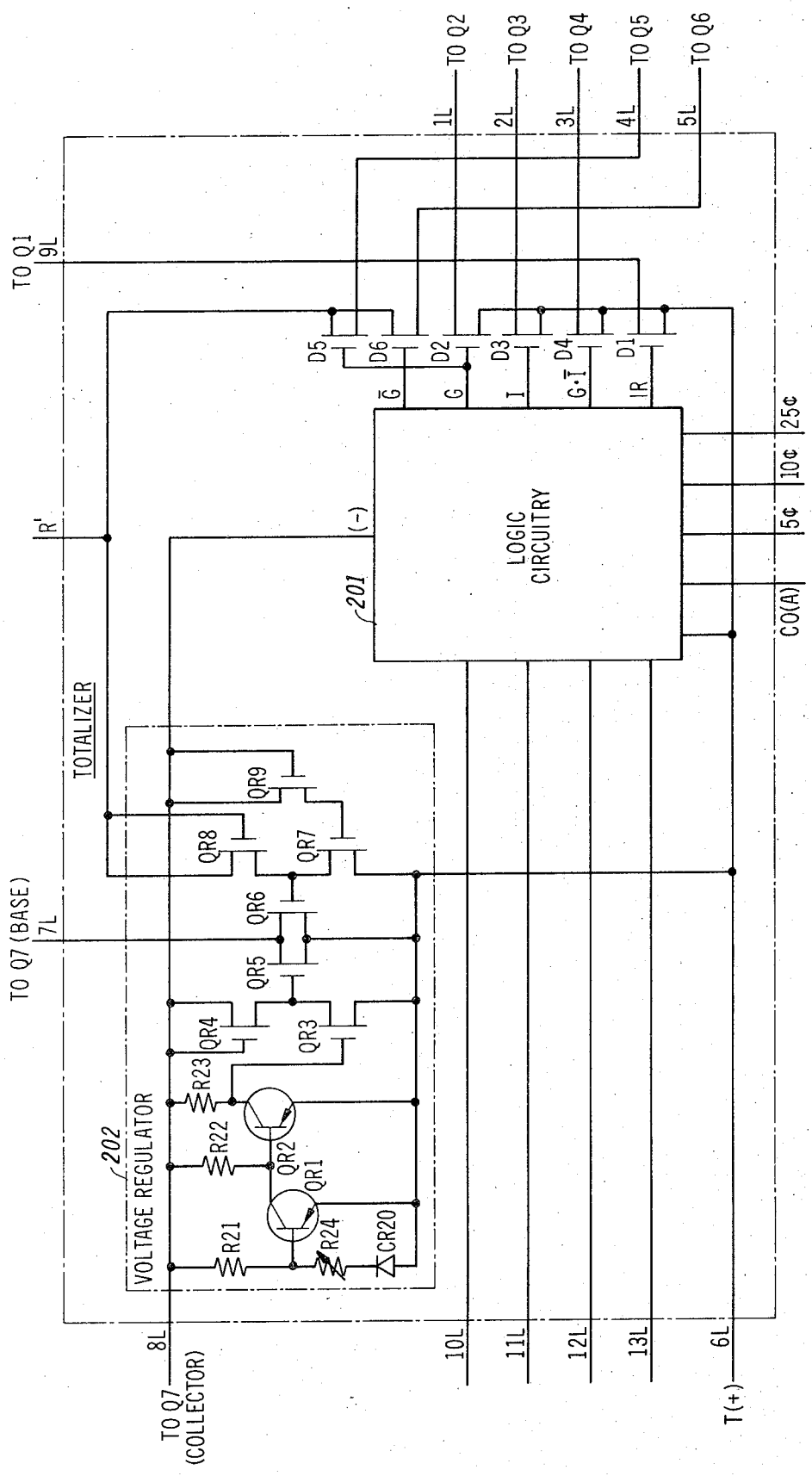
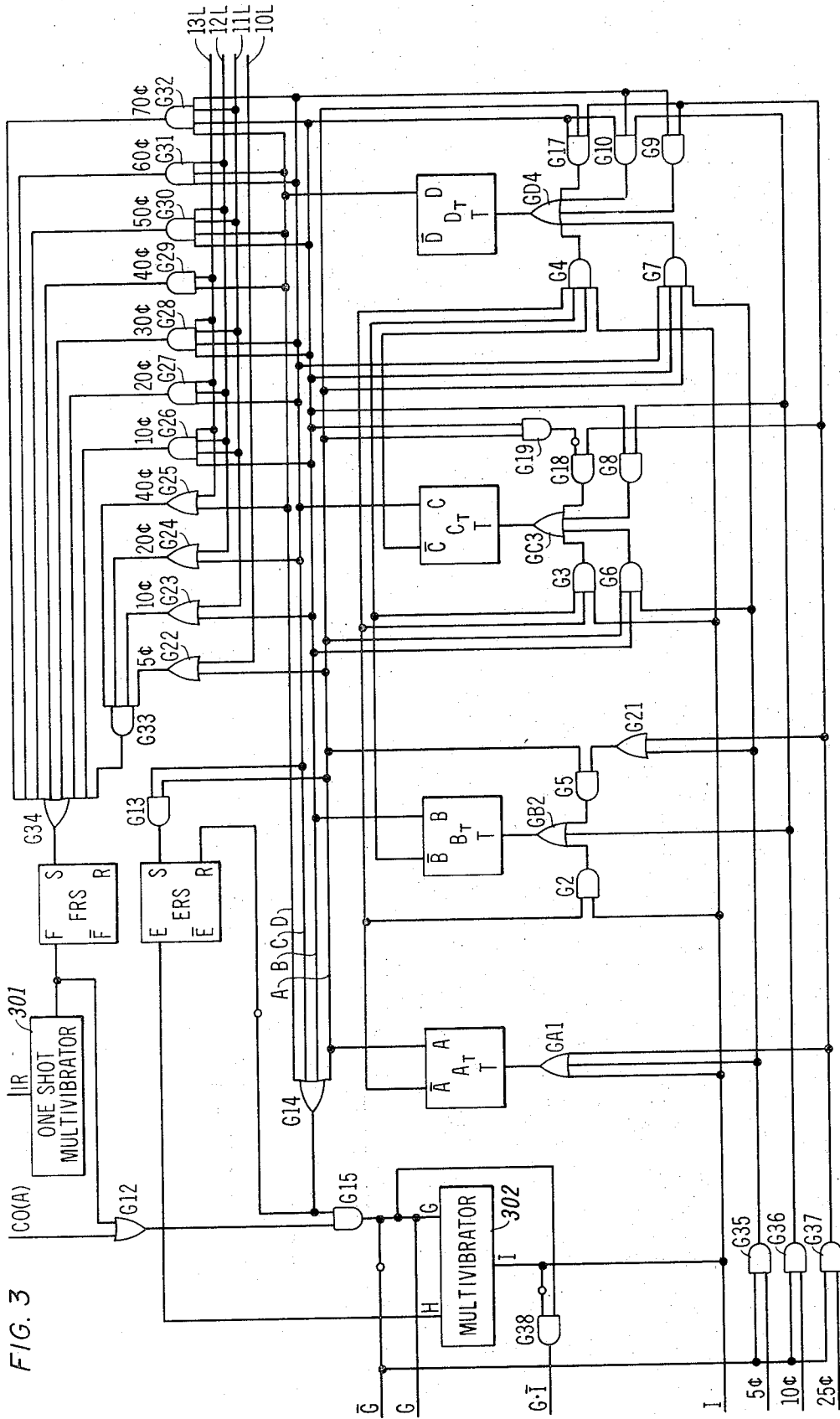


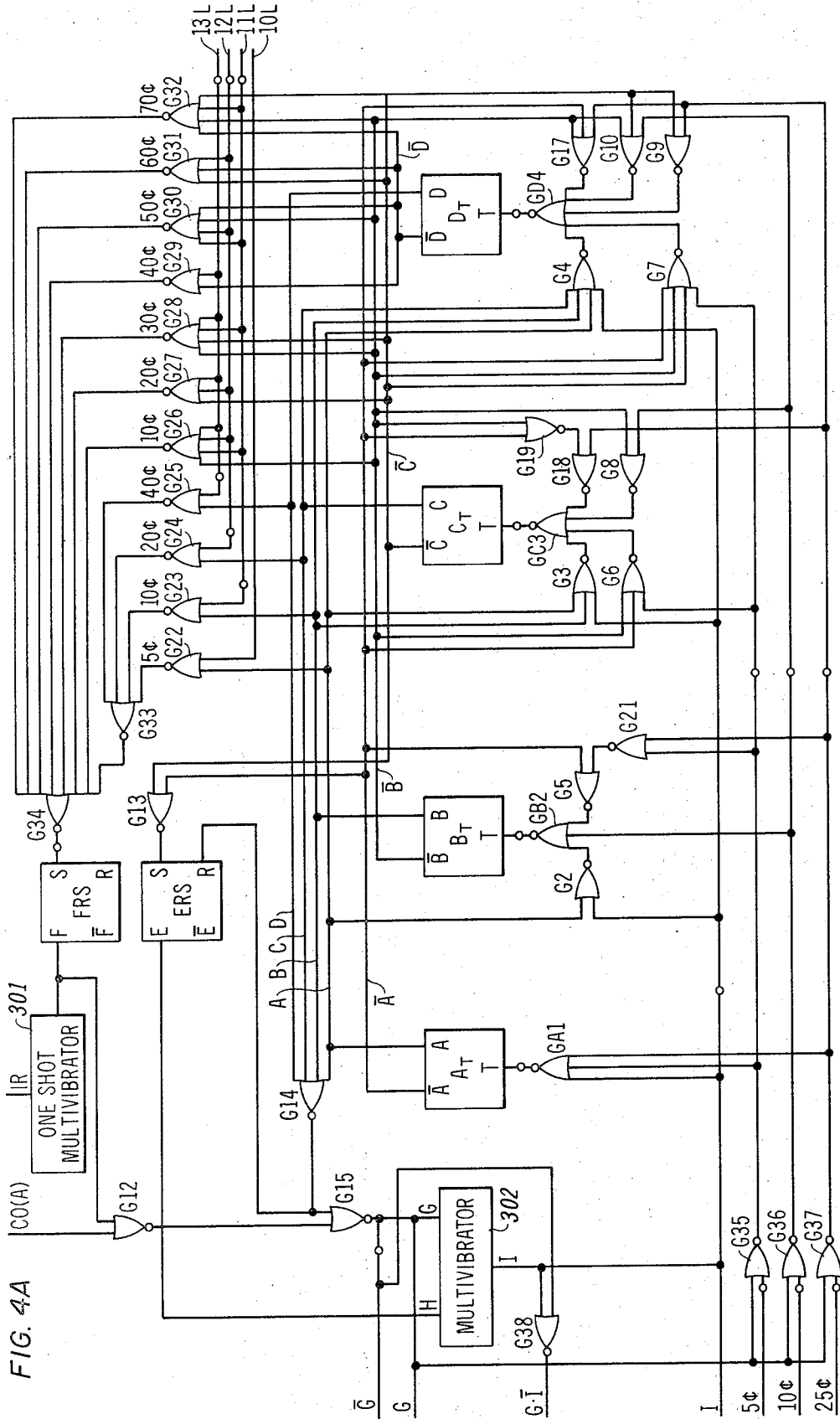
FIG. 1

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ATTORNEY

FIG. 2







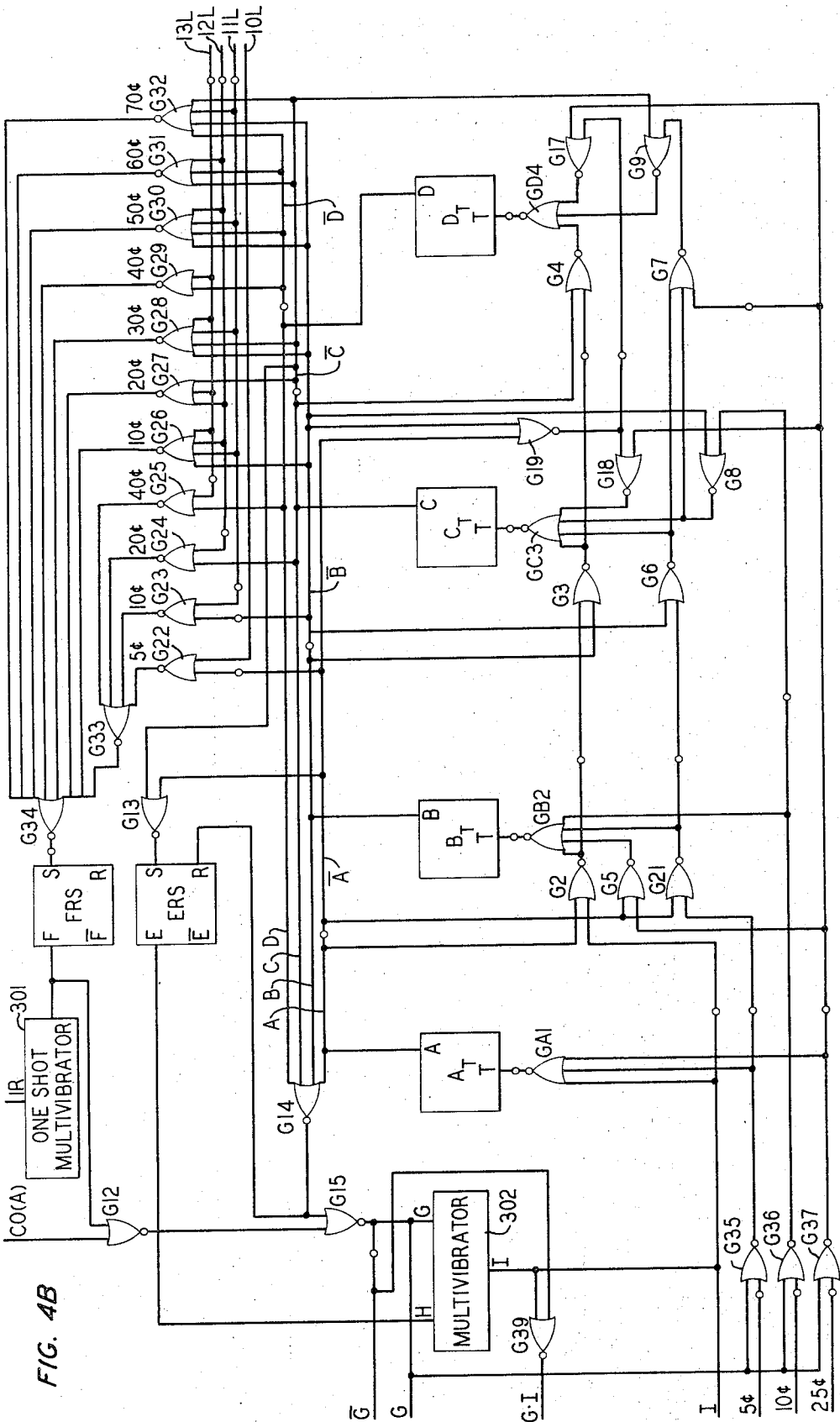


FIG. 5A

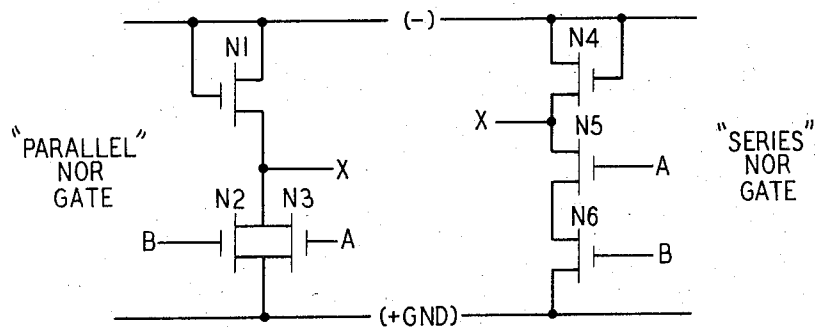


FIG. 5B

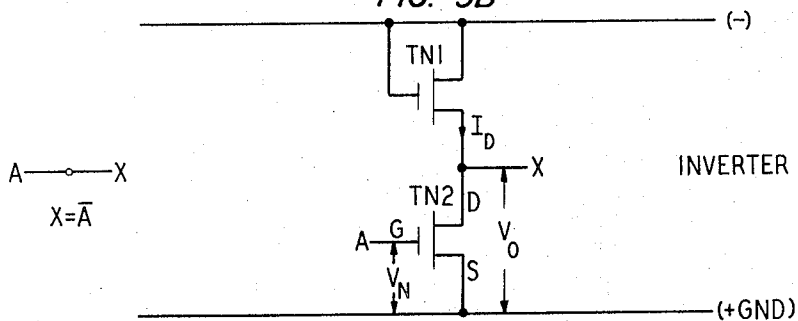


FIG. 5C

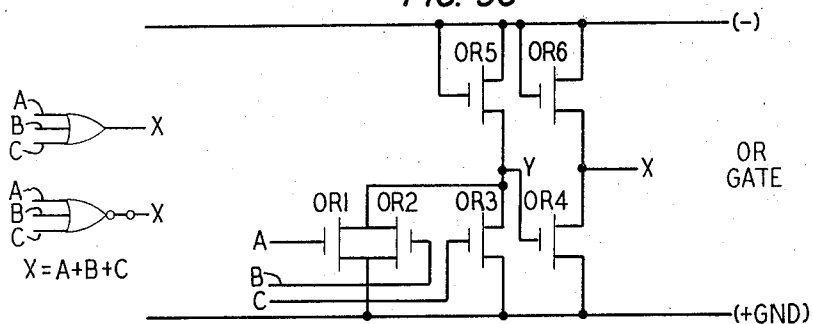


FIG. 5D

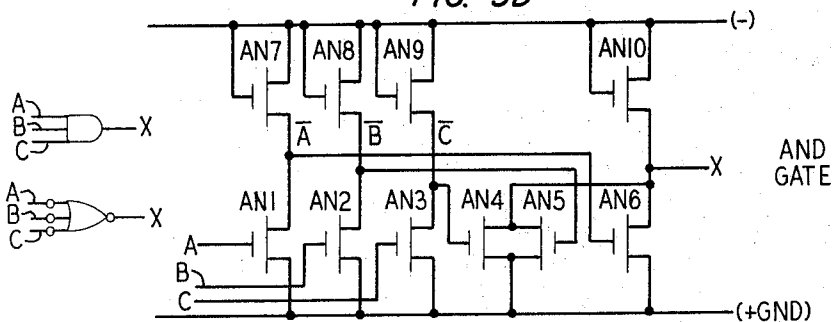


FIG. 6A

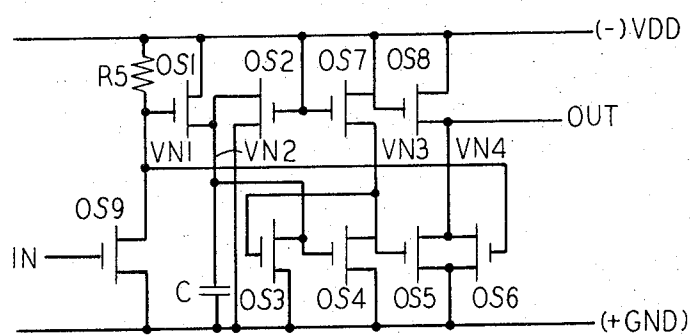


FIG. 6B

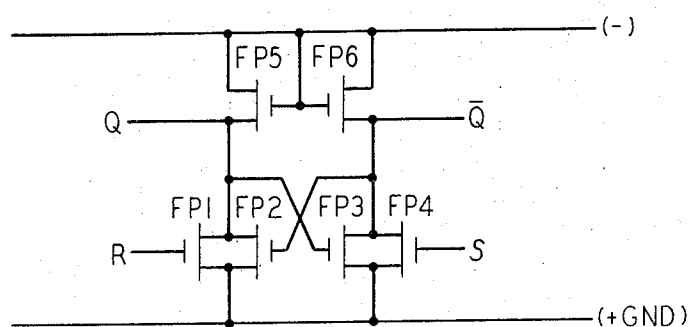


FIG. 7A

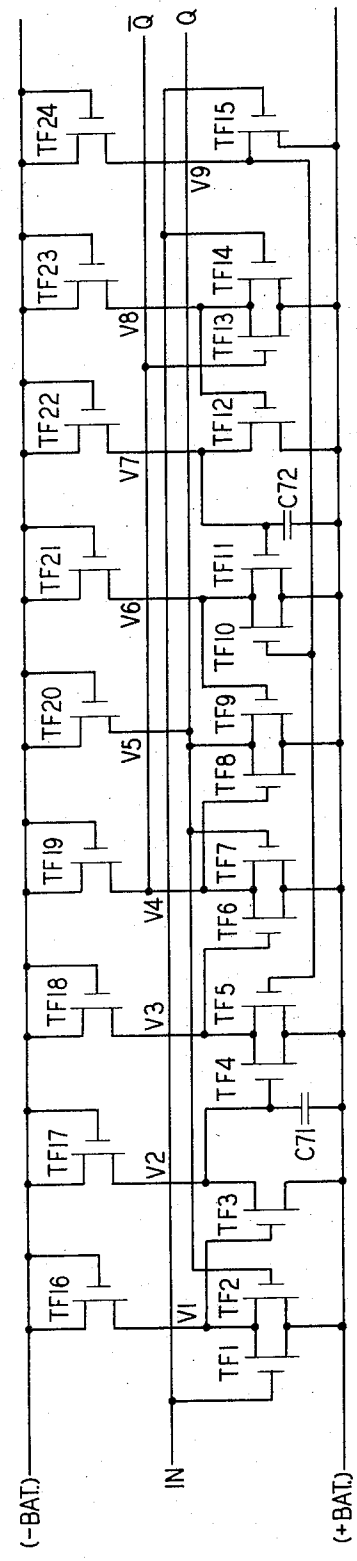


FIG. 7B

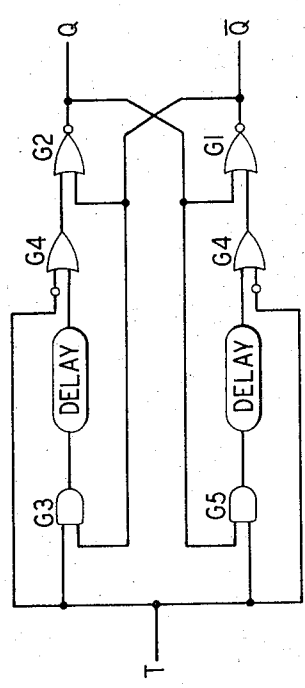
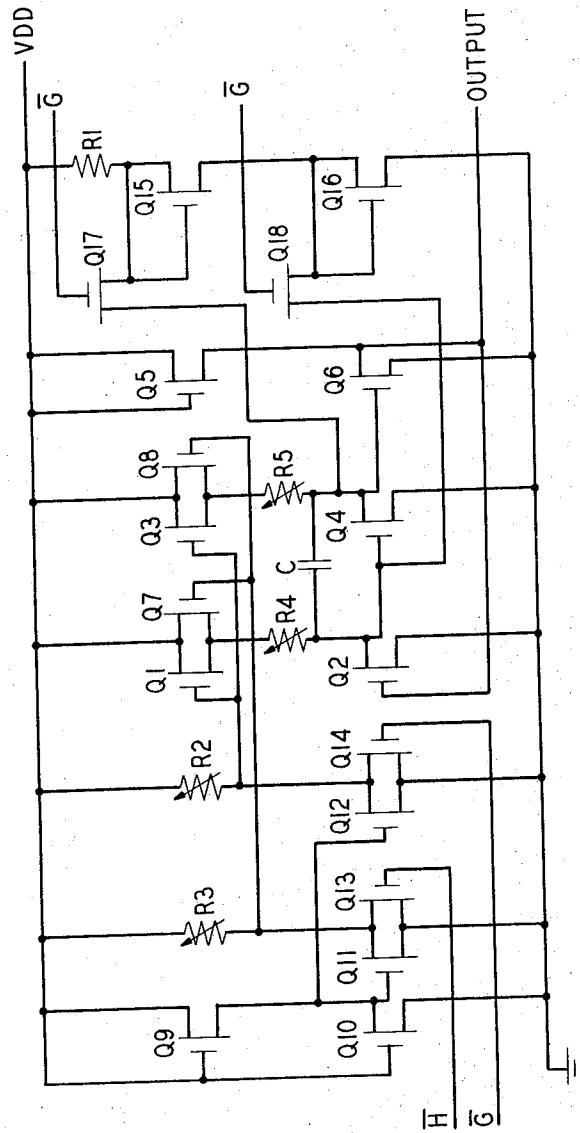


FIG. 8



COIN OPERATED TELEPHONE SET EMPLOYING ELECTRONIC TOTALIZER

This is a continuation, of application Ser. No. 101,607 filed Dec. 28, 1970 now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to totalizer arrangements for coin operated apparatus and particularly to totalizer arrangements adapted for use in coin operated telephone sets.

2. Description of the Prior Art

One conventional coin deposit totalizer that is widely used in pay telephone sets is described by E. R. Andregg and K. E. Voyles in U.S. Pat. No. 3,239,609, issued Mar. 8, 1966. Totalizing and storing the amount of the deposit is accomplished by mechanically rotating a shaft through a prescribed angular increment for each nickel equivalent deposited, power for the shaft rotation being derived from the gravity fall of the deposited coins as they strike protruding fingers attached to the shaft. Cams located on the shaft operate switches to provide the necessary switching logic. The operation of a pulsating electromechanical stepping arrangement moves the shaft incrementally back to its zero position and simultaneously activates an oscillator to generate coin deposit signals corresponding to the "read-out" stepping movement of the totalizer shaft.

The electromechanical operation of coin totalizer equipment in combination with the use of mechanical energy from the gravity fall of deposited coins has long been considered a narrowly restrictive arrangement insofar as possible improvements are concerned. For example, the possibility of adding more logic functions without sacrificing reliability is either very limited or nonexistent. Another example is the strict limitation on signaling flexibility imposed by destructive readout since the coin deposit information can be signaled only once for a deposit during the call sequence.

The general object of the invention is to improve and to simplify totalizers for coin operated apparatus, particularly coin operated telephones.

SUMMARY OF THE INVENTION

The foregoing object and additional objects are achieved in accordance with the principles of the invention by a totalizer that is entirely electronic rather than electromechanical both in its internal operation and in its control. The principles of the invention arise in part from a unique exploitation of solid-state and integrated circuit technology. For example, the low power drain, low supply voltage and high noise immunity of field effect transistors (FETs) have been utilized to simplify the heretofore unsolved problem of how to provide relatively extensive logic circuitry in a coin telephone environment. Also turned to account in accordance with the invention is the fact that dial-tone-first (DTF) telephone service has eliminated the requirement that a coin telephone totalizer must register and store coin deposits before loop current is present. DTF service is on a loop start basis, and the sequence of operation calls for the customer first to lift the handset, then to obtain dial tone, and then to deposit coins as required. As a result, it has been found possible to use loop current as the power source for the totalizer, providing that the power drain is kept sufficiently low to prevent undue loading of the circuit.

In accordance with one important aspect of the invention, coin deposit information is stored by a combination of IGFET flip-flop stages. Each of one group of these stages is a unique toggle flip-flop circuit that changes state when an input voltage changes from a relatively high level to a low level. In addition to the normal output, a conjugate output is used which enhances flexibility in the design of interface circuitry.

In accordance with another aspect of the invention, coin deposit signals are generated by an oscillator controlled by a free running multivibrator. The multivibrator turns on and off and changes signal pulse repetition rate upon the command of connecting logic circuitry.

A basic feature of the invention involves the use of logic circuitry to add (count-up) coin deposits and then to subtract (count-down) as the coin signal multivibrator generates coin pulses. The switching for up-counting and down-counting of the memory is provided by a series combination of simple logic gates.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a combination block and schematic circuit diagram of a coin telephone set employing a totalizer in accordance with the invention;

FIG. 2 is a combination block and schematic circuit diagram of the totalizer of FIG. 1;

FIG. 3 is a schematic circuit diagram of the logic circuitry shown in block form in FIG. 2;

FIG. 4A is a modification of the circuit shown in FIG. 3;

FIG. 4B is a modification of the circuit shown in FIG. 4A;

FIG. 5A is a schematic circuit diagram of parallel and series NOR gates in accordance with the invention;

FIG. 5B is a schematic circuit diagram of an invert circuit in accordance with the invention;

FIG. 5C is a schematic circuit diagram of an OR gate in accordance with the invention;

FIG. 5D is a schematic circuit diagram of an AND gate in accordance with the invention;

FIG. 6A is a schematic circuit diagram of the one shot multivibrator shown in block form in FIG. 3;

FIG. 6B is a schematic circuit diagram of an R-S flip-flop circuit shown in block form in FIG. 3;

FIG. 7A is a schematic circuit diagram of a toggle flip-flop circuit shown in block form in FIG. 3;

FIG. 7B is a diagram of the logic performed by the circuit of FIG. 7A; and

FIG. 8 is a schematic circuit diagram of the multivibrator circuit 302 shown in block form in FIG. 3.

DETAILED DESCRIPTION

As a preface to an examination of a specific embodiment of the invention, it will be useful to note those special functions and requirements that must be met by a coin telephone in a DTF system in addition to those met by a standard or home telephone set. In one way or another, the bulk of those functions and requirements involve the capabilities of the coin totalizer. First, coin deposit information must be stored until a preset initial rate has been deposited. The initial rate amount should be adjustable at the set for flexibility of operation. During the initial rate deposit period, a negative battery potential on the ring lead is provided by the central office. An indication to the central office that the initial rate has been deposited is achieved by the detection of a local ground (through the coin relay)

over the tip lead with the ring lead open. This capability requires that the circuit used to close local ground includes a latching device since the loop current is zero during the initial rate deposit ground test. It is necessary that coin deposit signals be generated as soon as the deposit is made when the operator is on the line. During the subsequent deposit period, positive battery potential is used on the ring side at the central office.

Coin collection and coin refund are controlled by the application of ± 115 volts to the tip lead at the central office. The ground at the station for initial rate and ground checking is removed during transmission and dialing in order to reduce the unbalanced noise on the line. Finally, all totalizing functions requiring electrical power must be accomplished using line power to ensure that services are available even in the absence of local power.

Coin Telephone Circuit Arrangement

In FIG. 1 a totalizer 101 in accordance with the invention is shown in block form together with an RC oscillator 102 in combination with an equalizer circuit 103 and a telephone speech network 104. Other major elements of a coin telephone set are also shown in order to ensure a complete disclosure of the source of the totalizer inputs and the utilization of the totalizer outputs as well as a complete disclosure of how the apparatus interacts in the environment of coin operated equipment — in this case, a coin operated telephone. The equalizer 103 and the speech network 104 may be of the type disclosed by J. E. Edington and M. L. Warnock in their U. S. patent application Ser. No. 774,376, filed on Nov. 8, 1968, now U.S. Pat. No. 3,579,253. The coin deposit signals which are transmitted to the central office (not shown) are generated by the RC oscillator 102, which may be of any suitable conventional type, similar for example to the twin-T notch oscillator employed in multifrequency tone generating telephone dials and described in U.S. Pat. No. 3,424,870, issued to R. L. Breeden and R. M. Rickert on Jan. 28, 1969. Power to the oscillator 102 is supplied by connecting it across the line by way of a conducting path 21, a transistor Q2 and a conducting path 23. A coin deposit tone is generated when bias voltage is applied by way of the lead 20-3.

The totalizer block 101 contains the logic which controls all of those coin telephone set functions that directly or indirectly involve coin deposits. Power from the line is supplied to the totalizer 101 on leads 6 and 8 and by way of a transistor Q7 with the current through that transistor being regulated by the output on lead 7. The totalizer block 101 also includes a voltage sensing circuit (not shown) which changes the output on lead 7 to regulate the power supplied to the various elements of the totalizer logic circuitry. The coin chute inputs to the totalizer 101 are the coin deposit leads indicated 5 cents, 10 cents and 25 cents, each corresponding to the deposited amount that produces an input on that lead. Inputs 10, 11, 12 and 13 are used to set the initial rate amount. The various combinations of the four switches A_s, B_s, C_s and D_s, either operated or nonoperated, change the initial rate in fixed 5 cents increments from 0 through 75 cents.

The CO(A) lead is used to indicate to the totalizer 101 that the loop battery is positive on the ring side R of the line which allows the totalizer to read out deposits immediately. When the ring lead R is negative, the

CO(A) lead is at the same potential as the tip lead but when the tip lead is negative, the diode CR1 is blocking and the CO(A) lead is not at the tip potential. The output leads 1 through 5 and 9 provide the following functions:

Lead 1 turns on transistor Q2 to connect the coin deposit oscillator 102 across the line.

Lead 2 turns on transistor Q3 to connect the bias supply to the coin deposit oscillator 102 when coin deposit tones are being generated.

Lead 3 turns on transistor Q4 to connect a resistor R2 across the line during the silent interval of coin deposit signaling in order to reduce the switching transients on the line.

Lead 4 turns on transistor Q5 to connect the equalizer 103 across the line during coin deposit signaling.

Lead 5 turns on transistor Q6 to connect the speech network 104 during conversation.

Lead 9 (after the initial rate has been deposited) pulses transistor Q1 on for a period of time long enough to operate a relay B (indicated by its windings B₁ and B₂ and by its contacts B1), which is the initial rate latching relay.

The local ground connection G, when applied, is made directly to the tip lead T so that the polarity guard comprising the diodes CR2, CR3, CR4 and CR5 can be inserted between the set components and the line. Since both positive and negative coin batteries are required, the tip-to-ground path cannot be through a diode of the polarity guard. The local ground G is "lifted" during conversation by the A relay through contact A1. Without this precaution, the local ground would induce unbalanced line noise, causing interference and distortion. The local ground path contains the circuit elements employed in the standard DTF circuit as shown, for example, in the copending application of J. E. Edington and M. L. Warnock, cited above. These elements include the hopper trigger contacts HT, the coin relay CR, the A relay contacts A1 and the coin return network CRN which is shunted by contacts B1 of the B relay. The winding B₁ of the B relay is in series with the local ground and its operation resets the latching initial rate mechanism (not shown) when coins are collected or refunded.

Circuit Operation (Correct Customer Procedure)

As a further aid to an understanding of a detailed description of the internal totalizer circuits, an explanation is presented at this point to clarify the steps involved in placing a call and the steps involved in the corresponding circuit operations in terms of the arrangement shown in FIG. 1. When the customer lifts the handset HS, switching contacts SH are closed to connect the set to the line. The ring-to-tip battery potential causes transistor Q7 to turn on supplying battery to the totalizer circuit 101, and transistor Q6 turns on connecting the speech network 104. The loop current causes a "start" at the central office and dial tone is connected and transmitted to the set. In addition, loop current operates the A relay to open the local ground path at the break contact A1. The dial pulse contacts DP are made operative and at that point, the customer is free to dial out the called number.

The central office talk battery is connected with the ring lead R negative causing the CO(A) lead to be at tip potential. A coin deposit results in a signal on the

5 cents, 10 cents or 25 cents input lead to the totalizer 101. The source for a coin deposit signal is illustrated schematically in FIG. 1 by mechanical switch transfer contacts c_{n1} , c_{n2} and c_{n3} . It is to be understood, however, that the signal may be produced by any suitable sensor arrangement such as the development of a voltage by arranging for a deposited gravity-dropping coin to strike a piezoelectric wafer. The totalizer then stores the coin deposit information until the preset initial rate amount is reached. When the amount deposited equals or exceeds the initial rate amount, a pulse is generated on the totalizer lead 9 which turns transistor Q1 on and operates the B relay through the winding B₂. The totalizer then reads out (returns to "0"), but the B relay remains operated. The details of the readout sequence are explained at a later point.

As soon as the customer has dialed enough digits to determine if the call is to be a "charge" call or coinless, the central office makes a local ground test if the call requires an initial rate deposit. This ground test is a -48 volt battery on the tip lead T with the ring lead R open and is current limited to prevent the resetting of the B relay and the operation of the coin relay CR. This battery arrangement does not cause current flow through the coin return network CRN so the only way current can flow is through the normally open B1 contact. Since this contact is closed, the initial rate deposit test is met and the call proceeds normally. A coin collect or a refund signal at the end of the call returns the B relay to normal. The coin return network CRN breaks over and becomes a low impedance to the ± 115 volts used for collector refund. This condition allows the return or collection of coins when the B1 contact is not operated.

A toll call is initiated in the same manner as described in the preceding sequence except that a coin deposit is not required to dial the operator. The talk battery is reversed during the time the operator is servicing the call to place a positive potential on the ring lead R. This polarity allows the CO(A) lead to the totalizer 101 to go negative with respect to the tip lead T and causes the totalizer to read out on each deposit as soon as the deposit is made. The readout sequence begins as soon as the totalizer has registered the deposit by the following conditions:

Transistor Q6 is turned off to disable the speech network 104.

Transistor Q5 is turned on to connect the coin deposit signal oscillator equalizer circuit 103.

Transistor Q2 is turned on to connect power to the coin deposit signal oscillator 102.

Transistor Q3 turns on to initiate a tone burst for the first "beep" signal indicating a deposit.

In accordance with a feature of the invention a multi-vibrator circuit in the totalizer controls the tone duration and repetition rate by alternately turning transistor Q3 off and on until the number of tones generated is equal to the nickel equivalent of the deposit. Transistor Q4 is turned on when transistor Q3 is off to connect resistor R2 across the line and maintain a constant load to the line. As soon as the totalizer read out to "0" the circuit reverts to the "talk" state in which transistor Q6 is on and in which transistors Q2, Q3, Q4 and Q5 are off. The collect or refund action at the termination of the call resets the B relay as in the local call sequence.

The central office option of automatic local overtime deposit detection proceeds in the same way as in a conventional DTF coin telephone. This procedure includes

a local ground test (with +48 volt tip to ground) to detect the presence of a 5 cents deposit. The coin return network CRN is a low impedance to the positive battery so that the local ground test result is determined by the state of the hopper trigger contacts HT which close on any deposit.

The memory in the totalizer unit 101, which is provided, as indicated above, by a combination of flip-flop stages requires power to carry out its storage function. Additionally, the memory unit must be set to "0" when the power is initially applied in order to ensure against a false indication that a deposit has been made. Also, in order to avoid the possibility of losing stored information, power must be supplied to the memory circuits during all interruptions in line current, including those caused by dial pulsing and central office switching. Furthermore, the memory state must be set to "0" on a call initiation or when line power is restored after a coin collection, after a coin refund, or after a ground test is made. In accordance with the invention, power is supplied in the circumstances indicated by storing a charge on a capacitor in the totalizer power supply of sufficient magnitude to bridge the dialing and central office switching interruptions, but of insufficient magnitude to bridge the long power interruptions that occur during coin disposal or tests. Each memory stage is so constructed that it automatically assumes a "0" state when power is supplied.

Circuit Operation (Incorrect Customer Procedures)

Although the general operation of the circuit shown in FIG. 1 is similar to that of the DTF coin telephone as disclosed by Edington and Warnock in the U. S. patent application cited above, some differences arise as a result of the substitution of the electronic totalizer of the invention for the conventional electromechanical unit. There are also differences in operation that occur whenever the set is used in a manner other than prescribed by normal or proper calling procedures. These situations may be identified as follows:

Call abandoned with the totalizer off "0"

This situation may occur if a customer hangs up after depositing an amount less than the initial rate. The conventional electromechanical totalizer makes it necessary to hole the line until the unit steps back to the "home" position. The electronic unit recycles on the interruption and the loop current can be under direct control of the switching contacts.

Incorrect registration of deposits made too close together

The electronic totalizer registers the deposit and originates the coin deposit signal as soon as the sensor in the chute is operated. Accordingly, the total readout time of the totalizer is reduced by the amount of time necessary to rotate the shaft and to power the stepping coil on the electromagnetic unit. A nominal value for this time is approximately 0.2 seconds which substantially reduces the probability of this type of misregistration.

Deposit made with handset on-hook

In this case, the coin deposit will not be refunded until the customer lifts the handset, obtains dial tone and then hangs up. The conventional electromechanical unit operates in substantially the same manner

since the totalizer can restore before the central office recognizes the "start."

FIG. 2 is an expanded diagram of the totalizer block 101 of FIG. 1 with FET drivers D1-D6 and a voltage regulator circuit 202 shown in schematic form and with a FET transistor logic circuit 201 represented in block form. The block and schematic portions of FIG. 2 taken together contain all of the FET devices used in the set. These devices may readily be fabricated in the form of beam-leaded integrated circuit chips. All FETs shown may be P channel-enhancement mode devices with a nominal threshold of one volt. The schematic circuit portion of FIG. 2 has been simplified in that the substrate lead is not shown but is understood to be connected to the positive battery by way of lead 6.

FETs D1 through D6 are drivers for the bipolar transistors Q1 through Q6 of FIG. 1 which are used to control the oscillator and speech network as described above. Each of the FETs D1 through D4 is in series with the base of a corresponding one of the NPN bipolar transistors so that the operation of each FET turns on the transistor associated therewith when the gate voltage becomes more negative than the threshold voltage of the FET. The FET drivers D1 through D6 are in turn controlled by the following outputs from the logic circuitry:

FET D1 is turned on by way of lead IR when the initial rate amount has been deposited.

FETs D2 and D5 are turned on by way of lead G when the coin deposit signal readout is in process. FET D3 is on (which is to say that the I lead is "high" — or at a relatively high voltage) when the coin deposit tone is generated.

FET D4 is turned on by way of the $\bar{G}$ lead when the coin deposit signal readout is in process and the coin deposit oscillator 103 (FIG. 1) is in its silent interval of signaling.

FET D6 is turned on by way of the $\bar{G}$ lead when the coin deposit readout is not in process, i.e., for other functions of the coin telephone.

The voltage regulator 202 maintains a constant voltage, constant current supply for the logic circuit 201. The basic feature of operation of the voltage regulator 202 is that a change in the supply is inverted and fed to transistor Q7 which controls the supply voltage. This arrangement results in a very high impedance circuit to prevent loading the line. The regulator 202 and transistor Q7 (FIG. 1) maintain the operating voltage for the logic at a level of 5.1 volts for a voltage at the set of from 7.5 to 20 volts with a regulation of approximately ± 2 percent for aging, temperature and load changes.

Details of the logic circuitry 201 of FIG. 2 are shown in FIG. 3. The toggle flip-flop stages A_T through D_T are toggled on the transition of the T lead from a logical "1" to a logical "0". The circuit is basically a ripple counter gated to count up on coin deposits and to count down when the coin deposit signal is generated. A multivibrator 302 controls the coin deposit signals and the count-down operation with an output on the I lead. Gates G35, G36 and G37 are used to inhibit read-in while the totalizer is in the down-count mode.

Count-Down Operation (Readout)

During the time the totalizer is reading out, the 5 cents, 10 cents and 25 cents leads are at "0" which in turn causes the output gates G5 through G10, G17, G18 and G21 to be "0" also. Lead $\bar{G}$ is low causing

gates G35, G36 and G37 to block any input information. This condition puts each toggle stage under control of the preceding stages and the I lead. Thus, toggle flip-flop B_T is under control of gate G2, toggle flip-flop C_T is under control of gate G3 and toggle flip-flop D_T is under control of gate G4. Since the input to these gates is the conjugate output from the preceding stages, the stage of the memory is stepped down one unit for each cycle of the I lead. The read-out continues as long as the G lead on the multivibrator 302 is high. When all stages are at "0," the output of gates G14 and G15 are "0" to stop the down-count at a home position. The output of gate G13 sets toggle stage E_T when the deposit is 25 cents, causing the H lead on the multivibrator 302 to go high, which in turn causes high speed readout for a quarter deposit. Stage E_T is reset when the totalizer reaches the home position through the invert 16 of the output of gate G14.

Count-Up Operation (Store)

The requirement that the inputs to the totalizer be 5 cents, 10 cents and 25 cents leads to a more complicated gating in the up-count portion of the totalizer. The I lead is low during the store operation, causing the outputs of gates G2, G3 and G4 to be "0." The $\bar{G}$ lead is high to couple all inputs to the count-up portion of the circuit. The store function is accomplished as follows:

Gate GA1 toggles stage A_T on a 5 cents or a 25 cents deposit.

Gates G21 and G5 toggle stage B_T , when A is high, to go from 01 to 10 or 11 to 00 (in binary notation) on a 5 cents or 25 cents deposit, the binary number dashes or blanks indicating that the value in that location is of no significance. The outputs of the toggle flip-flops are arranged in the order $D_T C_T B_T A_T$ to correspond to conventional binary notation so that $D_T = 2^3$, $C_T = 2^2$, $B_T = 2^1$, and $A_T = 2^0$. The binary number 0011 specifies, therefore, that A_T and B_T are high with C_T and D_T low.

Gate G6 is required to toggle stage C_T , when stages A_T and B_T are high, to go from -011 to -100 on a 5 cents deposit.

Gate G7 is required to toggle stage D_T , when stages A_T , B_T and C_T are high, to go from 0111 to 1000 on a 5 cents deposit.

Gate G8 is required to toggle stage C_T , when B_T is high, to go from 01 to 10 (or 11 to 00) on a 10 cents deposit.

Gate G9 is required to toggle stage D_T , when stage C_T is high, to go from 01-- to 10-- on a 25 cents deposit.

Gate G10 is required to toggle stage D_T , when stages B_T and C_T are high, to go from 011 to 100 on a 10 cents deposit.

Gates G17, G18 and G19 are required to meet the possible combination of a quarter deposit when the totalizer has a 15 cents store. In binary notation, this is from 0001 to 1000 and requires a direct set on stage D_T , since stage C_T did not change state. Gate G18 toggles stage C_T when either stages A_T or B_T is low (gate G19) on a 25 cents deposit to take care of all other combinations of 25 cents deposits and memory stages. Gate G17 toggles stage D_T when A_T and B_T are high to account for this special case. Thus, for a store of 0011 and a 25 cents deposit, stage C_T is not changed (gates G20 and G18 outputs are "high"); stages A_T and B_T are

toggled (gates G1 and G5); and stage D_T is toggled to result in a store of 1000. A similar transition occurs for a store of 0111 = 35 cents, to 1100 = 60 cents on a 25 cents deposit.

Initial Rate

The output from the totalizer circuit to set the initial rate relay B (FIG. 1) is generated by the one shot multivibrator circuit 301 under control of the flip-flop stage F. A deposit that equals or exceeds the preset initial rate amount will set flip-flop stage F, causing the one shot multivibrator 301 to generate a pulse of sufficient duration to operate the latching rate relay B (FIG. 1). The initial rate amount is adjusted by connecting leads L10, L11, L12, L13 of FIG. 1 either to battery or to ground. The combinations of these connections result in 16 possible initial rate amounts—from 0 cents to 75 cents.

Gates G22 through G34 are required to provide an output when a deposit equals or exceeds the initial rate amount; for example, an initial rate amount of 5 cents would be satisfied by a 5 cents, 10 cents or 25 cents deposit. An initial rate amount of 10 cents is set by connecting leads L10, L12 and L13 high and lead L11 low. The outputs of gates G22, G24 and G25 are always high since one input to an OR gate causes the output to go high. The AND gates G26, G28, G30 and G32 have a "0" output since one input is always 0. Thus, the output of gate G33 goes high for a memory state such that stage B_T is high; gate G27 goes high when stage C_T is high; gate G29 goes high when stage D_T is high, and gate G31 goes high when stages D_T and C_T are high. The output of gate G34 is, therefore, $B+C+D(DC)$ and any memory state greater than 5 cents will have at least one of these stages high. (In the immediately preceding expression for the output of gate G34, "+" indicates logical OR, and "." indicates logical AND.) The unused gates and redundant logic state (DC) are required for other initial rate amounts.

Store — Readout Control

The state of the G lead on the multivibrator 302 determines whether the totalizer reads out or stores a deposit. The G lead output of gate G15 is high only when the totalizer store is greater than "0" and the output of gate G12 is high. The output of gate G12 is high if stage F is high (initial rate made) or if the CO(A) lead is high (subsequent deposit). Thus, the totalizer will read out after the initial rate amount has been deposited or immediately after the deposit, depending on the polarity of the central office, supplied by way of the CO(A) lead.

The logic functions as shown in FIG. 3 utilize the standard OR and AND gates, but logic implementation in accordance with the principles of the invention can take any one of several forms, depending upon a variety of considerations. Changes to a different form can be executed by making use of the Boolean algebraic identity $A + \bar{B} = \bar{A} \cdot \bar{B}$, where the bar over the variable indicates the conjugate (NOT), the "+" operation indicates the logical OR operation, and the "." indicates a logical AND. Accordingly, the identity immediately above states that NOT (A or B) is the same as (NOT A AND NOT B). By repeated use of this identity, the AND and OR gates can be made using any one of the basic gates (AND, OR, NOR and NAND) and inverts (NOT). For example, an AND gate is made using a

NOR gate with all inputs inverted while an OR gate is made of a NOR gate followed by an invert.

The primary considerations employed in accordance with the invention to select the most desirable basic gate form for a commercial version of the circuit are the following:

The area on the chip used to supply the gating function should be a minimum.

The difference in voltage levels between a "0" and a "1" for a given chip area and supply voltage should be a maximum.

A logical "1" should be the presence of a voltage (as opposed to a zero voltage level) to minimize false signals introduced by noise in the input-output leads. This condition results in fixing the input leads at ground level when no input is present and effectively shorts out any introduced noise.

The toggle flip-flop best suited for P-channel MOS-FET implementation (at the supply voltage available) toggles on the transition from a negative to a zero voltage. To maintain the same logic format of toggling, the flip-flop on the transition from a logical "1" to a "0," the negative voltage is divided as a logical "1" or "high."

Schematic circuit diagrams of the basic building blocks for all of the logic functions employed in the totalizer are shown in FIG. 5A, 5B, 5C and 5D. FIG. 5A shows both a parallel and a series NOR gate. The circuits illustrated are for a two-input stage but may readily be expanded or reduced for a larger gate or for an invert. IGFETs N1 and N4 are used as load resistors, while IGFETs N2, N3, N5 and N6 are the active devices. All devices are P-channel enhancement mode.

In the parallel NOR gate of FIG. 5A when either A or B is negative, device N2 or N3 is on, and the output at point X is clamped to near the ground potential. This output level is dependent on the relative parameters of N1 and N2 (or N3). A gate with more inputs is formed by adding more active devices in parallel with N2 and N3. Since the output is near ground potential (0) when either A or B is negative (1), this gate is a NOR, that is, X is "1" when neither A NOR B is "1." This arrangement is a "negative logic" form since the more negative voltage is defined as a logical "1."

In the series gate of FIG. 5A, the voltage at the output is low when both A and B are negative and the output level is dependent on the parameters of N4 compared to N5 and N6 in series. To obtain the same level of "0" output voltage for the series gate (as compared to the parallel gate) N5 and N6 must be twice as large as N3 or N2. A gate with more inputs requires additional series devices and a corresponding increase in size for each of the input devices. Device size consideration as well as chip layout problems associated with the series NOR gate of FIG. 5A combine to make the parallel gate the preferred form for use in a commercial electronic totalizer environment. Invert, OR and AND circuits may advantageously be of the form shown in FIG. 5B, 5C and 5D, respectively.

The invert circuit of FIG. 5B is the basic building block used, in accordance with the invention, in developing all of the logic functions of the totalizer in integrated circuit form. In the configuration shown, the field effect transistor (FET) TN1 is used as a load device, and the FET TN2 is the active device. It can be shown, by solving for the voltage V_o, that the output is dependent on the ratio of the transistor parameters.

The actual values of the β parameters of the FET devices TN1 and TN2 are dependent on the speed required, the chip area and the power absorption requirements. Since the totalizer of the invention is intended to be operated with line power when used in a telephone set, a minimum β is desirable for the TN1 device. Typical of β values are 0.75 and $7.5 \mu\text{A}/\text{V}^2$ for the load and active devices, respectively. The required speed of operation for the overall circuit is relatively low so that the required turnon time of the invert stage is set only by the operation of other parts of the circuit such as the toggle flip-flops. The maximum power absorbed by an invert stage (or gate) can be found by calculating the current through the load device when the output is at a minimum. A drain of 7.0 microamperes is illustrative for an approximate power absorption of 39 microwatts per stage.

The OR logic function is implemented by the circuit shown in FIG. 5C which utilizes FETs OR1 through OR6. The output at point Y is high when neither A, B, NOR C is high. The output X is high only when Y is low, resulting in a high for X when either A, B, or C is high. The added invert section is often not required in the actual logic implementation, since the output $Y = \bar{X}$ may be the signal required for the next gate in the logic sequence. An example would be an OR gate feeding an AND gate, since the AND gate requires an invert on the input as explained hereinbelow.

The implementation of an AND gate employed in accordance with the invention is shown in FIG. 5D. FETs AN1 through AN10 are employed to form a three-input NOR gate with all inputs inverted. The output X is high when neither A, B, NOR C is high, which is true only if A, B and C are all high. As in the case of the OR gate, the inverts are not always essential in a logic circuit since the conjugate of the input (A, B and C in this case) is often available.

The one shot multivibrator 301 of FIG. 3 is shown in detailed schematic circuit form in FIG. 6A. As explained above, this multivibrator is employed to put out a timed pulse, after the initial rate amount has been deposited, to operate a latching relay. This arrangement is used to minimize the power drain resulting from the relay operate current and to provide a local ground path for the initial rate ground test.

The circuit employs a total of nine FETs, OS1-OS9, a resistor R5 and a capacitor C. The basic feature of the circuit's operation involves the charging of the voltage VN2 through the OS1 FET when the input voltage is low and the discharging of this voltage through the OS2 FET after the output goes high. The complete operation of the circuit may best be explained in terms of the timing sequence that occurs in the course of one operating cycle. Before the initial rate amount is deposited, the devices OS1, OS4 and OS6 are on to set the voltage VN3 and VN4 low. FET OS1 is on to charge the timing capacitor C to a voltage determined by the ratio of the size of the devices OS1 and OS2. The OS2 device is on all the time and is used as a discharge path for the timing capacitor C. As soon as the input level goes high, the device OS6 turns off to let the output go high, and the device OS1 turns off to allow the discharge of timing capacitor C through the on resistance of the OS2 device. The output remains high until the VS2 voltage discharges to a point where the device OS4 begins to turn off causing the voltage VN3 to increase to turn on devices OS3 and OS5. As soon as the device OS3 be-

gins to turn on, the RC time constant is decreased owing to the parallel discharge path through the OS3 device. Device OS5 changes the output to "0." This mechanism limits the amount of time the stage is in the active region to minimize the amplification of noise and timing variations resulting from parameter changes. The magnitude of the capacitor is selected to ensure adequate time to operate the rate relay for maximum parameter variations.

A detailed schematic circuit diagram for the FRS and ERS flip-flops shown in block form in FIG. 3 is shown in FIG. 6B. This circuit employs the FETs FP1 through FP6 and is the basic cross-coupled (bistable) invert stage with an added input device in parallel with each active device. A high input on the R lead causes the Q lead to go low ($\bar{Q}$ high), and a "1" on the S lead sets Q high. The stage is used with external logic so that R and S cannot be high at the same time inasmuch as the output is undefined for this condition.

An illustrative schematic circuit diagram for the toggle flip-flop circuits A_T , B_T , C_T and D_T shown in block form in FIG. 3 is shown in FIG. 7A. The logic provided by this circuit is illustrated by the logic diagram of FIG. 7B. A total of 24 FETs, TF1 through TF24, are employed with correspondence between these devices and the logic functions are follows: devices TF1 and TF2 form AND gate 3; devices TF4 and TF5 form AND gate 4; devices TF6 and TF7 together with TF8 and TF9 provide the cross-coupled NOR gate for the basic memory; devices TF10 and TF11 form AND gate 5; devices TF13 and TF14 provide the AND gate 6; and device TF15 forms the invert required for the T input to gates 4 and 6. The delay is caused by the two discrete capacitors connected to voltage designation terminals V2 and V7. The invert formed by the device TF3 provides the dual functions of the invert (or the input to gate 4) to convert a NOR to an AND gate and provides the delay in conjunction with the capacitor.

Only a single transition of the flip-flop output need be explained since the circuit is completely symmetrical. Assume first that the output of the circuit is such that $\bar{Q}$ is high (negative) and the input is high. Devices TF1, TF4, TF8, TF11, TF13, TF14 and TF15 are on, resulting in holding V1, V3, V5, V6, V8 and V9 low. Both capacitors C71 and C72 are charged since V2 and V7 are high. As soon as the input goes low, the devices TF1, TF14 and TF15 turn off, causing TF3, TF5 and TF10 to turn on. This condition results in setting V2, V3, V5, V6 and V8 low with V1, V4 and V7 high. Note that the output V5 has not changed and that only one of the capacitors, C71, has been discharged. The transition of the input from a "0" to a "1" causes the stage to toggle. With a high input devices TF1, TF8, TF11, TF13, TF14 and TF15 turnon, but this time the gate of the TF4 device is held low by the capacitor C71. This condition allows V3 to go high (since both TF4 and TF5 are off), device TF6 to turn on and clamp V4 to a low value, and V5 to go high (both devices TF8 and TF9 are now off). The RC time constant of the capacitor C71 and the on resistance of the device TF17 is long enough to ensure that the stage has toggled fully until V2 reaches a threshold voltage.

The actual values of the device parameters of the circuit of FIG. 7A are dictated by the same requirements as the invert sections forming it. For example, the value of the capacitors is dictated by the speed of the basic memory section, the rise time of the input pulse and the

capacitive load on the output V5. It is found that a one p.f. capacitor is sufficient if the load on the circuit is the input to one other gate. The requirement that the memory stage always be in the "0" state when the power is turned on is met by putting all of the load (outputs to other gates) on the V5 terminal. This slows the rise of V5, when the power is turned on, to set the stage at "0" and also requires that the rise time of V2 be long.

A schematic circuit diagram for the multivibrator 302 shown in block form in FIG. 3 is shown in FIG. 8. The basic circuit is made up of three invert sections Q6, Q4 and Q2 with their associated load devices. Since the output of the third invert is connected to the input of the first, the triple invert section has no stable operating point. The addition of the timing capacitor C causes the basic circuit to act as a multivibrator with the capacitor charge path through the FETs Q2 and Q3-Q8 for one-half cycle and through the devices Q4 and Q1-Q7 for the other half cycle.

Two-speed operation is provided by the H lead through Q13 which turns on the parallel load devices Q7 and Q8 when high-speed operation is desired. The circuit is turned on by the G lead (and/or H lead) which turns on the load devices Q3 and Q1. The section formed by the devices Q15, Q16, Q17 and Q18 is used to set the node voltages (when the circuit is turned off) so that the first output pulse is the same as the subsequent pulses. Devices Q9, Q10, Q11 and Q12 are used for threshold and temperature compensation in order to stabilize the output.

The circuit of FIG. 4A was developed from the circuit of FIG. 3 to replace all of the AND gates with a NOR gate having all inputs inverted and placing all OR gates with a NOR followed with an invert. Additional modifications may be accomplished in accordance with the invention to facilitate further the layout of the chip, and these modifications result in the logic diagram shown in FIG. 4B. The changes from FIG. 4A were arrived at primarily through the cascading of logic gates in order to minimize the number of leads on the chip.

It is to be understood that the embodiment described herein is merely illustrative of the principles of the invention. Various modifications thereto may be effected by persons skilled in the art without departing from the spirit and scope of the invention.

We claim:

1. A coin operated telephone set having terminals connectable to a telephone line comprising, in combination:

a speech network, an equalizer circuit, a coin deposit signal oscillator, and a combination electronic totalizer and logic control circuit connected in parallel across said terminals;

said totalizer including a solid state device ripple counter circuit;

means responsive to the deposit of a coin for initiating up-counting by said counter;

first means for controlling the generation of readout signals by said oscillator;

second means for controlling the repetition rate of said readout signals;

third means for controlling whether the totalizer reads out or stores coin deposit information;

fourth means for initiating count-down operation of said totalizer simultaneously with said generation of said readout signals;

each of said first, second, third and fourth means including a respective portion of said logic control circuit and a common multifunction multivibrator.

2. Apparatus in accordance with claim 1 wherein said counter comprises a combination of IGFET toggle flip-flop circuits.

3. A coin operated telephone set comprising, in combination:

a pair of terminals connectable to a telephone line; a speech network, an equalizer circuit, a coin deposit signal generator and an electronic coin totalizer;

first, second, third and fourth means for connecting said network, said equalizer circuit, said generator and said totalizer, respectively across said terminals;

said totalizer including a plurality of toggle flip-flops and logic control circuitry;

means responsive to the deposit of coins for initiating count-up action by said flip-flops;

said logic control circuitry including a multifunction multivibrator circuit for initiating the operation of said generator, for controlling the repetition rate of readout signals from said generator and for initiating count-down operating of said totalizer simultaneously with said generation of said readout signals.

4. Apparatus in accordance with claim 3 wherein each of said first, second and third means comprises a respective transistor switch, each of said switches being directly controlled by an IGFET logic element.

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