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(54) **VOLT-SECOND BALANCED PFCPWM POWER CONVERTER**

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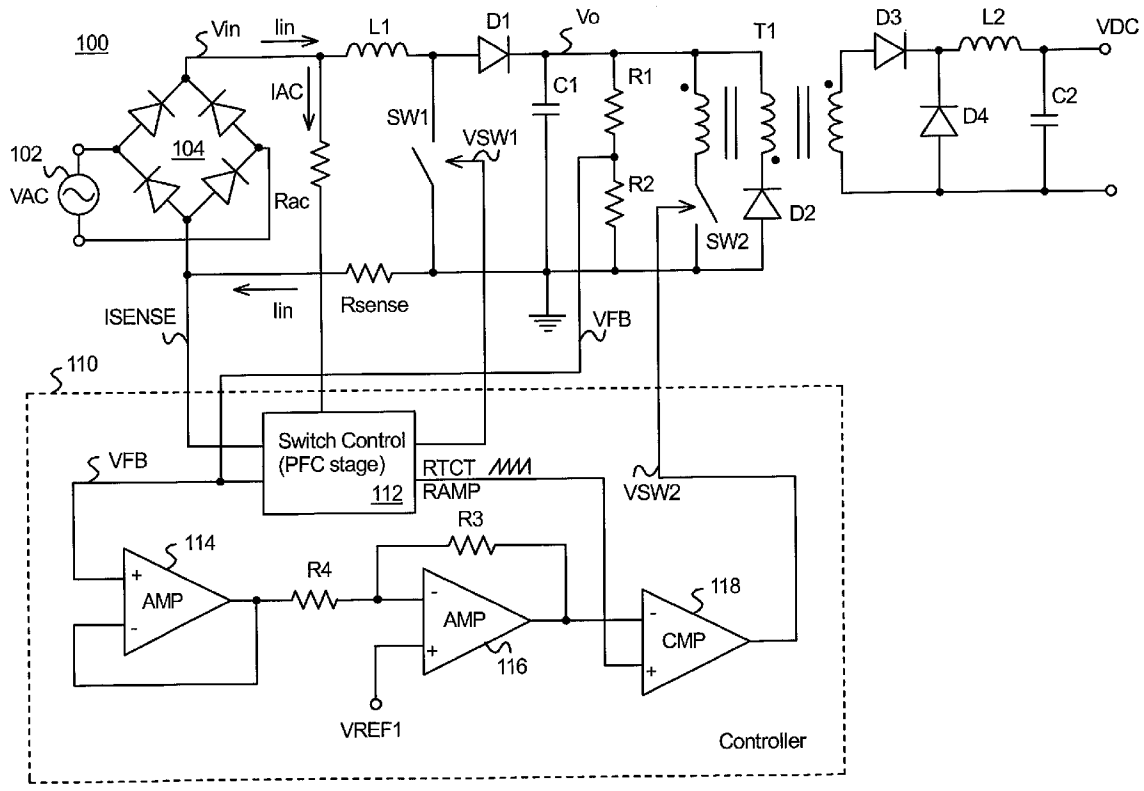
(57) **ABSTRACT**

A volt-second balanced, power factor correction (PFC), pulse-width modulation (PWM) two-stage power converter. A first PFC stage receives an AC input signal and forms a regulated intermediate output voltage. A second stage receives the intermediate output voltage and forms a regulated DC output voltage. A level of the intermediate output voltage is monitored and used to adjust the duty cycle of a main power switch in the PWM stage. By adjusting the PWM duty cycle based on the level of the intermediate output voltage, rather than the DC output voltage, the PWM converter is volt-second balanced. Further, when a controller for the power converter is implemented as an integrated circuit, a pin is not required for monitoring the regulated DC output. Accordingly, the number of pins is minimized.



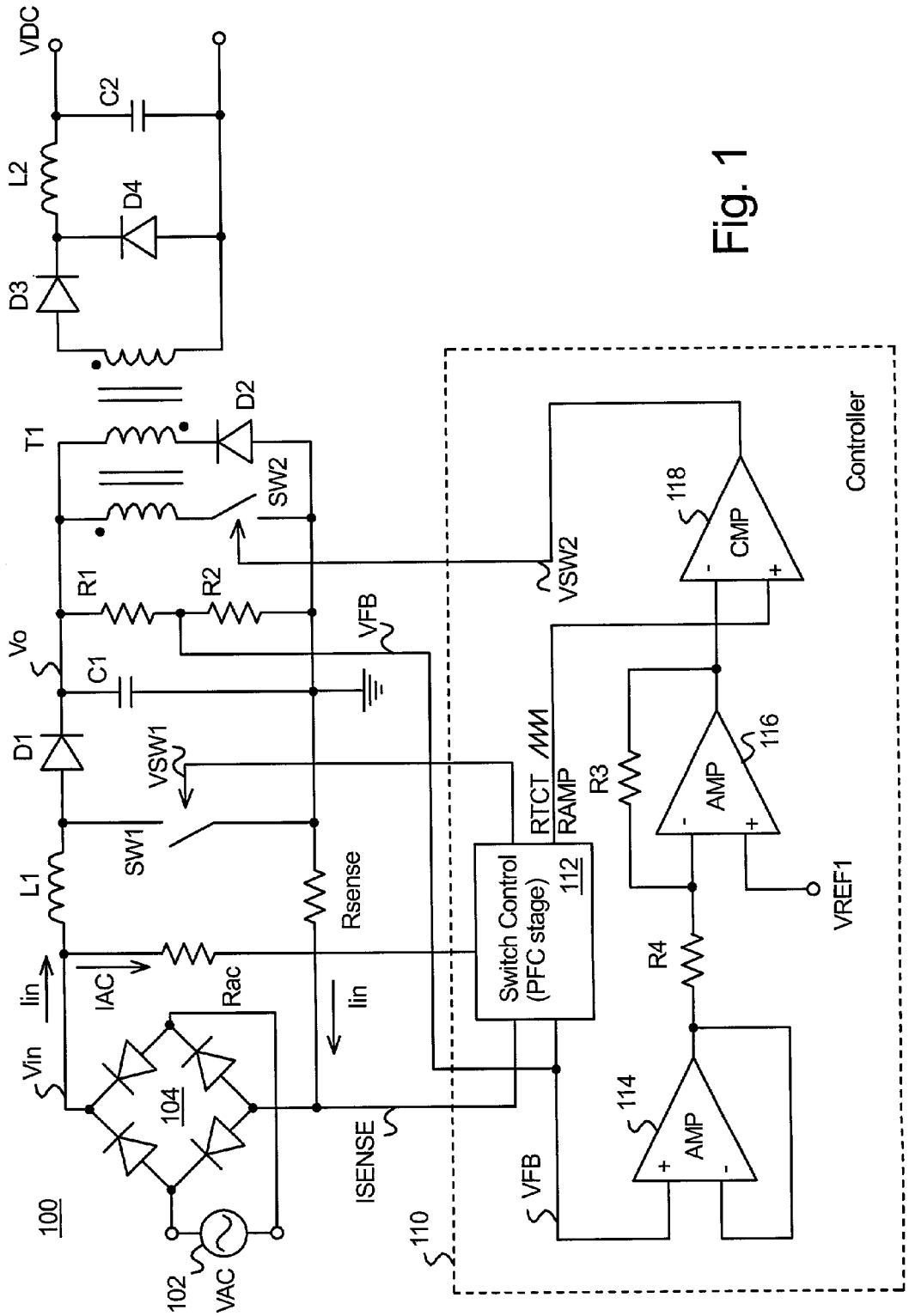

VDC
C2
L2
D4
D3
T1
D2
SW2
R1
R2
VFB
Vo
C1
D1
VSW1
SW1
L1
Rsense
Iin
IAC
Rac
Vin
104
100
102
VAC
ISENSE
110
Switch Control
(PFC stage)
112
RTCT
RAMP
R3
R4
VSW2
CMP
118
AMP
116
AMP
114
VREF1
VFB
Controller

Fig. 1

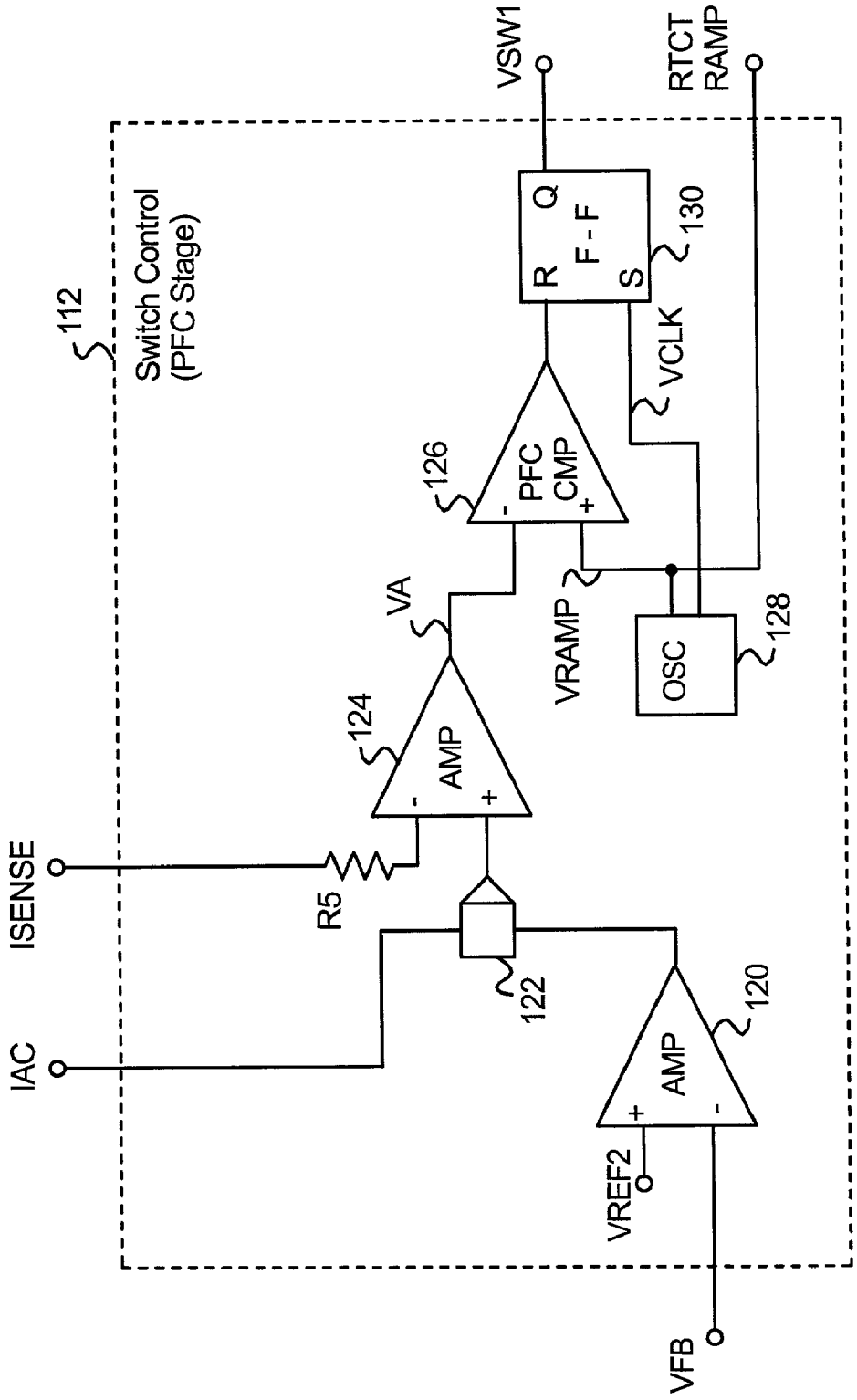

112
Switch Control
(PFC Stage)
VSW1
RTCT
RAMP
Q
R
F - F
S
130
VCLK
126
PFC
CMP
VA
VRAMP
OSC
128
124
AMP
ISENSE
R5
122
IAC
120
AMP
VREF2
VFB

Fig. 2

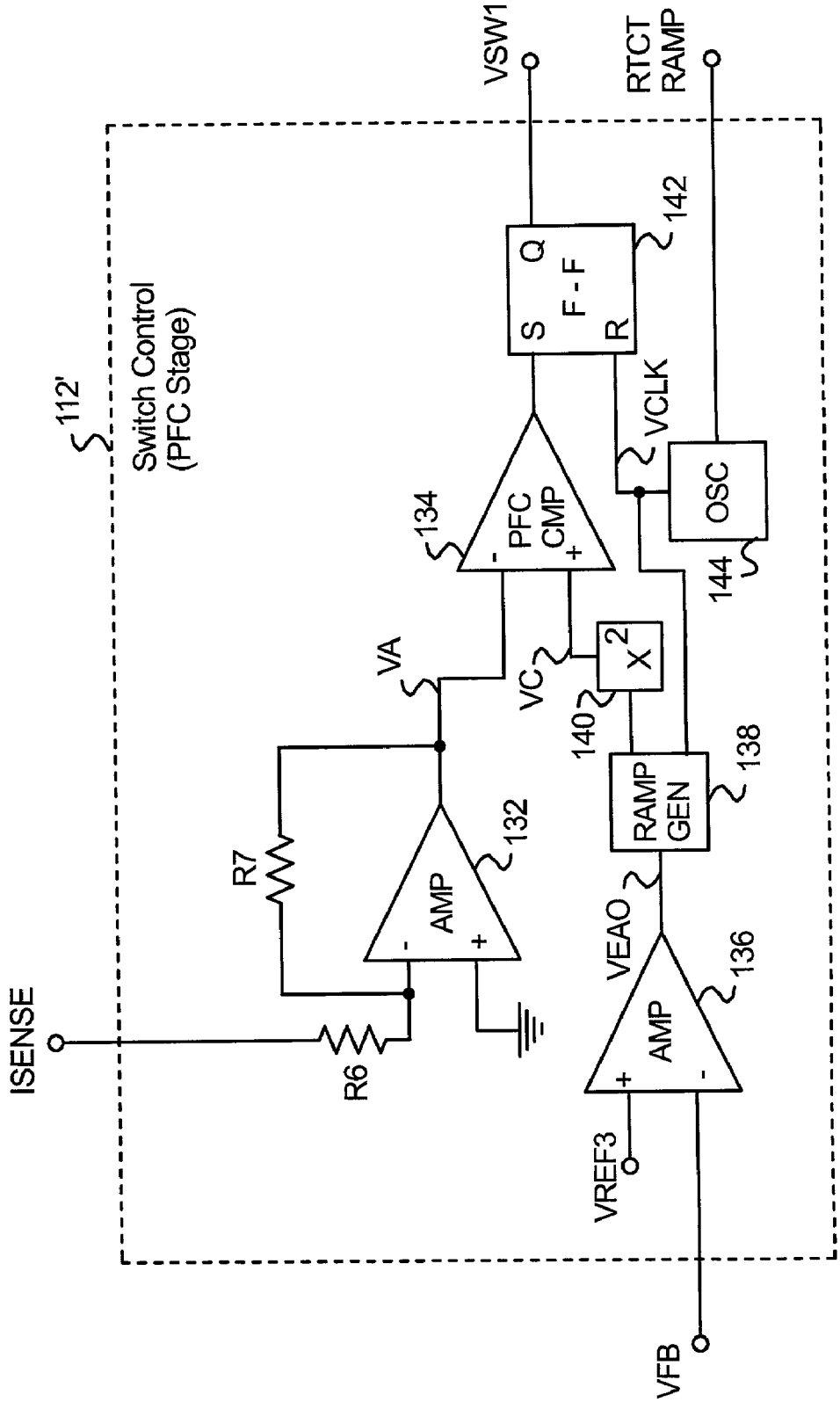

112'
Switch Control
(PFC Stage)
VSW1
RTCT
RAMP
142
S
Q
F - F
R
VCLK
134
PFC
CMP
OSC
144
VA
VC
X 2
140
138
RAMP
GEN
R7
132
AMP
VEAO
136
AMP
ISENSE
R6
VREF3
VFB

Fig. 3

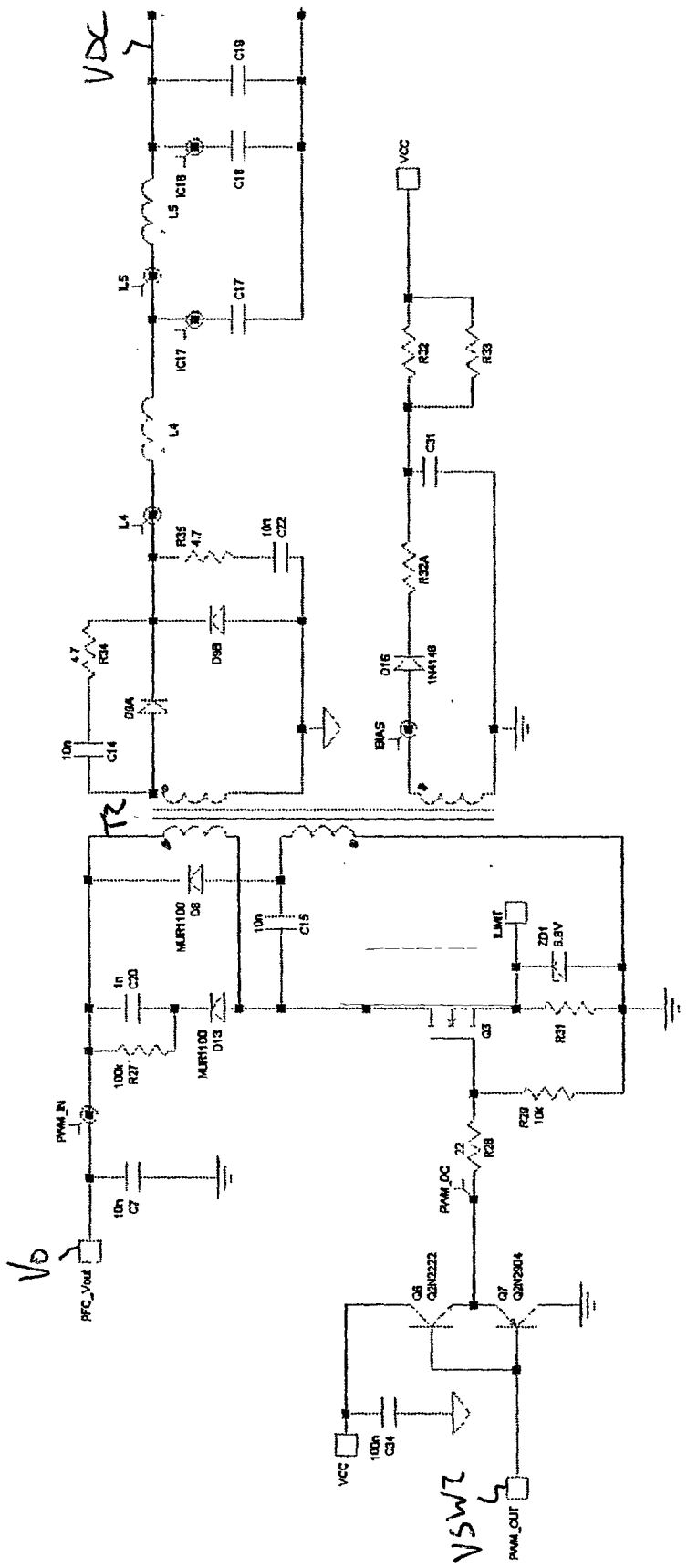

VDC
C19
C18
IC18
L5
IL5
C17
IC17
L4
IL4
R35 4.7
10n C22
4.7 R34
D9B
D9A
10n C14
TR
MUR1100 D8
10n C15
1n C20
100k R27
MUR1100 D13
PWM_IN
10n C7
VFC_Vout
VCC
R32
R33
C31
R32A
D16 1N4148
IBIAS
ILIMIT
ZD1 5.6V
Q3
R31
R29 10K
R28 22
PWM_DC
Q6 Q2N2222
Q7 Q2N2904
VCC
100n C34
PWM_OUT
VSW2

Fig. 4

VOLT-SECOND BALANCED PFCPWM POWER CONVERTER

[0001] This application claims the benefit of U.S. Provisional Application Serial No. 60/300,492, filed Jun. 21, 2001.

FIELD OF THE INVENTION

[0002] The invention relates to switching power converters. More particularly, the invention relates to PFC-PWM two-stage power converters.

BACKGROUND OF THE INVENTION

[0003] A conventional PFC-PWM two-stage power converter includes a first PFC stage and a second PWM stage. An intermediate voltage formed by the PFC stage is monitored and switching in the PFC is adjusted in a feedback loop in response to the monitored intermediate voltage. A DC output voltage of the PWM stage is monitored and switching in the PWM stage is adjusted in a feedback loop in response to this monitored DC output voltage. Thus, a controller for the converter monitors both the intermediate voltage and the DC output voltage.

[0004] It is desired to provide an improved PFC-PWM two-stage power converter. It is to these ends that the present invention is directed.

SUMMARY OF THE INVENTION

[0005] The invention is a volt-second balanced, power factor correction (PFC), pulse-width modulation (PWM) two-stage power converter. A first PFC stage receives an AC input signal and forms a regulated intermediate output voltage. A second stage receives the intermediate output voltage and forms a regulated DC output voltage. A level of the intermediate output voltage is monitored and used to adjust the duty cycle of a main power switch in the PWM stage. By adjusting the PWM duty cycle based on the level of the intermediate output voltage, rather than the DC output voltage, the PWM converter is volt-second balanced. Further, when a controller for the power converter is implemented as an integrated circuit, a pin is not required for monitoring the regulated DC output. Accordingly, the number of pins is minimized.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] **FIG. 1** illustrates a schematic diagram of a PWM-PFC two-stage power converter in accordance with the present invention.

[0007] **FIG. 2** illustrates a schematic diagram of a controller for the power converter of **FIG. 1** in accordance with an aspect of the present invention;

[0008] **FIG. 3** illustrates a schematic diagram of an alternate embodiment of a controller for the power converter of **FIG. 1** in accordance with an aspect of the present invention; and

[0009] **FIG. 4** illustrates a schematic diagram of an alternate embodiment of a PWM stage of a power converter in accordance with an aspect of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

[0010] **FIG. 1** illustrates a schematic diagram of a PWM-PFC two-stage power converter **100** in accordance with the present invention. A power supply **102**, such an AC power source, may provide a signal VAC that is coupled across input terminals of a bridge rectifier **104**. A first output terminal of the rectifier **104** may be coupled to a first terminal of an inductor L1. A second terminal of the inductor L1 may be coupled to an anode of a rectifying diode D1 and to a first terminal of a switch SW1 (e.g., a MOSFET). A cathode of the diode D1 may be coupled to a first terminal of a capacitor C1.

[0011] A second output terminal of the rectifier **104** may be coupled to a first terminal of a current-sensing resistor Rsense. A second terminal of the current-sensing resistor Rsense, a second terminal of the switch SW1 and a second terminal of the capacitor C1 may be coupled to a ground node. Collectively, the inductor L1, switch SW1, diode D1, and capacitor C1 form a power factor correction (PFC) stage of the power converter **100**.

[0012] When the switch SW1 is closed, current from the rectifier **104** charges the inductor L1 with energy. When the switch SW1 is opened, energy stored in the inductor L1 is discharged into the capacitor C1. An output voltage Vo is formed by the PFC stage across the capacitor C1. A controller **110**, such as an integrated circuit controller, may control the switch SW1 to regulate an output voltage formed at the first terminal of a capacitor C1. The controller **110** may include a conventional PFC controller **112**.

[0013] A resistive divider including resistors R1 and R2 may be coupled across the capacitor C1. A feedback voltage VFB that is representative of the voltage Vo may be coupled to the PFC controller **112**. In addition, the current-sensing resistor Rsense may be coupled to the PFC controller **112**. Also, a first terminal of an input voltage sensing resistor Rac may be coupled to the first output terminal of the rectifier **104**. A second terminal of resistor Rac may be coupled to the PFC controller **112**.

[0014] To form a switch control signal VSW1, the PFC controller **112** may receive a signal Isense formed at the first terminal of the sensing resistor Rsense that is representative of an input current Iin drawn from the source **102** and the signal VFB that is representative of the output voltage Vo. The PFC controller **112** may also receive a signal IAC that is representative of a rectified input voltage Vin formed by the rectifier **104**. The switch control signal VSW1 may be coupled to control the switch SW1 to maintain the input current substantially in phase with the input voltage VAC in addition to regulating the output voltage Vo. A periodic ramp signal RTCT may be generated by the controller **112**, such as by an oscillator (**128** in **FIG. 2** and **144** in **FIG. 3**) of the controller **112**, and may be used to control the switching frequency of the switch SW1.

[0015] The intermediate output voltage Vo of the PFC stage serves as an input source for pulse-width modulation (PWM) stage of the converter **100**. More particularly, the first terminal of the capacitor C1 may be coupled to a first terminal (designated with a "dot" according to the "dot" convention for designating winding polarity) of a first winding of a transformer T1 and to a first terminal of a second winding of the transformer T1. The second winding may be inductively coupled to the first winding. A second terminal of the first winding may be coupled to a first terminal of a switch SW2 (e.g., a MOSFET). A second terminal (designated with a "dot") of the second winding may be coupled

to a cathode of a diode D2. A second terminal of the switch SW2 and an anode of the diode D2 may be coupled to the ground node.

[0016] A third winding of the transformer T1 may be inductively coupled to the second winding. A first terminal of the third winding may be coupled to an anode of a diode D3. A cathode of the diode D3 may be coupled to a cathode of a diode D4 and to a first terminal of an inductor L2. A second terminal of the inductor L2 may be coupled to first terminal of a capacitor C2. A second terminal of the third winding may be coupled to an anode of the diode D4 and to a second terminal of the capacitor C2. A regulated output voltage VDC may be formed across the capacitor C2 by the PWM stage.

[0017] The feedback signal VFB may be coupled to a non-inverting input of an amplifier **114**. An inverting input of the amplifier **114** may be coupled to an output of the amplifier **114** and to a first terminal of a resistor R4. A second terminal of the resistor R4 may be coupled to a first terminal of a resistor R3 and to an inverting input of an amplifier **116**. A reference voltage Vref1 (e.g., 2.5 volts) may be coupled to a non-inverting input of the amplifier **116**. A second terminal of the resistor R3 may be coupled to an output of the amplifier **116** and to a first input terminal of a comparator **118**. The periodic ramp signal RTCT may be coupled to a second input terminal of the comparator **118**. An output of the comparator **118** forms a switch control signal VSW2. The switch control signal VSW2 controls the switch SW2 to form the output voltage VDC.

[0018] More particularly, when the switch SW1 is closed, the transformer T1 is charged with energy. When the switch is opened, the energy is discharged into the capacitor C2 through the inductor L2. The diode D2 rectifies current in the second winding of the transformer T1, while the diodes D3 and D4 rectify current in the third winding of the transformer T1. The transformer T1 is part of an active clamping circuit. It will be apparent, however, that another topology may be used for the PFC stage.

[0019] A duty cycle of the switch SW2 controls the level of the output voltage VDC. When the intermediate output voltage Vo is at a desired level (e.g., 380 volts), then the duty cycle of the switch SW2 is preferably approximately 50%. This steady-state duty-cycle can be adjusted by selecting component values, such as inductance values and winding ratios for the transformer T1, based on expected power consumption by a load (not shown) that receives the output voltage VDC.

[0020] When the intermediate voltage Vo rises under transient conditions, so does the feedback voltage VFB. In response, the duty cycle for the switch SW2 is decreased. Conversely, when the intermediate voltage Vo falls, so does the feedback voltage VFB. In response, the duty cycle for the switch SW2 is increased. Accordingly, the output voltage VDC of the PWM stage is regulated (i.e. maintained substantially constant) by the controller **110** monitoring the voltage at the input of the PWM stage (i.e. the intermediate voltage Vo) rather than the output voltage VDC.

[0021] **FIG. 2** illustrates a schematic diagram of an exemplary controller **112** for the PFC stage of the power converter of **FIG. 1** in accordance with an aspect of the present invention. The controller **112** uses average current-mode control to adjust the switching duty cycle of the switch SW1. The output voltage sensing signal VFB may be coupled to a first input of an amplifier **120**. A second input of the amplifier **120** may be coupled to receive a reference voltage VREF2. An output of the amplifier **120** forms an error signal which is representative of a difference between the intermediate output voltage Vo and a desired level for the intermediate output voltage Vo. The error signal may be coupled to a first input of a multiplier **122**. The input voltage sensing signal IAC may be coupled to a second input of the multiplier **122**.

[0022] An output of the multiplier **122** may be coupled to a first input terminal of an amplifier **124**. The input current sensing signal ISENSE may be coupled to a second input of the amplifier **124** via a resistor R5. An output of the error amplifier **124** may be coupled to a first input terminal of a modulating comparator **126**. An oscillator **128** may form a clock signal VCLK and a linear periodic ramp signal VRAMP that is synchronized to the clock signal VCLK. The ramp signal VRAMP may be coupled to a second input terminal of the modulating comparator **126**. The ramp output of the oscillator **128** may be formed, for example, by charging a capacitor (not shown) with a constant current. An output of the modulating comparator **126** may be coupled as an input R of a flip-flop **130**. The clock output VCLK of the oscillator **128** may be coupled as an input S of the flip-flop **130**. An output Q of the flip-flop **130** may form the switch control signal VSW1.

[0023] The signal output from the amplifier **124** modulates up and down. When compared to the linear ramp signal from the oscillator **128**, this adjusts the switching duty cycle of the PFC stage of the power converter **100** so as to regulate the intermediate output voltage Vo. More particularly, the amplifier **124** adjusts the switching duty cycle under closed loop control to maintain a voltage differential across its inputs to nearly zero volts. This forces the input current Iin to follow the waveform of the rectified sine wave of the input voltage Vin. The current control loop and the power delivery circuitry must have at least enough bandwidth to follow this waveform. It will be apparent that configuration of the controller **112** is exemplary and that modifications may be made.

[0024] **FIG. 3** illustrates a schematic diagram of an alternate embodiment of a controller **112'** for the power converter **100** of **FIG. 1** in accordance with an aspect of the invention. The controller **112'** uses input current shaping to adjust the duty cycle of the switch SW1. The current sensing signal ISENSE is coupled to a first terminal of a resistor R6. A second terminal of the resistor R6 may be coupled to the first input of an amplifier **132** and to a first terminal of a resistor R7. A second terminal of the resistor R7 may be coupled to the output of the amplifier **132**, while a second input of the amplifier **132** may be coupled to a ground node. A signal VA formed at the output of the amplifier **132** is representative of the input current Iin. The signal VA may be coupled to a first input of a comparator **134**.

[0025] The voltage sensing signal VFB may be coupled to a first input terminal of an amplifier **136**. A second input terminal of the amplifier **136** may be coupled to receive a reference voltage VREF4. An output of the amplifier **136** forms an error signal VEAO which is representative of a difference between the output voltage Vo and a desired level for the output voltage Vo.

[0026] A ramp generator **138** receives the error signal VEAO as an input and integrates the signal VEAO. Thus, the slope of a periodic ramp signal formed by the ramp generator **138** depends on the then-current level of the error signal VEAO. The signal from the ramp generator **138** is then applied to a squaring element **140**. An output of the squaring element **140** is applied to the second input terminal of the comparator **134**.

[0027] An output of the comparator **134** may be coupled to a set input S of a flip-flop or latch **142**. An oscillator **144** may form a clock signal VCLK, which is coupled to a reset input of the flip-flop **142**. In addition, the oscillator **144** may form a periodic linear ramp signal RTCT RAMP for use by the PWM stage. A Q output of the flip-flop **142** may form the switch control signal VSW1 which controls the duty cycle of the switch SW1 so as to regulate the intermediate output voltage Vo formed by the PFC stage.

[0028] The signal VSW1 may be reset to a logical low voltage level upon a leading edge of each pulse in the clock signal VCLK. When the signal VC exceeds the signal VA, the output of the comparator **134** may set the flip-flop **142** such that the switch control signal VSW1 returns to a logical high voltage level. Thus, the duty cycle of the switch SW1 is controlled with negative feedback to maintain the input current En in phase with the input voltage Vin and to regulate the output voltage Vo. It will be apparent that leading or trailing edge modulation techniques may be utilized and that other types of modulation may be used, such as frequency modulation. Unlike the average current-mode controller illustrated in **FIG. 2**, the input voltage sensing signal IAC is not required. Accordingly, the resistor Rac may be omitted from **FIG. 1**.

[0029] Other switching power supplies that perform power factor correction are described in: U.S. Pat. No. 5,804,950, entitled, "Input Current Modulation for Power Factor Correction;" U.S. Pat. No. 5,742,151, entitled, "Input Current Shaping Technique and Low Pin Count for PFC-PWM Boost Converter;" U.S. Pat. No. 5,798,635, entitled, "One Pin Error Amplifier and Switched Soft Start for an Eight Pin PFC-PWM Combination Integrated Circuit Converter Controller;" and co-pending U.S. patent application Ser. No. _____, filed May 31, 2002, and entitled, "Power Factor Correction with Carrier Control and Input Voltage Sensing" the contents of all of which are hereby incorporated by reference.

[0030] Advantages of the invention are that the PWM converter is volt-second balanced. This is because the PWM duty cycle is adjusted based on the level of the intermediate output voltage Vo, rather than the output voltage VDC.

[0031] In one embodiment, the windings ratio between the first winding (in series with the switch SW2) and second winding (in series with the diode D2) of the transformer T1 **(FIG. 1)** may be: 2:1. In other words, the first winding has twice as many windings as the second winding. The voltage Vo may have, for example, a regulated level of 380 volts. Thus, when the switch SW2 is closed, 380 volts is applied across the first winding of the transformer. Due to the windings ratio, 190 volts is induced across the second winding (and the voltage across the diode D2 is, thus, 570 volts). In addition, when the switch SW2 is closed, a volt-second product for the first winding is equal to the duration of the switch being closed (D) times the voltage Vo. Where the duty cycle (D) is 50%, this yields a volt-second product of 50% times 380 volts or 190 volt-seconds. This represents a level of magnetic flux in the first winding induced during the charging phase. If allowed to build over multiple switching cycles, this could lead to saturation of the transformer T1.

[0032] When the switch SW2 is opened, the voltage Vo is applied across the second winding. As a result, a voltage of 760 volts is induced across the first winding. Thus, when the switch SW2 is open, a volt-second value for the first winding is equal to the duration of the switch being opened (1-D) times the voltage Vo. Where the duty cycle is 50%, the volt-second product for the discharge phase is 50% times 760 volts or 380 volt-seconds. Therefore, because the volt-second product during discharging is at least as great as the volt-second product during charging the power converter can be said to be volt-second balanced.

[0033] The maximum duty-cycle (D) given the above winding ratio is ⅔ or 66.6%. Thus, for charging, the volt-second product is ⅔ times 380 volts or 253 volt-seconds. And, for discharging, the volt-second product is ⅓ times 760 volts or 253 volt-seconds. Thus, the duty-cycle for the switch SW2 is preferably maintained below 66.6% (e.g., 50%).

[0034] Thus, by controlling the duty-cycle of the switch SW2 based on the voltage Vo, the duty-cycle is maintained such that the transformer T1 is volt-second balanced. This is true despite changes in the PWM output voltage VDC or changes in the intermediate output voltage Vo. It will be apparent that other parameters may be selected, while maintaining this volt-second balance in accordance with the present invention. For example, a different windings ratio may be selected for the transformer T1.

[0035] Further, when the controller **110** for the power converter **100** is implemented as an integrated circuit, a pin is not required for monitoring the regulated output VDC. Accordingly, the number of pins is minimized. Further, the periodic ramp signal generated by the PFC controller **112** may be used as a PWM ramp for the PWM stage. This also reduces the need for an additional pin.

[0036] **FIG. 4** illustrates a schematic diagram of an alternate embodiment of PWM stage of a power converter in accordance with an aspect of the present invention. The output voltage Vo of the PFC stage may be applied to a first terminal of a capacitor C7, to a first terminal of a resistor R27, to a first terminal of a capacitor C20 to a cathode of a diode D8 and to a first terminal (designated with a "dot") of a first primary winding of a transformer T2. A second terminal of the capacitor C7 may be coupled to a ground node. A second terminal of the resistor R27 and a second terminal of the capacitor C20 may be coupled to a cathode of a diode D13. An anode of the diode D13 may be coupled to a second terminal of the first primary winding of the transformer T2, to a first terminal of a capacitor C15 and to a drain of a transistor Q3.

[0037] An anode of the diode D8 may be coupled to a second terminal of the capacitor C15 and to first terminal of a second primary winding of the transformer T2. A drain of the transistor switch Q3 may be coupled to a first terminal of a resistor R31 and to a cathode of a Zener diode ZD1. A second terminal (designated with a "dot") of the second

primary winding of the transformer T2, a second terminal of the resistor R31 and an anode of the diode ZD1 may be coupled to the ground node.

[0038] The PWM switch control signal VSW1 may be coupled to base terminals of transistors Q6 and Q7. A supply voltage VCC may be coupled to a first terminal of a capacitor C34 and to a collector of the transistor Q6. An emitter of the transistor Q6 may be coupled to a first terminal of a resistor R28 and to a collector of the transistor Q7. A second terminal of the resistor 28 may be coupled to a gate of the transistor Q3 and to a first terminal of a resistor R29. A second terminal of the capacitor C34, a second terminal of the resistor R29 and an emitter of the transistor Q7 may be coupled to a ground node.

[0039] Thus, the transistor switch Q3 operates in accordance with the switch control signal VSW1. When the switch Q3 is closed, current is induced in the first and second primary windings of the transformer T2 which charges the primary windings with energy. When the switch Q3 is open, energy from the primary windings is discharged to first and second secondary windings of the transformer T2. Also during each switching cycle, the resistor R29, the diode D13 and capacitors C20, C15 function as a snubber to limit induced voltages at the primary windings of the transformer T2. As a result, the volt-second product applied to each primary winding of the transformer T2 tends to remain balanced for each phase of the switching cycle of the switch Q3. The arrangement of FIG. 4 operates similarly to that of FIG. 1 in that the PWM converter is substantially volt-second balanced. In other words the volt-second product during the discharging phase is at least as great as the volt-second product during the charging phase.

[0040] A first terminal (designated with a "dot") of the second secondary winding of the transformer T2 may be coupled to a first terminal of a capacitor C14 and to an anode of a diode D9A. A second terminal of the capacitor C14 may be coupled to a first terminal of a resistor R34. A second terminal of the resistor R34 may be coupled to a cathode of the diode D9A, to a cathode of a diode D9B, to a first terminal of an inductor L4 and to a first terminal of a resistor R35. A second terminal of the resistor R35 may be coupled to a first terminal of a capacitor C22. A second terminal of the first secondary winding of the transformer T2, an anode of the diode D9B and a second terminal of the capacitor C22 may be coupled to a ground node.

[0041] A second terminal of the inductor L4 may be coupled to a first terminal of a capacitor C17 and to a first terminal of an inductor L5. A second terminal of the inductor L5 may be coupled to a first terminal of a capacitor C18 and to a first terminal of a capacitor C19. A second terminal of the capacitors C17, C18 and C19 may be coupled to a ground node. The output voltage VDC of the PWM stage may be formed across the capacitors C18 and C19.

[0042] A first terminal (designated with a "dot") of the second secondary winding of the transformer T2 may be coupled to an anode of a diode D16. A cathode of the diode D16 may be coupled to a first terminal of a resistor R32A. A second terminal of the resistor R32A may be coupled to a first terminal of a capacitor C31, to a first terminal of a resistor R32 and to a first terminal of a resistor R33. A second terminal of the second secondary winding of the transformer T2 and a second terminal of the capacitor C31 may be coupled to a ground node. Second terminals of the resistors R32 and R33 may be coupled together. The supply voltage VDC may be formed at a second terminals of the resistors R32 and R33.

[0043] Thus, while the foregoing has been with reference to particular embodiments of the invention, it will be appreciated by those skilled in the art that changes in these embodiments may be made without departing from the principles and spirit of the invention, the scope of which is defined by the appended claims.

What is claimed is:

1. A two stage power converter comprising:

a power factor correction stage for forming an intermediate voltage; and

a pulse width modulation stage for receiving the intermediate voltage and for forming a DC output voltage wherein a duty cycle of the pulse width modulation stage is adjusted in response to a level of the intermediate voltage.

2. The power converter according to claim 1, wherein a periodic ramp signal formed for controlling timing of switching in the power factor correction stage is compared to a signal representative of the intermediate voltage for controlling a switch of the pulse width modulation stage.

3. The power converter according to claim 1, wherein the power factor correction stage comprises:

a first switch for modulating a first input current drawn from an alternating-current (AC) source; and

a power factor correction controller for controlling the first switch so as to maintain the first input current substantially in phase with an input voltage of the source and for forming the intermediate output voltage across a first energy storage element.

4. The power converter according to claim 3, wherein the power factor correction controller performs average current mode control.

5. The power converter according to claim 3, wherein the power factor correction controller performs input current shaping.

6. The power converter according to claim 1, wherein the pulse width modulation stage comprises:

means for forming an error signal that is representative of the intermediate output voltage and a desired level for the intermediate output voltage; and

means for comparing the error signal to a periodic ramp signal wherein an output of said means for comparing controls the duty cycle of the pulse width modulation stage.

7. The power converter according to claim 6, wherein switching in the pulse width modulation stage is synchronized with switching in the power factor correction stage.

8. The power converter according to claim 7, wherein the periodic ramp signal is synchronized with switching the power factor correction stage.

9. The power converter according to claim 1, wherein the pulse width modulation stage comprises an active clamping circuit.

10. The power converter according to claim 1, wherein the pulse width modulation stage is substantially volt-second balanced when the duty-cycle is less than 66.6 percent.

11. The power converter according to claim 1, wherein the pulse width modulation stage is substantially volt-second balanced for when the duty-cycle is fifty percent.

12. The power converter according to claim 1, further comprising a controller for controlling switching the power factor correction stage and in the pulse width modulation stage the controller being implemented as an integrated circuit and lacking a pin for monitoring the DC output voltage.

13. A controller for a two stage power converter comprising:

a power factor correction stage controller for controlling switching in a power factor correction stage of the power converter for forming an intermediate voltage; and

a pulse width modulation stage controller for monitoring the intermediate voltage and for adjusting a duty cycle of the pulse width modulation stage in response to a level of the intermediate voltage.

14. The controller according to claim 13, comprising means for comparing a periodic ramp signal formed for controlling timing of switching in the power factor correction stage to a signal representative of the intermediate voltage for controlling switching in the pulse width modulation stage.

15. The controller according to claim 13, wherein the power factor correction stage controller controls a first switch so as to maintain the first input current substantially in phase with an input voltage of the source and for forming the intermediate output voltage across a first energy storage element.

16. The controller according to claim 15, wherein the power factor correction controller performs average current mode control.

17. The controller according to claim 15, wherein the power factor correction controller performs input current shaping .

18. The controller according to claim 13, wherein the pulse width modulation stage comprises:

means for forming an error signal that is representative of the intermediate output voltage and a desired level for the intermediate output voltage; and

means for comparing the error signal to a periodic ramp signal wherein an output of said means for comparing controls the duty cycle of the pulse width modulation stage.

19. The controller according to claim 18, wherein switching in the pulse width modulation stage is synchronized with switching in the power factor correction stage.

20. The power converter according to claim 13, wherein the controller is implemented as an integrated circuit and lacking a pin for monitoring the DC output voltage.

21. A method for performing power conversion comprising:

modulating a first input current drawn from an alternating-current (AC) source with a first switch for maintaining the first input current substantially in phase with an input voltage of the source and for forming an intermediate output voltage across a first energy storage element; and

modulating a second input current from the first energy storage element for forming a DC output voltage across a second energy storage element, wherein a duty cycle for modulating the second input current is based on a level of the intermediate output voltage.

22. The method according to claim 21, further comprising:

forming a first error signal that is representative of a difference between the intermediate output voltage and a desired level for the intermediate output voltage; and

comparing the first error signal to a periodic ramp signal, wherein a result of said comparing controls the duty cycle for modulating the second input current.

23. The method according to claim 22, further comprising sensing a level of the first input current and the level of the intermediate output voltage for controlling a duty cycle for modulating the first input current.

24. The method according to claim 23, further comprising sensing a level of the input voltage for controlling the duty cycle of the first input current.

25. The method according to claim 23, further comprising:

forming a second error signal that is representative of a difference between the intermediate output voltage and a desired level for the intermediate output voltage;

integrating the second error signal thereby forming a signal that is representative of an integration of the second error signal; and

comparing the signal that is representative of an integration of the second error signal to a signal that is representative of the input current, wherein a result of said comparing controls the duty cycle for modulating the first input current.

26. The method according to claim 22, wherein said periodic ramp signal is synchronized with operation of the first switch.

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