(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 February 2013 (07.02.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/019284 A2

(51) International Patent Classification:
H02H 9/02 (2006.01)

(21) International Application Number:
PCT/US2012/027094

(22) International Filing Date:
29 February 2012 (29.02.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/194,386 29 July 2011 (29.07.2011) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) **Title**: CIRCUIT INTERRUPTER WITH IMPROVED SURGE SUPPRESSION

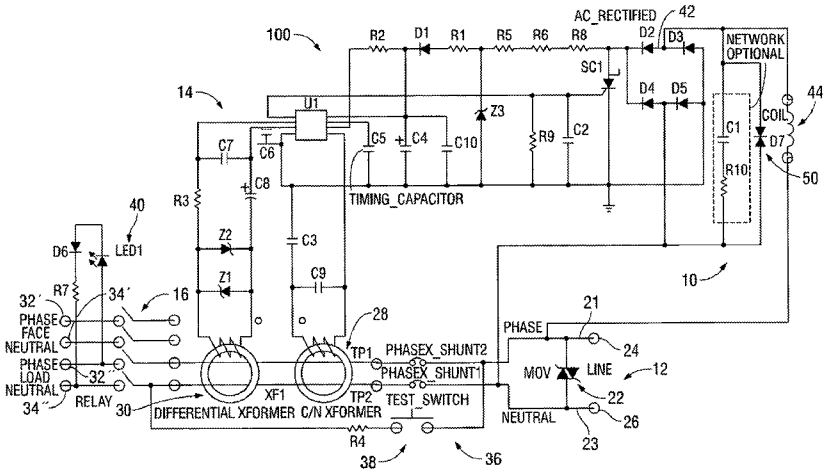


FIG. 1

(57) **Abstract**: A circuit interrupter, such as a GFCI or AFCI product, is provided having a suppression and protection circuit and circuit interrupter circuitry. In one configuration, a semiconductor device and a voltage clamping device or surge protector, such as a metal oxide varistor (MOV), are utilized in the circuit interrupter for handling transient surges and overvoltage conditions. The semiconductor device, such as a SIDCA and a TVS diode, is connected to a solenoid or trip coil of the circuit interrupter circuitry to limit the amount of current through the semiconductor device. The MOV is placed between phase and neutral conductors of the circuit interrupter circuitry.

WO 2013/019284 A2

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

CIRCUIT INTERRUPTER WITH IMPROVED SURGE SUPPRESSION

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to commonly owned application Ser. No. 11/079,557, filed Mar. 14, 2005, now U.S. Pat. No. 7,082,021, entitled Circuit Interrupter with Improved Surge Suppression, which is a continuation of application Ser. No. 09/829,339, filed Apr. 9, 2001, now U.S. Pat. No. 6,900,972, both of which are incorporated herein in their entirety by reference. This application is also related to the patent applications which are related to U.S. Pat. No. 7,082,021 and identified therein. These applications are the following:

This application is related to commonly owned application Ser. No. 09/812,288, filed Mar. 20, 2001, now U.S. Pat. No. 7,049,910, entitled Circuit Interrupting Device with Reset Lockout and Reverse Wiring Protection and Method of Manufacture, which is a continuation-in-part of application Ser. No. 09/379,138 filed Aug. 20, 1999, now U.S. Pat. No. 6,246,558, which is a continuation-in-part of application Ser. No. 09/369,759 filed Aug. 6, 1999, now U.S. Pat. No. 6,282,070, which is a continuation-in-part of application Ser. No. 09/138,955, filed Aug. 24, 1998, now U.S. Pat. No. 6,040,967, all of which are incorporated herein in their entirety by reference.

This application is related to commonly owned application Ser. No. 09/812,875, filed Mar. 20, 2001, now U.S. Pat. No. 7,031,125, entitled Reset Lockout for Sliding Latch GFCI, which is a continuation-in-part of application Ser. No. 09/688,481 filed Oct. 16, 2000, now U.S. Pat. No. 6,437,700, both of which are incorporated herein in their

entirety by reference.

This application is related to commonly owned application Ser. No. 09/813,683, filed Mar. 21, 2001, now U.S. Pat. No. 6,693,779, entitled IDCI With Reset Lockout and Independent Trip, herein incorporated in its entirety by reference.

This application is related to commonly owned application Ser. No. 09/812,601, filed Mar. 20, 2001, now abandoned, entitled Neutral Switch Test Mechanism for a Circuit Interrupter, herein incorporated in its entirety by reference.

FIELD OF THE INVENTION

The present invention relates to surge suppression, and in particular to circuit interrupters, such as ground fault circuit interrupters (GFCI), arc fault circuit interrupters (AFCI) and related products with enhanced transient suppression and protection characteristics.

BACKGROUND OF THE INVENTION

Circuit interrupters, such as GFCI and AFCI, are electronic devices connected to power lines. They require having protection against surges known to "travel" in power lines. UL 943 standard for GFCIs and UL 1699 for AFCIs require these devices to pass unwanted tripping tests for combination waveform and surge immunity tests at levels of 2kV(1kA), 4kV(2kA) and 6kV(3kA).

To protect circuit interrupting electronic devices against the power line surge, it is commonly known to use MOV (metal oxide varistors) devices. MOV devices are

capable of clamping voltage at a predetermined level and dissipating surge energy up to another predetermined level.

Known circuit interrupting products typically include an MOV positioned across the power lines of the circuit interrupting product, with the MOV providing some surge protection to the circuit interrupting product circuitry by clamping transient voltages to acceptable levels.

An MOV is typically a non-linear resistance that has a very high resistance below its threshold voltage and is typically modeled as an open circuit. At voltages above the threshold voltage, the resistance is nearly zero and the voltage above the threshold is dissipated. The amount of energy that an MOV dissipates is generally related to the size of the device, typically a disc or 9, 10, 14, 20, or 40 mm or the like. A larger MOV typically dissipates more energy, but takes up more space, may be more costly and may require more open space around the device.

The nature of the clamping and the amount of energy that may be dissipated is determined by the size of the disc and voltage rating associated with a disc type MOV. Heretofore, GFCI/AFCI and other circuit interrupting products have typically been limited to handling transient voltages of 6 kV at 3000 A.

When overvoltage conditions occur, protection components such as the MOV in the typical GFCI and AFCI may not survive, if they are selected to only operate under 120V conditions. For example, a MOV in the typical GFCI operating beyond its rating at overvoltage may disintegrate, and thus such conditions may also destroy the rest of the electronics in the GFCI product and possibly cause a fire. Furthermore, an MOV may

fail by rupturing, exploding or igniting. Such failure conditions are potentially dangerous.

Due to the requirements of circuit protection products withstanding abnormal overvoltage conditions, 120V devices cannot use MOV rated below 230V-240V. In the event of surge pulses, such devices cannot clamp voltage fast enough so the peak voltage during surge can reach 600V-800V which may cause electronic components of the devices to malfunction or the device may trip which is undesired. For this reason, additional protection is needed to better protect GFCI/AFCI and other circuit interrupting devices and satisfy UL standard requirements.

SUMMARY OF THE INVENTION

Accordingly, in view of the discussion above, there exists a need for a surge protection circuit which allows components such as a surge protector or voltage clamping device to survive power conditions exceeding voltage and current ratings, and thus enabling a circuit interrupting product, such as a ground fault circuit interrupter (GFCI) or arc fault circuit interrupter (AFCI) product to survive overvoltage conditions.

A suppression and protection circuit is used in conjunction with circuit interrupter circuitry, such as circuitry in a GFCI or AFCI product. In embodiments described herein, a surge protector or voltage clamping device, such as a metal oxide varistor (MOV), is utilized in the circuit interrupting product for handling transient surges and overvoltage conditions. In embodiments described herein, the circuit interrupting product further includes the use of a semiconductor protection device in addition to MOV.

In embodiments described herein, the semiconductor device is preferably either a TVS diode or a SIDAC (Silicon Diode for Alternating Current) marketed, for example, under the names SIDACtor, Transil or TSPD. To work properly these semiconductor devices (in difference to MOV) require to be in series with a current limiting component to limit possible current through them. The present disclosure provides embodiments where a TVS or SIDAC is used with the solenoid or trip coil of the GFCI as the current limiting component.

Nominal voltage for both TVS and SIDACs has to be selected to be above (or close to maximum) peak voltage applied to the circuit interrupter during abnormal overvoltage. Therefore, TVS or SIDAC devices with nominal voltage of 350V/400V are preferable. Additionally, because of the nature of TVS and SIDAC devices of clamping voltage faster than MOV and because current through these devices is limited by the trip coil of the GFCI, the maximum voltage applied to the device electronics is limited to 400V-500V (depending on the semiconductor device used).

A preferred TVS diode for protection of a circuit interrupter, such as a GFCI product, is the SMBJ350CA manufactured by Littelfuse, Inc., Chicago, Illinois. A preferred SIDAC for protection of a circuit interrupter is the SIDACtor P350SCMCLRP also manufactured by Littelfuse, Inc.

In particular, in one embodiment according to the present disclosure, there is provided a circuit interrupter having a housing; at least one input conductor disposed at least partially within the housing and capable of being electrically connected to a source of electricity; at least one output conductor disposed within the housing and capable of

conducting electrical current to a load when electrically connected to said at least one input conductor; and circuit interrupter circuitry disposed within the housing and configured to break the electrical connection between the input and output conductors in response to the occurrence of a ground fault or test cycle. The circuit interrupter circuitry includes a solenoid coil. The circuit interrupter further has a surge protection circuit having a semiconductor device for reducing surge voltage applied to the circuit interrupter circuitry. The solenoid coil limits the current through the semiconductor device.

In an alternate embodiment, the circuit interrupter includes a reset mechanism is provided and is configured to reset the electrical connection between the input and output conductors when the reset mechanism is activated.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a schematic diagram of a GFCI circuit having a suppression and protection circuit and a TVS diode according to a first embodiment of the present disclosure;

FIG. 2 illustrates a schematic diagram of a GFCI circuit having a suppression and protection circuit and a SIDAC according to a second embodiment of the present disclosure;

FIG. 3 illustrates a schematic diagram of a GFCI circuit having a suppression and protection circuit and a TVS diode according to a third embodiment of the present disclosure; and

FIG. 4 illustrates a schematic diagram of a GFCI circuit having a suppression and protection circuit and a SIDAC according to a fourth embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A circuit interrupter having improved transient and overvoltage suppression is described. The commonly owned U.S. patents referred to above describe circuit interrupting devices and are incorporated herein in their entirety by reference. For example, U.S. Pat. No. 7,049,910 describes a circuit interrupting device having a reset mechanism with a reset lockout portion. The reset lockout portion prevents the reestablishing of electrical continuity in open conductive paths if the circuit interrupting portion is non-operational, if an open neutral condition exists or if the device is reverse wired. The circuit interrupter can be a GFCI and/or other related product having a circuit interrupter, such as an AFCI and a fuse, event though the present disclosure refers mainly to a GFCI product.

The GFCI and/or related products, such as an AFCI, in accordance with the present disclosure include a suppression and protection circuit which interfaces between power inputs and a ground fault circuit interrupter (GFCI) circuit connected to a load. The GFCI and/or related products can also include a reset mechanism with a reset lockout portion. The suppression and protection circuit providing enhanced suppression of transient surges for the circuit interrupter as well as protection from overvoltage conditions, while the circuit interrupter is operational. The suppression and protection circuit 10 includes an overvoltage prevention circuit having a surge protector or voltage clamping device, such as a metal oxide varistor (MOV), and a semiconductor protection device, such as, for example, a TVS diode or a SIDAC (Silicon Diode for Alternating Current) marketed, for example, under the names SIDACtor, Transil or TSPD. The

suppression and protection circuit is described in greater detail with reference to embodiments shown by FIGs. 1-4.

FIG. 1 illustrates one example embodiment of the suppression and protection circuit 10 and an interrupter or GFCI circuit 14 forming a GFCI product 100. The circuit 10 includes an MOV 22 positioned between input power lines as the power inputs 12, for example, an alternating current (AC) line connection having a phase line 24 and a neutral line 26. The lines 24, 26 are connected to phase line and neutral line conductors 21, 23 of the GFCI 100.

The lines 24, 26 are also connected through the MOV 22 and through a ground neutral transformer 28 and a differential or sensing transformer 30 to the load 16, which may include two phase load connections 32' and 32" and two neutral load connections 34' and 34". A test line 36 may also be provided in a manner known in the art including, for example, a test switch 38 and a resistor R4 having a 15 KOhms resistance. Optionally, a relay 40 and/or circuit breaker known in the art may be provided, as further described herein, connecting the differential transformer 30 to the load lines 32', 32", 34' and 34".

A processor U1 of the GFCI circuit 14 is connected via a plurality of pins or connectors to the transformers 28, 30 in a manner known in the art, for example, using capacitors C3 and C6-C9, resistor R4, and diodes Z1, Z2. In the example embodiment shown in FIG. 1, the resistor R3 has a 100 ohm resistance, and the capacitors C3 and C6-C9 have capacitances of 0.01μF, 100pF, 0.0033μF, 10μF, and 100pF, respectively, each having a voltage rating of 50 V, except for the capacitor C8 having a voltage rating of 6.3

V.

The processor U1 may be, for example, a model LM1851 ground fault interrupter controller commercially available from "NATIONAL SEMICONDUCTOR", capable of providing ground fault protection for AC power outlets in consumer and industrial environments. The processor U1 is also connected via its pins/connectors to the MOV 22 in a manner known in the art, for example, using capacitors C10, C4 and C5 having capacitances of 0.01μF, 1μF, and 0.018μF, respectively, at 50 V; a capacitor C2 having a 680pF capacitance at 500 V; resistors R1 and R2 having 15 kohms and 2Mohms resistances, respectively; a diode D1; a rectifier SC1 such as a silicon controlled rectifier (SCR); and a set of diodes D2-D5 forming a bridge diode circuit or configuration 42, as shown in FIG. 1.

The circuit 10 further includes a semiconductor protection device 50, such as a SIDAC D7 shown in FIG. 1 connected to the bridge diode circuit 42 and to the neutral line 26. An optional snubber circuit (C1, R10) 52 may be connected in parallel to the semiconductor protection device 50. The snubber circuit 52 can be used in addition to the described protection device 50 to improve the noise immunity by eliminating noise.

In the example embodiment shown by FIG. 1, the MOV 22 and the semiconductor protection device 50 are connected to an inductor 44. The inductor 44 may be a solenoid coil or bobbin acting as a trip coil, such that the inductor 44 also functions as an actuator to disengage the relay mechanism 40 on the load side. More specifically, the MOV 22 provides primary protection against overvoltage conditions on

the power line and the semiconductor protection device 50 provides secondary and faster protection. The inductor 44 or trip coil is used as a voltage dropping component or

resistive component which is necessary for operation of the semiconductor protection device 50.

In the embodiment shown in FIG. 1, the MOV 22 clamps the voltage exposed to the capacitor C1 to be within the voltage rating of the capacitor C1, for example, 400 V. As in the prior art, the MOV 22 itself in a GFCI product is capable of handling transient surges and overvoltage conditions of, for example, less than 2-6 kV at 3 kA surge. Using the semiconductor protection device 50 in the disclosed suppression and protection circuit 10, transient voltages exceeding, for example, 2 kV at 3 kA and even 6 kV at 3 kA, are suppressed. Accordingly, the MOV 22 in the GFCI product is capable of handling voltages exceeding a root-mean-square (RMS) voltage rating of the MOV 22, permitting the MOV 22 to survive and provide primary protection from other transient, surge, and overvoltage conditions, as described herein.

During operation, the MOV 22 performs the functions of clamping and passing surge current through its terminals, thereby protecting the rest of the circuit interrupter circuitry. However, the MOV 22 reacts too slowly to the overvoltage condition compared to the semiconductor protection device 50. Therefore, at the beginning of the surge pulse, the voltage applied to the circuit interrupter circuitry may reach 800V or more causing the destruction of the GFCI product without the use of the device 50. The semiconductor protection device 50 provides secondary protection to prevent the destruction of the GFCI product. The device 50 performs the function of clamping the excess voltage much faster compared with the MOV 22, such that the GFCI product gets exposed voltage drops below 400-500V. The inductor 44 or trip coil is used as a resistive

component to perform the functions of dropping the excess voltage and limiting current through the semiconductor protection device 50. In this manner, the surge suppression and overvoltage protection of a GFCI product which includes the circuit 10 and the GFCI circuit 14 is significantly improved.

Referring to FIGS. 2-4, other sample embodiments of other GFCI products in accordance with the present disclosure are described. The operation and functions of the MOVs 22', 22" and 22"' and the operation and functions of the semiconductor protection devices 50', 50" and 50"' are similar, if not identical, to the operation and functions of the MOV 22 and semiconductor protection device 50, respectively. In FIG. 2, the GFCI product 100' is similar to the GFCI product 100 except for including a TVS D7' as the semiconductor protection device 50'. The MOV 22' is a variable resistance that may have an effect as voltage changes.

In FIG. 3, as in the first embodiment shown by FIG. 1, the GFCI product 100" includes a semiconductor protection device 50" which is a SIDAC D7". The device 50" is connected to the bridge diode circuit 42 and to ground. The MOV 22" is a variable resistance that may have an effect as voltage changes.

In FIG. 4, as in the second embodiment shown by FIG. 2, the semiconductor protection device 50"' is a TVS D7"'. The device 50"' is connected to the bridge diode circuit 42 and to ground. The MOV 22"' is a variable resistance that may have an effect as voltage changes.

TVS diodes and SIDAC are manufactured in small SMT packages (SMA (400W) and SMB (600W)). This allows MOV miniaturization to create semiconductor protection devices in small housings capable of fitting into a standard wall box.

Voltage clamping devices include without limitation selenium cells, Zener diodes, silicon carbide varistors and metal oxide varistors (MOVs).

Additionally, it is known in the art to provide a visual indication that a device equipped with surge suppression is still operating with surge suppression capability. In an embodiment of the present invention, a visual indicator is provided to indicate that the device is operating with adequate surge suppression capability. Similarly, an alarm such as an audio indicator may be provided to indicate that the device is no longer operating with adequate surge suppression capabilities.

While there have been shown and described and pointed out the fundamental features of the invention, it will be understood that various omissions and substitutions and changes of the form and details of the device described and illustrated and in its operation may be made by those skilled in the art, without departing from the spirit of the invention.

What is claimed is:

1. A circuit interrupter comprising:

a housing;

at least one input conductor disposed at least partially within said housing and capable of being electrically connected to a source of electricity;

at least one output conductor disposed within said housing and capable of conducting electrical current to a load when electrically connected to said at least one input conductor;

circuit interrupter circuitry disposed within said housing and configured to break said electrical connection between said input and output conductors in response to the occurrence of a fault or test cycle, said circuit interrupter circuitry including a solenoid coil;

a reset mechanism configured to reset said electrical connection between said input and output conductors when said reset mechanism is activated; and

a surge protection circuit comprising a semiconductor device for reducing surge voltage applied to said circuit interrupter circuitry, wherein said solenoid coil limits the current through said semiconductor device.

2. The circuit interrupter of claim 1, wherein the surge protection circuit further comprising a surge protector coupled between phase and neutral conductors of the circuit interrupter.

3. The circuit interrupter of claim 2, wherein the surge protector coupled between phase and neutral conductors of the circuit interrupter comprises a metal oxide varistor (MOV) to shunt over voltage between the phase and neutral conductors.

4. The circuit interrupter of claim 1, wherein the semiconductor device is selected from the group consisting of a SIDAC and a TVS diode.

5. The circuit interrupter of claim 1, wherein the semiconductor device is connected directly to the solenoid coil.

6. The circuit interrupter of claim 1, wherein the semiconductor device is connected to the solenoid coil via a bridge diode circuit, and wherein the solenoid coil is a trip coil functioning as a voltage dropping component.

7. The circuit interrupter of claim 1, wherein the semiconductor device is connected to the neutral conductor of the circuit interrupter.

8. The circuit interrupter of claim 1, wherein the semiconductor device is connected in parallel to an RC circuit for improving noise elimination.

9. The circuit interrupter of claim 1, wherein the circuit interrupter is selected from the group consisting of a GFCI, an AFCI, and a fuse.

10. The circuit interrupter of claim 1, wherein said reset mechanism has a reset lock-out responsive to the activation of said circuit interrupter so as to be movable between a lock-out position wherein said reset lock-out inhibits resetting of said electrical connection between said input and output conductors and a reset position wherein said reset lock-out does not inhibit resetting of said electrical connection between said input and output conductors, wherein when said reset mechanism is activated said circuit interrupter is activated to facilitate movement of said reset lock-out from said lock-out position to said reset position by said reset mechanism and resets said electrical connection between said input and output conductors.

11. The circuit interrupter of claim 1, wherein the fault is one of a ground fault and an arc fault.

12. A circuit interrupter comprising:

a housing;

at least one input conductor disposed at least partially within said housing and capable of being electrically connected to a source of electricity;

at least one output conductor disposed within said housing and capable of conducting electrical current to a load when electrically connected to said at least one input conductor;

circuit interrupter circuitry disposed within said housing and configured to break said electrical connection between said input and output conductors in response to the occurrence of a fault or test cycle, said circuit interrupter circuitry including a solenoid coil; and

a surge protection circuit comprising a semiconductor device for reducing surge voltage applied to said circuit interrupter circuitry, wherein said solenoid coil of the circuit interrupter circuitry limits the current through said semiconductor device.

13. The circuit interrupter of claim 12, wherein the surge protection circuit further comprising a surge protector coupled between phase and neutral conductors of the circuit interrupter.

14. The circuit interrupter of claim 13, wherein the surge protector coupled between phase and neutral conductors of the circuit interrupter comprises a metal oxide varistor (MOV) to shunt over voltage between the phase and neutral conductors.

15. The circuit interrupter of claim 12, wherein the semiconductor device is selected from the group consisting of a SIDAC and a TVS diode.

16. The circuit interrupter of claim 12, wherein the semiconductor device is connected directly to the solenoid coil, and wherein the solenoid coil is a trip coil functioning as a voltage dropping component.

17. The circuit interrupter of claim 12, wherein the semiconductor device is connected to the solenoid coil via a bridge diode circuit.

18. The circuit interrupter of claim 12, wherein the semiconductor device is connected to the neutral conductor of the circuit interrupter.

19. The circuit interrupter of claim 12, wherein the semiconductor device is connected in parallel to an RC circuit for improving noise elimination.

20. The circuit interrupter of claim 12, wherein the circuit interrupter is selected from the group consisting of a GFCI, an AFCI, and a fuse.

21. The circuit interrupter of claim 12, wherein the fault is one of a ground fault and an arc fault.

22. A method for protecting a circuit interrupter during an over voltage condition, said method comprising:

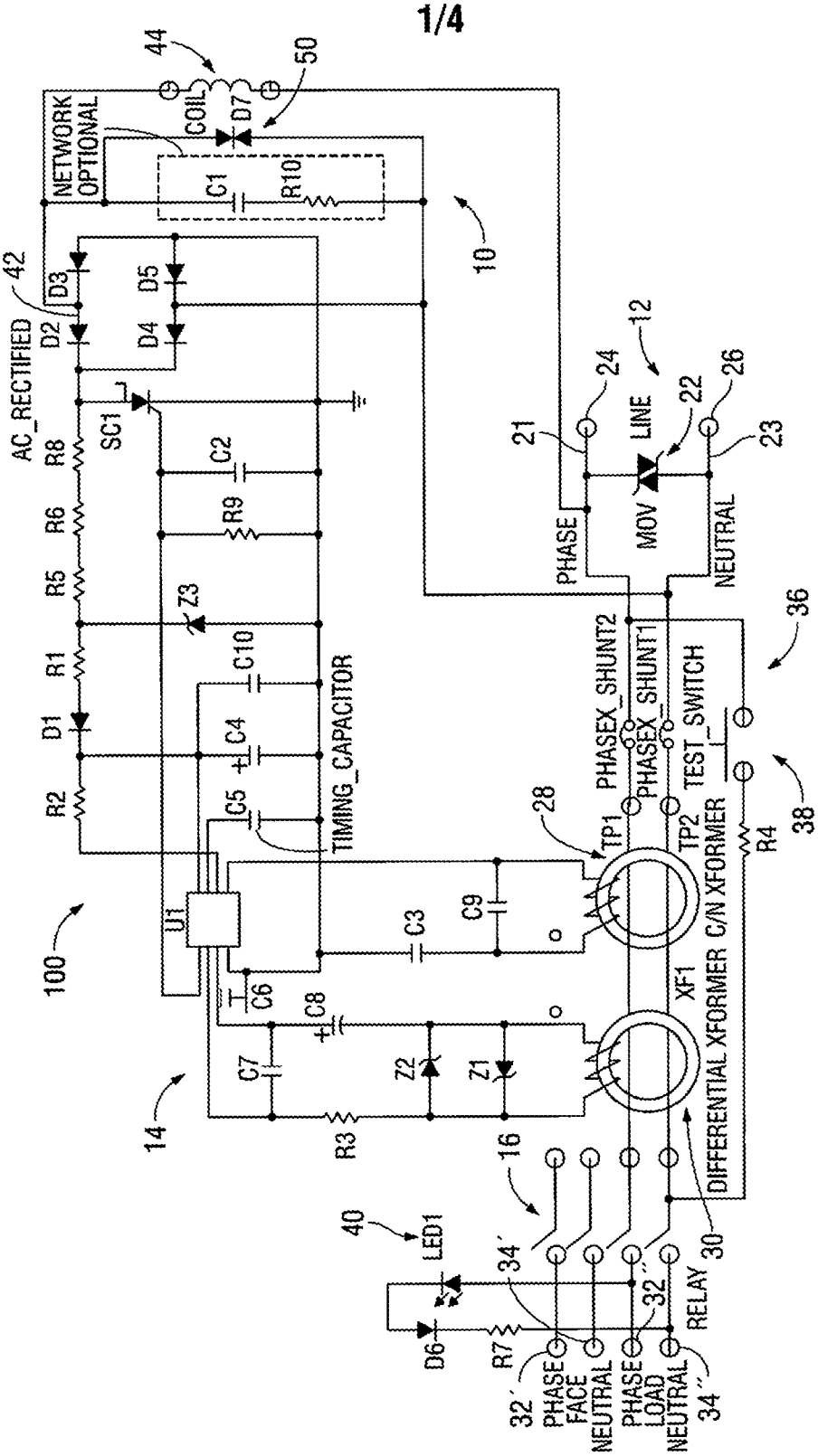
connecting a semiconductor device to a solenoid coil of the circuit interrupter to pass low frequency voltage signals to the circuit interrupter while blocking high frequency signals; and

coupling a surge protector between phase and neutral conductors of the circuit interrupter to shunt over voltage between the phase and neutral conductors.

23. The method of claim 22, wherein the semiconductor device is selected from the group consisting of a SIDAC and a TVS diode.

24. The method of claim 22, wherein the surge protector is a metal oxide varistor (MOV).

25. The method of claim 22, wherein the circuit interrupter is selected from the group consisting of a GFCI, an AFCI, and a fuse.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PHASEX_SHUNT1
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FIG. 1

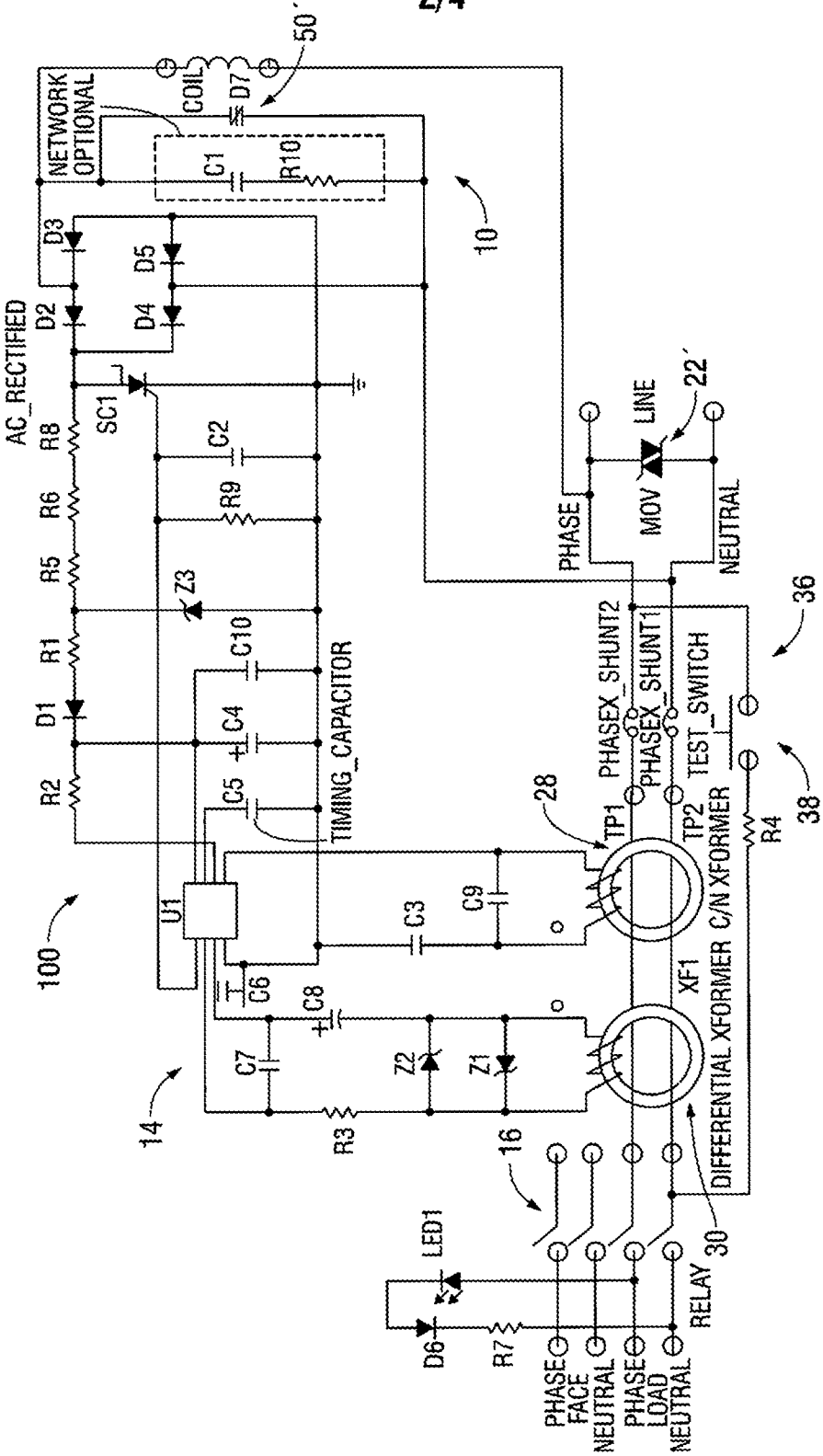
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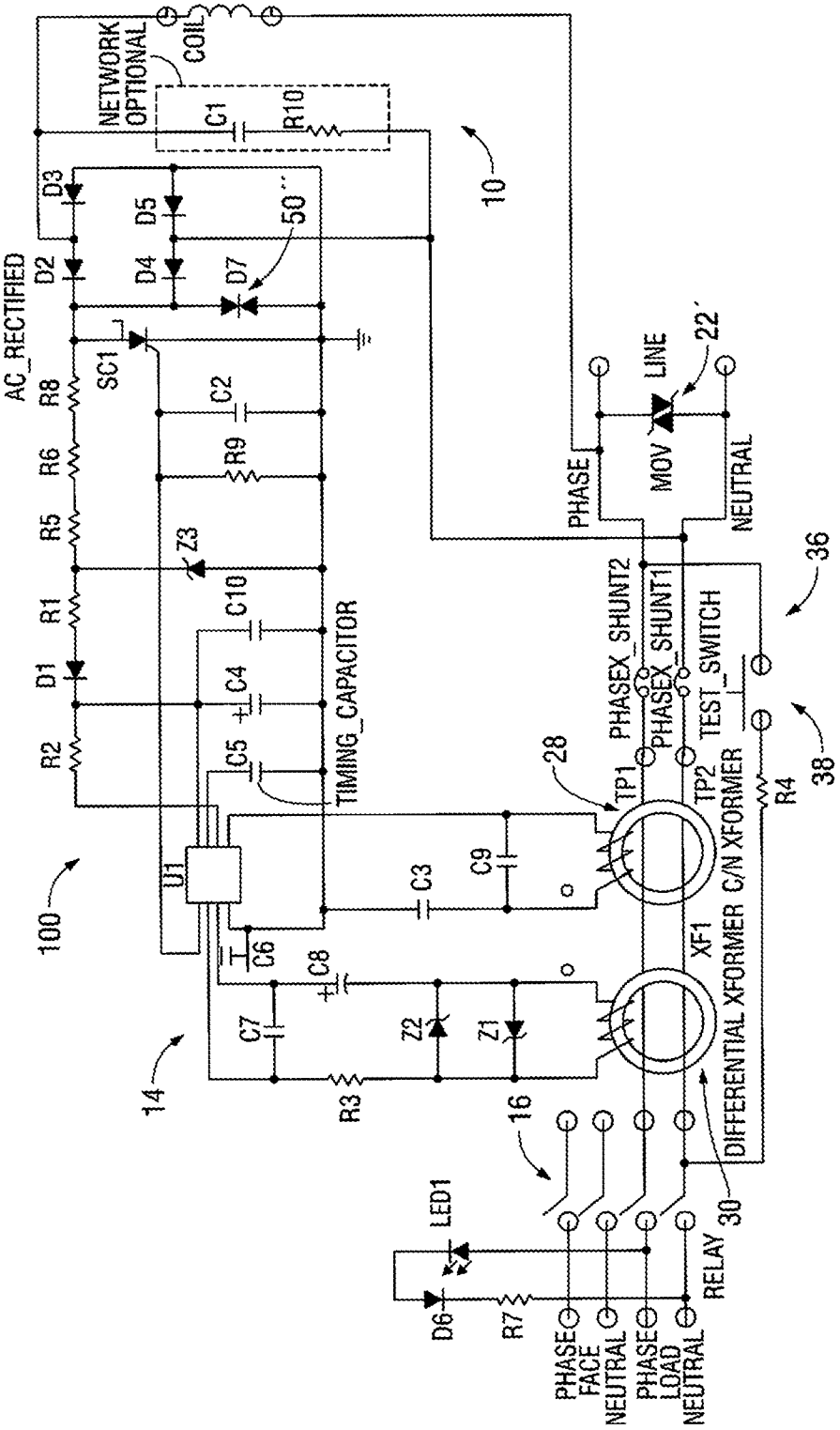
FIG. 2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RELAY
30
DIFFERENTIAL XFORMER C/N
XF1
TP1
TP2
PHASEX_SHUNT2
PHASEX_SHUNT1
TEST_SWITCH
R4
38
36
PHASE
MOV
LINE
22'
NEUTRAL

FIG. 3

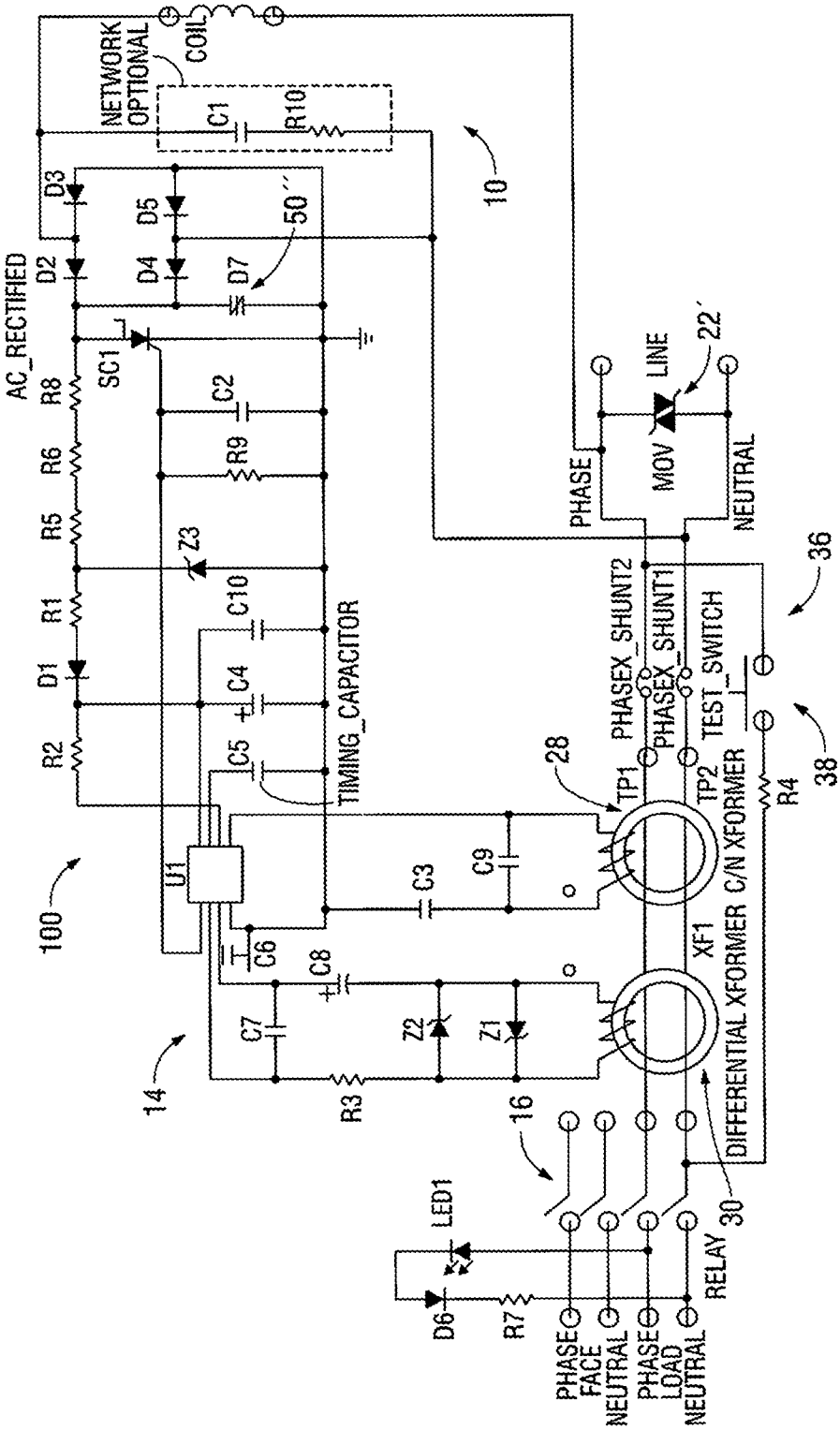
NETWORK OPTIONAL
COIL
C1
R10
D3
D5
50''
D2
D4
D7
10
AC_RECTIFIED
SC1
R8
C2
R6
R9
R5
Z3
R1
C10
D1
C4
R2
C5
TIMING_CAPACITOR
U1
100
C3
C9
C6
C8
C7
Z2
Z1
R3
14
16
LED1
D6
R7
PHASE FACE NEUTRAL
PHASE LOAD NEUTRAL
RELAY
30
DIFFERENTIAL XFORMER C/N XFORMER
XF1
28
TP1
TP2
PHASEX_SHUNT2
PHASEX_SHUNT1
TEST_SWITCH
R4
38
36
PHASE
MOV
LINE
22'
NEUTRAL

FIG. 4