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(54) TECHNIQUES TO TRANSMIT COMMANDS TO A TARGET DEVICE

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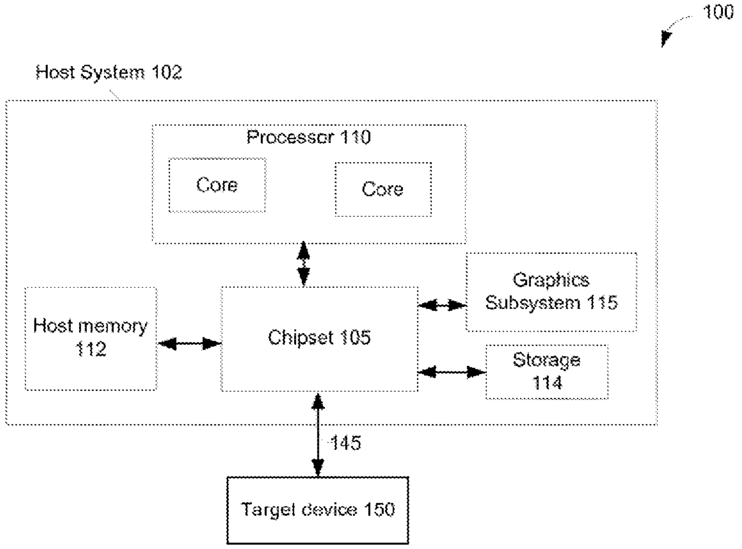
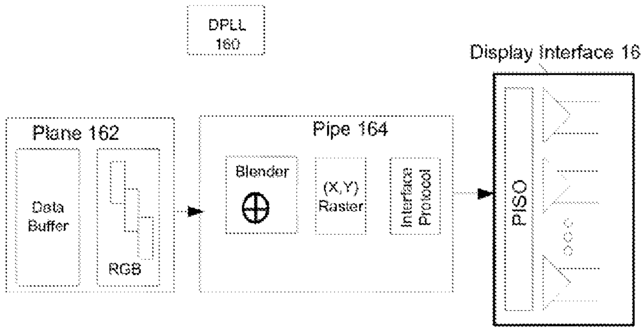
(57) ABSTRACT

Techniques are described to transmit commands to a display device. The commands can be transmitted in header byte fields of secondary data packets. The commands can be used to cause a target device to capture a frame, enter or exit self refresh mode, or reduce power use of a connection. In addition, a request to exit main link standby mode can cause the target enter training mode without explicit command to exit main link standby mode.





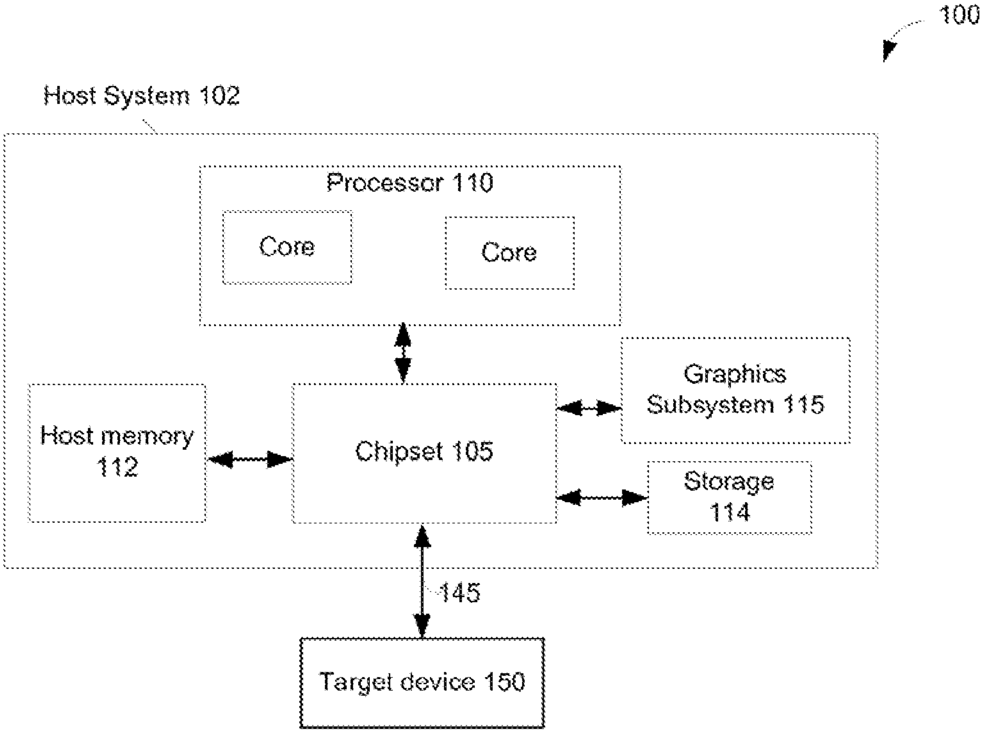

100
Host System 102
Processor 110
Core
Core
Graphics Subsystem 115
Host memory 112
Chipset 105
Storage 114
145
Target device 150

FIG. 1A

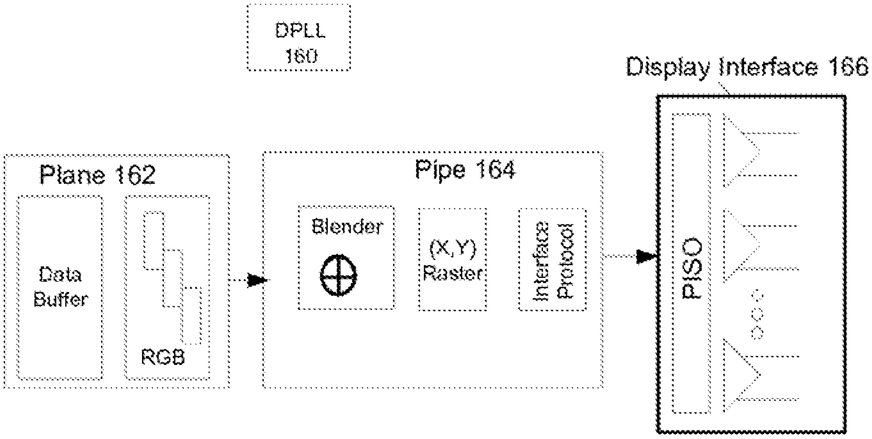

DPLL 160
Display Interface 166
Plane 162
Data Buffer
RGB
Pipe 164
Blender
(X,Y) Raster
Interface Protocol
PISO

FIG. 1B

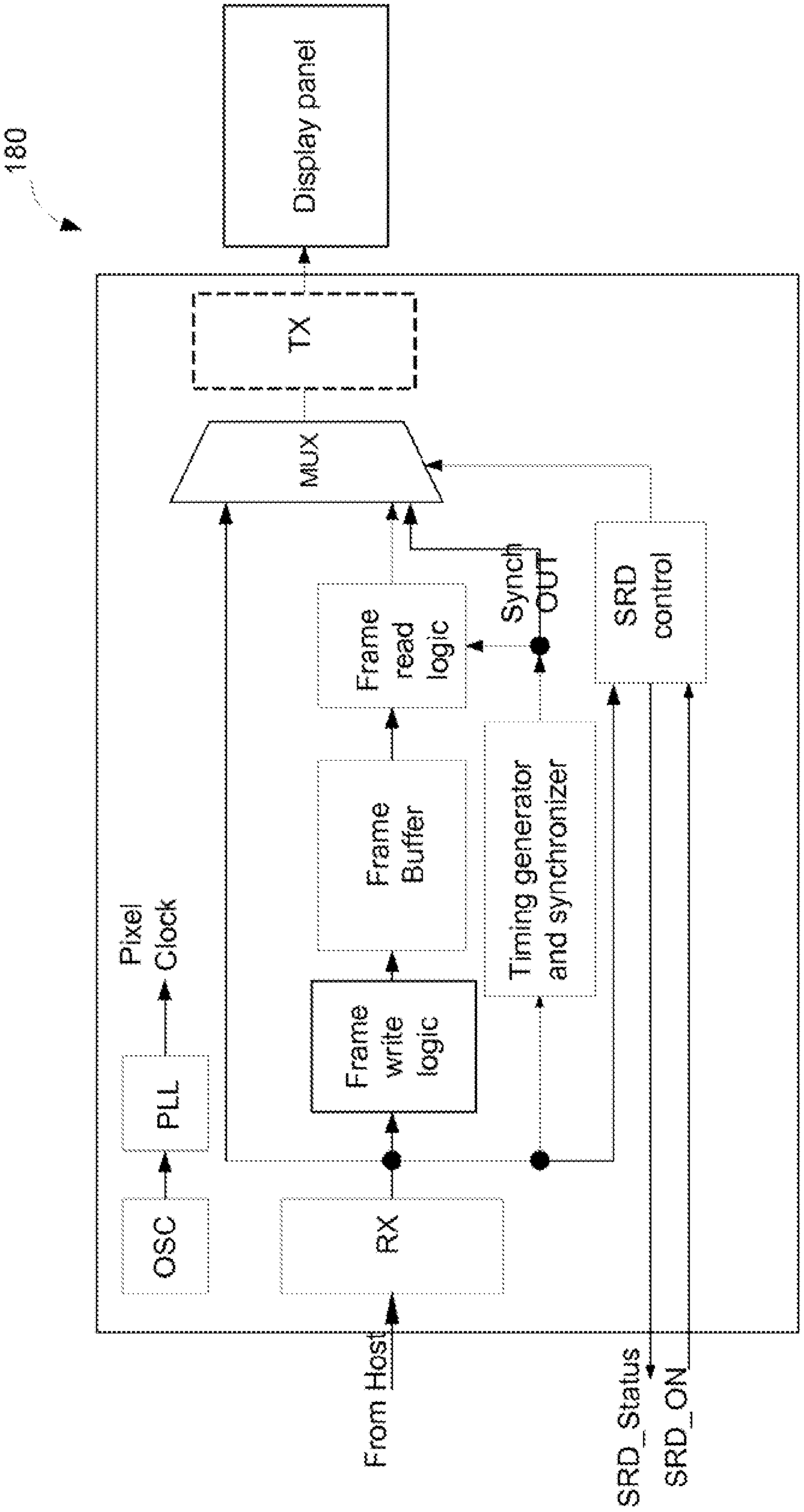

180
Display panel
TX
MUX
Synch OUT
SRD control
Frame read logic
Frame Buffer
Timing generator and synchronizer
Frame write logic
Pixel Clock
PLL
OSC
RX
From Host
SRD_Status
SRD_ON

FIG. 1C

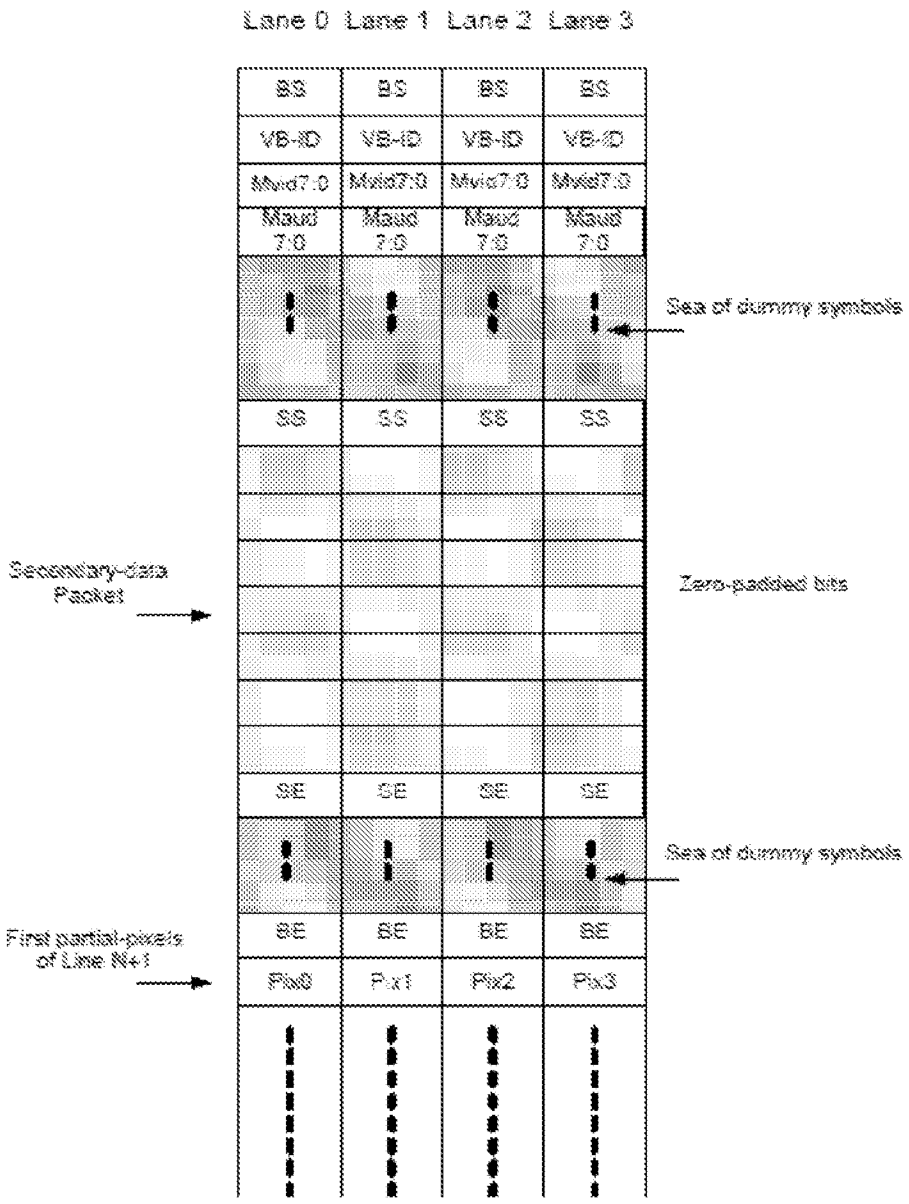
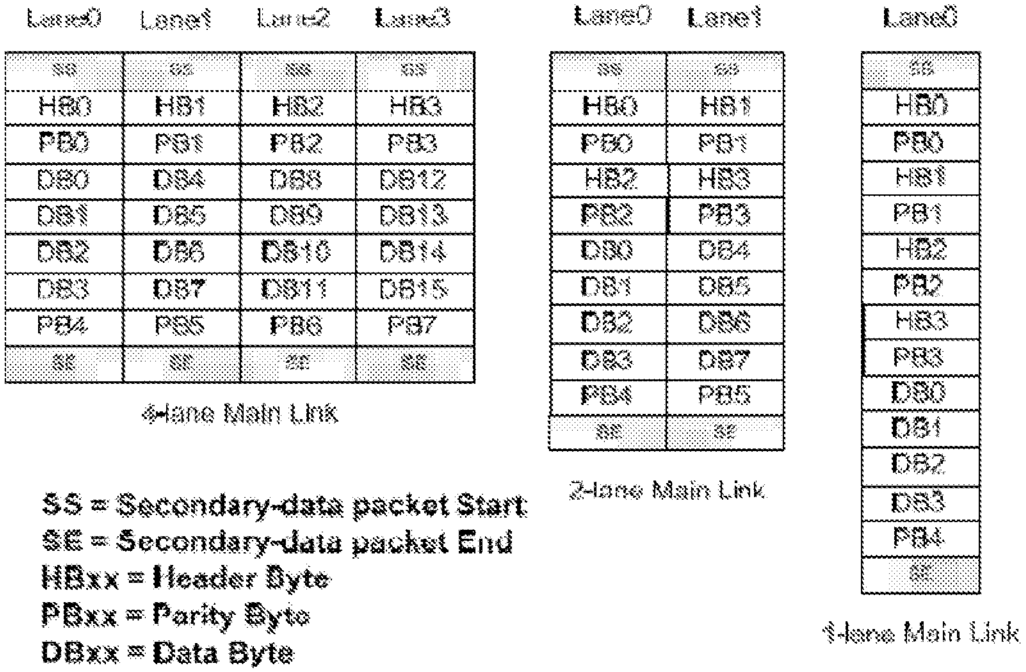


Figure 2-14: Secondary Data Insertion

FIG. 2



Lane0	Lane1	Lane2	Lane3
SS	SS	SS	SS
HB0	HB1	HB2	HB3
PB0	PB1	PB2	PB3
DB0	DB4	DB8	DB12
DB1	DB5	DB9	DB13
DB2	DB6	DB10	DB14
DB3	DB7	DB11	DB15
PB4	PB5	PB6	PB7
SE	SE	SE	SE

4-lane Main Link

Lane0	Lane1
SS	SS
HB0	HB1
PB0	PB1
HB2	HB3
PB2	PB3
DB0	DB4
DB1	DB5
DB2	DB6
DB3	DB7
PB4	PB5
SE	SE

2-lane Main Link

Lane0
SS
HB0
PB0
HB1
PB1
HB2
PB2
HB3
PB3
DB0
DB1
DB2
DB3
PB4
SE

1-lane Main Link

SS = Secondary-data packet Start
SE = Secondary-data packet End
HBxx = Header Byte
PBxx = Parity Byte
DBxx = Data Byte

Figure 2-24: Extension Packet Mapping over the Main Link

FIG. 3

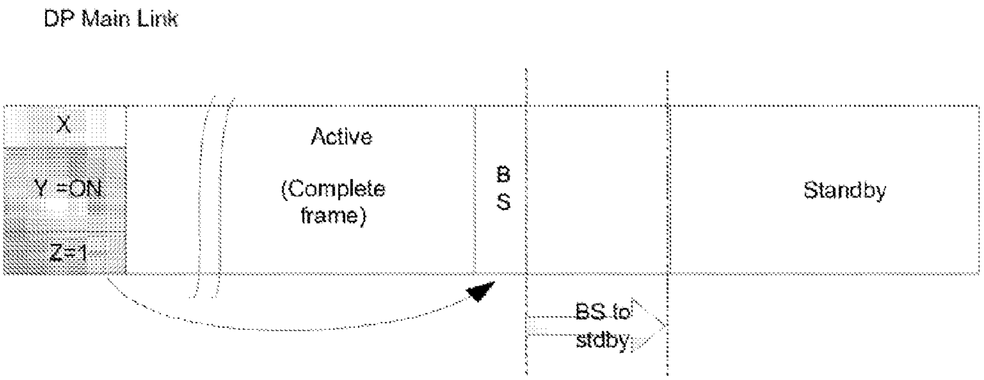

DP Main Link
X
Y =ON
Z=1
Active
(Complete frame)
B S
Standby
BS to stdby

FIG. 4

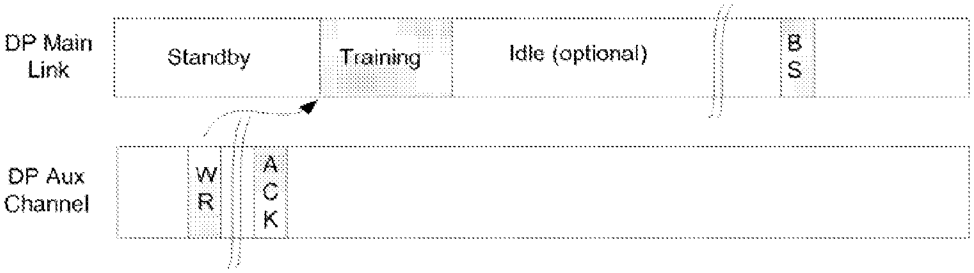

DP Main Link
Standby
Training
Idle (optional)
B S
DP Aux Channel
W R
A C K

FIG. 5

TECHNIQUES TO TRANSMIT COMMANDS TO A TARGET DEVICE

RELATED APPLICATION

[0001] This application is a continuation of U.S. application Ser. No. 12/890,217, entitled "TECHNIQUES TO TRANSMIT COMMANDS TO A TARGET DEVICE" filed Sep. 24, 2010 which is related to co-pending U.S. patent application serial number 12/286,192, entitled "Protocol Extensions in a Display Port Compatible Interface," inventors Kwa et al., filed Sep. 29, 2008, now patented as U.S. Pat. No. 7,961,656 issued on Jun. 14, 2011 (attorney docket number P27579).

FIELD

[0002] The subject matter disclosed herein relates generally to techniques for regulating power consumption.

RELATED ART

[0003] Multimedia operations in computer systems are very common. For example, personal computers are often used to process and display video. Power consumption by computers is a concern. It is desirable to regulate power consumption by personal computers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the drawings and in which like reference numerals refer to similar elements.

[0005] FIG. **1**A depicts a system in accordance with an embodiment.

[0006] FIG. **1**B depicts an example of components of a host system whose power consumption can be controlled, in accordance with an embodiment.

[0007] FIG. **1**C depicts a high level block diagram of a timing controller for a display device in accordance with an embodiment.

[0008] FIG. **2** depicts an example format of signals transmitted over multiple lanes of a DisplayPort interface.

[0009] FIG. **3** depicts an example manner of communication of secondary data packets over one and more lanes of a DisplayPort interface.

[0010] FIG. **4** depicts an example of a sequence of events for entry into main link standby mode.

[0011] FIG. **5** depicts an example of a sequence of events for exit from main link standby mode.

DETAILED DESCRIPTION

[0012] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrase "in one embodiment" or "an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in one or more embodiments.

[0013] FIG. **1**A depicts a system **100** in accordance with an embodiment. System **100** may include a source device such as a host system **102** and a target device **150**. Host system **102** may include a processor **110** with one or more cores, host memory **112**, storage **114**, and graphics subsystem **115**. Chipset **105** may communicatively couple devices in host system **102**. Graphics subsystem **115** may process video and audio. System **100** can be implemented in a handheld personal computer, mobile telephone, set top box, or any computing device. Any type of user interface is available such as a keypad, mouse, and/or touch screen.

[0014] In accordance with various embodiments, processor **110** may execute a software driver (not depicted) that determines whether to (1) instruct target device **150** to capture an image and repeatedly display the captured image, (2) power down components of graphics subsystem **115**, and (3) power down components of target device **150**. The driver may determine whether to initiate actions (1), (2), or (3) based at least on: a change in the system timer period, triangle or polygon rendering, any processor core is not in low power mode, any mouse activity, vertical blanking interrupts are used, and/or overlay is enabled. For example, powering down components may involve reducing voltage regulators to the lowest operating voltage level. For example, when the processor **110** executes a Microsoft Windows compatible operating system, the driver may be a kernel mode driver.

[0015] For example, host system **102** may transmit commands to target device **150** using interface **145**. In some embodiments, interface **145** may include a Main Link and an AUX channel, both described in Video Electronics Standards Association (VESA) DisplayPort Standard, Version 1, Revision 1a (2008) as well as revisions and variations thereof. In various embodiments, host system **102** (e.g., graphics subsystem **115**) may form and transmit communications to target device **150** at least in a manner described with respect to co-pending U.S. patent application having Ser. No. 12/286,192, entitled "Protocol Extensions in a Display Port Compatible Interface," inventors Kwa et al., filed Sep. 29, 2008 (attorney docket number P27579).

[0016] Target device **150** may be a display device with capabilities to display visual content and/or render audio content. For example, target device **150** may include control logic such as a timing controller (TCON) that controls writing of pixels as well as a register that directs operation of target device **150**. Target device **150** may have access to a memory or frame buffer from which to read frames for display.

[0017] Various embodiments include the capability to transmit secondary data packets over interface **145** to target device **150**. Secondary data packets can be used to command target device **150**.

[0018] FIG. **1**B depicts an example of components of host system **102** whose power consumption can be controlled (e.g., power consumption decreased or increased), in accordance with an embodiment. The components can be in a chipset, processor, or graphics subsystem. For example, the display phase lock loop (PLL) **160**, display plane **162**, display pipe **164**, and display interface **166** of host **102** can be powered down or up. PLL may be a system clock for the display plane **162**, display pipe **164**, and/or display interface **166**. For example, display plane **162** may include a data buffer and RGB color mapper, which transforms data from buffer to RGB. Display plane **162** may include an associated memory controller and memory input/output (IO) (not depicted) that could also be power managed. Pipe **164** may include a blender of multiple layers of images into a composite image, X, Y coordinate rasterizer, and interface protocol packetizer. The interface protocol packetizer may be compliant at least with

Display Port or Low-voltage differential signaling (LVDS), available from ANSI/TIA/EIA-644-A (2001), as well as variations thereof. Display interface **166** may include a DisplayPort or LVDS compatible interface and a parallel-in-serial-out (PISO) interface.

[0019] FIG. **1**C depicts a high level block diagram of a timing controller for a display device in accordance with an embodiment. Timing controller **180** has the capability to respond to instructions from a host device to enter a self refresh display (SRD) mode that may include powering down components and/or capturing an image and repeatedly outputting the captured image to a display. In response to signal SRD_ON from a host, SRD control block activates the frame buffer to capture a frame and the SRD control block controls the multiplexer (MUX) to transfer the captured frame to the output port. After the frame buffer captures a frame, the host may read a register in the panel that indicates that the capture has taken place and that the timing controller displays a captured image. After the signal SRD_ON is deactivated, SRD control block deactivates the frame buffer and associated logic and causes the MUX to transfer incoming video from the input port (RX in this case) to the output port (TX). Timing controller **180** may use less power because the frame buffer is turned off and the logic clock gated when the self refresh display mode is exited. In various embodiments, SRD_ON and SRD_STATUS can be signals or configured in a register.

[0020] FIG. **2** depicts an example format of signals transmitted over multiple lanes on a DisplayPort compatible interface. In particular, FIG. **2** reproduces FIG. **2-14** of the Video Electronics Standards Association (VESA) DisplayPort Standard, Version 1, Revision 1a (2008) (hereafter "DP 1.1a specification"). However, embodiments of the present invention can be used in any version and variation of DisplayPort as well as other standards. DisplayPort specifies the availability of secondary data packets to transmit information at the vendor's discretion. Vendor-specific extension packets are a type of secondary data packet that can be used to control the display self refresh functionality over embedded DisplayPort (eDP). The basic structure of the header information for these secondary data packets is described in table 2-33 of section 2.2.5 of the DP1.1a specification, which is reproduced below in table 1.

TABLE 1

Byte#	Content
HB0	Secondary-data Packet ID
HB1	Secondary-data Packet type
HB2	Secondary-data-packet-specific header byte0
HB3	Secondary-data-packet-specific header byte1

[0021] FIG. **3** depicts an example manner of communication of secondary data packets over one and more lanes of a DisplayPort compatible interface. In particular, FIG. **3** reproduces FIG. **2-24** of the DP1.1a specification. As shown, secondary data packets can include header bytes, parity bytes, and data bytes.

[0022] In accordance with various embodiments, the following table provides an example of commands that can be transmitted in header bytes of secondary data packets, in accordance with various embodiments. Commands can be performed by a target device such as a display with capability to perform self refresh display.

TABLE 2

Byte#	Example of Contents
HB0	Specifies generation number of specification: 00h: Revision 0 (Haswell generation) All other values reserved
HB1	04h (extension packet type indicator as defined by DP1.1a specification)
HB2	Bits 0-2 used for controls Bits 7:3 = Reserved (all 0's)
HB3	Reserved (all 0's)

[0023] Various embodiments provide controls in bits 0-2 of header byte HB2. Table 3 describes example commands in bits **0**, **1**, and **2** in header byte HB**2**.

TABLE 3

Control Field Bit	Definition
B0: Frame Type	B0 = 0 means current frame is identical to the one previously sent. B0 = 1 means current frame is different from the previously sent frame.
B1: Source SRD State	Source SRD state control field indicates the source's display controller state, which is used as a command by the target device to manage its local controller. B1 = 0 means SRD_Off. Source state is such that normal display processing occurs and the eDP link remains active. B1 = 1 means SRD_On. Source state is such that normal display processing may be disabled and the eDP link may be placed in standby.
B2: Link Standby Enable	B2 = 0 means main link to remain in normal active state. B2 = 1 enables main link to enter standby state.

[0024] Bit B**0** indicates whether a frame to be sent to a target device has not changed from a previous frame that was sent to the target device. Bit B**0** indicates whether a target device is to store an incoming image in a buffer. The target device can be a display with capability to enter self refresh display mode and display an image from a buffer. Bit B**0** can be used where an application is to update an image on a display. An update can be made to wakeup a panel and tell the panel that one or more modified frame(s) are to be transmitted to the display and to store the frames. After storing the frames, the display and display system can return to low power state and the display system can use the updated frame for self refresh display.

[0025] Bit B**1** indicates whether the target device is to enter self refresh display mode or remain in normal operation. Bit B**1** also indicates whether normal display processing occurs and the link between the source and target device remains in normal active state.

[0026] Bit B**2** indicates whether to power down a main link. For example, the main link can be a differential pair wire having connectors, d+ and d–. The link can transmit RGB content or other types of content. The link can be powered down or enter lower power mode.

[0027] Standard Embedded DisplayPort implementations support two link states: (1) full on ("Normal Operation") in which video data is transmitted to a panel and (2) full off ("ML Disabled") in which a lid is closed on a laptop and the display interface is turned off because video is not required. The standard Embedded DP implementation also supports an intermediate set of training-related transitional states. SRD adds an additional state: "ML Standby." State "ML Standby" enables a receiver to implement additional power management techniques for additional power reductions. For example, a receiver bias circuitry and PLLs can be turned-off. For example, components described with regard to FIG. **1**B can enter lower power state or turn-off. State "ML Standby" can turn off a display interface and display link but use an image stored in panel for SRD.

[0028] FIG. **4** depicts an example of a sequence of events for entry into ML standby mode. A DisplayPort main link can be used to transmit signals X, Y, and Z. In some embodiments, header byte HB**2** can be used to transmit signals X, Y, and Z. Signal X represents whether the current frame, that is to be transmitted after a VBI, is modified or unmodified relative to a previously transmitted frame. In this example, the value of signal X can indicate that the current frame is modified or unmodified relative to the previously transmitted frame. In this example, it does not matter whether frame is modified or unmodified. Signal Y indicates whether SRD is on or off. In this case, signal Y indicates that SRD state is ON. Signal Z indicates whether a link standby entry is to occur. In this case, signal Z indicates link standby is to be entered.

[0029] In some embodiments, header byte HB**2** can be used to transmit signals X, Y, and Z. To transmit X, Y, and Z, the following scheme can be used: bit B**0** represents X, bit B**1** represents Y, and bit B**2** represents Z.

[0030] Segment "Active"**0** can include RGB color data for transmission to a display. Segment "BS" can indicate a start of a vertical blank interval in the system. Segment "BS to stdby" indicates a delay between a start of a vertical blank interval and a start of standby mode.

[0031] FIG. **5** depicts an example of a sequence of events for exit from ML standby mode. In particular, states of the main link and auxiliary channel are described. The main link state is in state "Standby." The source initiates ML Standby exit using an AUX channel to transmit a write operation. Command WR can be used to write to register address location 00600h to wake up the target device and cause the target device to exit ML standby mode. Other register address locations can be used. The target device monitors location 00600h and wakes up on reading a wake up command in that location. After some delay, the target device transmits command ACK to the host using an AUX channel to indicate acknowledgement of receipt of the WR command. The length of the delay between receipt of WR and transmission of ACK can be defined by the DisplayPort Specification.

[0032] On detecting the write event, the target device power-ups the main link receiver and re-enters the training state to be ready for link training Accordingly, as shown, the main link enters the state "Training " Re-entering the training state after exiting standby mode without explicit command provides faster synchronization. After the source completes sending the write transaction, the source may initiate link training The transmitter may initiate either full training or Fast Link Training as described in the DP specification. A target device could be turned off and lose awareness of need to train when it wakes up. Causing the target device to train immediately after exiting standby allows full power down of a DP receiver.

[0033] The graphics and/or video processing techniques described herein may be implemented in various hardware architectures. For example, graphics and/or video functionality may be integrated within a chipset. Alternatively, a discrete graphics and/or video processor may be used. As still another embodiment, the graphics and/or video functions may be implemented by a general purpose processor, including a multicore processor. In a further embodiment, the functions may be implemented in a consumer electronics device.

[0034] Embodiments of the present invention may be implemented as any or a combination of: one or more microchips or integrated circuits interconnected using a motherboard, hardwired logic, software stored by a memory device and executed by a microprocessor, firmware, an application specific integrated circuit (ASIC), and/or a field programmable gate array (FPGA). The term "logic"**0** may include, by way of example, software or hardware and/or combinations of software and hardware.

[0035] Embodiments of the present invention may be provided, for example, as a computer program product which may include one or more machine-readable media having stored thereon machine-executable instructions that, when executed by one or more machines such as a computer, network of computers, or other electronic devices, may result in the one or more machines carrying out operations in accordance with embodiments of the present invention. A machine-readable medium may include, but is not limited to, floppy diskettes, optical disks, CD-ROMs (Compact Disc-Read Only Memories), and magneto-optical disks, ROMs (Read Only Memories), RAMs (Random Access Memories), EPROMs (Erasable Programmable Read Only Memories), EEPROMs (Electrically Erasable Programmable Read Only Memories), magnetic or optical cards, flash memory, or other type of media/machine-readable medium suitable for storing machine-executable instructions.

[0036] The drawings and the forgoing description gave examples of the present invention. Although depicted as a number of disparate functional items, those skilled in the art will appreciate that one or more of such elements may well be combined into single functional elements. Alternatively, certain elements may be split into multiple functional elements. Elements from one embodiment may be added to another embodiment. For example, orders of processes described herein may be changed and are not limited to the manner described herein. Moreover, the actions of any flow diagram need not be implemented in the order shown; nor do all of the acts necessarily need to be performed. Also, those acts that are not dependent on other acts may be performed in parallel with the other acts. The scope of the present invention, however, is by no means limited by these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are possible. The scope of the invention is at least as broad as given by the following claims.

What is claimed is:

1. An apparatus comprising:

logic to form at least a first bit and a second bit in a secondary data packet, wherein the first bit is to indicate whether to enter self refresh and the second bit is to indicate whether to store a frame for display into a frame buffer and wherein the secondary data packet is in compliance with a DisplayPort specification.

2. The apparatus of claim **1**, wherein the first bit is to indicate whether to enter self refresh or remain in normal operation.

3. The apparatus of claim **1**, comprising:

logic to set the first bit to indicate to enter self refresh based at least on at least one of: a change in the system timer period, triangle or polygon rendering, any processor core is not in low power mode, any mouse activity, vertical blanking interrupts are used, or overlay is enabled.

4. The apparatus of claim **1**, wherein the second bit is to indicate whether a transmitted frame for display is identical to a previously transmitted frame for display.

5. The apparatus of claim **1**, comprising:

logic to cause powering down of components, the components comprising one or more of: a display phase lock loop (PLL), display plane, display pipe, or display interface.

6. The apparatus of claim **1**, comprising:

an interface communicatively coupled to the logic to form at least a first bit and a second bit in a secondary data packet;

a display controller communicatively coupled to the interface; and

a frame buffer, the display controller to cause storage of a frame for display into the frame buffer in response to an indication to enter self refresh and an indication to store a frame for display into the frame buffer.

7. The apparatus of claim **6**, comprising:

a display communicatively coupled to the frame buffer, the display to display at least one frame for display from the frame buffer.

8. The apparatus of claim **1**, wherein the DisplayPort specification comprises DisplayPort specification version 1.1a.

9. The apparatus of claim **1**, wherein the logic comprises any or a combination of:

one or more integrated circuits, hardwired logic, software executed by a microprocessor, or a field programmable gate array.

10. At least one computer-readable medium, comprising instructions stored thereon, which, if executed by one or more processors, cause the one or more processors to:

form at least a first bit and a second bit in a secondary data packet, wherein the first bit is to indicate whether to enter self refresh and the second bit is to indicate whether to store a frame for display into a frame buffer and wherein the secondary data packet is in compliance with a DisplayPort specification.

11. The at least one computer-readable medium of claim **10**, wherein the first bit is to indicate whether to enter self refresh or remain in normal operation.

12. The at least one computer-readable medium of claim **10**, comprising instructions stored thereon, which, if executed by one or more processors, cause the one or more processors to:

set the first bit to indicate to enter self refresh based at least on at least one of a change in the system timer period, triangle or polygon rendering, any processor core is not in low power mode, any mouse activity, vertical blanking interrupts are used, or overlay is enabled.

13. The at least one computer-readable medium of claim **10**, wherein the second bit is to indicate whether a transmitted frame for display is identical to a previously transmitted frame for display.

14. The at least one computer-readable medium of claim **10**, comprising instructions stored thereon, which, if executed by one or more processors, cause the one or more processors to:

cause powering down of components, the components comprising one or more of: p**1** a display phase lock loop (PLL), display plane, display pipe, or display interface.

15. The at least one computer-readable medium of claim **10**, wherein the DisplayPort specification comprises DisplayPort specification version 1.1a.

16. A computer-implemented method comprising:

forming at least a first bit and a second bit in a secondary data packet, wherein the first bit is to indicate whether to enter self refresh and the second bit is to indicate whether to store a frame for display into a frame buffer and wherein the secondary data packet is in compliance with a DisplayPort specification.

17. The computer-implemented method of claim **16**, wherein the first bit is to indicate whether to enter self refresh or remain in normal operation.

18. The computer-implemented method of claim **16**, comprising:

setting the first bit to indicate to enter self refresh based at least on at least one of a change in the system timer period, triangle or polygon rendering, any processor core is not in low power mode, any mouse activity, vertical blanking interrupts are used, or overlay is enabled.

19. The computer-implemented method of claim **16**, wherein the second bit is to indicate whether a transmitted frame for display is identical to a previously transmitted frame for display.

20. The computer-implemented method of claim **16**, comprising:

causing powering down of components, the components comprising one or more of: a display phase lock loop (PLL), display plane, display pipe, or display interface.

21. The computer-implemented method of claim **16**, wherein the DisplayPort specification comprises DisplayPort specification version 1.1a.

22. An apparatus comprising:

a controller to receive at least a first bit and a second bit from a secondary data packet, wherein the first bit is to indicate whether to enter self refresh and the second bit is to indicate whether to store a frame for display into a frame buffer and wherein the secondary data packet is in compliance with a DisplayPort specification.

23. The apparatus of claim **22**, comprising:

a frame buffer, the controller to cause storage of a frame for display into the frame buffer in response to an indication to enter self refresh and an indication to store a frame for display into the frame buffer.

24. The apparatus of claim **22**, comprising:

an interface communicatively coupled to the controller, the interface to receive the secondary data packet.

25. The apparatus of claim **23**, comprising:

a display communicatively coupled to the frame buffer, the display to display at least one frame for display from the frame buffer.

26. The apparatus of claim **22**, wherein the first bit is to indicate whether to enter self refresh or remain in normal operation.

27. The apparatus of claim **22**, wherein the second bit is to indicate whether a transmitted frame for display is identical to a previously transmitted frame for display.

28. The apparatus of claim **22**, wherein the DisplayPort specification comprises DisplayPort specification version 1.1a.

29. The apparatus of claim **22**, wherein the controller comprises any or a combination of: one or more integrated circuits, hardwired logic, software executed by a microprocessor, or a field programmable gate array.

30. At least one computer-readable medium, comprising instructions stored thereon, which, if executed by one or more processors, cause the one or more processors to:

receive at least a first bit and a second bit from a secondary data packet, wherein the first bit is to indicate whether to enter self refresh and the second bit is to indicate whether to store a frame for display into a frame buffer and wherein the secondary data packet is in compliance with a DisplayPort specification.

31. The at least one computer-readable medium of claim **30**, wherein the first bit is to indicate whether to enter self refresh or remain in normal operation.

32. The at least one computer-readable medium of claim **30**, wherein the second bit is to indicate whether a transmitted frame for display is identical to a previously transmitted frame for display.

33. The at least one computer-readable medium of claim **30**, wherein the DisplayPort specification comprises DisplayPort specification version 1.1a.

34. A computer-implemented method comprising:

receiving at least a first bit and a second bit from a secondary data packet, wherein the first bit is to indicate whether to enter self refresh and the second bit is to indicate whether to store a frame for display into a frame buffer and wherein the secondary data packet is in compliance with a DisplayPort specification.

35. The method of claim **34**, wherein the first bit is to indicate whether to enter self refresh or remain in normal operation.

36. The method of claim **34**, wherein the second bit is to indicate whether a transmitted frame for display is identical to a previously transmitted frame for display.

37. The method of claim **34**, wherein the DisplayPort specification comprises DisplayPort specification version 1.1a.

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