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(81) Designated States (unless otherwise indicated, for every
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CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,
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OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
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UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,

(54) Title: MULTI-CHIP PACKAGE WITH OFFSET 3D STRUCTURE

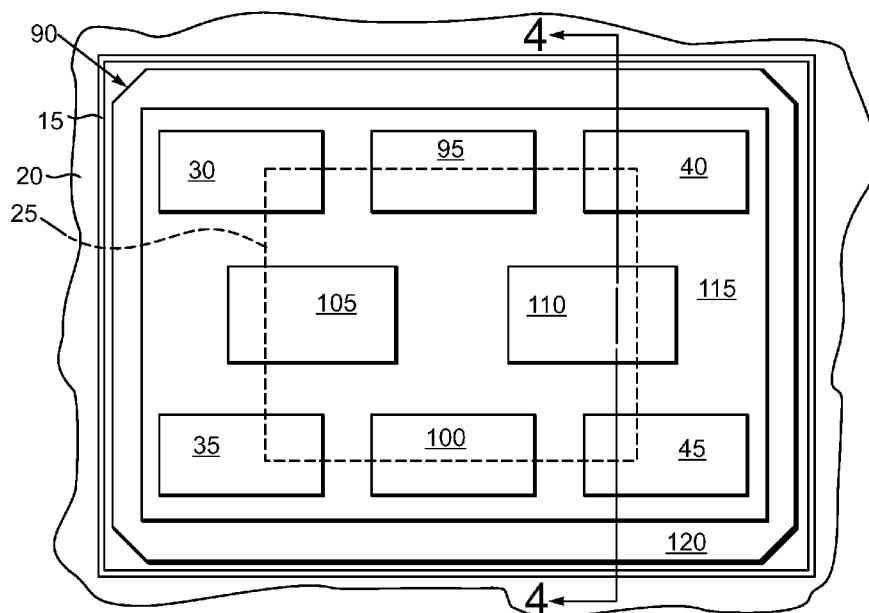


FIG. 3

(57) Abstract: Various semiconductor chip devices and methods of manufacturing the same are disclosed. In one aspect, a semiconductor chip device is provided that has a reconstituted semiconductor chip package (115) that includes an interposer (125) that has a first side and a second and opposite side and a metallization stack (145) on the first side, a first semiconductor chip (25) on the metallization stack and at least partially encased by a dielectric layer (165) on the metallization stack, and plural semiconductor chips (40, 45) positioned over and at least partially laterally overlapping the first semiconductor chip.

TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/024826**A. CLASSIFICATION OF SUBJECT MATTER****H01L 25/065(2006.01)i, H01L 25/07(2006.01)i, H01L 23/00(2006.01)i, H01L 23/498(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/065; H01L 21/50; H01L 21/98; H01L 23/31; H01L 23/48; H01L 25/18; H01L 25/07; H01L 23/00; H01L 23/498

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: semiconductor chip device, semiconductor chip package, interposer, metallization stack, dielectric layer, overlapping, circuit board socket

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014-0203457 A1 (SAMSUNG ELECTRONICS CO., LTD.) 24 July 2014 See paragraphs [0052]-[0099] and figures 4, 17.	1-20
Y	CN 106558574 A (HUAWEI TECHNOLOGIES CO., LTD.) 05 April 2017 See paragraphs [0121]-[0279] and figures 1, 11.	1-20
A	US 2017-0018534 A1 (SHINKO ELECTRIC INDUSTRIES CO., LTD.) 19 January 2017 See paragraphs [0156]-[0159] and figure 25.	1-20
A	US 2015-0255427 A1 (SK HYNIX INC.) 10 September 2015 See paragraphs [0031]-[0035] and figure 1.	1-20
A	US 2011-0084373 A1 (DAESIK CHOI et al.) 14 April 2011 See paragraphs [0045]-[0099] and figures 1-6.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/US2019/024826

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0203457 A1	24/07/2014	KR 10-2014-0095182 A KR 10-2021077 B1 US 9123630 B2	01/08/2014 11/09/2019 01/09/2015
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