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(54) Title: COMPONENTS AND CONFIGURATIONS FOR TEST AND VALUATION OF INTEGRATED OPTICAL BUSSES

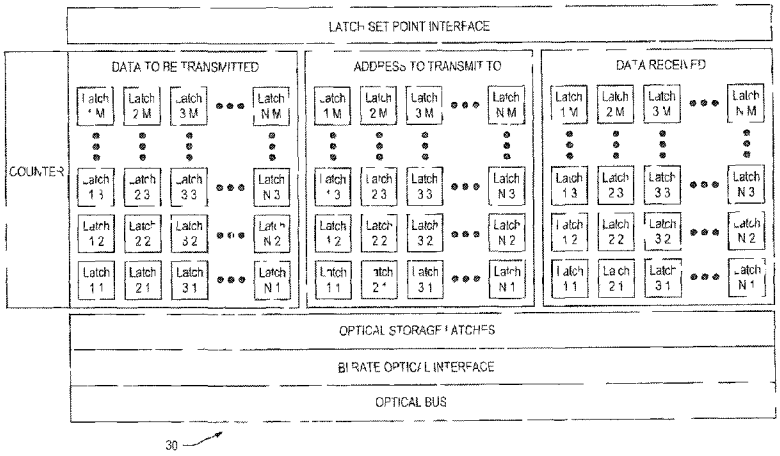

FIG 1

(57) Abstract: An apparatus and method is provided for the testing of an optical bus, that method comprising; loading transmission test data and address information for at ieast one receiving cell via an electronic bus in a first register; setting a clock rate for the optical bus; employing the optical bus to transmit the test data from the first register to the at least one receiving cell; reading out received test data from the receiving cell via the electronic bus; correlating the received test data from the first register with the transmission test data; analyzing errors in the received data and handling of the received data by the bus.

WO 2010/025250 A1

COMPONENTS AND CONFIGURATIONS FOR TEST AND VALUATION OF INTEGRATED OPTICAL BUSSES

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Richard Berger

FIELD OF THE INVENTION

[0001] This invention relates to the field of test components for photonic communications devices and more particularly to a test for a system to allow the transfer of data between an optical bus and electrical components having different clock speeds.

BACKGROUND OF THE INVENTION

[0002] Optical busses operate at high bus speeds, unmatched by even the most advanced electronic components. The pairing of such electrical devices with optical devices can lead to latency and conflicts. As optical busses evolve to operate at data rates beyond the capability of current characterization equipment, there is a need to develop test and evaluation methods that allow accurate characterization while decoupling the characterization from electronic test equipment and methods that will induced their own lag and latency to the measurements.

[0003] The biggest challenge with employing an ail optical bus is that the clock speed of the optical bus. For example the real on chip digital clock rates today are 2-4 GHz, As technology evolves, electronic clock rates may reach a staggering 10-12GHz. This is still a fraction of the 40-120GHz clock rates that an all optical bus should be able to obtain. This fractional variation in clock rate induces a lag in the write/read

cycle if the information is taken directly from the electronic component to the optical bus.

SUMMARY OF THE INVENTION

[0004] One embodiment of the present invention provides a method for the testing of an optical bus, that method comprising: loading transmission test data and address information for at least one receiving cell via an electronic bus in a first register; setting a clock rate for the optical bus; employing the optical bus to transmit the test data from the first register to the at least one receiving cell; reading out received test data from the receiving cell via the electronic bus; correlating the received test data from the first register with the transmission test data; analyzing errors in the received data and handling of the received data by the bus.

[0005] The feaiures and advantages described herein are not all-inclusive and, in particular, many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification, and claims. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and not to limit the scope of the inventive subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

(00061 Figure 1 is a block diagram illustrating a basic high speed FIFO core configured in accordance with one embodiment of the present invention.

[0007] Figure 2 is a block diagram illustrating a system for the testing of an optical bus configured in accordance with one embodiment of the present invention.

[0008] Figure 3 is a flow chart illustrating a method for the testing of an optical bus configured in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0009] One embodiment of the present invention provides an apparatus for testing an architecture that employs an intermediary for the rapid transfer to and from an optical bus, while allowing the same information to be transferred to and from the electronic components at their own more leisurely clock cycle. One example of such architecture is illustrated in **Figure 1** illustrates a basic high speed FIFO core used to characterize *and* demonstrate an optical bus. To enable lower clock rate electronic components to fully interface the high speed optical bus without introducing a limitation based on their much slower clock speed such an embodiment utilizes an optical latch that will allow information to be loaded from the optical bus. To realize this type of optical storage element two nonlinear interferometers creating an optical R-S fiip-flop or optical latch are employed.

[00 10J In such an embodiment, an optical latch is triggered on by the set pulse. Later in the cycle, it is triggered off by a reset pulse which allows the output from the much faster optical bus to be brought into a cell without slowing it down. In embodiments utilizing a second Latch the gating of information to the bus can be controlled at a much greater rate of operation than could be achieved with the electronic component alone, and such a configuration will allow storage and rapidly gating information to optical components,

JOOIlI in one embodiment of the present invention, the electronic component writes a state to the optical latch. Once the bus comes active the information is rapidly clocked into the optical bus through the second latch. Slightly simpler output architecture can be achieved by running the output of the latch through an optically addressed bus

switch. This can be further extended by combining latches to achieve a serial to parallel converter to rapidly burst in data serially at each wavelength.

[0012] One embodiment of the present invention provides a simple method to illustrate all the key principles, of intra-chip photonic networks, necessary for application in various multi-processor architectures. In addition, through application of varying numbers of these cells such an embodiment allows a user to demonstrate the scaling of these technologies as well.

[0013] An example of the one embodiment of the present invention, illustrated in **Figure 2** includes a large photonic ASIC 20, in one embodiment, 18mm by 18mm, is manufactured with a set of first-in-first-out (FIFO) registers 30 at each corner of the die as well as physically adjacent to one another. These registers 30 will be connected to both electrical 32 and optical buses 34 to measurably illustrate the power-performance gains possible through migration to optical bussing.

[0014] The optical busses **34,** in such an embodiment, will also employ optical clock distribution and will be capable of greater than ITB/s transfer rates. Both electrical 32 and optical busses 34 will be organized to allow both point-to-point and broadcast data transfers in either direction, and will cross over each other to demonstrate the flexibility of the tested optical technology.

[0015] External to the ASIC 20, data will be sourced and captured by large RAMs (not illustrated), to confirm data transfer and capture bit error rate (BER) information, and to allow transfer of mass amounts of data.

[0016] As illustrated in Fig. 3 one embodiment of the present invention provides a method for testing an optical bus, Load data to be sent and address locations are loaded into a plurality of first in first out (FIFO) registers with an electronic bus. 112 The optical bus clock rate is set to a desired test level. 114 The optical bus is employed to transfer data to the respectively addressed receiving cells. 116 The data contained in the receiving cells is read out using the electronic data bus. 118 The data received by the receiving cells is correlated with transmitted data at each site to analyze errors and how the data was handled. 120

[0017] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS

What is claimed is:

1. A system for the testing of optical buses, the system comprising:

A plurality of registers disposed on a ASIC;

An electrical bus connecting said plurality of registers.

2. A method for the testing of an optical bus, said method comprising:

Loading transmission test data and address information for at least one receiving celt via an electronic bus in a first register;

Setting a clock rate for said optical bus;

Employing said optical bus to transmit said test data from said first register Lo said at least one receiving cell;

Reading out received test data from said receiving cell via said electronic bus;

Correlating said received lest data from said first register with said transmission test data;

Analyzing errors in said received data and handling of said received data by said bus.

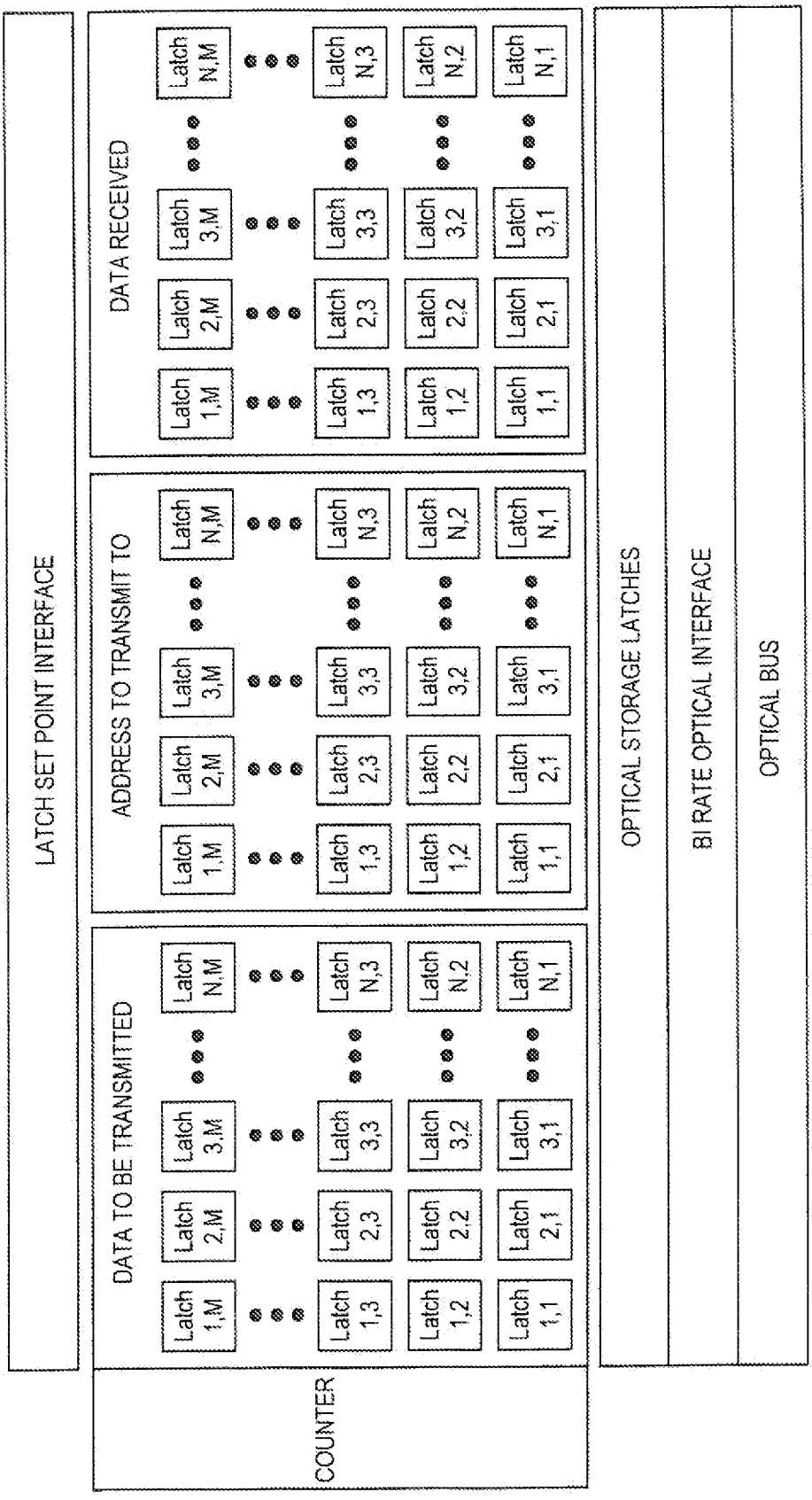
LATCH SET POINT INTERFACE
COUNTER
DATA TO BE TRANSMITTED
ADDRESS TO TRANSMIT TO
DATA RECEIVED
Latch 1,1
Latch 1,2
Latch 1,3
Latch 1,M
Latch 2,1
Latch 2,2
Latch 2,3
Latch 2,M
Latch 3,1
Latch 3,2
Latch 3,3
Latch 3,M
Latch N,1
Latch N,2
Latch N,3
Latch N,M
OPTICAL STORAGE LATCHES
BI RATE OPTICAL INTERFACE
OPTICAL BUS
30

FIG. 1

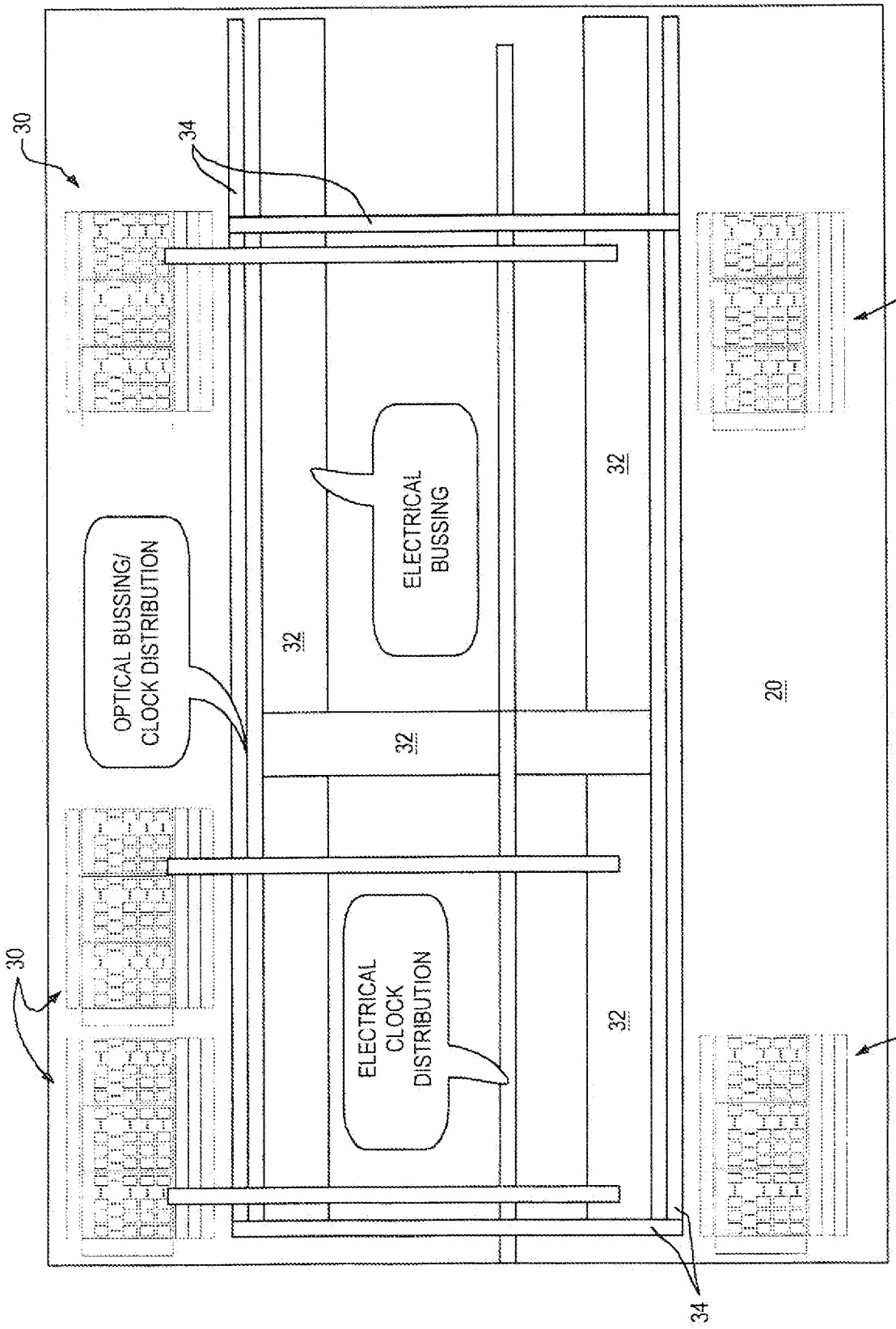
30
34
OPTICAL BUSSING/
CLOCK DISTRIBUTION
ELECTRICAL
BUSSING
32
32
32
20
ELECTRICAL
CLOCK
DISTRIBUTION
32
30
30
30
34

FIG. 2

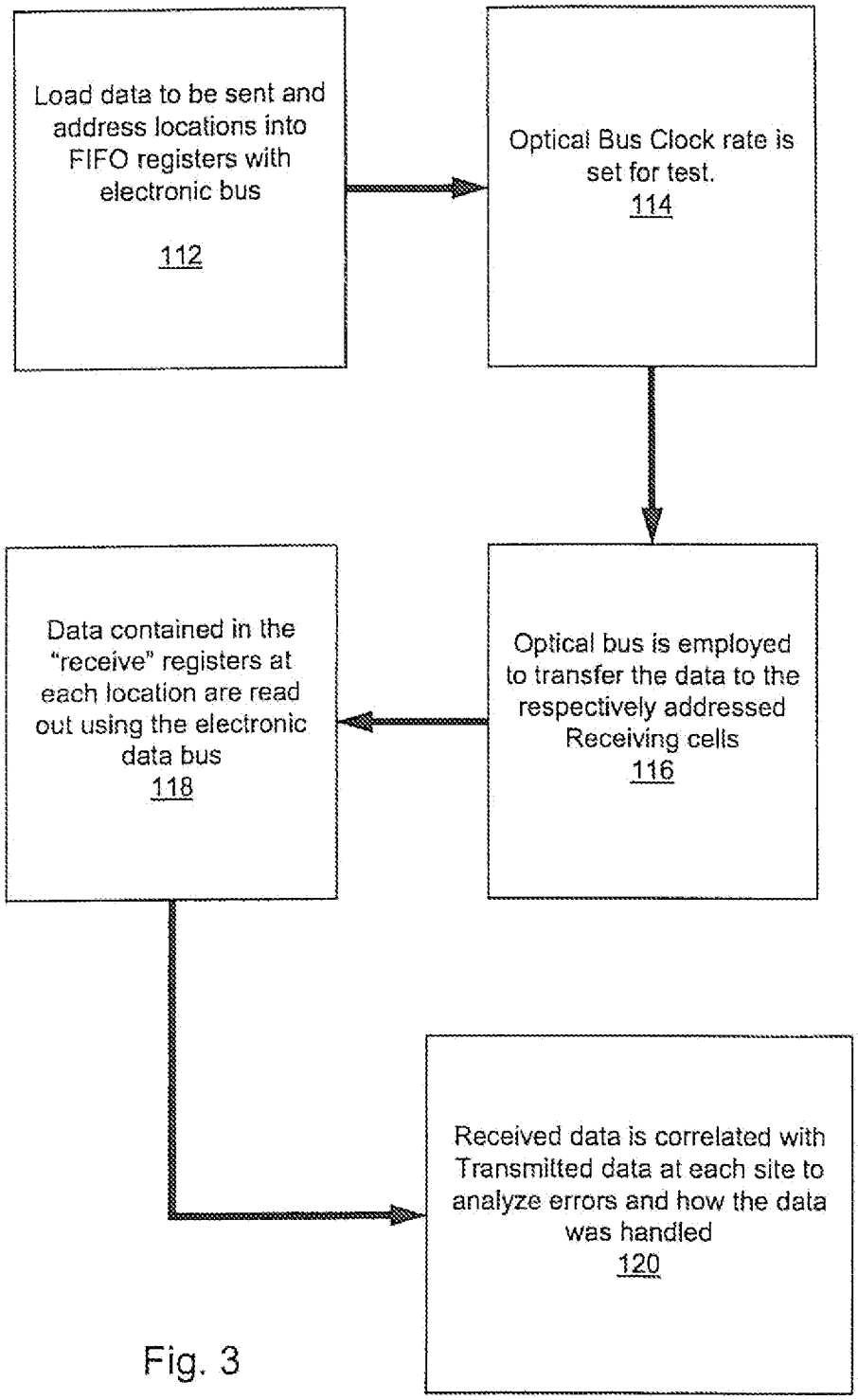
Load data to be sent and address locations into FIFO registers with electronic bus
112
Optical Bus Clock rate is set for test.
114
Optical bus is employed to transfer the data to the respectively addressed Receiving cells
116
Data contained in the "receive" registers at each location are read out using the electronic data bus
118
Received data is correlated with Transmitted data at each site to analyze errors and how the data was handled
120

Fig. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/US 09/55195

A CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G02B 6/1 2 (2009 0 1)
USPC - 385/14
According to International Patent Classification (IPC) or to both national classification and IPC

B FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC 385/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 385/14, 15, 24 (keyword limited - see below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST(PGPB,USPT,EPAB,JPAB), Google Scholar
Search Terms Used fiberoptic, optical, bus, cross connect, ASIC, testing, clock, data, compare, correlate, error

C DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X	US 6 959 126 B 1 (Lofland et al), 25 October 2005 (25 10 2005) entire document, especially col 5 In 25 to col 7 In 56, col 13 In 18-24	1 2
A	US 2007/0122148 A 1 (Welch et al), 3 1 May 2007 (31 05 2007), entire document	1-2
A	US 6,580 531 B 1 (Swanson et al), 17 June 2003 (17 06 2003), entire document	1-2

D Further documents are listed in the continuation of Box C **D**

*	Special categories of cited documents	'T	later document published after the international filing date or priority date and not in conflict with the application but cjled to understand the principle or theory underlying the invention
''A	documenl defining the general state ol the art which is not considered Io be of particular relevance		
ł	earlier application or patent but published on or after the international filing date	'X '	document of particular relevance the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
L	documenl which may ihrow doubis on pπoπly cla ιm(s) or which is tiled Io establish the publication dale of another citation or other special reason (as specified)	' Y	document of particular relevance the claimed invention cannol be considered to involve an invenlive step when the documenl is combined with one or more other such documents such combination being obvious to a person skilled in the art
O	document relcmng Io an oral disclosure use exhibition or other means		
P	document published prior to the international filing date but later than the priority date claimed	'&	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 October 2009 (21 10 2009)	**2 9 OCT Z0Q3.**
Name and mailing address of the ISA/US Mail Stop PCT, Attn ISA/US, Commissioner for Patents P O Box 1450, Alexandria, Virginia 22313 1450 Facsimile No 571 $27_3.32_0$ 1	Authorized officer Lee W Young PCT Hetpdesk 571 272 4300 PCT OSP 571 272 7774

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