(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 April 2015 (02.04.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/042643 A1

(51) International Patent Classification:
H03F 3/213 (2006.01)

(21) International Application Number:
PCT/AU2014/000936

(22) International Filing Date:
25 September 2014 (25.09.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2013903771 30 September 2013 (30.09.2013) AU

(71) Applicant: **THE UNIVERSITY OF MELBOURNE** [AU/AU]; Grattan Street, University of Melbourne, Melbourne, Victoria 3010 (AU).

(72) Inventors: **SKAFIDAS, Efstratios**; C/- UoM Commercial Ltd, The University of Melbourne, Melbourne, Victoria 3010 (AU). **DUONG, Hoa Thai**; C/- UoM Commercial Ltd, The University of Melbourne, Melbourne, Victoria 3010 (AU). **EVANS, Robin J**; C/- UoM Commercial Ltd, The University of Melbourne, Melbourne, Victoria 3010 (AU). **LE, Viet Hoang**; C/- UoM Commercial Ltd, The University of Melbourne, Melbourne, Victoria 3010 (AU). **HUYNH, Anh**; C/- UoM Commercial Ltd, The University of Melbourne, Melbourne, Victoria 3010 (AU).

(74) Agent: **GRIFFITH HACK**; GPO Box 1285, Melbourne, Victoria 3001 (AU).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: A MULTI-STAGE CMOS AMPLIFIER CIRCUIT

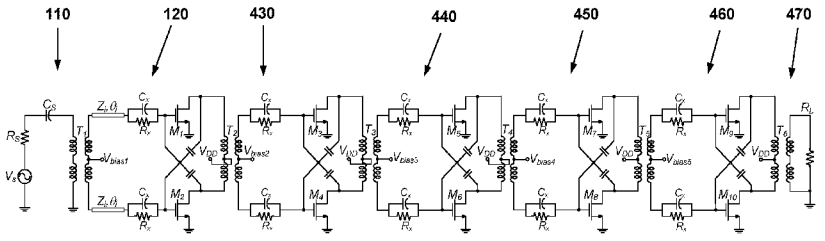

Figure 4

(57) Abstract: A multi-stage CMOS power amplifier circuit comprises a plurality of amplifier stages (120,430,440,450,460) connected by respective ones of a plurality of transformers (T_2-T_5), wherein each transformer (T_2-T_5) comprises a first winding in a first metal layer of a CMOS chip and a second winding arranged in a second metal layer of the CMOS chip superimposed on the first winding, wherein the first and second windings of each transformer have a width (W) and a radius (R), and impedance matching between the amplifier stages is provided by the width (W) and the radius (R) of the respective transformers (T_2-T_5).

WO 2015/042643 A1

A MULTI-STAGE CMOS AMPLIFIER CIRCUIT

Field

The present invention relates to a multi-stage CMOS amplifier circuit and a CMOS power amplifier suitable for a stage of the multi-stage CMOS amplifier circuit.

Background

There has been considerable interest in automotive radar systems as they have the potential to provide a more secure and comfortable driving environment. Radar technology forms the basis for advanced automotive features such as collision avoidance, intelligent cruise control, auxiliary speed detection, blind spot detection, lane change warning, and automatic parking assist. Recently, interest has focussed on the 76-77 GHz frequency band because it is available for automotive applications in most parts of the world, with few national restrictions in operational parameters such as bandwidth, output power.

Currently, these systems are only available in premium cars because of their cost. Accordingly, there is a research into delivering these devices more cheaply, for example, by using relatively cheap CMOS technology. A power amplifier circuit is one of the key components in a radar system.

Accordingly, there is a need for an appropriate CMOS based amplifier circuit.

Summary

In a first aspect, the invention provides a multi-stage CMOS power amplifier circuit comprising a plurality of amplifier stages connected by respective ones of a

plurality of transformers, wherein each transformer comprises a first winding in a first metal layer of a CMOS chip and a second winding arranged in a second metal layer of the CMOS chip superimposed on the first winding, wherein:

the first and second windings of each transformer have a width and a radius; and

impedance matching between the amplifier stages is provided by the width and the radius of the respective transformers.

In an embodiment, the first winding of at least one of the plurality of transformers has a first winding bias port for providing a voltage to one or more transistors of a connected amplifier stage.

In an embodiment, the first winding comprises a loop between two first winding connectors for connecting to an amplifier stage and the bias port is located opposite the two first winding connectors.

In an embodiment, the second winding of at least one of the plurality of transformers has a second winding bias port for providing a voltage to one or more transistors of a connected amplifier stage.

In an embodiment, the second winding comprises a loop between two connectors for connecting to an amplifier stage and the bias port is located opposite the two connectors.

In an embodiment, the second winding of said at least one of the plurality of transformers has a second winding bias port for providing a voltage to a connected amplifier stage;

the second winding comprises a loop between two second winding connectors for connecting to an amplifier

stage; and

the second winding bias port of the second winding is located opposite the two second winding connectors and the first winding bias port.

In an embodiment, the multi-stage CMOS power amplifier circuit comprises five amplifier stages.

In an embodiment, at least one of the width and the radius is different for a first one of the transformers relative to a second one of the transformers.

In an embodiment, a first transformer connected to an input of an input amplifier has a first width and a first radius and a second transformer connected to an output of the input amplifier has a second radius smaller than the first radius.

In an embodiment, a last transformer connected to an output of an output amplifier has a last transformer width greater than said first width and a last transformer radius greater than said first radius.

In an embodiment, said input amplifier stage comprises a pair of transmission lines for input matching of the circuit.

In an embodiment, each amplifier stage comprises:

first and second transistors;

first and second RC circuits each comprising a resistor and capacitor connected in parallel, the first and second RC circuits connected between the respective gates of the first and second transistors and first and second ports of a transformer which provides the input to the respective amplifier stage; and

first and second cross-coupling capacitors, the first cross-coupling capacitor connected between the gate of the

first transistor and the drain of the second transistor and the second cross-coupling capacitor connected between the gate of the second cross-coupling capacitor and the drain of the first transistor.

In a second aspect, the invention provides a differential CMOS power amplifier for a multi-stage transformer connected amplifier circuit, the power amplifier comprising:

first and second transistors;

first and second RC circuits each comprising a resistor and capacitor connected in parallel, the first and second RC circuits connected between the respective gates of the first and second transistors and first and second input ports of the amplifier circuit; and

first and second cross-coupling capacitors, the first cross-coupling capacitor connected between the gate of the first transistor and the drain of the second transistor and the second cross-coupling capacitor connected between the gate of the second cross-coupling capacitor and the drain of the first transistor.

In an embodiment, the differential CMOS power amplifier comprises a pair of transmission lines for input matching of the circuit.

Accordingly, embodiments of the invention are capable of providing a 77 GHz power amplifier based on multiple passive transformer-coupled architectures in 65-nm CMOS technology. The proposed architecture provides a DC blocking property, a power supply with RF choke, differential to differential/single-ended conversion, input/output and interstage matching of the passive transformers such that embodiments of the invention may provide a high gain, low power and compact power amplifier at 77 GHz.

Brief Description of the invention

Embodiments of the invention will be described with reference to the accompanying drawings in which:

Figure 1 shows an input matching network for the first stage of the 77 GHz power amplifier of an embodiment of the invention;

Figure 2 is a simplified equivalent single-ended input matching network in which neutralization capacitors C_n are neglected;

Figure 3A is a simplified network of Figure 1 and Figure 3B is an equivalent circuit of Figure 3A;

Figure 4 show a five-stage 77 GHz differential power amplifier of an embodiment of the invention;

Figure 5 shows bias circuits for the power amplifier of the embodiment;

Figure 6 shows a 1-to-1 transformer layout of the embodiment;

Figure 7 is a die micrograph of the proposed 77 GHz power amplifier circuit;

Figure 8 is a graph of measured S-parameters of the five-stage 77 GHz power amplifier;

Figure 9 is a graph of the measured reverse isolation the 77 GHz power amplifier; and

Figure 10 is a graph of the gain, output power and power added efficiency responses.

Detailed description

Referring to the drawings, there is shown an embodiment of a multi-stage CMOS power amplifier circuit having a plurality of amplifier stages connected by respective ones of a plurality of transformers. The illustrated embodiment has five amplifier stages but other configurations can be achieved using the same technique. In the embodiments impedance matching is achieved by configuring the radius and/or width of the windings of the transformers. The embodiments employ a differential CMOS power amplifier that has an RC circuit and cross-coupling capacitors.

Figure 1 shows the input matching network of the 77 GHz five-stage power amplifier. The input 110 is represented by a voltage source V_s having and associated resistance R_s and capacitance C_s. The input 110 is coupled to an input amplifier stage 120 by first transformer T_1. In the embodiment, each amplifier stage comprises a differential power amplifier formed by first and second transistors M_1 and M_2.

In an embodiment, the differential power amplifier is neutralized by adding cross coupled capacitors (C_n) to cancel the inherent parasitic capacitance C_{gd} of the two transistors M_1 and M_2 and provide high isolation from the output to the input. In order to improve stability, an RC network (R_x, C_x) provided by a resistor R_x and a capacitor C_x connected in parallel, is connected between each port of the transformer at the gate of each transistor M_1, M_2. In the input stage, transmission lines 121,122 are provided between the ports of the input transformer T_1 and the RC networks. The transmission lines 121,122 are used for tuning the input matching, where Z_i is the characteristic impedance and θ_i is electrical length of the transmission line.

Figure 2 depicts an equivalent single-ended input matching network for the architecture in Figure 1, where the network between the gate and drain ports is represented by the Y-Matrix 210. Input impedances Z_A and Z_B of the network are calculated in accordance with equations (1) and (2), respectively. The unilateralization condition is satisfied when $Y_{12} = 0$, the input impedance Z_A can be simplified as shown in (3).

$$Z_A = \frac{1}{1/R_s + sC_s} + \left[sC_{gs1} + \frac{(1 + g_{m1}R_L)Y_{12}}{Y_{12}R_L + 1} \right]^{-1} \quad (1)$$

$$Z_B = Z_i \frac{Z_A + jZ_i \tan\theta_i}{Z_i + jZ_A \tan\theta_i} \quad (2)$$

$$(Z_A)_u = \frac{1}{1/R_s + sC_s} + \frac{1}{sC_{gs1}} \quad (3)$$

A simplified network derived from the network 100 of Figure 1 is shown in Figure 3. In Figure 3A k is the coupling coefficient between primary and secondary ports of the transformer, r_1 and r_2 represent the conductor losses, and L_1 and L_2 are inductance values for the primary and secondary windings of the transformer, respectively.

In the equivalent circuit of Figure 3A shown in Figure 3B, the effects of Z_B in the secondary circuit have been converted into a series reflected impedance Z_D in the primary circuit of the transformer. The reflected impedance Z_D and input impedance Z_{in} can be calculated by equations (4) and (5), respectively.

$$Z_D = \frac{(\omega M)^2}{2Z_B + sL_2 + r_2} \quad (4)$$

$$Z_{in} = r_1 + sL_1 + \frac{1}{sC_s} + \frac{(\omega M)^2}{2Z_B + sL_2 + r_2} \quad (5)$$

$$Z_{in} = R_o \quad (6)$$

where $M = k\sqrt{L_1 L_2}$ is the mutual inductance of the transformer.

Therefore, the input matching condition can be obtained from equation (6). By equating the real and imaginary parts of a complex condition (6), dimensions of the circuit can be derived. To simplify the matching condition, L_1 and L_2 are set to resonate with C_s and $imag\{2Z_B\}$, respectively. Therefore, from equations (5) and (6), the matching condition can be written as equation (7)

$$R_o = r_1 + \frac{(\omega M)^2}{real\{2Z_B + r_2\}} \qquad (7)$$

Figure 4 shows the architecture of the transformer-coupled five-stage power amplifier of an embodiment. The five-stage power amplifier circuit 400 comprises the input 110 and input 120 (first) amplifier stages shown in Figure 1, second 430, third 440, fourth 450, and output 460 (fifth) amplifier stages. The output stage 460 is coupled by transformer T_6 to load 470. It is assumed that the resistance of the load R_L is 50 Ohms.

The power amplifier circuit 400 was designed for a 1.2 V supply and 11 dBm (12 mW) output power for radar automotive applications. With $V_{DS,sat}$ =0.22 V, the voltage swing at the output is $V_{DD} - V_{DS,sat}$ =0.98 V. Therefore, the required current consumption for the final stage of the power amplifier is $2^*P_{max}/(V_{DD} - V_{DS,sat})$= 24.5 mA.

With 0.24 mA/μm current density at the peak frequency f_{MAX}, in order to obtain highest gain at 77 GHz, the width of the transistors M_9,M_{10} of the output stage 460 is selected as 24.5 mA/(0.24 mA/μm) ≈ 100 μm. Transistor widths for the transistors of the first (M_1,M_2), second (M_3,M_4), third (M_5,M_6), and fourth (M_7,M_8) amplifier stages are also chosen by the same method to be 50 μm, 60 μm, 70 μm, and 80 μm

respectively.

The transformers T_1-T_6 are designed taking into account the co-considerations of maximum output power and sufficient power matching. The transformers T_1-T_6 also provide the DC blocking property, power supply with RF choke, single-ended to differential conversion, differential to differential conversion, input, output and interstage matchings. The required bias voltages for each stage V_{bias_i} where i = 1...5 is generated from the current mirror circuit as shown in Figure 5. In the embodiment, bias current supplies I_{Ref} = 100 µA have been used.

Figure 6 shows the layout 600 of each of the transformers of the embodiment. Each transformer winding 610,620 is a single loop extending between the of the input section connectors V_{in+},V_{in-} and output section connectors V_{out-},V_{out+} respectively. As shown in Figure 6, each loop 610,620 is octagonal-shaped due to limitations on implementing a circular loop in the CMOS process at the required dimensions. In this respect, the embodiment was designed for fabrication using a 65-nm CMOS process with eight metal layers. In the embodiment, the output section (secondary winding 610) is on the top thick aluminium layer, the input section (primary winding 620) is on the second top thick metal layer, and the ground plane 630 is on the bottom metal layer of the 65-nm CMOS technology. It will be appreciated that relative positions of the input and output sections can be reversed. That is, that either the input winding or output winding be superimposed on the other winding to allow for inductive coupling.

Bias signals which can be used either as a bias voltage V_{bias} or power supply V_{DD} of the input and output sections respectively are taken from the primary winding bias port V_{b_i} and the secondary winding bias V_{b_o}, respectively as shown in Figure 6. As shown in Figure 6, the bias ports

are located diametrically opposite the connectors of the winding to which they belong and between the connectors of the other winding. This arrangement makes the circuit size more compact.

As indicated above by configuring the width (W) and radius (R) of each pair of primary and secondary windings such that at least one of the width and the radius is different for a one of the transformers relative to another one of the transformers, the matching condition in equation (7) can be obtained.

Dimensions of the required transformers for the five-stage amplifier circuit 400 were extracted by HFSS v.12 (High Frequency Structural Simulator version 12, available from ANSYS Inc. of Canonsburg, Pennsylvania, USA). A summary of the details of transformers and circuit components is given in Table 1. The power loss contribution of each transformer is about 1.5 dB.

It will be apparent that in an embodiment, the width of the transformer is kept the same for each of T_1-T_5 such that matching is achieved by varying the radius, e.g. such that a second transformer has a smaller radius than the first transformer. The final transformer T_6 has a larger width, in part, because it carries more power than the other transformers.

Varying the radius (R) of the transformer shifts the matching network into the correct frequency band. The effect of R is mostly related to varying the inductance and conductor losses (r1, r2) of the primary and secondary sections of the transformer in order to change the matching property of the network. It will be appreciated that for lower frequency bands, a larger R is required. However, if R is too large, the transformer will occupy a large physical area of the chip. In that case, more turns

are required for the transformer. In order to have an appropriate bandwidth, R of each stage is chosen to cover a wide frequency range.

Varying the width (W) of the transformer changes the coupling coefficient k between the primary and secondary sections of the transformer and hence the capacitance of the matching network. In addition, wider width W allows a higher maximum power and results in lower conductor losses (r1, r2).

Table 1 - Detailed Circuit Components of the Proposed Power Amplifier

Component	Value
V_{DD}	1.2 V
C_n	8 fF
C_x	260 fF
R_x	248 Ω
M_1, M_2	50/0.06 μm/μm
M_3, M_4	60/0.06 μm/μm
M_5, M_6	70/0.06 μm/μm
M_7, M_8	80/0.06 μm/μm
M_9, M_{10}	100/0.06 μm/μm
I_{Ref}	100 μA
C_s	62 fF
(Z_i, θ_i)	(56 Ω, 11°)
$T_1(W_1, R_1)$	(5 μm,21 μm)
$T_2(W_2, R_2)$	(5 μm,19 μm)
$T_3(W_3, R_3)$	(5 μm,18 μm)
$T_4(W_4, R_4)$	(5 μm,17 μm)
$T_5(W_5, R_5)$	(5 μm,17 μm)
$T_6(W_6, R_6)$	(5.4 μm,25 μm)

Experimental Results

The power amplifier circuit 400 was fabricated using a 65-nm CMOS process with eight metal layers: a micrograph of the amplifier circuit 400 is shown in Figure 7. The size of the power amplifier including input/output and DC pads is 0.4 x 0.85 mm^2.

On-wafer S-parameter measurements up to 100 GHz have been performed by a ME7808B Broadband VNA produced by Anritsu Corporation of Kanagawa Japan and a probe station produced by Suss MicroTec of Garching, Germany. Figure 8 shows the S-parameter measurement results for the power amplifier 400. The measured results show very good matching at input S_{11} and output S_{22} ports with return losses less than -10 dB in the 67-100 GHz frequency range. The transmission gain (S_{21}) of the power amplifier is 18.5 dB at 77 GHz.

Figure 9 shows the measured reverse isolation of the power amplifier 400. The isolation between input and output (S_{12}) is better than -42 dB within the bandwidth from 65 to 100 GHz range. At 77 GHz, the reverse isolation is about -48 dB.

To perform output power measurement, a 60 GHz passive up-mixer was used to up-convert a 17 GHz signal to a 77 GHz input signal before feeding to the amplifier 400. Then, the 77 GHz output signal of the amplifier is down-converted to 17 GHz by a 60 GHz passive down-mixer before connecting to a 40 GHz spectrum analyzer (an MS2668C spectrum analyser produced by Anritsu Corporation of Kanagawa). Calibration for the conversion loss has been taken into account for this measurement.

Figure 10 shows the output power performance the power amplifier 400 in terms of gain 1010, output power 1020 and power added efficiency (PAE) 1030. The measured results show that an output compression point (OP_{1dB}) of +9.5 dBm and a saturated output power of +10.5 dBm were measured at

77 GHz.

As can be seen from the results, a constant gain of 18.5 dB with good linearity has been achieved for input power less than -10 dBm and maximum PAE of 7.1 %. The DC power consumption of the power amplifier 400 is 150 mW.

The performance of the power amplifier circuit 400 is compared in Table 2 with the CMOS 77 GHz power results described in the following references:

[1] T. Suzuki, Y. Kawano, M. Sato, T. Hirose and K. Joshin, "60 and 77 GHz power amplifier in standard 90 nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 562-563. Feb. 2008.

[2] B. Wicks, E. Skafidas, and R. Evans, "A 77-95 GHz Wideband CMOS Power Amplifier," *Microwave Integrated Circuit Conf.*, pp. 555-559. Feb. 2008.

[3] J. Lee, C. C. Chen, J. H. Tsai, K. Y. Lin and H. Wang, "A 68-83 GHz power amplifier in 90 nm CMOS," *2009 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 437-440, June 2009.

[4] Y. A. Li, M. H. Hung, S. J. Huang, and J. Lee, "A Fully-Integrated 77 GHz FMCW Radar System in 65 nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 216-217, Feb. 2010.

[5] T. Y. Chang, C. S. Wang, and C. K. Wang, "A 77 GHz power amplifier using transformer-based power combiner in 90 nm CMOS," *Proc IEEE CICC*, pp. 1-4, Sept. 2010.

It will be apparent from Table 2 that power amplifier 400 provides the highest gain with competitive output power and relatively compact size.

Table 2 - Comparison With Published CMOS mm-Wave Power Amplifier Results

	Ref [1]	Ref [2]	Ref [3]	Ref [4]	Ref [5]	5-stage amplifier
Technology	90nm CMOS	130nm CMOS	90nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS
Frequency (GHz)	77	77	68-83	77	77	76-77
P_{sat} [dBm]	6.3	8.1	11	10.5	13.2	10.5
P_{1dB} [dBm]	4.7	6.3	7.5	6.7	11.2	9.5
PAE [%]	-	0.5	6.5	8.4	10.4	7.1
ain [dB]	8.5	6	17.6	13.7	9.9	18.5
Voltage Supply [V]	1.2	2.5	2.4	1.2	1.2	1.2
Power Consumption [mW]	142.2	337.5	379	115	140.4	150
Chip Size [mm2]	0.675	0.64	0.656	NA	0.105[a]	0.34

([a]Pads are excluded from the chip size in Ref [5])

In the claims which follow and in the preceding description of the invention, except where the context requires otherwise due to express language or necessary implication, the word "comprise" or variations such as "comprises" or "comprising" is used in an inclusive sense, i.e. to specify the presence of the stated features but not to preclude the presence or addition of further features in various embodiments of the invention.

It is to be understood that, the reference to prior art publications does not constitute an admission that the publication form part of the common general knowledge in the art in any country.

CLAIMS:

1. A multi-stage CMOS power amplifier circuit comprising a plurality of amplifier stages connected by respective ones of a plurality of transformers, wherein each transformer comprises a first winding in a first metal layer of a CMOS chip and a second winding arranged in a second metal layer of the CMOS chip superimposed on the first winding, wherein:

the first and second windings of each transformer have a width and a radius; and

impedance matching between the amplifier stages is provided by the width and the radius of the respective transformers.

2. A multi-stage CMOS power amplifier circuit as claimed in claim 1, wherein the first winding of at least one of the plurality of transformers has a first winding bias port for providing a voltage to one or more transistors of a connected amplifier stage.

3. A multi-stage CMOS power amplifier circuit as claimed in claim 2, wherein the first winding comprises a loop between two first winding connectors for connecting to an amplifier stage and the bias port is located opposite the two first winding connectors.

4. A multi-stage CMOS power amplifier circuit as claimed in any one of claims 1 to 3, wherein the second winding of at least one of the plurality of transformers has a second winding bias port for providing a voltage to one or more transistors of a connected amplifier stage.

5. A multi-stage CMOS power amplifier circuit as claimed in claim 4, wherein the second winding comprises a loop between two connectors for connecting to an amplifier

stage and the bias port is located opposite the two connectors.

6. A multi-stage CMOS power amplifier circuit as claimed claim 3, wherein:

the second winding of said at least one of the plurality of transformers has a second winding bias port for providing a voltage to a connected amplifier stage;

the second winding comprises a loop between two second winding connectors for connecting to an amplifier stage; and

the second winding bias port of the second winding is located opposite the two second winding connectors and the first winding bias port.

7. A multi-stage CMOS power amplifier circuit as claimed in any one of claims 1 to 6, comprising five amplifier stages.

8. A multi-stage CMOS power amplifier circuit as claimed in any one of claims 1 to 7, wherein at least one of the width and the radius is different for a first one of the transformers relative to a second one of the transformers.

9. A multi-stage CMOS power amplifier circuit as claimed in claim 1, wherein a first transformer connected to an input of an input amplifier has a first width and a first radius and a second transformer connected to an output of the input amplifier has a second radius smaller than the first radius.

10. A multi-stage CMOS power amplifier circuit as claimed in claim 9, wherein a last transformer connected to an output of an output amplifier has a last transformer width greater than said first width and a last transformer radius greater than said first radius.

11. A multi-stage CMOS power amplifier circuit as claimed in claim 9 or claim 10, wherein said input amplifier stage comprises a pair of transmission lines for input matching of the circuit.

12. A multi-stage CMOS power amplifier circuit as claimed in any one of claims 1 to 11, wherein each amplifier stage comprises:

first and second transistors;

first and second RC circuits each comprising a resistor and capacitor connected in parallel, the first and second RC circuits connected between the respective gates of the first and second transistors and first and second ports of a transformer which provides the input to the respective amplifier stage; and

first and second cross-coupling capacitors, the first cross-coupling capacitor connected between the gate of the first transistor and the drain of the second transistor and the second cross-coupling capacitor connected between the gate of the second cross-coupling capacitor and the drain of the first transistor.

13. A differential CMOS power amplifier for a multi-stage transformer connected amplifier circuit, the power amplifier comprising:

first and second transistors;

first and second RC circuits each comprising a resistor and capacitor connected in parallel, the first and second RC circuits connected between the respective gates of the first and second transistors and first and second input ports of the amplifier circuit; and

first and second cross-coupling capacitors, the first cross-coupling capacitor connected between the gate of the first transistor and the drain of the second transistor and the second cross-coupling capacitor connected between the gate of the second cross-coupling capacitor and the drain of the first transistor.

14. A differential CMOS power amplifier as claimed in claim 13, comprising a pair of transmission lines for input matching of the circuit.

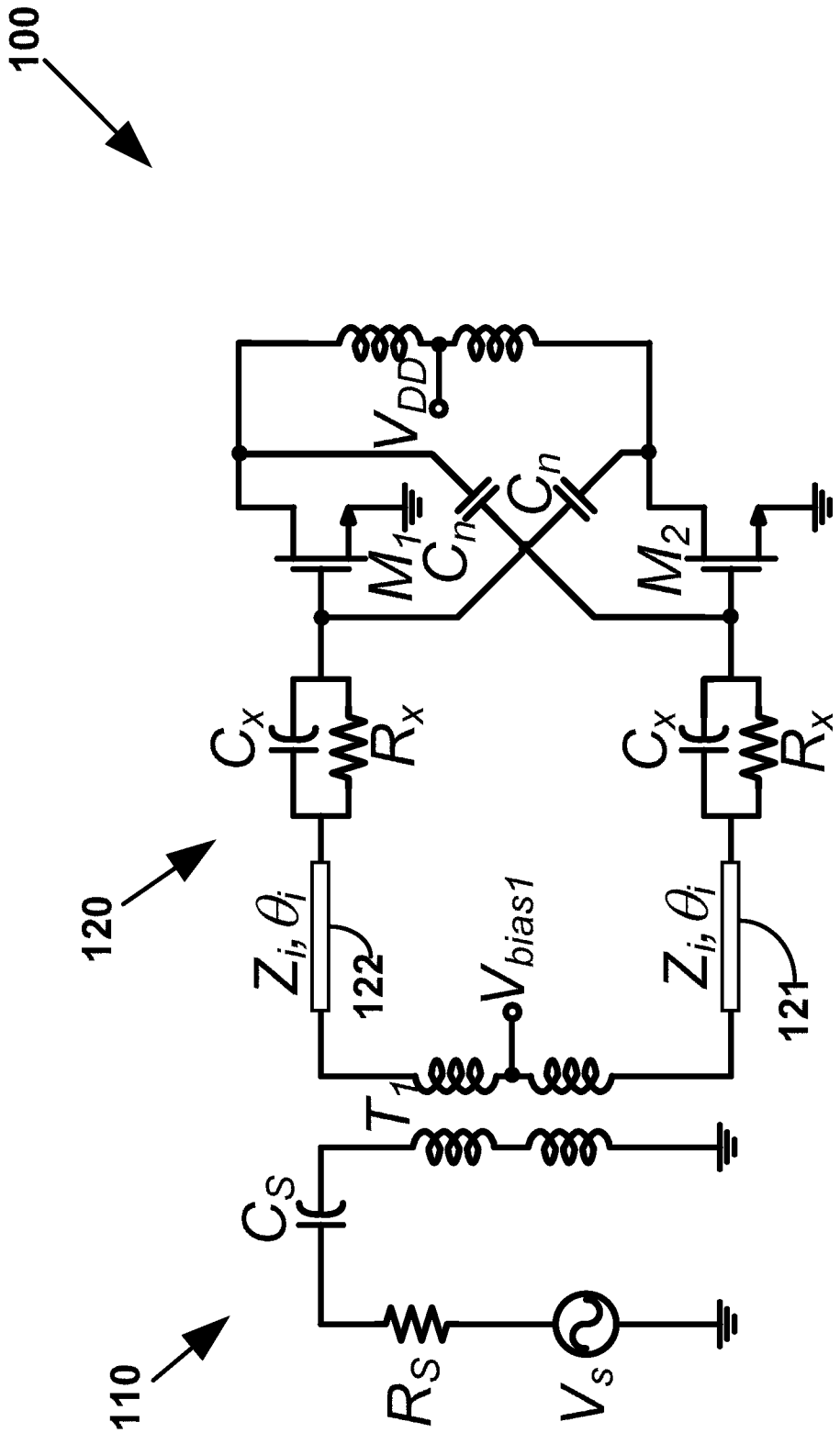
100
V_{DD}
C_n
C_n
M_1
M_2
C_x
R_x
C_x
R_x
120
Z_i, θ_i
122
V_{bias1}
Z_i, θ_i
121
T_1
C_S
110
R_S
V_s

Figure 1

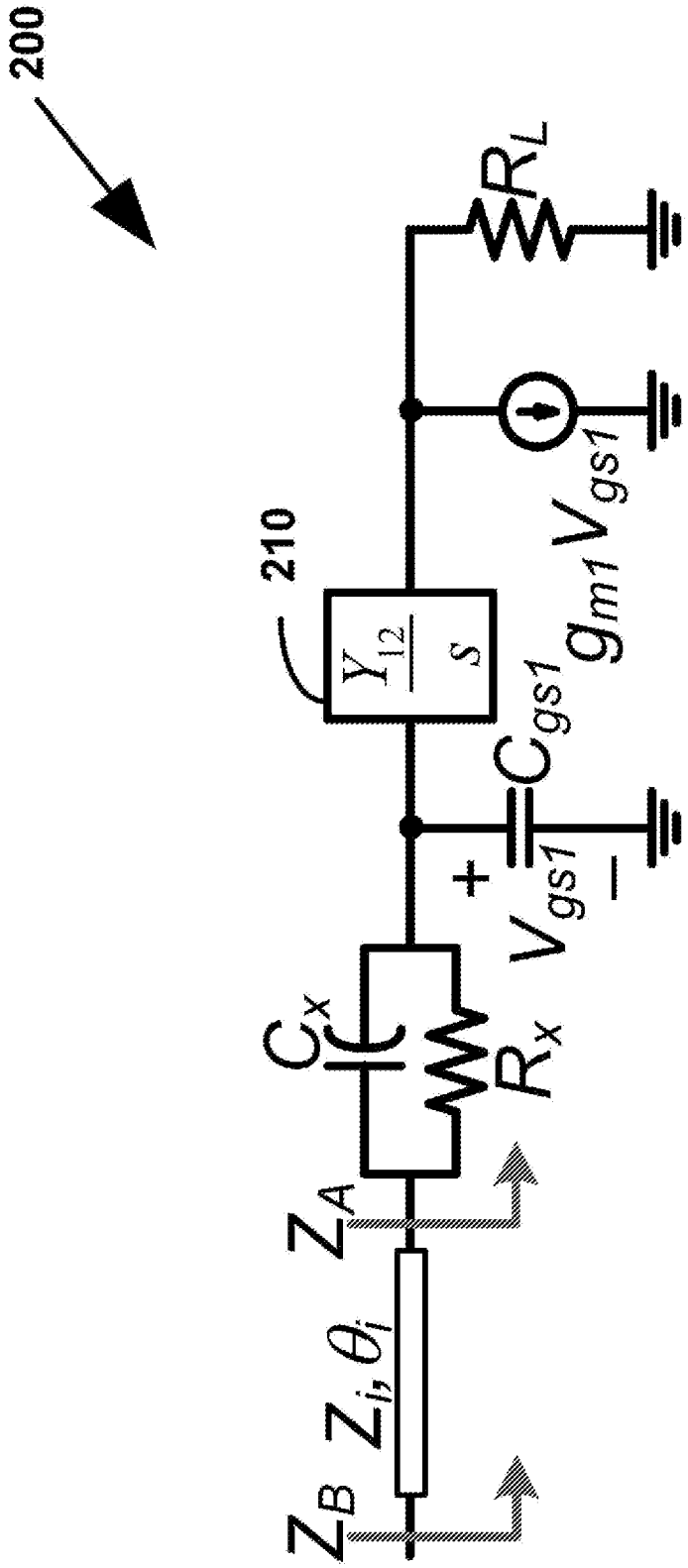

Figure 2

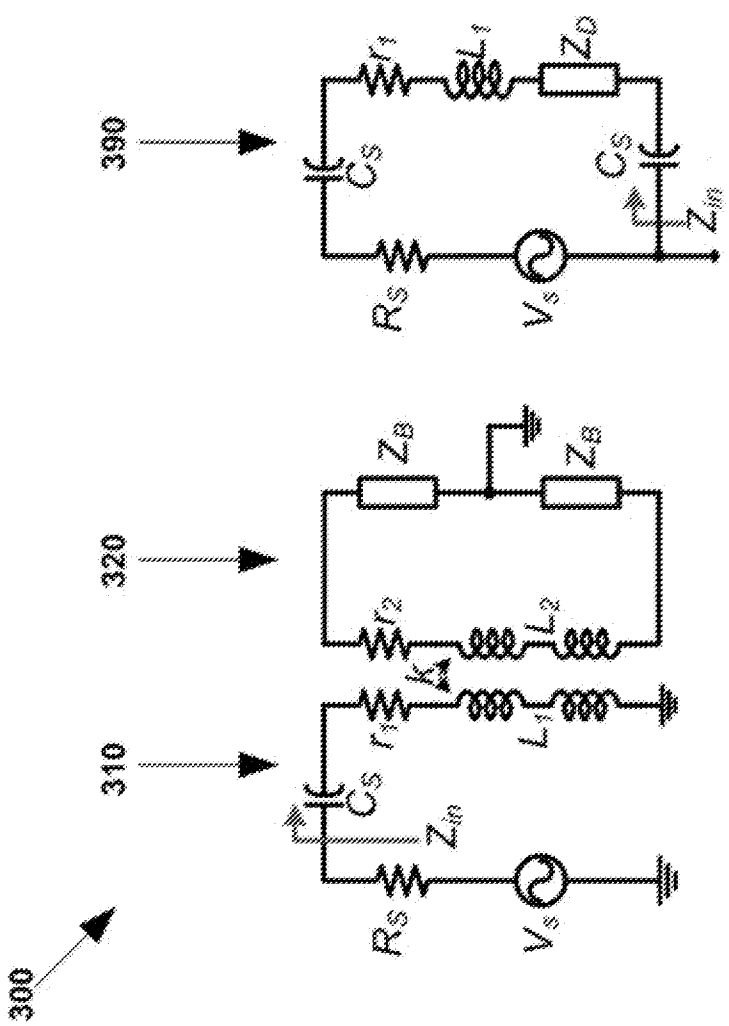

Figure 3A

Figure 3B

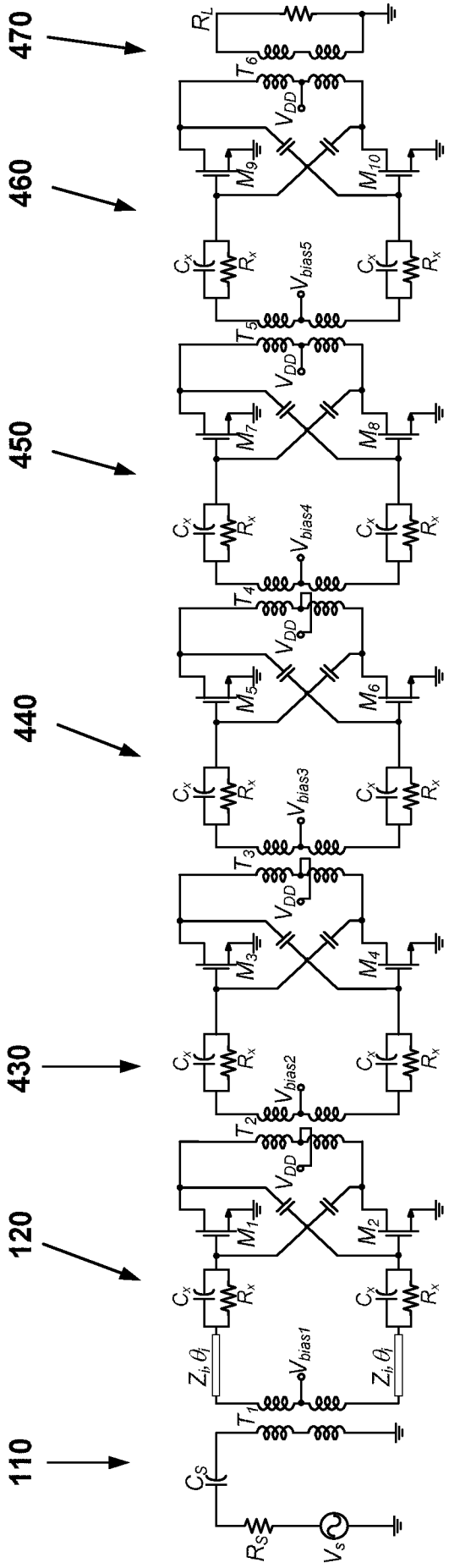
110
120
430
440
450
460
470
C_S
R_S
V_s
T_1
T_2
T_3
T_4
T_5
T_6
M_1
M_2
M_3
M_4
M_5
M_6
M_7
M_8
M_9
M_{10}
V_{DD}
V_{bias1}
V_{bias2}
V_{bias3}
V_{bias4}
V_{bias5}
C_x
R_x
Z_i, θ_i
R_L

Figure 4

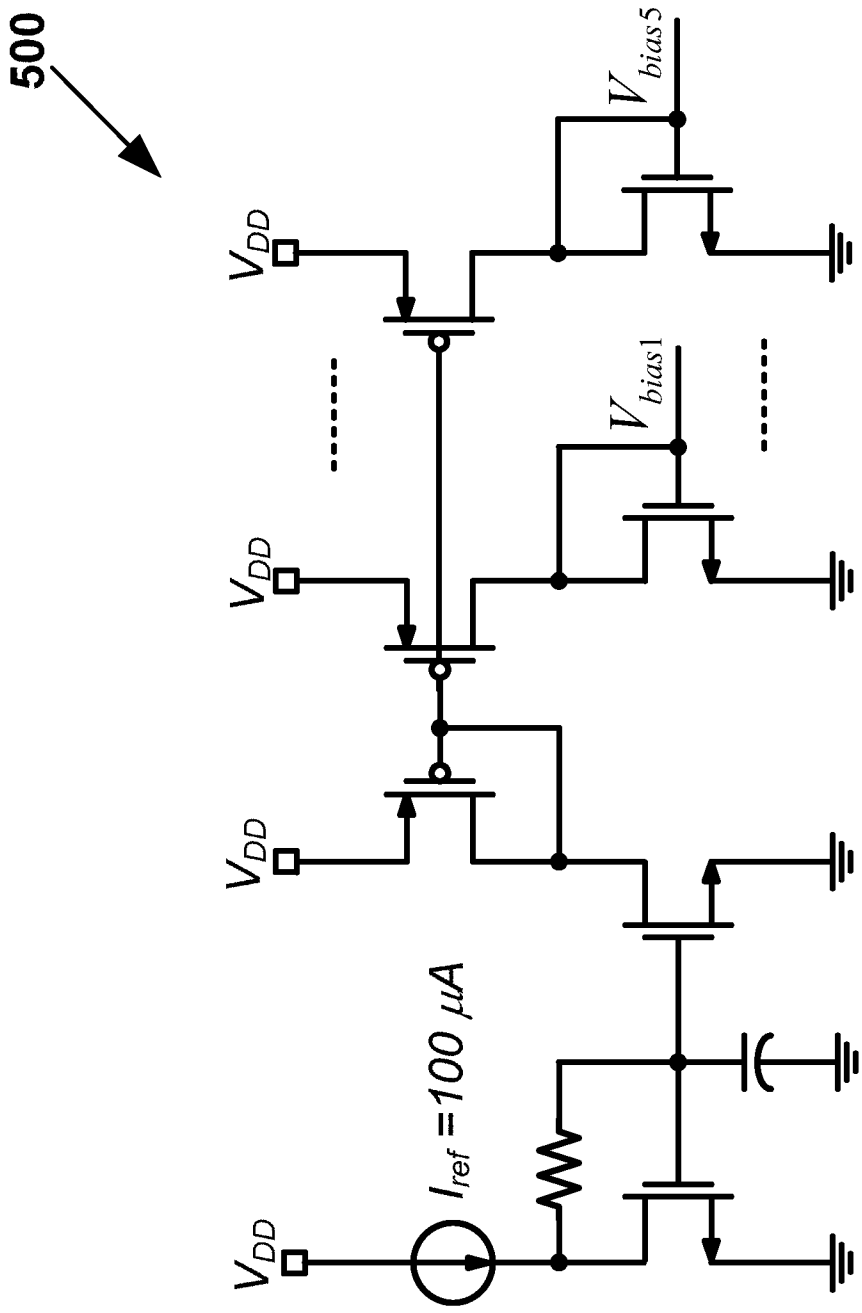

Figure 5

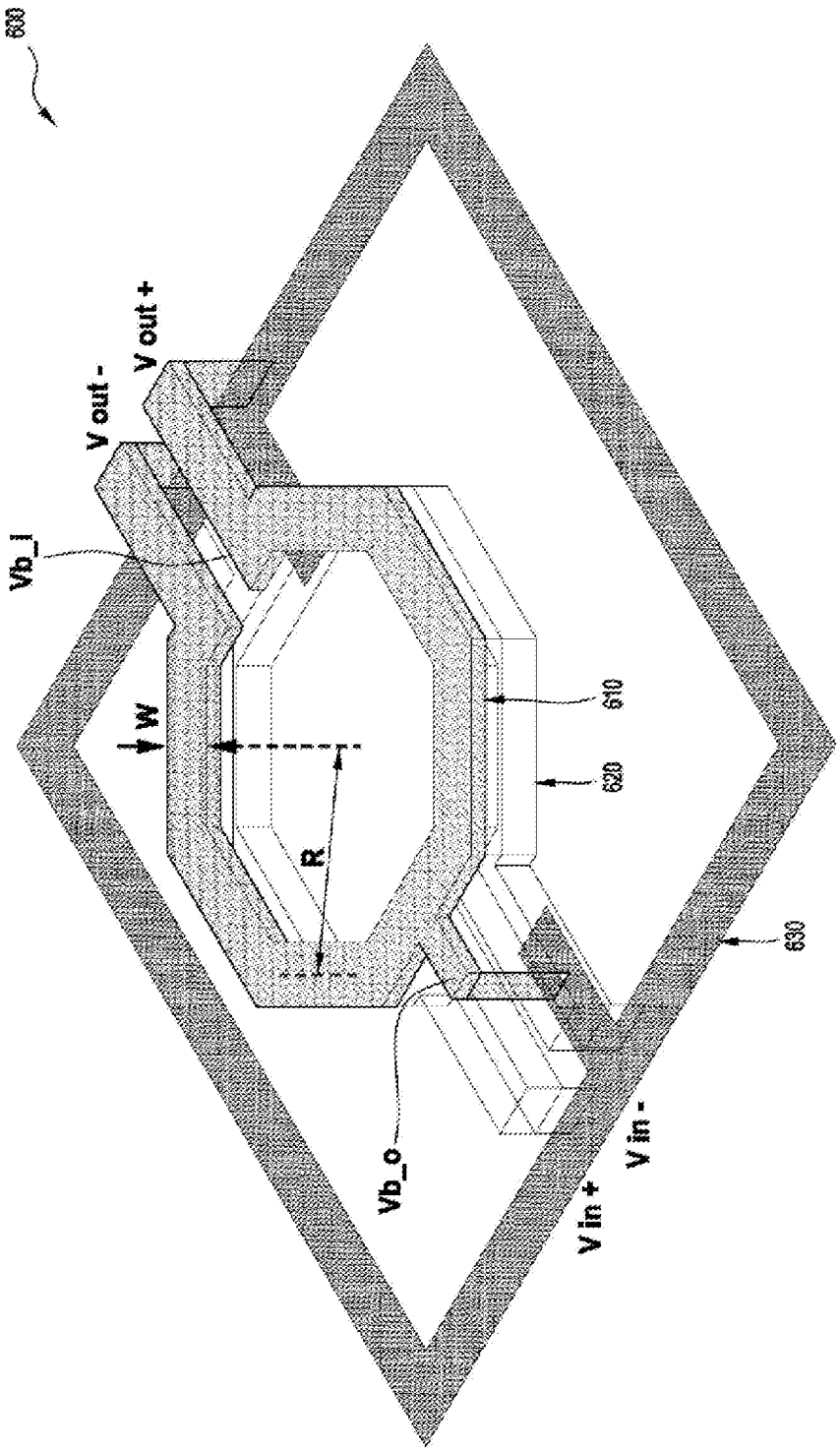

Figure 6

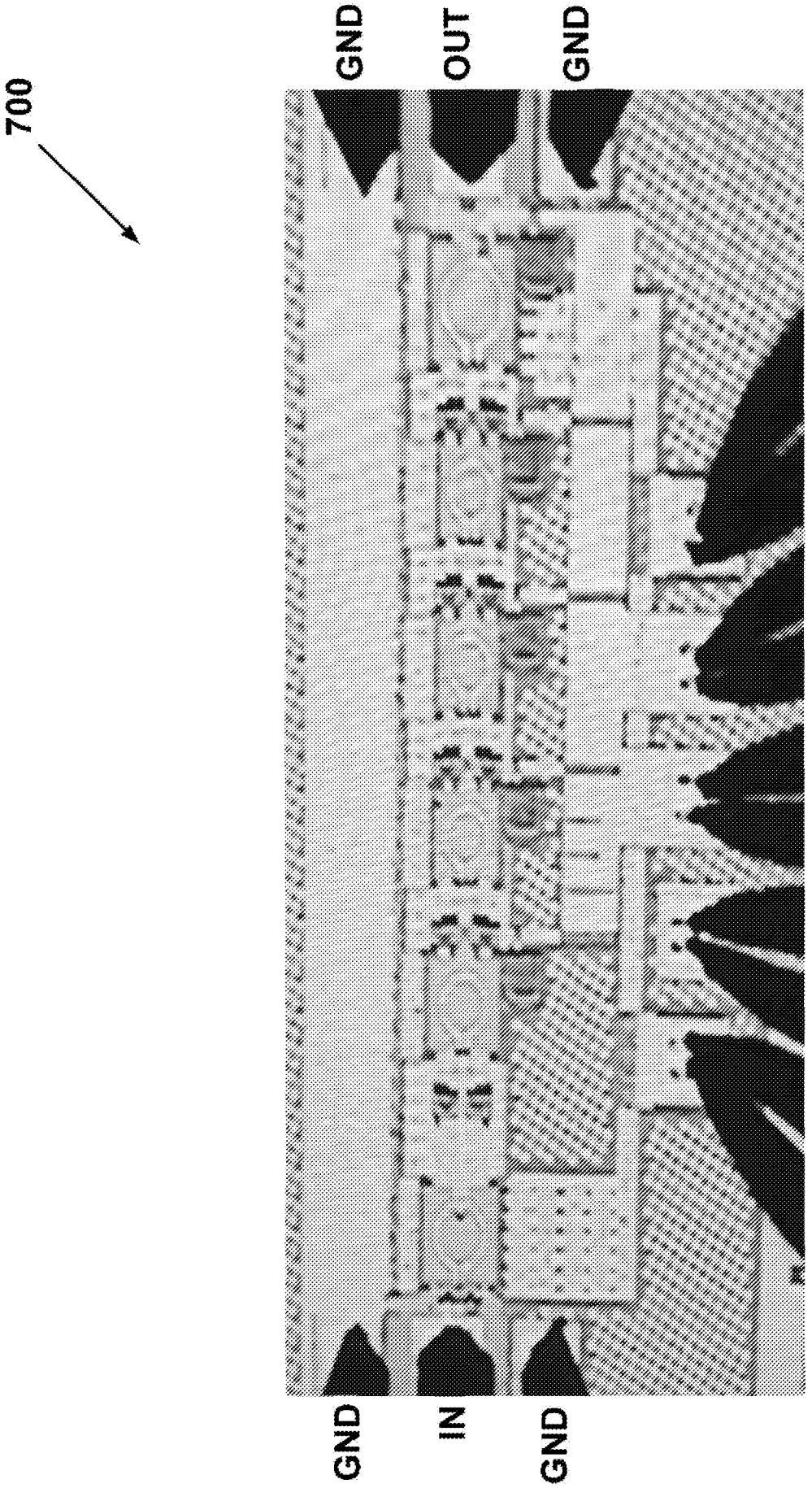

Figure 7

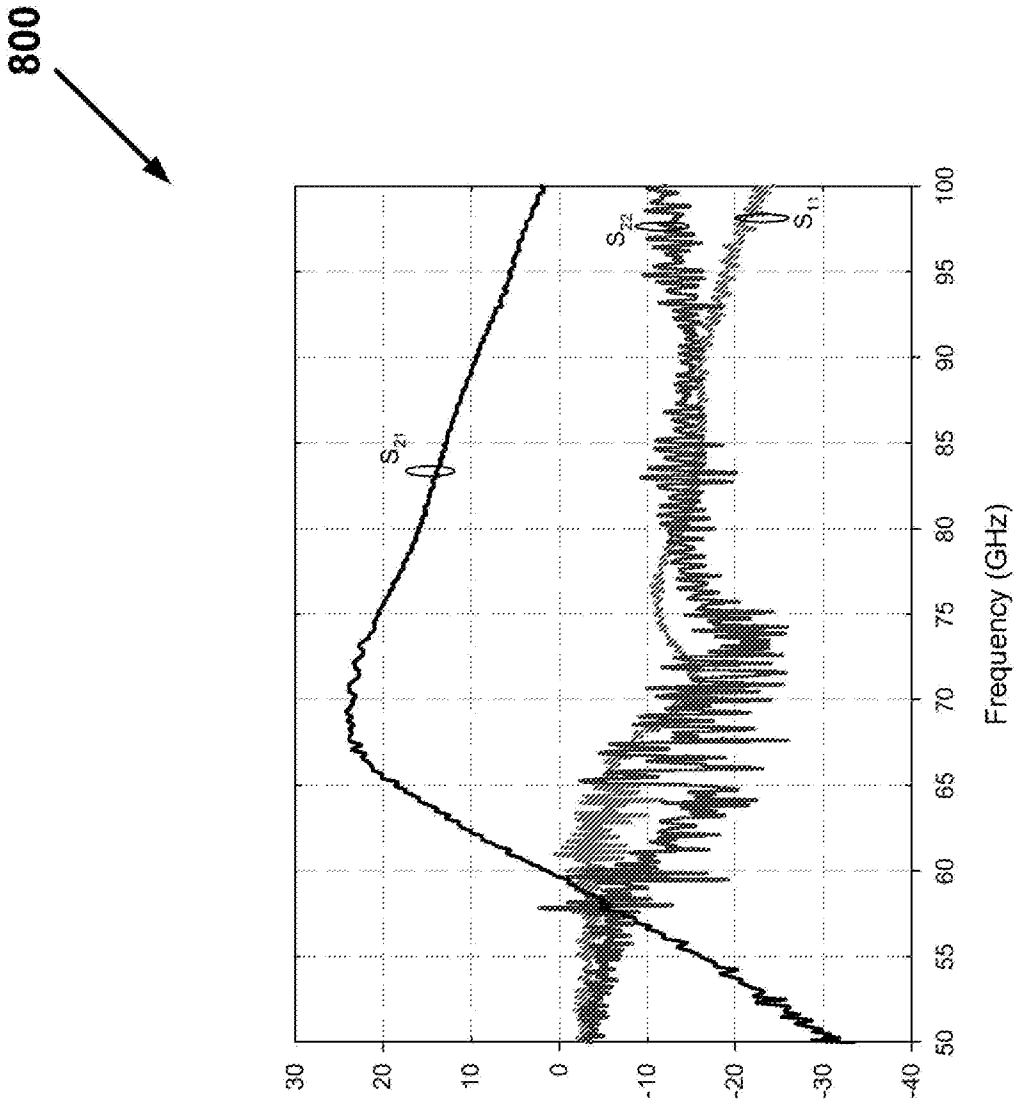
800
30
20
10
0
-10
-20
-30
-40
50
55
60
65
70
75
80
85
90
95
100
Frequency (GHz)
S21
S22
S11

Figure 8

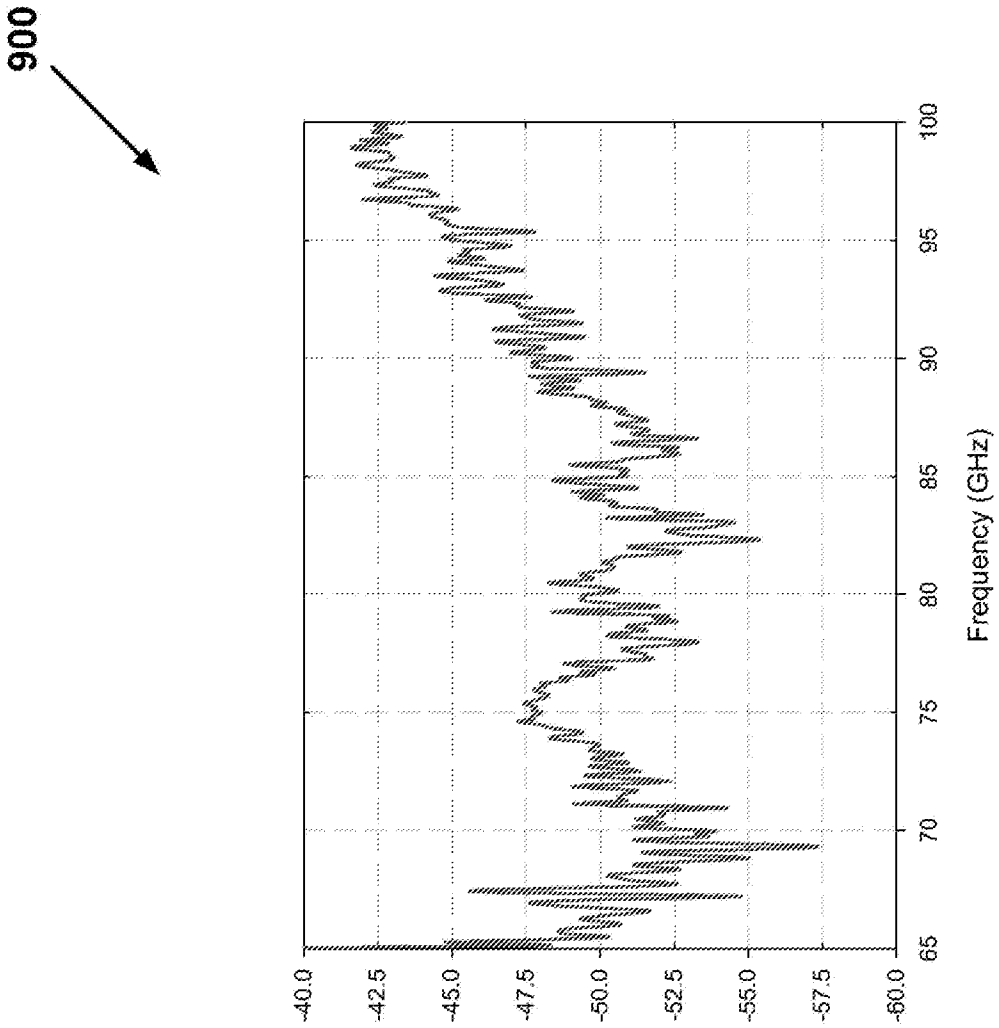
900
-40.0
-42.5
-45.0
-47.5
-50.0
-52.5
-55.0
-57.5
-60.0
65
70
75
80
85
90
95
100
Frequency (GHz)

Figure 9

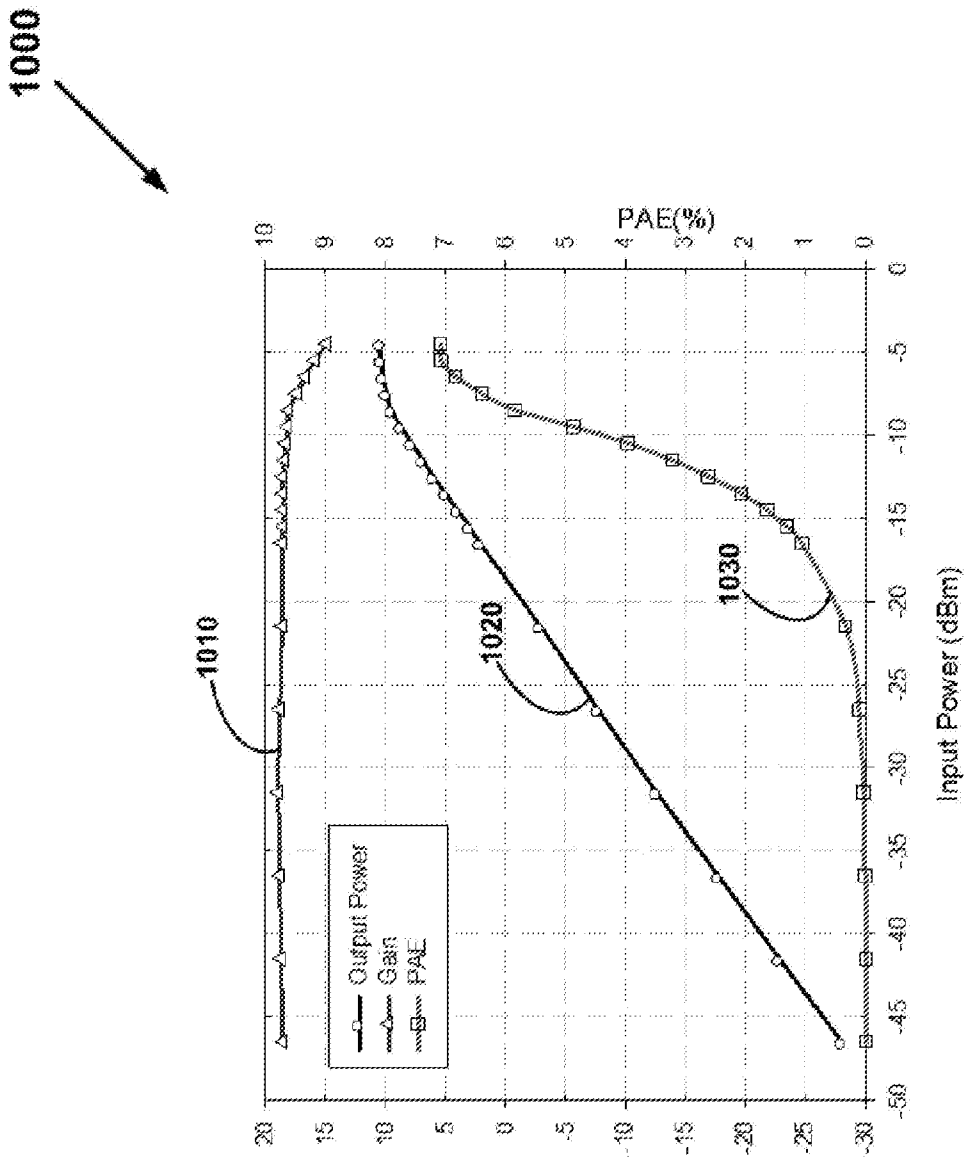
1000
PAE(%)
Input Power (dBm)
Output Power
Gain
PAE
1010
1020
1030

Figure 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2014/000936

A. CLASSIFICATION OF SUBJECT MATTER

H03F 3/213 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Searched EPODOC, WPI, INSPEC using keywords: CMOS, amplifier, transformer, stage, impedance match, width, radius, layer, and other similar terms.

Searched Google Patents and Google Scholar using keywords: transformer, coupled, stage, CMOS, amplifier, metal layer, impedance matching, differential, and other similar terms.

Searched Google Patents using the applicant and inventor names, and searched Google Scholar using the inventor names.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 December 2014	18 December 2014
Name and mailing address of the ISA/AU	**Authorised officer**
AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaustralia.gov.au	Shuchin Taher AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. 0262832862

INTERNATIONAL SEARCH REPORT C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		International application No. **PCT/AU2014/000936**
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CHOWDHURY, D. et al., 'Design Considerations for 60 GHz Transformer-Coupled CMOS Power Amplifiers', *IEEE Journal of Solid-State Circuits, 2009*, vol. 44, no.10, pages 2733-2744. See the whole document, in particular, the abstract, fig. 9, 13, 20, 21, section II, III and V.	1-12
A	DUONG, H. T. et al., 'A 77 GHz automotive radar transmitter in 65-nm CMOS', *IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), 2012*, pages 171-173. See the whole document.	
A	Bi, X. et al., '60GHz unilateralized CMOS differential amplifier', *International Conference on Microwave and Millimeter Wave Technology (ICMMT), 2010*, pages 204-207. See the whole document.	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2014/000936

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:

because they relate to subject matter not required to be searched by this Authority, namely:

the subject matter listed in Rule 39 on which, under Article 17(2)(a)(i), an international search is not required to be carried out, including

2. ☐ Claims Nos.:

because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos:

because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See Supplemental Box for Details

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-12

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT	International application No. PCT/AU2014/000936

Supplemental Box

Continuation of: **Box III**

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

This Authority has found that there are different inventions based on the following features that separate the claims into distinct groups:

• **Claims 1-12** are directed to a multi-stage CMOS power amplifier circuit. The features recited as follows are specific to this group of claims: "*each transformer comprises a first winding in a first metal layer of a CMOS chip and a second winding arranged in a second metal layer of the CMOS chip superimposed on the first winding, wherein: the first and second windings of each transformer have a width and a radius; and impedance matching between the amplifier stages is provided by the width and the radius of the respective transformers*"

• **Claims 13-14** are directed to a differential CMOS power amplifier: The features recited as follows are specific to this group of claims: "*the power amplifier comprising: first and second transistors; first and second RC circuits each comprising a resistor and capacitor connected in parallel, the first and second RC circuits connected between the respective gates of the first and second transistors and first and second input ports of the amplifier circuit; and first and second cross-coupling capacitors, the first cross-coupling capacitor connected between the gate of the first transistor and the drain of the second transistor and the second cross-coupling capacitor connected between the gate of the second cross-coupling capacitor and the drain of the first transistor*"

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

When there is no special technical feature common to all the claimed inventions there is no unity of invention.

In the above groups of claims, the identified features may have the potential to make a contribution over the prior art but are not common to all the claimed inventions and therefore cannot provide the required technical relationship. The only feature common to all of the claimed inventions is **a multi-stage transformer connected CMOS power amplifier circuit**. However it is considered that this feature is generic in the art.

Therefore this common feature cannot be a special technical feature. Hence there is no special technical feature common to all the claimed inventions and the requirements for unity of invention are consequently not satisfied *a priori*.

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/AU2014/000936**

This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document/s Cited in Search Report		**Patent Family Member/s**	
Publication Number	**Publication Date**	**Publication Number**	**Publication Date**

End of Annex

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.