Title: DUTY CYCLE TRANSLATOR METHODS AND APPARATUS

Abstract: Methods and apparatus for translating duty cycle information in duty-cycle-modulated signals to higher frequencies or higher data rates. An exemplary duty cycle translator includes a duty cycle evaluator, a high-speed digital counter, and a comparator. The duty cycle evaluator generates a first digital number representing a duty cycle of a low-frequency input duty-cycle-modulated (DCM) signal. The comparator compares the first digital number to a second digital number generated by the high-speed digital counter, and generates, based on the comparison, an output DCM signal having a higher frequency or data rate than the frequency or data rate of the low-frequency input DCM signal but a duty cycle that is substantially the same as the duty cycle of the low-frequency input DCM signal.
Duty Cycle Translator Methods and Apparatus

FIELD OF THE INVENTION

[0001] The present invention relates in general to electrical and electronic systems and in particular to methods and apparatus for translating duty cycle information in a duty-cycle-modulated signal to higher frequencies.

BACKGROUND OF THE INVENTION

[0002] Duty cycle modulation is a technique in which pulses, or a relationship among pulses, in a pulse wave are varied to encode information or control power delivery to a load. The term "duty cycle" refers to the fraction of time a duty-cycle-modulated (DCM) signal is active high over some specified interval of time, often the time interval between consecutive rising edges of the pulse waveform. In general, duty cycle may be used to describe periodic, semi-periodic, and aperiodic DCM signals. In a periodic DCM signal, for example, the interval of time corresponds to the period of the signal, and the duty cycle is defined for each signal period as the fraction of time during which the signal is high.

[0003] DCM signals are generated in various ways. In one commonly-used approach, pulse widths of a signal are varied to produce the desired DCM signal. DCM signals generated using this approach are referred to as a "pulse width modulated" or "PWM" signals. In another approach the pulse widths are fixed but the times between pulses are varied to produce a DCM signal having a variable pulse density. DCM signals generated by this latter approach are referred to as "pulse density modulated" or "PDM" signals or, alternatively, "pulse-frequency modulated" or "PFM" signals.
There are various circumstances where it is necessary or it would be desirable to translate duty cycle information in DCM signals to higher frequencies or higher data rates. The present invention addresses these needs and desires.

SUMMARY OF THE INVENTION

Methods and apparatus for translating duty cycle information in duty-cycle-modulated signals to higher frequencies or higher data rates are disclosed. An exemplary duty cycle translator includes a duty cycle evaluator, a high-speed digital counter, and a comparator. The duty cycle evaluator generates a first digital number representing a duty cycle of a low-frequency input duty-cycle-modulated (DCM) signal. The comparator compares the first digital number to a second digital number generated by the high-speed digital counter, and generates, based on the comparison, an output DCM signal having a higher frequency or data rate than the frequency or data rate of the low-frequency input DCM signal but a duty cycle that is substantially the same as the duty cycle of the low-frequency input DCM signal.

Further features and advantages of the invention, including descriptions of the structure and operation of the above-summarized and other exemplary embodiments of the invention, will now be described in detail with respect to accompanying drawings, in which like reference numbers are used to indicate identical or functionally similar elements.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a duty cycle translator, according to an embodiment of the present invention;
FIG. 2 is a circuit diagram of a duty cycle translator, according to an embodiment of the present invention;

FIGS. 3A and 3B are signal diagrams illustrating how the output duty-cycle-modulated (DCM) signal $S_{out}$ (FIG. 3B) of a duty cycle translator of the present invention has a higher frequency than the input DCM signal $S_{in}$ (FIG. 3A) but the same duty cycle;

FIG. 4 is a circuit diagram of a duty cycle translator, according to an embodiment of the present invention;

FIG. 5 is a diagram of direct current to direct current (DC-DC) converter, according to an embodiment of the present invention;

FIG. 6 is diagram of a digital-to-analog converter (DAC), according to an embodiment of the present invention;

FIG. 7 is diagram of a switching amplifier, according to an embodiment of the present invention;

FIG. 8 is a diagram of a power supply module for a light emitting device, according to an embodiment of the present invention;

FIG. 9 is a schematic diagram of an exemplary DCM signal generator that may be used to generate the low-frequency DCM signal in the power supply module in FIG. 8; and

FIGS. 10A-D are signal diagrams of signals generated by the DCM signal generator in FIG. 9.
DETAILED DESCRIPTION

[00017] Referring to FIG. 1, there is shown an exemplary duty cycle translator 100, according to an embodiment of the present invention. The duty cycle translator 100 comprises first and second digital counters 102 and 104, a phase-locked loop (PLL) 106, a latch (or other similar memory device) 108, and a digital magnitude comparator 110, and may be formed using discrete components, one or more integrated (IC) chips, or a combination of discrete components and IC chips. As explained in detail below, the duty cycle translator 100 operates to translate an input duty-cycle-modulated (DCM) signal $S_{in}$ to a higher frequency output DCM signal $S_{out}$ while preserving the duty cycle information contained in the original input DCM signal $S_{in}$. In some of the exemplary embodiments described below, the input DCM signal $S_{in}$ is described as being periodic. However, as will be appreciated by those of ordinary skill in the art with the benefit of the detailed description that follows, the duty translator methods and apparatus of the present invention are not limited to operating on periodic DCM signals. Accordingly, for the purpose of this disclosure, the term "duty-cycle-modulated signal" will refer to and incorporate within its meaning periodic, aperiodic, and variable periodicity (i.e., semi-periodic) signals, including, for example, pulse-width modulated (PWM) signals and pulse-density modulated (PDM) signals (i.e., pulse-frequency modulated (PFM) signals).

[00018] The first digital counter 102 and latch 108 are configured to generate an n-bit digital number representing the duty cycle of the input DCM signal $S_{in}$, and together comprise one way of implementing what may be referred to as a "duty cycle evaluator." The first digital counter 102 is configured to receive the input DCM signal $S_{in}$ at its enable (EN) input, and the latch 108 is configured to receive the input DCM signal $S_{in}$ at
its clock (CLK) input. The clock input of the first digital counter 102 is configured to receive a first digital counter clock signal of frequency $f_i = K_1 \times f_{in}$, where $K_1$ is a resolution factor and $f_{in}$ is the input frequency of the input DCM signal $S_{in}$. The first digital counter clock signal is generated by the PLL 106 (or other suitable clock generating or recovery circuit) based on pulse transitions in the input DCM signal $S_{in}$.

[00019] Upon detecting a rising edge of a pulse in the input DCM signal $S_{in}$, the first digital counter 102 commences counting from zero, at a rate $f_1$, and continues counting until the latch 108 detects the falling edge of the pulse, at which time the present count of the first digital counter 102 is latched into the latch 108 and coupled to the "B" input of the digital magnitude comparator 110. The present count is represented by an n-bit digital number that is proportional to the width (i.e., duration) of the pulse and is representative of the duty cycle of the input DCM signal $S_{in}$ for the period being measured. The first digital counter 102 and latch 108 repeat this count and latch operation on subsequent pulses in the input DCM signal $S_{in}$, generating and latching a unique count for each pulse received.

[00020] The second digital counter 104 is configured to repeatedly and continuously count from zero to $K_2-1$, according to a second digital counter clock applied to the clock (CLK) input of the second digital counter 104. The second digital counter clock has a frequency $f_2 = K_2 \times f_{out}$, where $K_2$ is a resolution factor, $f_{out} = M \times f_{in}$ is the frequency of a high-frequency clock, and $M$ is an integer or non-integer multiplier greater than unity. The count from the second digital counter 104 is an m-bit digital number that is coupled to the "A" input of the digital magnitude comparator 110.

[00021] The resolution factors $K_1$ and $K_2$ of the first and second digital counters 102
and 104 may be integers or non-integers. In one embodiment of the invention, K1 and K2 are both integer powers of two, such that \(2^n = K_1\) (\(n = \log_2 K_1\)) and \(2^m = K_2\) (\(m = \log_2 K_2\)). Using K1 and K2 that are integer powers of two is beneficial in that it affords the ability to implement the duty cycle translator 100 using low-cost digital circuitry. K1 and K2 may also be equal or unequal. In one embodiment of the invention \(K_1 = K_2 = 2^7 = 128\) so that \(n = m = 7\), thereby providing seven-bit resolution for each of the first and second digital counters 102 and 104.

[00022] The low-frequency input clock and high-frequency output clock may or may not be related. In one embodiment of the invention, the two clocks are harmonically related such that \(f_{\text{out}} = M \times f_{\text{in}}\) and \(M\) is positive integer representing the harmonic order of the high-frequency clock. As illustrated in FIG. 2, harmonically related clocks requires the use of only a single PLL 206 to generate the first and second digital counter clocks for the first and second digital counters 102 and 104.

[00023] Following each pulse in the input DCM signal \(S_{\text{in}}\), the digital magnitude comparator 110 compares the n-bit digital number held by the latch 108 and representing the duration of the pulse to the continuously incrementing count from the second digital counter 104. As the second digital counter 104 counts from zero, its count eventually exceeds the count held by the latch 108, causing the "A < B" output of the digital magnitude comparator 110 to transition low. Because the high-frequency clock has a frequency \(f_{\text{out}}\) that is \(M\) times higher than the frequency \(f_{\text{in}}\) of the low-frequency input clock, i.e., because \(f_{\text{out}} = M \times f_{\text{in}}\), the second digital counter 104 completes \(M\) count cycles (each count cycle ranging from 0 to \(K_2-1\)) for each period \(1/f_{\text{in}}\) of the low-frequency input clock. The digital count at input A becomes greater than the count applied to input
B once during each of these $M$ count cycles. Accordingly, the "A < B" output of the digital magnitude comparator 110, which is the output from which the desired output DCM signal $S_{out}$ is produced, also transitions from high to low $M$ times for each period $1/\text{fin}$ of the low-frequency input clock, the transition times depending on the width of the particular pulse being processed.

Whereas the duty cycle translator 100 operates to increase the input frequency from $f_{in}$ to $f_{out}$, the duty cycle information in the output DCM signal $S_{out}$ remains unchanged from the duty cycle information contained in the original input DCM signal $S_{in}$. This is illustrated in FIGS. 3A and 3B, where for a multiplier $M = 4$ and periodic input DCM signal $S_{in}$, having an input duty cycle of 25% and frequency $f_{in}$ (FIG. 3A), the duty cycle translator 100 translates the input signal $S_{in}$ to an output signal $S_{out}$ having a 4X higher output frequency $f_{out} = M \times f_{in} = 4f_{in}$ but unchanged duty cycle of 25% (FIG. 3B).

The exemplary duty cycle translator 100 in FIG. 1 works well for input DCM signals $S_{in}$ that are periodic, such as PWM signals. For input DCM signals $S_{in}$ that are aperiodic or have a variable periodicity, the duty cycle translator 400 shown in FIG. 4 may be used. The duty cycle translator 400 may be referred to as a "generalized" duty cycle translator since it is operable to translate duty cycle information for input DCM signals $S_{in}$ of all types, including periodic, aperiodic, and variable-periodicity or semi-periodic signals.

The generalized duty cycle translator 400 comprises a duty cycle evaluator 401 that includes first and second digital counters 402 and 404 and a digital divider 406; a third digital counter 408; and a digital magnitude comparator 410. The first and second
digital counters 402 and 404 are configured to count at a measuring clock rate \( f_1 \) determined by the desired or required measuring resolution, and measure the period and active high time (i.e., pulse duration) of each cycle of the input DCM signal \( S_{in} \). The first digital counter 402 is edge-triggered and counts between consecutive rising edges of the incoming input DCM signal \( S_{in} \). The second digital counter 404 is level-triggered and counts during times when the input DCM signal \( S_{in} \) is active high. At the end of each cycle of the input DCM signal \( S_{in} \), a divide command commands the digital divider 406 to divide the count at the output of the second digital counter 404 by the count at the output of the first digital counter 402, thereby producing an \( n \)-bit digital number representing the duty cycle of the input DCM signal \( S_{in} \) for that cycle of the input DCM signal \( S_{in} \). Immediately following the divide command, the first and second digital counters 402 and 404 are reset to zero and counting begins for the next cycle of the input DCM signal \( S_{in} \). In general, because the input DCM signal \( S_{in} \) has a variable periodicity and variable duty cycle, the digital divider 406 produces a unique \( n \)-bit digital number for each cycle of the input DCM signal \( S_{in} \).

[00027] The third digital counter 408 is configured to repeatedly and continuously count from zero to \( K2-1 \) count (zero to \( K2-1 \) is one "count cycle") at a rate \( f_2 \), where \( f_2 > fout > f_1 \), producing an \( m \)-bit digital number. The digital magnitude comparator 410 is configured to compare the incrementing \( m \)-bit digital number to the \( n \)-bit digital number produced by the duty cycle generator 401. (Note that the most-significant bits of the \( m \)-and \( n \)-bit digital numbers are aligned at the "A" and "B" inputs so that each digital number represents a fraction ranging from 0 and 1.) At the beginning of each count cycle of the third digital counter 408, the \( m \)-bit digital number is zero, so the "A < B" output of
the digital magnitude comparator 410, which is the output from which the desired output DCM signal $S_{out}$ is produced, is high. Eventually the m-bit digital number increments to a value that exceeds the n-bit digital number from the duty cycle generator 401, and the "A < B" output of the digital magnitude comparator 410 drops and remains low until the full count cycle (0 to K2-1) completes. Once the count cycle has completed, the third digital counter 408 resets to zero and a new count cycle is started.

[00028] The third digital counter 408 completes multiple count cycles for each period of the input DCM signal $S_{in}$, the total number of count cycles completed depending on how much higher $f_{out}$ is compared to the measuring clock frequency $f_i$ and on the duration of the next adjacent cycle of the input DCM signal $S_{in}$. This result is an output DCM signal $S_{out}$ having a higher frequency $f_{out}$ (or data rate) than the input DCM signal $S_{in}$, but the same duty cycle information.

[00029] Duty cycle translators similar to the duty cycle translators 100 and 400 described above are employed in various application-specific embodiments of the invention described below.

[00030] FIG. 5 is a block diagram of a switch-mode direct current to direct current (DC-DC) converter 500 that employs a duty cycle translator 506 similar to the duty cycle translator 100 or duty cycle 400, according to an embodiment of the present invention. The DC-DC converter 500 comprises one or more high-speed switches (e.g., bipolar junction transistors (BJTs) or field effect transistors (FETs) 502), a duty cycle modulation (DCM) regulator 504, the duty cycle translator 506, an energy storage inductor 508, and an output capacitor 510.

[00031] The DC-DC converter 500 is formed using discrete components, one or more
IC chips, or a combination of discrete components and IC chips. In one embodiment, for example, the DCM regulator 504, duty cycle translator 506, and high-speed switches are formed in a single IC chip. In another embodiment, the DCM regulator 504 and duty cycle translator 506 are formed in a first silicon-based IC chip (e.g., as manufactured according to a standard complementary metal-oxide-semiconductor (CMOS) semiconductor manufacturing process), and the high-speed switches 502 are formed in a second, compound-semiconductor-based (e.g., silicon carbide (SiC), gallium arsenide (GaAs), gallium nitride (GaN), indium phosphide (IP)) IC chip.

[00032] The DC-DC converter 500 operates by alternately coupling and decoupling the energy storage inductor 508 to and from the DC input by controlling the one or more high-speed switches 502 in response to a high-frequency DCM control signal generated by the duty cycle translator 506. When the high-speed switches 502 cause the energy storage inductor 508 to be coupled to the DC input, current through the energy storage inductor 508 rises linearly while energy builds up and is stored in the inductor's 508's magnetic field. When the high-speed switches 502 switch and decouple the energy storage inductor 508 from the DC input, the inductor current falls linearly and energy that had been previously stored in the inductor's 508's magnetic field discharges into the output capacitor 510 and DC-DC converter's load 512. The output capacitor 510 is selected to have a capacitance such that the R-C time constant, where R represents the load resistance of the load 512 and C represents the capacitance of the output capacitor 510, is much longer than the period of the high-frequency DCM control signal. This results in a DC output voltage $V_{\text{out}}$ which on average equals the DC input voltage $V_{\text{i}}$ multiplied by the duty cycle of the high-frequency DCM control signal, i.e., $V_{\text{out,avg}} = D \times$
The output of the DC-DC converter 500 is regulated by feeding back the DC output voltage $V_{out}$ to the DCM regulator 504. In one embodiment of the invention, the DCM regulator 504 comprises a PWM regulator configured to generate a PWM signal having a frequency $f_i$ and a duty cycle that varies depending on to what degree the actual output voltage deviates from its desired value. The duty cycle translator 506 is substantially similar to the duty cycle translator 100 or duty cycle translator 400 shown and described above in connection with FIG. 1 and FIG. 4, and operates to translate the DCM signal to a high-frequency DCM signal having the same duty cycle information as the DCM signal. Driving the one or more high-speed switches 502 using the high-frequency DCM signal (instead of using the lower-frequency DCM signal) allows much smaller energy storage inductor 508 and output capacitor 510 values to be used. Indeed, for a high-frequency clock that is one hundred times higher than the low-frequency input clock, i.e., for $f_{out} = M \times f_{in} = 100 \times f_{in}$, the energy storage inductor 508 and output capacitor 510 values can be reduced by as much as 99%.

FIG. 6 is a block diagram of a sigma-delta digital-to-analog converter (DAC) 600 that employs a duty cycle translator 604 similar to the duty cycle translator 100 or duty cycle translator 400, according to an embodiment of the present invention. The sigma-delta DAC 600 comprises a sigma-delta modulator 602, the duty cycle translator 604 and a low-pass filter (LPF) 606. Like the DC-DC converter 400, the DAC 600 is formed using discrete components, one or more IC chips, or a combination of discrete components and IC chips.

The sigma-delta modulator 602 operates to transform a multi-bit digital input
signal (e.g., a pulse code modulated (PCM) signal) to a single-bit serial signal. The single-bit serial signal may contain a series of fixed-width pulses, the density of pulses over time representing the magnitude of the digital input signal. This single-bit serial signal may be referred to as a pulse-density modulated (PDM) signal. Similar to a PWM signal, the PDM signal is a DCM signal, the only difference being in how the duty cycle $D = t/T$ is modulated. For the PWM signal, the signal period $T$ is fixed and $t$ is allowed to vary within $0 < t < T$, whereas for the PDM signal, $t$ is fixed and modulation is accomplished by varying the low time $(T - t)$ between consecutive pulses.

[00036] The duty cycle translator 604 of the sigma-delta DAC 600 is similar to the duty cycle translator 100 shown and described above. It operates to generate a high-speed DCM signal having a higher speed (i.e., pulse rate) but same duty cycle information as the DCM signal produced at the output of the sigma-delta modulator 602. The high-speed DCM signal is coupled to the input of the LPF 606. The LPF 606 functions essentially to average the high-speed DCM signal. Accordingly, since the density of pulses in the high-speed DCM signal represents the average amplitude of the input signal over time, the analog version of the original multi-bit digital input signal from the high-speed DCM signal is recovered by the LPF 606. Using the duty cycle translator 604 allows the LPF component values to be made smaller than would otherwise be required, by as much as the ratio $f_{\text{out}}/f_{\text{in}}$, where $f_{\text{in}}$ is the frequency of the DCM signal applied to the duty cycle translator input and $f_{\text{out}} = M \times f_{\text{in}}$ is the frequency of the high-frequency clock of the duty cycle translator 604.

[00037] FIG. 7 is a block diagram of a switching amplifier 700 that employs a duty cycle translator 704 similar to the duty cycle translator 100 or duty cycle translator 400,
according to an embodiment of the present invention. The switching amplifier 700 comprises a sigma-delta modulator 702, the duty cycle translator 704, a switching stage 706, an inductor 708, and an output capacitor 710, and is formed using discrete components, one or more IC chips, or a combination of discrete components and IC chips. In one embodiment, the sigma-delta modulator 702 and duty cycle translator 704 are formed in one IC chip and the components of the switching stage 706 are formed in a second IC chip. In another embodiment, the sigma-delta modulator 702, duty cycle translator 704, and switching stage 706 are all formed in a single IC chip.

[00038] The sigma-delta modulator 702 and duty cycle translator 704 function similar to the sigma-delta modulator 702 and duty cycle translator 704 of the sigma-delta DAC 700 in FIG. 7, creating complementary high-speed DCM signals at the "A < B" and "A > B" outputs of the duty cycle translator 704. The complementary high-speed DCM signals have a higher pulse rate than the lower-speed DCM signal applied to the input of the duty cycle translator 704 but have the same duty cycle information as the lower-speed DCM signal. (It should be pointed out that rather than using the sigma-delta modulator 702 to generate the DCM signal, a pulse-width modulator can be alternatively used, similar to as in conventional Class-D switching amplifier. The DCM (PWM) signal produced by the pulse-width modulator would then be translated to a higher frequency using the duty cycle translator 704.)

[00039] The switching stage 706 of the switching amplifier 700 comprises first and second transistors 712 and 714, such as metal-oxide-semiconductor field-effect transistors (MOSFETs), metal-semiconductor FETs (MESFETs), heterojunction BJTs, high-electron-mobility transistors (HEMTs), or other suitable switching devices.
gates of the first and second transistors 712 and 714 are driven by the complementary high-speed DCM signals produced at the "A < B" and "A > B" outputs of the duty cycle translator 704. Depending on the type and input characteristics of the transistors 712 and 714 used for the switching stage, an output driver and/or level-shifter may be included between the output of the duty cycle translator 704 and switching stage 706, as will be appreciated and understood by those of ordinary skill in the art. (It should be mentioned that for similar reasons an output driver and/or level-shifter may also be used in the DC-DC converter 500 in FIG. 5 and in other embodiments of the invention.)

[00040] The output of the switching stage 706 is fed to the inductor 708 and output capacitor 710, which together form an LPF. The L-C LPF has a cut-off frequency much lower than the switching frequency of the switching stage 706. Hence, switching energy from the switching stage 706 is prevented from reaching the load 716 (which in the case of an audio input comprises one or more speakers). The L-C LPF also functions to average the output signal of the switching stage 706 to form an amplified analog signal (e.g., an audio signal) having signal characteristics corresponding to the modulation in the original digital input signal. Similar to the DC-DC converter 400 described above, employing the duty cycle translator 704 affords the ability to use smaller-sized and lower-valued components for the L-C LPF.

[00041] FIG. 8 is a block diagram of a light-emitting diode (LED) power supply module 800 for an LED light bulb or other light-emitting device, according to an embodiment of the present invention. The LED power supply module 800 comprises an alternating current to direct current (AC-DC) converter 802, a regulator 804, a DCM signal generator 806, and a duty cycle translator 808. Like the other embodiments of the
invention, the LED power supply module 800 is formed using discrete components, one or more IC chips, or a combination of discrete components and IC chips. As explained in further detail below, the duty cycle translator 808 is configured to generate a high-frequency DCM signal for controlling the dimming of a plurality of LEDs 812, which may be connected in series, parallel, or individually controlled and powered as described in U.S. Patent Application No. 12/897,066, entitled "Power Conversion and Control Systems and Methods for Solid-State Lighting," which is hereby incorporated by reference.

[00042] The AC-DC converter 802 comprises a rectifier and switch-mode, step-down converter or transformer, as is understood by those of ordinary skill in the art. Alternatively, a direct conversion AC-DC converter is used, such as, or similar to, the rectifier-less direct conversion AC-DC converter described in co-pending and commonly assigned U.S. Patent Application No. 12/841,608, entitled "AC/DC Power Conversion Methods and Apparatus," which is hereby incorporated by reference. Employing a direct conversion AC-DC converter of this type is advantageous in that it reduces parts count and manufacturing costs, lowers power consumption, and results in an overall reduction in size of the LED power supply module 800.

[00043] The DC voltage $V_{\text{DC}}$ produced at the output of the AC-DC converter 802 is supplied to the regulator 804. The regulator 804 comprises a current or voltage regulator for regulating the voltage $V_{\text{LED}}$ supplied across, or current $I_{\text{LED}}$ flowing through, the plurality of LEDs 812.

[00044] The DCM signal generator 806 is configured to generate a low-frequency DCM signal from a dimmer-modified AC input voltage $V_{\text{in}}'(\text{AC})$ provided by the
TRIAC dimmer switch 810. The DCM signal generator 806 may be implemented in various ways. FIG. 9 is schematic diagram of an exemplary DCM signal generator 900 that may be used. The DCM signal generator 900 comprises first and second comparators 902 and 904, an inverting amplifier 906, a first voltage divider including resistors 908 and 910 (or, alternatively, capacitors), a second voltage divider including resistors 912 and 914 (or, alternatively, capacitors), and an OR logic gate 916. The first and second voltage dividers may not be necessary depending on the acceptable input voltage ranges of the various amplifiers. If, however, the dimmer-modified AC input voltage Vin'(AC) is not within the acceptable input ranges, it is scaled down using the first and second voltage dividers. Specifically, the first voltage divider scales the dimmer-modified AC input voltage Vin'(AC) down to a scaled, dimmer-modified AC input voltage aVin'(AC) so that the voltage is within the acceptable input voltage range limit of the first and second comparators 902 and 904, and the second voltage divider scales the DC voltage Vin(DC) from the output of the AC-DC converter 802 by the same amount to produce a scaled DC voltage aVin(DC). The first comparator 902 compares the scaled, dimmer-modified AC input voltage aVin'(AC) to the scaled DC voltage aVin(DC), producing a high output voltage level when Vin'(AC) > Vin(DC) and a low output voltage level when Vin'(AC) < Vin(DC). The inverting amplifier 906 inverts the scaled DC voltage aVin(DC) to produce a scaled, inverted DC voltage -aVin(DC). The second comparator 904 compares the scaled, inverted DC voltage -aVin(DC) to the scaled, dimmer-modified AC input voltage aVin'(AC), producing a high output voltage when Vin'(AC) < -Vin(DC) and a low output voltage when Vin'(AC) > -Vin(DC).

Finally, as illustrated in the timing signal diagrams in FIGS. 10A-D, the OR logic gate...
generates the desired low-frequency DCM signal, which has a logic high ("1") whenever |Vin'(AC)| > Vin(DC) and a logic low ("0") for all other times.

[00045] The low-frequency DCM signal has a duty cycle that varies depending on the dim setting of the TRIAC dimmer switch 810. The low-frequency DCM signal could be used to control the dimming of the plurality of LEDs 812 directly. However, to avoid any perceptibility of flickering, according to one embodiment of the invention it is first translated up in frequency by the duty cycle translator 808. Similar to the duty cycle translators 100 and 400 described above, the duty cycle translator 808 operates to translate the low-frequency DCM signal to a high-frequency DCM signal. Whereas the high-frequency DCM signal has a higher frequency it contains the same duty cycle information as the original, low-frequency DCM signal.

[00046] The high-frequency DCM signal is used to control the power available to the plurality of LEDs 812 depending on the dim setting of the TRIAC dimmer switch 810. In one embodiment, the regulator 804 comprises a current source that is controlled by the high-frequency DCM signal, thereby duty cycling the LED current I_{LED} in accordance with the duty cycle information in the high-frequency DCM signal.

[00047] While various embodiments of the present invention have been described, they have been presented by way of example and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail may be made to the exemplary embodiments without departing from the true spirit and scope of the invention. Accordingly, the scope of the invention should not be limited by the specifics of the exemplary embodiments but, instead, should be determined by the appended claims, including the full scope of equivalents to which such claims are entitled.
CLAIMS

What is claimed is:

1. A duty cycle translator, comprising:
   a duty cycle evaluator configured to receive an input duty-cycle-modulated (DCM) signal and generate a first digital number representing a duty cycle of the input DCM signal;
   a first digital counter configured to generate a second digital number; and
   a comparator configured to compare the first and second digital numbers and generate an output DCM signal having a higher frequency or higher data rate than a frequency or data rate of the input DCM signal and a duty cycle that is substantially the same as a duty cycle of the input DCM signal.

2. The duty cycle translator of Claim 1 wherein said duty cycle evaluator comprises:
   a second digital counter configured to generate a count representing a portion of a period of the input DCM signal during which the input DCM signal is high;
   a third digital counter configured to generate a count representing a period of the input DCM signal; and
   a divider configured to divide the count from said second digital counter by the count from said third digital counter to generate said first digital number.

3. The duty cycle translator of Claim 1 wherein said duty cycle evaluator
comprises:

- a second digital counter configured to generate said first digital number; and
- a memory device configured to store said first digital number while said comparator compares the first and second digital numbers.

4. The duty cycle translator of Claim 1 wherein said second digital counter is configured to complete $M$ count cycles for each period of the input DCM signal, where $M$ is a multiplier greater than or equal to one.

5. A duty cycle translator, comprising:

- a first digital counter configured to count at a first rate and generate a first digital number representing a duration of a pulse in an input duty-cycle-modulated (DCM) signal;
- a second digital counter configured to count at a second rate higher than the first rate of said first digital counter and generate a second digital number; and
- a comparator configured to compare the first digital number to the second digital number and generate an output DCM signal having a higher frequency or data rate than a frequency or data rate of the input DCM signal and a duty cycle that is substantially similar to a duty cycle of the input DCM signal.

6. The duty cycle translator of Claim 5, further comprising a memory device configured to:

- receive and store the first digital number generated by said first digital counter for
one period of the input DCM signal; and

for subsequent periods of the input DCM signal, receive and store digital numbers from said first digital counter representing durations of pulses in the subsequent periods.

7. The duty cycle translator of Claim 5 wherein said second digital counter is configured to complete $M$ count cycles for each period of the input DCM signal, where $M$ is a multiplier greater than or equal to one.

8. The duty cycle translator of Claim 5 wherein said first and second digital counters are configured to count at rates that are harmonically related.

9. The duty cycle translator of Claim 5 wherein said first and second digital counters are configured to count at rates such that the output DCM signal has a frequency or data rate $M$ times higher than a frequency or data rate of the input DCM signal.

10. A method of translating duty cycle information in a duty-cycle-modulated (DCM) to a higher frequency or data rate, comprising:

receiving an input DCM signal;

generating a first digital number representing a duty cycle of the input DCM signal at a first rate;

generating a second digital number at a second rate higher than said first rate; and

comparing the first and second digital numbers to form an output DCM signal having a higher frequency or data rate than a frequency or data rate of the input DCM
signal and a duty cycle that is substantially the same as a duty cycle of the input DCM signal.

11. The method of Claim 10 wherein generating the first digital number at the first rate comprises:

   generating a first count representing a portion of a period of the input DCM signal during which the input DCM signal is high;

   generating a second count representing a period of the input DCM signal; and

   a divider configured to divide said first count by said second count to generate said first digital number.

12. The method of Claim 10 wherein said second digital counter is configured to complete $M$ counts cycles for each period of the input DCM signal, where $M$ is a multiplier greater than or equal to one.

13. A direct current to direct current (DC-DC) converter, comprising:

   one or more switches configured to alternately couple an energy storage inductor to and from a DC input voltage at a rate of a high-frequency duty-cycle-modulated (DCM) signal; and

   a duty cycle translator configured to generate the high-frequency DCM signal from a lower-frequency DCM signal, the high-frequency DCM signal having a higher frequency or higher data rate than a frequency or data rate of the lower-frequency DCM signal and a duty cycle that is substantially the same as a duty cycle of the lower-
frequency DCM signal.

14. The DC-DC converter of Claim 13 wherein said duty cycle translator comprises:
   a duty cycle evaluator configured to generate a first digital number representing a duty cycle of the lower-frequency DCM signal;
   a first digital counter configured to generate a second digital number; and
   a comparator configured to compare the first and second digital numbers and generate the high-frequency DCM signal.

15. A digital-to-analog converter (DAC), comprising:
   a sigma-delta modulator configured to generate a low-speed duty-cycle-modulated (DCM) signal from a digital input signal;
   a duty cycle translator configured to generate a high-speed DCM signal from the low-speed DCM signal, the high-speed DCM signal having a duty cycle substantially similar to a duty cycle of the low-speed DCM signal; and
   a low-pass filter configured to generate an analog output signal from the high-speed DCM signal.

16. The DAC of Claim 15 wherein said duty cycle translator comprises:
   a duty cycle evaluator configured to generate a first digital number representing a duty cycle of the low-speed DCM signal;
   a first digital counter configured to generate a second digital number; and
a comparator configured to compare the first and second digital numbers and generate the high-speed DCM signal.

17. A switching amplifier, comprising:

- a sigma-delta modulator configured to generate a low-speed duty-cycle-modulated (DCM) signal from a digital input signal;
- a duty cycle translator configured to generate complementary high-speed DCM signals from the low-speed DCM signal, one of the complementary high-speed DCM signals having a duty cycle that is substantially similar to a duty cycle of the low-speed DCM signal; and
- a switching stage configured to receive the complementary high-speed DCM signals and alternately couple and decouple an inductor to and from a power supply according to the duty cycle of the high-speed DCM signal that has a duty cycle substantially similar to a duty cycle of the low-speed DCM signal.

18. The switching amplifier of Claim 17 wherein said duty cycle translator comprises:

- a duty cycle evaluator configured to generate a first digital number representing a duty cycle of the low-speed DCM signal;
- a first digital counter configured to generate a second digital number; and
- a comparator configured to compare the first and second digital numbers and generate the high-speed DCM signal.
19. A power supply module for a light-emitting device, comprising:

an alternating current to direct current (AC-DC) converter configured to generate
a DC power supply from AC power provided by the AC mains, said DC power supply for
powering one or more light-emitting devices;

a duty cycle modulation signal generator configured to generate a low-frequency
duty-cycle-modulated (DCM) signal from an AC dimming signal provided by a dimmer
switch coupled to the AC mains;

a duty cycle translator configured to generate a high-frequency DCM signal from
said low-frequency DCM signal, said high-frequency DCM signal having a duty cycle
substantially similar to a duty cycle of said low-frequency DCM signal; and

circuitry for controlling dimming of the one or more light-emitting devices in
accordance with the duty cycle of said high-frequency DCM signal.

20. The power supply module of Claim 19 wherein said duty cycle translator
comprises:

a duty cycle evaluator configured to generate a first digital number representing a
duty cycle of the low-frequency DCM signal;

a first digital counter configured to generate a second digital number; and

a comparator configured to compare the first and second digital numbers and
generate the high-frequency DCM signal.
The diagram shows a block diagram of a digital signal processing system. It includes:

- A Magnitude Comparator
- A Latch
- A Digital Counter
- A PLL

The inputs are labeled as: A > B, A = B, and A < B (Output DCM Signal S_{out}).

The outputs include:

- The output of the Digital Counter
- The output of the PLL

The equations shown are:

- \( f_2 = K_2 \times f_{out} \)
- \( f_1 = K_1 \times f_{in} \)

The diagram also includes connections labeled as m, n.
$S_{in}$, $f_{in}$, duty cycle = 25%

FIG. 3A

$S_{out}$, $f_{out} = 4f_{in}$, duty cycle = 25%

FIG. 3B
FIG. 6

Digital Input Signal

SIGMA-DELTA MODULATOR

DCM Signal

Clock

DUTY CYCLE TRANSLATOR

High-Freq Clock

High-Speed DCM Signal

ANALOG LOW-PASS FILTER

Analog Output Signal
FIG. 10A

Vin' (AC) > Vin (DC)

FIG. 10B

Vin' (AC) < -Vin (DC)

FIG. 10C

Low-Freq. DCM Signal

FIG. 10D
INTERNATIONAL SEARCH REPORT

International application No. PCT/US2011/060674

A. CLASSIFICATION OF SUBJECT MATTER
   IPC(8) - H03K 7/08 (2012.01)
   USPC - 375/238

   According to International Patent Classification (IPC) or to both national classification and IPC.

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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   USPC - 332/106, 186; 375/238

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
   MicroPatent, Google Patents, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Relevant to claim No.</th>
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Date of the actual completion of the international search: 02 March 2012
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