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(54) Benævnelse: **BAGSIDEINTEGRERET SPÆNDINGSREGULATOR TIL INTEGREREDE KREDSLØB**

(56) Fremdragne publikationer:
WO-A1-2017/160284
WO-A1-2019/133019
US-A1- 2012 012 990
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US-A1- 2019 333 876

DESCRIPTION

Description

BACKGROUND

[0001] Application specific integrated circuit (ASIC) packages which include one or more ASIC dies are becoming increasingly capable of processing at high speeds. As the processing speed of the ASIC dies continue to increase, the power consumed by the ASIC dies may also increase. The increase in power consumption by the ASIC dies may lead to an increase of heat within the ASIC package, which may cause components in the ASIC package to fail or reduce the performance of the ASIC package.

[0002] WO 2019/133019 A1 discloses semiconductor packages and a method of forming the semiconductor packages. A semiconductor package includes a base die disposed on an interposer. The semiconductor package also has a plurality of dies on top of one another to form a stack on the base die.

[0003] US 20122032340 A1 discloses a semiconductor device that has a TSV wafer and semiconductor die mounted over the TSV wafer. A channel is formed through the TSV wafer. An encapsulant is deposited over the semi-conductor die and TSV wafer. Conductive TMV are formed through the encapsulant over the conductive TSV and contact pads of the semiconductor die.

[0004] WO 2017/160284 A1 discloses stairstep interposers with integrated conductive shields, and related assemblies and techniques. An interposer includes an insulating material having a stairstep structure with a first step surface, a second step surface, and a bottom surface to face a package substrate.

[0005] US2019/333876 recites a method and an apparatus for power delivery to a die stack via a heat spreader.

SUMMARY

[0006] The invention is defined by the independent claim. Dependent claims specify embodiments thereof.

[0007] One aspect of the disclosure provides an integrated circuit (IC) package. The IC package may include a packaging substrate, an IC die and an integrated voltage regulator die. The IC die may include a metal layer and a silicon layer. The metal layer may be connected to the packaging substrate. The integrated voltage regulator die may be positioned adjacent to the silicon layer and connected to the packaging substrate via one or more through mold vias (TMVs) or through dielectric vias (TDVs).

[0008] In some instances, the integrated voltage regulator die is connected to the silicone layer by a power distribution network (PDN). In some examples, the PDN includes one or more through silicon vias (TSVs) within the silicon layer. In some examples, the PDN further includes a redistribution layer configured to provide power from the integrated voltage regulator die to the TSVs. In some examples, the TSVs and redistribution layer form an inductor.

[0009] In some instances, each of the one or more TMVs are connected to the packaging substrate on a first end by a flip chip bump and to the integrated voltage regulator die at a second opposite end.

[0010] In some instances, the silicon layer is connected to the packaging substrate via one or more flip chip bumps.

[0011] In some instances, the packaging substrate is configured to connect to a land grid array (LGA) socket or ball grid array (BGA) socket. In some examples, power is delivered to the integrated voltage regulator die via the LGA socket or the BGA socket. In some examples, the packaging substrate includes a redistribution layer configured to route the power from the LGA socket or the BGA socket to the one or more TMVs.

[0012] In some instances, the IC die may be an application specific integrated circuit (ASIC) die.

[0013] Another aspect of the technology is directed to an integrated circuit (IC) package including a packaging substrate, an application specific integrated circuit (ASIC) die, and an integrated voltage regulator die. The ASIC die may include a metal layer and a silicon layer, the metal layer being connected to the packaging substrate. The integrated voltage regulator die may be positioned adjacent to the silicon layer and connected to the packaging substrate via one or more through mold vias (TMVs) or through dielectric vias (TDVs), the integrated voltage regulator die configured to provide power to the ASIC die.

[0014] In some instances, the integrated voltage regulator die is connected to the silicone layer by a power distribution network (PDN). In some examples, the PDN includes one or more through silicon vias (TSVs) within the silicon layer, and the integrated voltage regulator die is configured to provide power to the ASIC die via the TSVs. In some examples, the PDN further includes a redistribution layer configured to provide power from the integrated voltage regulator die to the TSVs. In some examples, the TSVs and redistribution layer form an inductor.

[0015] In some instances, each of the one or more TMVs are connected to the packaging substrate on a first end by a flip chip bump and to the integrated voltage regulator die at a second opposite end.

[0016] In some instances, the silicon layer is connected to the packaging substrate via one or more flip chip bumps.

[0017] In some instances, the packaging substrate is configured to connect to a land grid array (LGA) socket or ball grid array (BGA) socket. In some examples, power is delivered to the integrated voltage regulator die via the LGA socket or the BGA socket. In some examples, the packaging substrate includes a redistribution layer configured to route the power from the LGA socket or the BGA socket to the one or more TMVs.

[0018] In some instances, the IC package further includes deep trench capacitors embedded into the silicon layer or stacked on the silicon layer for use by the integrated voltage regulator die.

DESCRIPTION OF THE DRAWINGS

[0019]

FIGURE 1 is a side cut-away view of an ASIC package with an integrated voltage regulator die in accordance with aspects of the disclosure.

FIGURE 2A is a top-down view of a package substrate in accordance with aspects of the disclosure.

FIGURE 2B is a view of the bottom of a packaging substrate in accordance with aspects of the disclosure.

FIGURE 3A is a side cut-away view of an ASIC package with an integrated voltage regulator die in accordance with aspects of the disclosure.

FIGURE 3B is an exploded, side cut-away view of a portion of an ASIC package in accordance with aspects of the disclosure.

FIGURE 4A is a side cut-away view of an ASIC package showing power delivery to an integrated voltage regulator die in accordance with aspects of the disclosure.

FIGURE 4B is a side cut-away view of an ASIC package showing power delivery to an ASIC die from an integrated voltage regulator die in accordance with aspects of the disclosure.

FIGURE 5 is a top-down view of a packaging substrate with interior and exterior connectors in accordance with aspects of the disclosure.

FIGURE 6 is a side cut-away view of an ASIC package showing data communication in accordance with aspects of the disclosure.

DETAILED DESCRIPTION

[0020] The technology relates generally to integrating a voltage regulator die onto the backside of an application specific integrated circuit (ASIC) package. For example, and as shown in FIGURE 1, the ASIC package 101 includes an ASIC die 103 including a silicon substrate 131 and one or more metal layers 133. The ASIC die 103 may be positioned such that the metal layer is adjacent to a packaging substrate 109. An integrated voltage regulator die 105 may be mounted to the backside of the ASIC die 103, adjacent to the silicon substrate 131. Power may be delivered to the ASIC die 103 by the integrated voltage regulator die 105 using a backside power distribution network PDN 107 including through-silicon vias (TSVs) 171 and a redistribution layer 173. The ASIC package 201 may include a housing, such as housing 140 in which at least some of the components of the ASIC package 101 may be positioned.

[0021] As previously described, increases in processing speed of an ASIC die may increase the amount of power required to operate the ASIC die. An increase in power drawn by an ASIC die within a typical ASIC package may result in an increase of heat within the ASIC package due to copper losses generated by the wires and/or other such connections which carry the power through the ASIC package. Copper losses, also known as "I^2R losses", where 'I' is the current flowing through the copper wiring and 'R' is the resistance of the wiring, is the amount of heat dissipated as current passes through wiring. The increase in temperature generated by the increased power draw of the ASIC die may result in solder electromigration and potential failure of solder joints. The increase of temperature may also affect the thermal performance of the ASIC die and other components within the ASIC package, potentially leading to failure of the ASIC die, failure of other components of the ASIC package, or reduced processing performance.

[0022] To reduce or remediate the amount of copper losses generated by wires, planes, such as copper planes, redistribution layers, and/or other such connections which carry the power through the ASIC package to the ASIC die, a voltage regulator may be integrated into the ASIC package

[0023] The packaging substrate 109 may be configured to connect the ASIC package 101 to a circuit board or other such chip carrier. In this regard, the packaging substrate 109 may have arrays of connectors on its top side and bottom side, as shown in FIGURES 2A and 2B, respectively. In some instances, connectors may be included on the sides of the packaging substrate 109. Referring to FIGURE 1, although the packaging substrate 109 is shown as being outside of housing 140, the packaging substrate 109 may be positioned fully or partially within the housing 140.

[0024] Referring to FIGURE 2A, a top side 119 of the packaging substrate 109 shows a plurality of connectors, including connectors 191-193. For clarity, only a portion of the connectors on the top side 119 of the packaging substrate 109 are labeled. The connectors, including connectors 191-193, may be connector pads onto which other components of the ASIC package 101 may be connected, as described herein. The connector pads may be gold, nickel, tin, copper, solder, or other such conductive materials.

[0025] The top side 119 of the packaging substrate 109 may include any number of connector pads arranged in any layout. In this regard, the arrangement and number of connectors, including connector pads 191-193, shown in FIGURE 2A is merely for illustration. For instance, the number and arrangement of connector pads on the top side of the packaging substrate may be based on the design and arrangement of the ASIC die 103, integrated voltage regulator die 105, and/or other components within the ASIC package 101 to allow for the ASIC package to attach to the top side of the packaging substrate 119.

[0026] FIGURE 2B shows a bottom side 129 of the packaging substrate including a plurality of connectors, including connectors 197-199. For clarity, only a portion of the connectors on the bottom side 129 are labeled. The connectors, including connectors 197-199, may be configured to connect or otherwise mount the ASIC package 101 to a printed circuit board (PCB), socket, or other such chip carrier. The connectors may be solder balls, pins, sockets, etc. The connectors 197-199 may be gold, nickel, tin, copper, solder, or other such conductive material.

[0027] The bottom side 129 of the packaging substrate may include any number of connectors in any arrangement. In this regard, the arrangement and number of connectors, including connectors 197-199, shown in FIGURE 2B is merely for illustration. For instance, the connectors on the bottom side 129 of the packaging substrate may be solder balls arranged in a ball grid array (BGA). Other such arrangements and connectors may include contacts arranged in a land grid array (LGA), connector pins arranged in a pin grid array (PGA), etc.

[0028] The integrated voltage regulator die 105 may be connected to one or more connector pads on the top side 119 packaging substrate 109. For instance, the connection between the voltage regulator die 105 and the packaging substrate 109 may be made via one or more through mold vias (TMVs), such as TMV 305, as shown in FIGURE 3A. For clarity, only a portion of the TMVs shown in FIGURE 3A are labeled.

[0029] Each TMV may connect the integrated voltage regulator die 105 to the packaging substrate 109 via a connector pad or other such connector. For instance, the first end 315 of TMV 305 may be attached to a connector pad 399 and the opposite end 325 of the TMV 305 may be attached to the integrated voltage regulator die 105.

[0030] The connection between the TMVs and the connector pads may be made via a soldered flip chip bump. For example, FIGURE 3B shows an exploded side-view of a portion 301 of the ASIC package 101, including the connection between TMV 305 and connector pad

399. The first end 315 of the TMV 305 is connected to connector pad 399 on the top side 119 of the packaging substrate 109 via a soldered flip chip bump 398. Although the TMVs are shown as being connected via soldered flip chip bumps in FIGURE 3B, other connectors and connections may be used.

[0031] The metal layer 133 of the ASIC die 103 may also be connected to the packaging substrate 109. The connection of the metal layer 133 to the packaging substrate 109 may be made via flip chip bumps and connector pads, or other such connectors. For example, and as further shown in FIGURE 3B, flip chip bump 396 connects the metal layer 133 to connector pad 397, on the top side 119 of the packaging substrate. Although the flip chip bumps are shown in FIGURE 3B as being soldered onto connector pads, such as flip chip bump 396 being soldered onto connector pad 397, other connections may be used.

[0032] Power may be supplied to the ASIC package 101 by an external power source. In this regard, the external power source may provide power to the ASIC package 101 through the chip carrier to which the ASIC package 101 is mounted. For example, and as illustrated in FIGURE 4A, power, shown as arrow 490, may be supplied from an external power source (not shown) to the PCB 409. PCB 409 may supply the power to a connector on the packaging substrate.

[0033] The packaging substrate may include a redistribution layer etched onto, or otherwise embedded within, that routes power between the connectors on the bottom side 129 of the packaging substrate and connector pads 119 on the top side of the packaging substrate 109. For instance, power 490 delivered by the PCB, or other such chip mount, at connector 492 on the bottom side 129 of the packaging substrate 109 may be routed by the redistribution layer to connector pad 494 on the top side 119 of the packaging substrate. Although FIGURE 4A illustrates the power 490 being supplied to connector 492 and routed to connector pad 494, power may be supplied to any of the connectors on the bottom side of the packaging substrate 109, and in some instances, to more than one connectors. The power may be routed by the redistribution layer from the one or more connectors to one or more of the connector pads. For instance, power may be routed from one or more of the connectors on the bottom side 129 of the packaging substrate 109 to one, two, three, or more connector pads on the top side 119 of the packaging substrate 109.

[0034] Power may be carried from the packaging substrate 109 to the integrated voltage regulator die 105 by one or more TMVs. For example, FIGURE 4A shows power 490 being routed by TMV 405 from connector pad 494 to the integrated voltage regulator die 105. For clarity, power is shown being routed through only TMV 405. In some instances, power may be routed to the integrated voltage regulator die 105 by more than one TMV.

[0035] Power received by the integrated voltage regulator die may be considered the input power supply. The input power supply may be delivered to the integrated voltage regulator die 105 at a higher voltage level and lower current level than the input power supply delivered directly to the ASIC die. The integrated voltage regulator die 105 may provide power to the

ASIC die 103 with a different supply voltage level. For example, the integrated voltage regulator die 105 may operate as a switching voltage regulator and adjust the amount of voltage supplied to the ASIC die based on the needs of the ASIC die or other components within the ASIC package 101.

[0036] The integrated voltage regulator die 105 may deliver power to the ASIC die 107 via backside TSVs. For example, and as shown in FIGURE 4B, power, illustrated by arrow 480 may be provided from the integrated voltage regulator die 105 to a backside redistribution layer 173. The redistribution layer 173 may direct power to one or more TSV 470, including TSV 171, embedded within the silicon layer 131 of the ASIC die 107. Although FIGURE 4B illustrates power being delivered to all of the TSVs 470, power may be delivered to any number of TSVs.

[0037] Referring to FIGURE 4B, the backside redistribution layer 173 may be etched into and/or positioned above the silicon layer 131. The backside redistribution layer 173 together with the TSVs may be used to create inductors for use by the integrated voltage regulator die 105. Deep trench capacitors (DTCs) may also be embedded into the silicon layer 131 of the ASIC die 107 for use by the integrated voltage regulator die 105. In this regard, switching voltage regulators typically require many inductors and capacitors to operate. In instances where the integrated voltage regulator die 105 is a switching voltage regulator, the backside redistribution layer 173, the TSVs 470, as well as the DTC's embedded silicon (not shown) may provide at least some the functionality of inductors and capacitors. In some instances, the inductors and DTCs may be stacked onto the ASIC die.

[0038] As discussed herein, increases in processing speed of an ASIC die may increase the amount of power required to operate the ASIC die. An increase in power drawn by an ASIC die within an ASIC package without an integrated voltage regulator die may result in an increase of heat within the ASIC package due to copper losses generated by the wires and/or other such connections which carry the power through the ASIC package. By integrating the integrated voltage regulator die in the ASIC package, such as integrated voltage regulator die 105 in ASIC package 101, the power drawn by the ASIC package from an external power source may be limited, controlled, or otherwise regulated. For example, the integrated voltage regulator die 105 may cap the amount of power drawn by the components within ASIC package 101, such as ASIC die 107. In some examples, the integrated voltage regulator die 105 may include a closed loop feedback system to provide a steady voltage output.

[0039] In another example, the integrated voltage regulator die 105 may throttle the amount of power drawn, such as when the temperature of the ASIC die 107 is above a particular value or the ASIC die 107 does not require full power to operate. The integrated voltage regulator die 105 may also accept higher input voltages, thereby reducing the current supplied to the ASIC package 101 by an external power supply. Accordingly, the amount of current carried by the wires, traces, and/or other such connections on or within the ASIC package may be reduced, resulting in a decrease in the amount of copper losses and minimizing electromigration failure risk in the ASIC package. Moreover, the integrated voltage regulator die 105 may reduce overall power consumption and increase power efficiency of the ASIC package 101.

[0040] The voltage regulator may maintain a consistent power draw from the external power source, thereby preventing or reducing the number of increases in power carried by the wires, traces, and/or other such connections on or within the ASIC package 101. In some instances, the integrated voltage regulator die 105 can include a closed loop feedback system to minimize voltage fluctuations output. In this regard, a feedback sense line may monitor the voltage output by the integrated voltage regulator die 105 and feed monitored voltage level back to the integrated voltage regulator die 105. The feedback sense line may have high bandwidth, so the integrated voltage regulator die 105 may be able to compensate for voltage fluctuations quickly. By doing such, inductive noise caused by voltage fluctuations may be reduced.

[0041] A typical ASIC die will receive power from connectors on a packaging substrate which are closer to the ASIC die to reduce the amount of heat generated by power delivery. Consequently, data signals may be required to traverse longer paths from the ASIC die to connectors positioned on the exterior of the packaging substrate, thereby slowing the processing speed of the ASIC package. FIGURE 5 illustrates an interior and exterior collection of connectors, 595 and 590, respectively, on the top side 519 of a packaging substrate 509. In a typical ASIC package, power may be delivered by the connectors within the interior 595 of the packaging substrate 509 and data may be delivered by the connections within the exterior 590 of the packaging substrate 509.

[0042] Referring to FIGURE 6, by positioning the integrated voltage regulator die 605 above the ASIC die 607 and connecting the integrated voltage regulator die 505 to the packaging substrate through TMVs 615 positioned around the exterior of the ASIC die 607, the data connections between the ASIC die 607 and the packaging substrate 609 may be moved to the interior collection of connectors 695. Accordingly, the distance data needs to travel from the ASIC die 607 to the packaging substrate 609 may be reduced, as illustrated by arrows 696, resulting in improved communication speeds and reduced signal loss. The data connections may be routed by the redistribution layer in the packaging substrate and may include SERDES connections, parallel connections, serial connections, etc.

[0043] Although the example ASIC packages 101 and 601 described herein are described with reference to a single ASIC die 105, 605, respectively, each ASIC package may include any number of ASIC dies. Moreover, each ASIC package may include any number of voltage regulators or other components. Additionally, although the packages described herein are described as ASIC packages having ASIC dies, any type of die may be used, such as a memory die or integrated circuit die.

[0044] The features described herein allow for the integration of an integrated voltage regulator die into the ASIC package. By doing such, the copper losses generated by wires, traces, and/or other such connections which carry the power through the ASIC package to the ASIC die may be reduced. Moreover, by positioning the integrated voltage regulator die above the ASIC die, the distance data communications travel between the ASIC die and the PCB may be reduced.

REFERENCES CITED IN THE DESCRIPTION

Cited references

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- WO2019133019A1 [0002]
- US20122032340A1 [0003]
- WO2017160284A1 [0004]
- US2019333876A [0005]

Patentkrav

1. Integreret kredsløbs-, IC, hvilken pakke omfatter:
et emballeringssubstrat (109);
en IC-chip, der indbefatter et metallag (133) og et siliciumlag (131), hvor metallaget (133) er forbundet med emballeringssubstratet (109), og
en integreret spændingsregulatorchip (105) placeret stødende op til siliciumlaget (131) og forbundet med emballeringssubstratet (109) via ét eller flere formgennemgående huller, TMV'er (305) eller gennem dielektriske gennemgående huller, TDV'er,
hvor den integrerede spændingsregulatorchip (105) er konfigureret til at regulere strøm, der leveres til IC-chippen.

2. IC-pakke ifølge krav 1, hvor den integrerede spændingsregulatorchip (105) er forbundet med siliciumlaget (131) af et strømfordelingsnet, PDN.

3. IC-pakke ifølge krav 2, hvor PDN'et indbefatter et eller flere siliciumgennemgående huller, TSV'er (171), i siliciumlaget (131).

4. IC-pakke ifølge krav 3, hvor PDN'et endvidere indbefatter et omfordelingslag (173) konfigureret til at levere strøm fra den integrerede spændingsregulatorchip (105) til TSV'erne (171).

5. IC-pakke ifølge krav 4, hvor TSV'erne (171) og omfordelingslaget (173) danner en induktor.

6. IC-pakke ifølge et af krav 1 til 5, hvor hvert af det ene eller flere TMV'er (305) eller TDV'er er forbundet med emballeringssubstratet (109) i den første ende med en flip-chip-bump (396, 398) og med den integrerede spændingsregulatorchip (105) i en anden modsat ende.

7. IC-pakke ifølge et af krav 1 til 6, hvor siliciumlaget (131) er forbundet med emballeringssubstratet (109) via en eller flere flip-chip-bumbs (396, 398).

8. IC-pakke ifølge et af kravene 1 til 7, hvor emballeringssubstratet (109) er konfigureret til at blive tilsluttet et LGA- (landnet-array) stik eller et BGA- (kuglegitter-array) stik.

9. IC-pakke ifølge krav 8, hvor strømmen leveres til den integrerede spændingsregulatorchip (105) via LGA-stikket eller BGA-stikket.

10. IC-pakke ifølge krav 9, hvor emballeringssubstratet (109) indbefatter et omfordelingslag konfigureret til at lede strømmen fra LGA-stikket eller BGA-stikket til ét eller flere TMV'er (305).

11. IC-pakke ifølge et af krav 1 til 10, hvor IC-chippen omfatter en applikationsspecifik integreret kredsløbs-, ASIC, chip.

12. IC-pakke ifølge krav 11, hvor PDN'et indbefatter et eller flere siliciumgennemgående huller TSV'er (171) i siliciumlaget (131), og den integrerede spændingsregulatorchip (105) er konfigureret til at levere strøm til ASIC-chippen via TSV'erne (171).

13. IC-pakke ifølge krav 11 eller 12, hvor TSV'erne (171) og omfordelingslaget (173) danner en induktor til brug for den integrerede spændingsregulatorchip (105).

14. IC-pakke ifølge et af krav 11 til 13, hvor strømmen leveres til den integrerede spændingsregulatorchip (105) via LGA-stikket eller BGA-stikket, og emballeringssubstratet (109) indbefatter et omfordelingslag, der er konfigureret til at lede strømmen fra LGA-stikket eller BGA-stikket til det ene eller flere TMV'er (305) eller TDV'er.

15. IC-pakke ifølge krav 13 eller 14, og som endvidere omfatter dybdegravskondensatorer indlejret i siliciumlaget (131) eller stablet på siliciumlaget (131) til brug for den integrerede spændingsregulatorchip (105).

DRAWINGS

Drawing

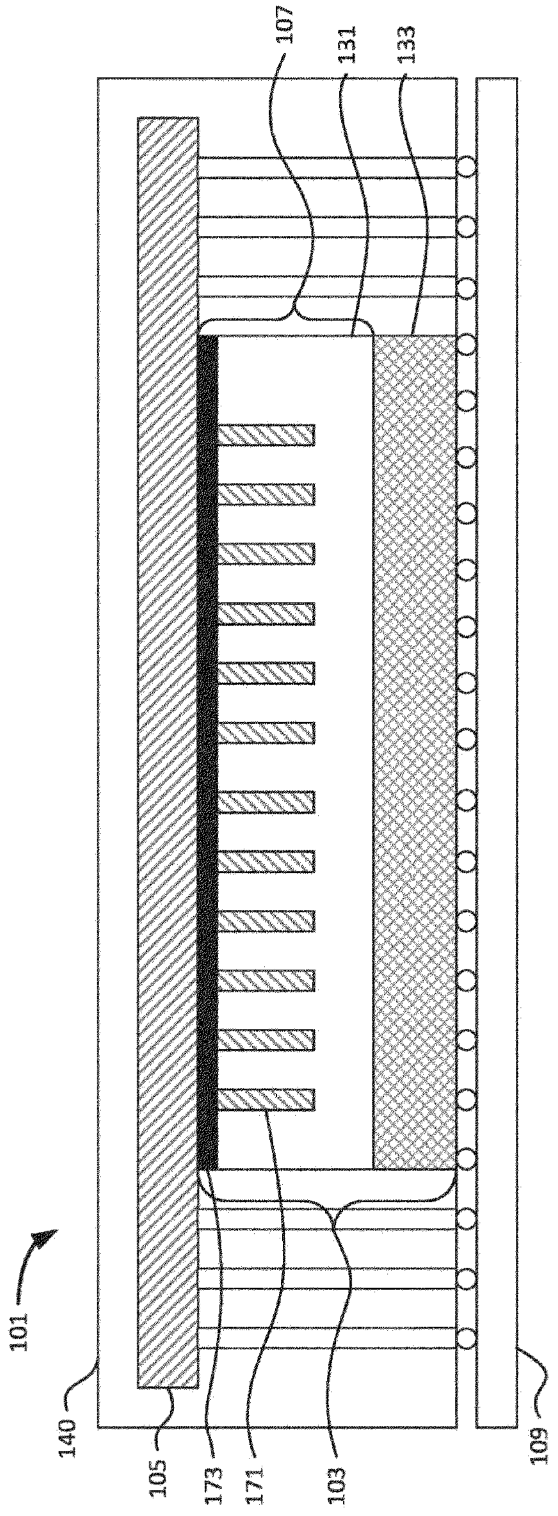

FIGURE 1

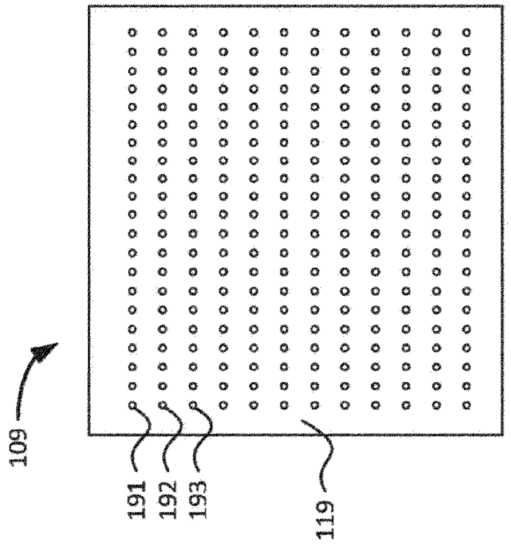

FIGURE 2A

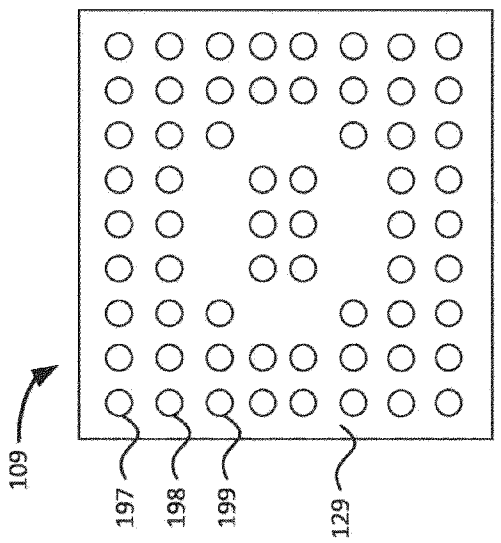

FIGURE 2B

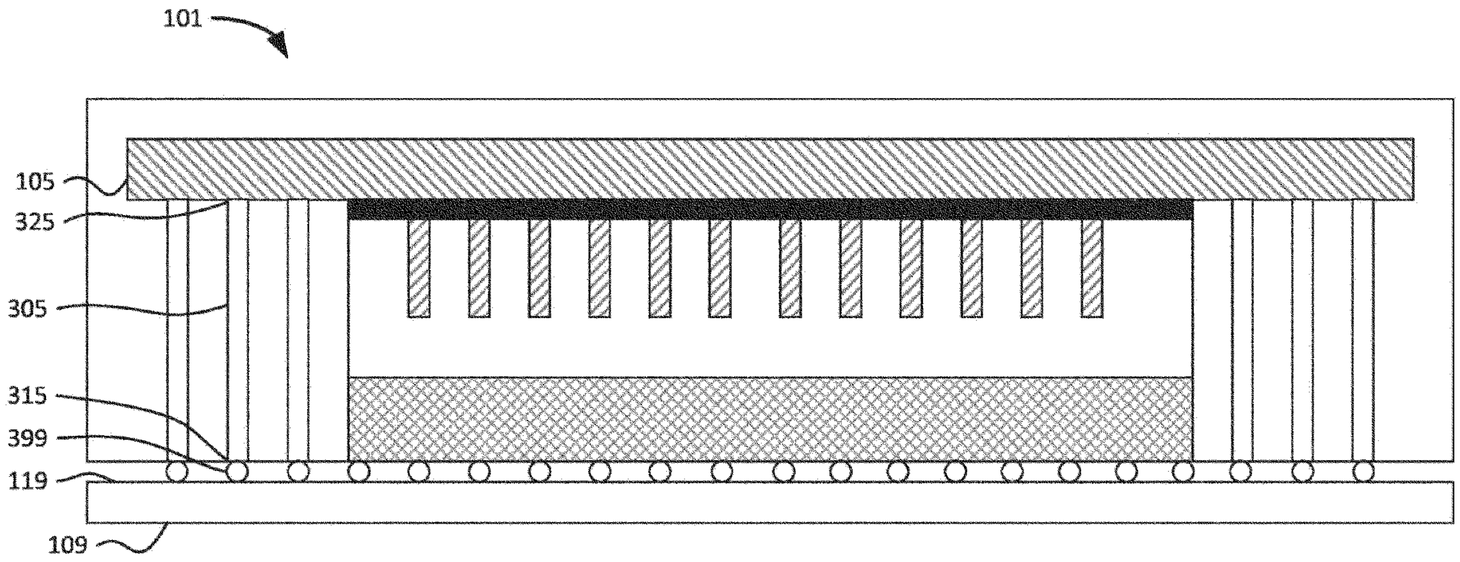

FIGURE 3A

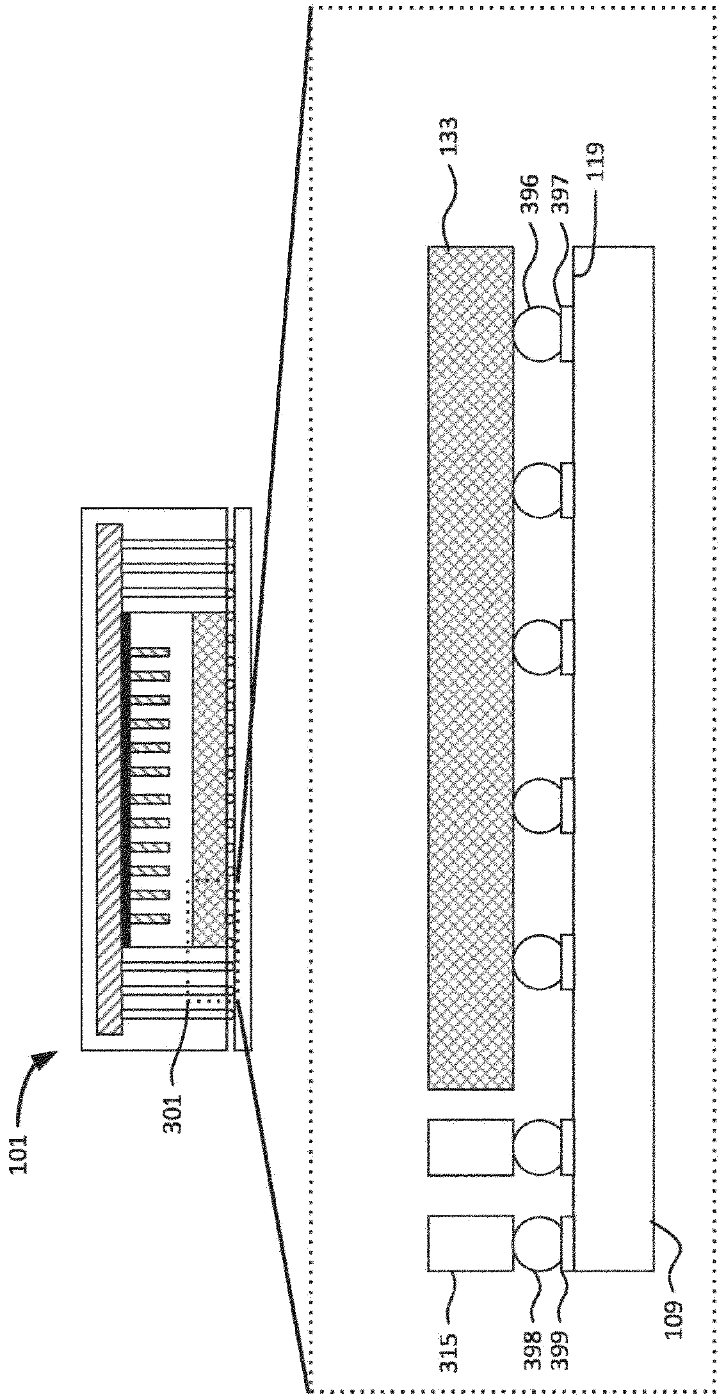

FIGURE 3B

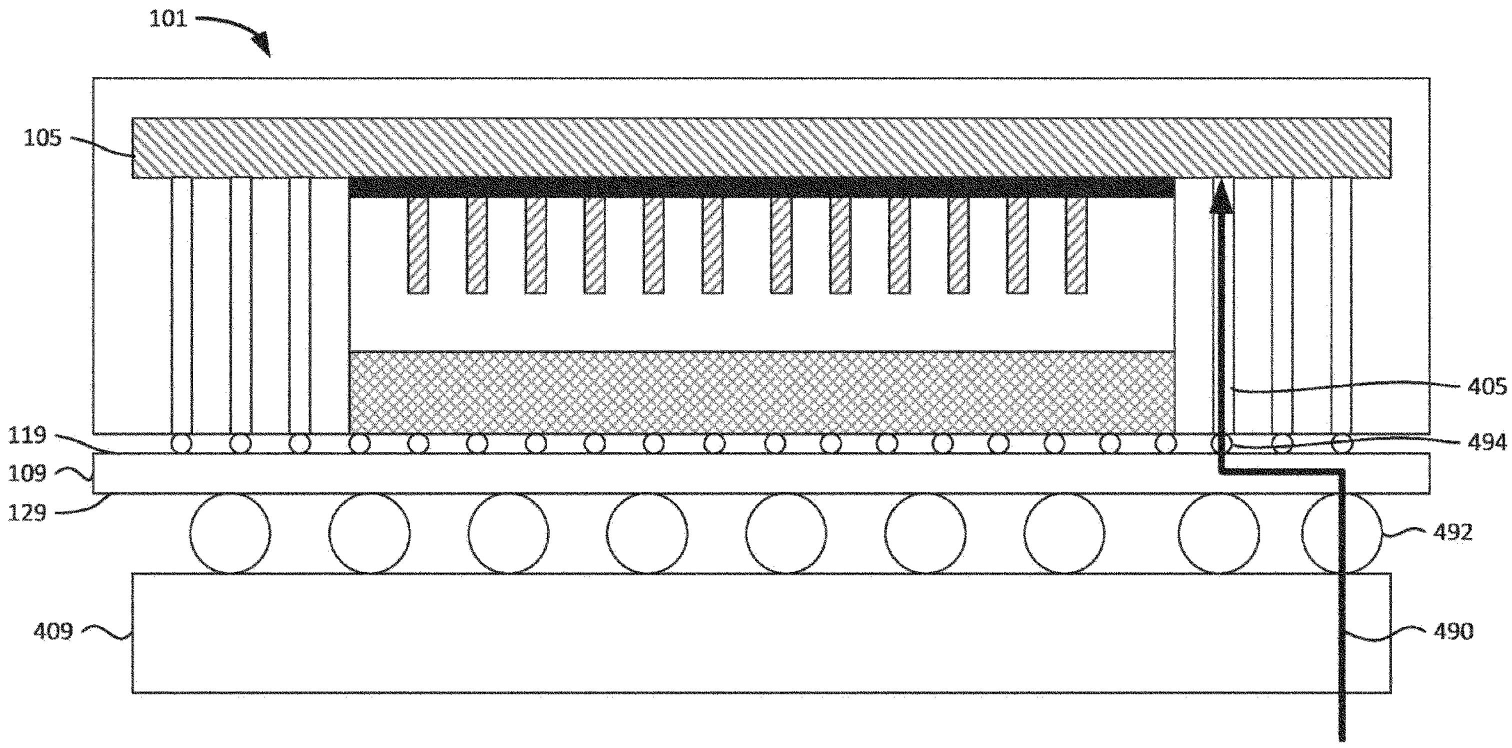

FIGURE 4A

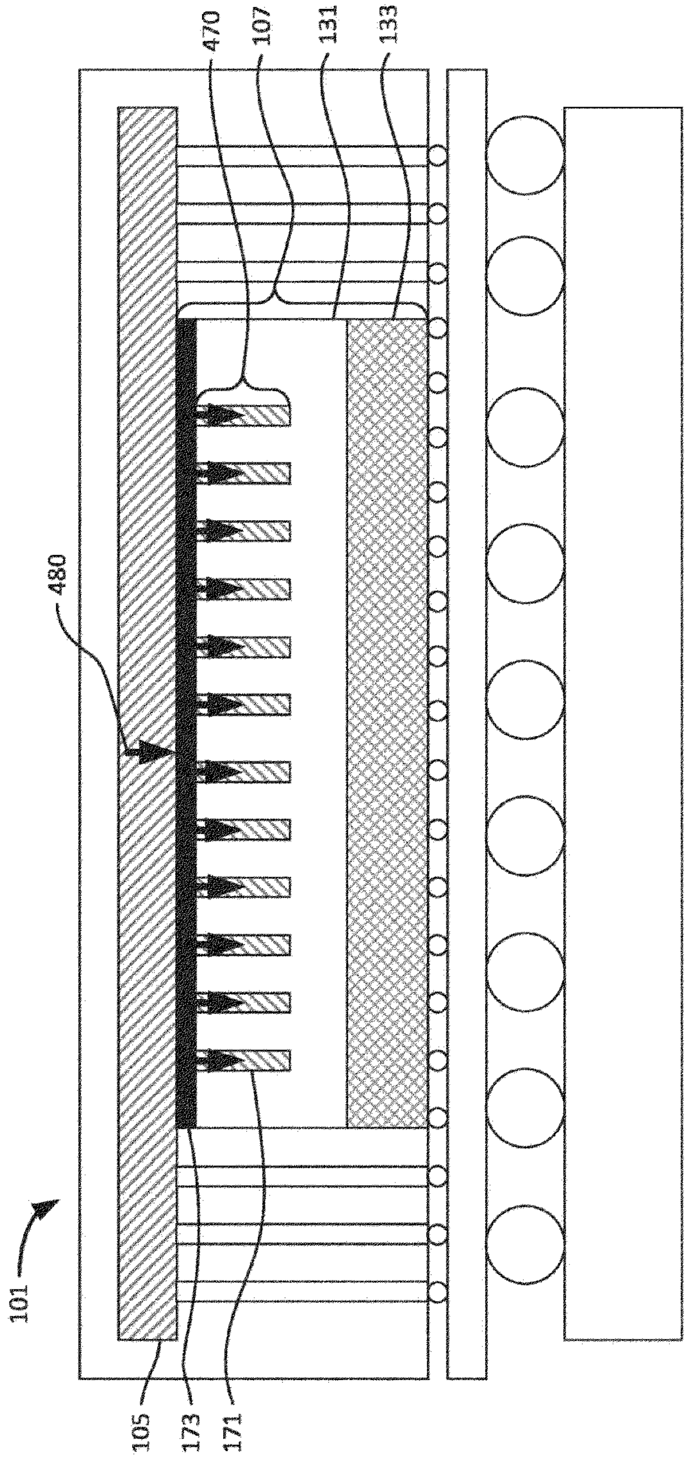

FIGURE 4B

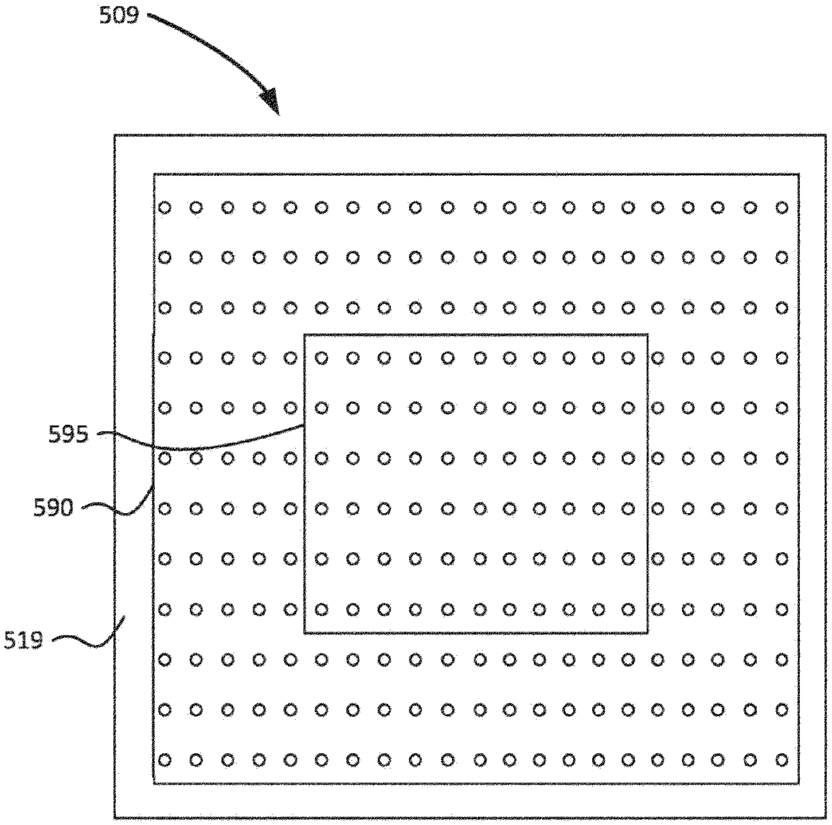

FIGURE 5

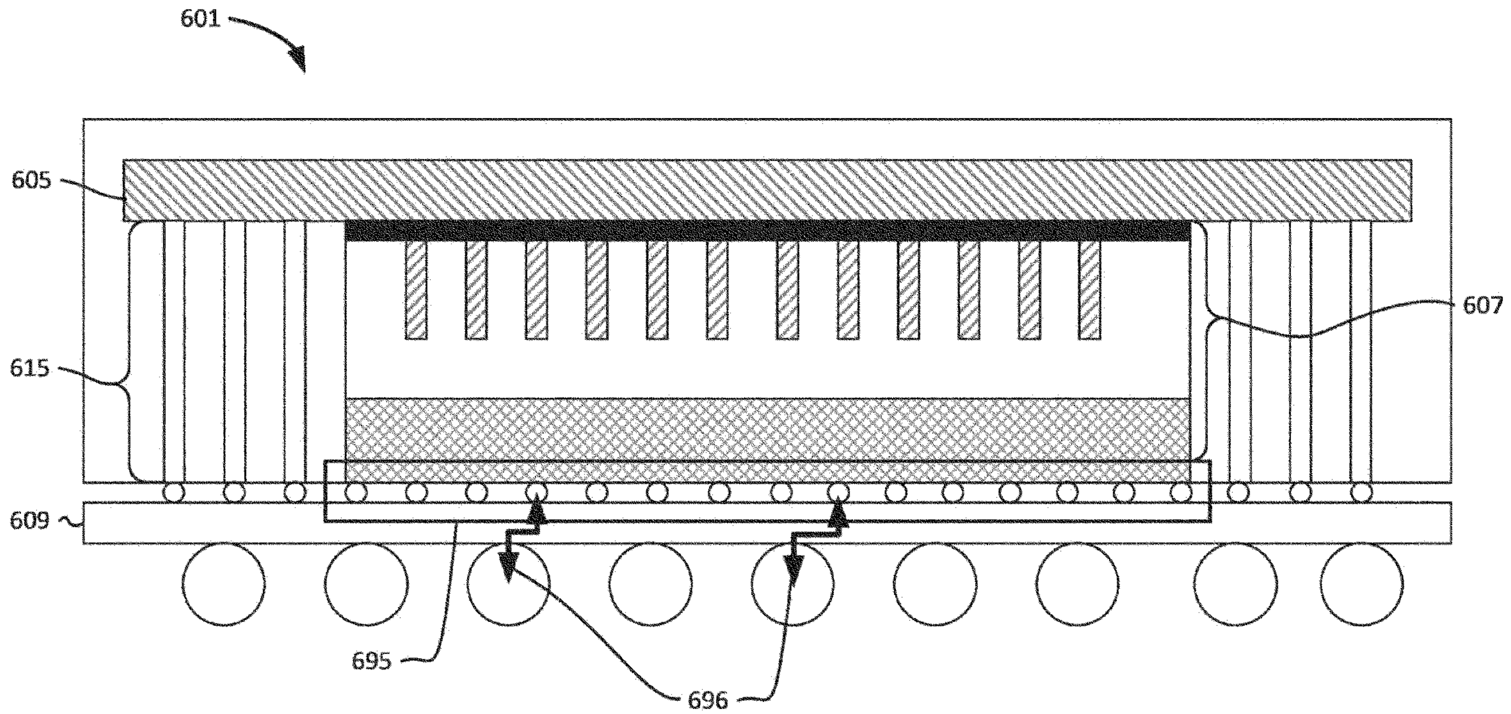

FIGURE 6