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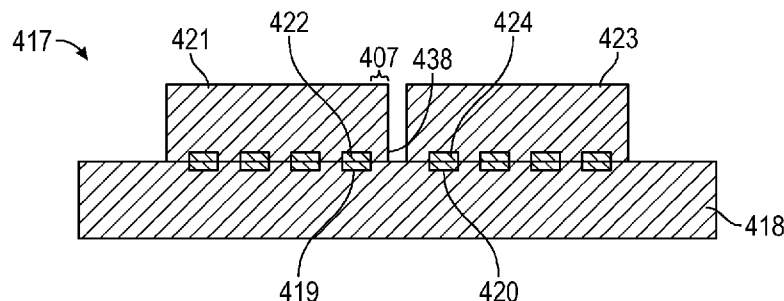


FIG. 4A

(57) Abstract: A bonded structure can include a carrier including a first conductive contact and a second conductive contact, a first singulated element including a third conductive contact directly bonded to the first conductive contact without an adhesive, and a second singulated element including a fourth conductive contact directly bonded to the second conductive contact without an adhesive, wherein the first and second conductive contacts are spaced apart by a contact spacing of no more than 250 microns.



BONDED STRUCTURES

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of priority to U.S. Provisional Patent Application No. 63/313,639, filed February 24, 2022, titled "BONDED STRUCTURES," the contents of which are hereby incorporated by reference in their entirety.

BACKGROUND

Field

[0002] The field relates to bonded structures, and, in particular, to bonded structures with increased area efficiency of circuitry and contacts.

Description of the Related Art

[0003] Semiconductor elements, such as semiconductor wafers or integrated device dies, can be stacked and directly bonded to one another without an adhesive. For example, nonconductive (dielectric or semiconductor) surfaces can be made extremely smooth and treated to enhance direct, covalent bonding, at room temperature and without application of pressure beyond contact. In some hybrid direct bonded structures, nonconductive field regions of the elements can be directly bonded to one another, and corresponding conductive contact structures can be directly bonded to one another.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1A shows a conventional method for singulating a wafer.

[0005] Figures 1B-1D show varying sizes of dies with edge exclusions from conventional methods.

[0006] Figures 2A-2H show a method for forming a die with reduced edge exclusion zones, according to various embodiments.

[0007] Figure 3 illustrates an example embodiment of a singulated element that can employ a reduced edge exclusion distance.

[0008] Figures 4A-4K show various embodiments of bonding structures.

[0009] Figures 5A-5B illustrate a process for forming a directly hybrid bonded structure without an intervening adhesive according to some embodiments.

DETAILED DESCRIPTION

[0010] For many years a trend had developed for integrating more and more functions on a chip to form systems-on-chip (SoC). More recently a trend has been to disaggregate circuitry into several chips and reassemble them in packaging processes. Advantages of such disaggregation include the ability to use different technologies for different chips or chiplets, which can be less expensive for some of the circuits, and the production of more chips or chiplets from a wafer compared to very large SoC chips, resulting in greater yield for a given level of contamination.

[0011] As shown in Figure 1A, a substrate 101 (*e.g.*, wafer) is provided on a dicing frame 102, and singulated into a plurality of singulated elements 103 divided at the saw streets 104. Conventional technology for device manufacture and assembly places limitations on the density of circuitry in the overall system, particularly where functions are disaggregated into multiple elements and aggregated by packaging. For example, vertical connections between stacked elements, such as copper pillars or solder balls 105, require some minimal spacing between pads, or spreading out the contacts by a redistribution layers (RDL). Such minimal spacing is exacerbated at the edges of laterally adjacent devices due to conventional exclusion zones at the device perimeters, due in part to the use of saws for singulation of chips from wafers. For example, conventional exclusion zones are utilized to space active regions and/or pads of the die from saw streets so as to reduce or minimize damage that may occur during the dicing or singulation process. Pick-and-place and/or bonding tools having limited alignment accuracy can also place limitations on the density of devices in the assembly. Substructural damage imparted to the devices near the die edge may reduce device yield. Conventional exclusion zones around the perimeters of chips represent lost real estate for active circuitry. If any interconnects or contact pads are provided in the exclusion zone, they are typically electrically inactive or “dummy” contact pads. Accordingly, electrically active pads (*e.g.*, pads that electrically connect to circuitry in the die, such as to a signal line, a power line, or ground) are spaced inwardly from the die edge by an exclusion zone.

[0012] Figures 1B-1D show singulated elements of various sizes. Each singulated element 103 may comprise a substrate 101 and solder balls 105 as described in connection with Figure 1A. As shown in Figures 1B-1D, electrically active bond pads may be spaced from the die edge 106 by an edge exclusion distance 107, which represents unused real estate of the die.

The edge exclusion distance 107 (and edge exclusion area) increases significantly with decreasing die size, such that, for small dies (*e.g.*, dies with maximum widths less than 4mm, less than 3mm, or less than 2mm), the edge exclusion distance occupies a relatively large proportion of the die. The increased exclusion distance 107 therefore reduces the useful area for devices in the die. For structures in which the dies are solder bonded to the carrier, the exclusion distance 107 is substantial, due to the large pitches between adjacent pads that are used to prevent solder bridging that would occur at finer pitches. Large edge exclusion zones reduce design flexibility for functional pad (input/output, or I/O) counts for a given die, and also increase distances for electrical connections among elements (such as passive components, chips or chiplets) in a system, resulting in degradation in the performance of the chip or chiplet. By way of example, a typical edge exclusion is approximately 200 μm using traditional methods for singulating dies. In one example, an 8mm x 12mm die with a 200 μm edge exclusion distance results in about 8.2% of the die area that is unused. In another example, a 4mm x 4mm die with a 200 μm edge exclusion distance results in about 19% of the die area that is unused. In another example, a 1mm x 1mm die with a 200 μm edge exclusion distance results in about 64% of the die area that is unused. Accordingly, there remains a continuing need to reducing the exclusion area in small dies to increase die design flexibility, the portion of the chip or chiplet designed for active or passive circuitry and afford higher functional I/O counts.

[0013] Figures 2A-2H illustrate an example process for forming singulated elements configured for direct hybrid bonding, according to various embodiments. As shown in Figure 2A, a substrate 201 (*e.g.*, a wafer) can include a bulk portion 208, and a bonding layer 209 over the bulk portion 208. The bonding layer 209 may comprise a dielectric material with at least partially embedded conductive contact features. The bonding layer 209 can include a plurality of nonconductive regions 210 and a plurality of conductive contacts 211 at least partially embedded in the bonding layer 209. Beneficially, when configured for direct hybrid bonding, the contacts 211 can be provided at a pitch 212 significantly smaller than pitches used in solder bonding. The substrate 201 can be planarized in Figure 2A. In some embodiments, the substrate is planarized through chemical mechanical polishing (CMP). In Figure 2B, a protective layer 213 (such as a photoresist) can be provided over the substrate 201. In some embodiments, the planarized surface 214 can have conductive contacts 211

recessed by a small amount (for example, less than 20 nm, less than 10 nm, or even less than 5 nm) below the surrounding nonconductive field regions 210. The protective layer 213 can be patterned to include recesses 215 in the protective layer in Figure 2C, and the substrate 201 can be transferred to a dicing frame 202 in Figure 2D. In Figure 2E, the substrate 201 can be singulated into a plurality of singulated elements 203. In the illustrated embodiment, the substrate 201 is singulated using an etching process, *e.g.*, a reactive ion etching (RIE) or plasma dicing process. Beneficially, compared to saw singulation, the RIE singulation process of the illustrated embodiments entails reduced damage to the edges of the dies, which can reduce defects at the edges and allow a smaller exclusion distance 207. In some embodiments, RIE singulation can result in an edge exclusion distance 207 of less than 40 μ , less than 20 μ m, less than 15 μ m, or less than 10 μ m. In Figure 2F, the protective layer 213 can be removed, and in Figure 2G, the bonding surfaces 214 can be processed, such as by ashing (*e.g.*, to remove debris from the protective layer), cleaning and/or a surface activation treatment (*e.g.*, nitrogen plasma treatment). In Figure 2H, the singulated dies 203 can be cleaned, rinsed, dried and prepared for direct bonding to another element, such as a carrier. In some embodiments, the patterned substrate 201 of Figure 2C may be singulated by a combination of dry etch, (*e.g.*, RIE), wet etchant, and a fine dicing blade. For example, RIE may be applied to remove dielectric material in the region below gaps in the resist mask. After dry etching, a suitable wet etchant may be employed to remove exposed conductive material. The remaining substrate (for example, bulk semiconductor material) may be cut by a fine dicing blade, laser dicing or by dry etch to complete the singulation.

[0014] In some embodiments, the sides of the singulated dies may be further processed. In some embodiments the side edges of the singulated dies may have etched surfaces (*e.g.*, surfaces without burrs or debris from saw singulation). The etched surfaces may include a pattern indicative of an etch process (*e.g.*, an RIE or wet etch process). In some embodiments the sidewalls may be slightly tapered. For example, the sidewalls may have an angle between 85° and 90° relative to the horizontal. In some embodiments, the sidewalls are substantially vertical. Limiting the taper of the sidewalls can be beneficial so as to allow the singulated dies to be brought closer together.

[0015] Figure 3 illustrates an example embodiment of a singulated element that can employ a reduced an edge exclusion distance and enable dies to be placed close together. A

singulated element 303, as seen in Figure 3, may have a plurality of conductive contacts 311 surrounded by a plurality of non-conductive regions 310. In some embodiments the plurality of conductive contacts 311 may comprise a conductive material. In some embodiments, the conductive material may comprise silver, gold, indium, nickel or copper or their various alloys. In another embodiment, the conductive material is copper. The singulated element 303 may comprise an edge exclusion distance 307, a pitch 312, and a width 316. The reduced edge exclusion distances 307 can be employed with and have advantages for any die size. Particularly acute advantages are obtained for relatively small dies (e.g., dies having maximum widths less than 8 mm, less than 6 mm, less than 4 mm, less than 3 mm, less than 2 mm), such as chiplets or discrete devices (e.g., passives) with particular functions. Figure 3 illustrates how smaller edge exclusion zones provide particular proportionate advantages for smaller dies as compared, for example, to the larger exclusion zones of Figures 1A-1D. For example, the methods and systems herein can result in an edge exclusion distance of about 50 μm . In one example, a 4mm x 4mm die can have a 50 μm edge exclusion distance using the methods and systems described herein which results in only about 4.9% of the die area that is unused. In another example, the methods and systems described herein may result in an edge exclusion distance of about 10 μm . In one embodiment, a 1mm x 1mm die can have a 10 μm edge exclusion distance using the methods and systems described herein which results in only about 4% of the die area that is unused. In another embodiment, the methods and systems described herein may result in an edge exclusion distance of about 5 μm . In one example, a 0.4mm x 0.4mm die may have a 5 μm edge exclusion distance using the methods and systems described herein which results in only about 5% of the die area that is unused. In some embodiments, a width of the edge exclusion is less than 10 μm , less than 5 μm , or less than 3 μm . In some embodiments, the edge exclusion can be in a range of 0.5 μm to 100 μm , in a range of 0.5 μm to 50 μm , in a range of 0.5 μm to 20 μm , in a range of 0.5 μm to 10 μm , in a range of 1 μm to 10 μm , or in a range of 2 μm to 10 μm . The reduced pitch 312 enabled by hybrid direct bonding techniques (and with dies singulated by RIE) facilitates a reduced edge exclusion region 307 as compared to conventional structures. Moreover, as shown in Figures 4A-4K, the reduced edge exclusion region 307 can allow components to be directly bonded next to one another and spaced apart by a very small gap. Beneficially, providing dies closely together can allow for effective die stitching in which closely-spaced dies are electrically connected through the

carrier with reduced latency and low electrical losses. In some embodiments, the ratio of the edge exclusion distance to the pitch is between 10 and 50. In some embodiments, the ratio of the edge exclusion distance to the pitch is less than 50, less than 15, less than 10, less than 5, or less than 2. In some embodiments, a width of the edge exclusion 307 is comparable to or less than the pitch of adjacent conductive features 311 adjacent to the edge of the die.

[0016] Figures 4A-4H show various embodiments of bonded structures. As seen in Figure 4A a bonded structure 417 can include a carrier 418 including a first conductive contact 419 and a second conductive contact 420. In some embodiments, the carrier 418 can be a substrate (e.g., a wafer, a package, a flat panel, or a temporary substrate comprising a redistribution layer) or a die. In some embodiments, the carrier 418 can comprise a bonding layer 409 (as seen in Figure 4K). The bonding layer may comprise a dielectric material with at least partially embedded conductive contact features. In some embodiments, the first conductive contact 419 and the second conductive contact 420 may be electrically connected (as seen in Figure 4K). The bonded structure 417 can include a first singulated element 421 including a third conductive contact 422 directly bonded to the first conductive contact 419 without an adhesive. The bonded structure can also include a second singulated element 423 including a fourth conductive contact 424 directly bonded to the second conductive contact 420 without an adhesive. In some embodiments, the bonded element 421 or 423 (or both) may comprise a singulated package. The singulated package may comprise of one or more dies at least partially embedded in an encapsulating material. In some embodiments, the conductive contacts are made of a conductive material. In some embodiments, the conductive material comprises gold, silver, indium, copper or nickel or their various alloys. In some embodiments, the conductive material is copper. An edge exclusion distance 407 between an outer edge 438 of the first singulated element 421 and the third conductive contact 422 can be less than 100 μm , for example, no more than 50 μm , or no more than 10 μm (e.g., in a range of 1 μm to 100 μm). In some embodiments, the first and second singulated elements comprise dies of a size 10 mm x 10 mm or smaller.

[0017] As seen in Figure 4B, the first singulated element 421 can comprise a thickness 427 and a lateral width 428. In some embodiments, the first singulated element 421 has a maximum lateral width 428 of no more than about 8 mm, no more than about 6 mm, no more than about 4 mm, no more than about 3 mm, or no more than about 2 mm. The second

singulated element 423 can comprise a thickness 429 and a width 430. In some embodiments, the second singulated element 423 has a maximum lateral width 430 of no more than about 8 mm, no more than about 6 mm, no more than about 4 mm, no more than about 3 mm, or no more than about 2 mm. The first conductive contact 419 and the second conductive contact 420 can be spaced apart by a contact spacing 425 of no more than 250 microns. In various embodiments, the contact spacing 425 is no more than 200 microns, no more than 100 microns, no more than 50 microns, no more than 10 microns, no more than 5 microns, or no more than 2 microns. For example, in various embodiments, the contact spacing 425 can be in a range of 1 micron to 250 microns, or in a range of 1 micron to 100 microns, or in a range of 1 micron to 20 microns. In some embodiments, the contact spacing 425 is between 0.4 times and 8 times the thickness 427 of the first singulated element 421. In some embodiments, the contact spacing 425 is no more than the thickness 427 of the first singulated element 421. In some embodiments, the contact spacing 425 is between 0.4 times and 8 times the thickness 429 of the second singulated element 423. In some embodiments, the contact spacing 425 is no more than the thickness 429 of the second singulated element 423. In some embodiments, the first singulated element 421 and second singulated element 423 can be spaced apart by an element spacing 426 of about 5 μm (microns) to about 60 μm , for example less than about 25 μm . In some embodiments, the element spacing 426 can be no more than 60 μm , no more than 20 μm , no more than 10 μm , no more than 9 μm , no more than 8 μm , or no more than 5 μm . In some embodiments, the element spacing 426 can be in a range of 1 μm to 25 μm , in a range of 1 μm to 15 μm , in a range of 1 μm to 10 μm , in a range of 1 μm to 8 μm , or in a range of 1 μm to 5 μm . In some embodiments, the ratio of the maximum lateral width 428 of the first singulated element 421 to the edge exclusion distance 407 is between 100 and 10 or is less than 50, less than 10, or less than 5, or less than 2. In some embodiments, the ratio of the maximum lateral width 430 of the second singulated element 423 to the edge exclusion distance 407 is between 100 and 10 or is less than 50, less than 10, or less than 5, or less than 2. In some embodiments, the element spacing 426 can be comparable to or less than to the edge exclusion distance 407.

[0018] As seen in Figure 4C, the width 428 of the first singulated element 421 can be longer than the width 430 of the second singulated element 423. As seen in Figure 4D, the thickness 427 of the first singulated element 421 can be longer than the thickness 429 of the second singulated element 423. In various embodiments, as shown in Figures 4B, the contact

spacing 425 can be no more than eight times a thickness (427 or 429) of at least one of the first singulated element 421 and second singulated element 423, or can be no more than twice a thickness (427 or 429) of at least one of the first singulated element 421 and second singulated element 423, or can be no more than a thickness (427 or 429) of at least one of the first singulated element 421 and second singulated element 423, or can be no more than 0.4 times a thickness (427 or 429) of at least one of the first singulated element 421 and second singulated element 423, or can be no more than a height of through substrate vias (TSVs) through the thickness of an element.

[0019] In the illustrated embodiments, the third conductive contact 422 can comprise an electrically active contact electrically connected to circuitry of the first singulated element 421. For example, the third conductive contact 422 can be connected to a signal line, a power line, or electrical ground. In any of the embodiments described herein, any of the conductive contacts may be connected to a signal line, a power line, or electrical ground. In various embodiments, at least one of the first singulated element 421 and the second singulated element 423 comprises an integrated device die having active circuitry. In various embodiments, the laterally outermost pads on a die may comprise active pads connected to a signal, power, or ground, as opposed to dummy pads. In some embodiments, as shown in Figure 4E, for example, the first singulated element 421 comprises an integrated device die having active circuitry and the second singulated element 423 comprises a passive component 432. As explained herein, at least one of the first and second singulated elements are singulated, in full or in part, using a reactive ion etching (RIE) technique for clean and sharp die edges.

[0020] As noted, the advantages of closer spacing between elements (dies, electrical components) and more particularly between active contacts of adjacent elements can apply to any sized elements. In some embodiments, relatively small elements (chipllets, component devices) are laterally spaced closely and bonded to a common carrier, where at least one of the overlying elements has a maximum lateral width of no more than about 8 mm, no more than about 6 mm, no more than about 4 mm, no more than about 3 mm, or no more than about 2 mm, although the principles and advantages taught herein are by no means limited to such small elements. In various embodiments, an edge exclusion distance 407 between an outer edge 438 of the first singulated element 421 and the third conductive contact 422 can be

less than 100 μm , for example, no more than 50 μm , or no more than 10 μm (e.g., in a range of 1 μm to 100 μm). In some embodiments, the ratio of the maximum lateral width to the edge exclusion distance is between 10 and 100. In some embodiments, the ratio of the maximum lateral width to the edge exclusion distance may be less than 100, less than 50, less than 25, less than 10, less than 5, or less than 2.

[0021] In some embodiments, as shown in the top plan view of Figure 4F, a bonded structure 417 can include a carrier 418 and a first element 433 directly bonded to the carrier 418 without an adhesive. As shown in Figure 4F, the first element 433 can include a cutout region 434. A second singulated element 423 can be directly bonded to the carrier 418 without an adhesive. The second singulated element 423 can be disposed at least partially laterally within the cutout region 434 of the first element 433. The use of the cutout region 434 can enable the bonding of small dies, chiplets or components (e.g., passive components such as inductors, capacitors, resistors) having different shapes and in close proximity to adjacent dies. In some embodiments, a third singulated element (not shown) can be directly bonded to the carrier 418 without an adhesive, with the second singulated element 423 disposed between the first element 433 and the third singulated element (not shown).

[0022] In some embodiments, as shown in Figure 4G, a third singulated element 435 can be directly bonded to the second singulated element 423. In some embodiments, the third singulated element 435 is directly bonded to the second singulated element 423 without an adhesive. A conductive via or TSV 431 can extend through the second singulated element 423 to connect to the third singulated element 435. In Figure 4G, the contact spacing 425 between closest active dies of adjacent elements can be no more than about four times (4x) a length (or height) of the conductive via 431. In other embodiments, the contact spacing 425 may be less than about 2x or less than about 1x the length of the conductive via 431. As will be understood, the length of a conductive through via (TSV) 431 is typically about equal to the thickness 429 of the element. In some embodiments, the via 431 may comprise a thermal via, passive via or element and the length of the via (TSV) 431 can be less than the thickness 429 of the element.

[0023] In some embodiments, as seen in Figure 4H, a third singulated element 435 can be directly bonded to the first singulated element 421 and the second singulated element 423. In some embodiments, the third singulated element 435 is directly bonded to the first

singulated element 421 and the second singulated element 423 without an adhesive. In some embodiments, the third singulated element 435 may comprise a singulated package. The singulated package may comprise one or more embedded dies at least partially embedded in an encapsulating material. In some embodiments, third singulated element 435 may comprise a singulated passive elements having a redistribution layer. The planar surface of the redistribution layer may be prepared for hybrid bonding. In some embodiments, the third singulated element 435 may comprise a singulated dielectric element having a redistribution layer. Conductive vias 431 can extend through the first singulated element 421 and the second singulated element 423 to connect to the third singulated element 435. The third singulated element 435 effectively acts as a bridge connecting the first singulated element 421 and second singulated element 423 (and/or connected to the underlying carrier 418). In some embodiments, a layer of dielectric material 439 (as described in conjunction with Figures 4I and 4J below) may be deposited on the first singulated element 421, the second singulated element 423, and the carrier 418 prior to the third singulated element 435 being bonded to the first singulated element 421 and second singulated element 423 (as seen in Figure 4H) or prior to the third singulated element 435 being bonded to the second singulated element 423 (as seen in Figure 4G). In some embodiments, the layer of dielectric material 439 may form a bonding layer 409 between the third singulated element 435 and the elements to which it is bonded. In some embodiments, the bonding layer 409 may comprise a dielectric material with at least partially embedded conductive contact features (such as contacts 419, 420).

[0024] In some embodiments, as seen in Figures 4I-4J-2, a layer of dielectric 439 can be deposited over the bonded structure 417. As seen in Figure 4I, a conformal coating of dielectric material 439 is deposited on the bonding structure 417. In some embodiments, the dielectric layer 439 may cover the carrier 418, the first singulated element 421, and the second singulated element 423. Additionally, the dielectric layer 439 may be placed over the bonding structure 417 such that a small amount 440 of the dielectric material 439 is disposed within the gap 441 between the first singulated element 421 and second singulated element 423. In some embodiments, as seen in figure 4I, the small amount 440 of dielectric 439 only extends a short distance into the gap 441. In some embodiments, as seen in Figure 4J, the dielectric layer 439 may be deposited on the bonding structure 417 such that the gap 441 between the first singulated element 421 and the second singulated element 423 is completely filled (or mostly

filled) with the dielectric layer 439. In some embodiments, as seen in Figure 4J-2, the dielectric layer 439 may be deposited on the carrier 418 such that the dielectric layer 439 on the carrier 418 is of a thickness of about the thickness of one of the singulated elements. In the illustrated embodiment, the dielectric layer 439 is illustrated as extending above the singulated element 421, 423. In other embodiments, the dielectric layer 439 can be planarized (e.g., using a CMP process) such that the top of the dielectric layer 439 is substantially flush with the element 421, 423. In the embodiments of Figures 4I-4J-2, the dielectric layer 439 can be prepared for hybrid bonding, and additional element(s) can be directly bonded to the dielectric layer 439. In some embodiments, conductive contacts can be formed in the dielectric layer 439, and the upper surface can be prepared for direct hybrid bonding. One or more additional elements can be directly hybrid bonded to the hybrid bonding layer including the dielectric layer 439. Accordingly, in various embodiments, the elements 421, 423 (such as those shown in Figure 4J-2) can be formed in a reconstituted element or wafer, and additional elements can be directly bonded to the reconstituted element or wafer. The dielectric layer 439 can comprise an inorganic dielectric material (such as silicon oxide, silicon nitride, silicon oxycarbonitride, etc.) to protect the dies and/or carrier. In other embodiments, the dielectric layer 439 can comprise an organic dielectric material (such as a molding material). In various embodiments, the dielectric layer 439 can comprise multiple layers.

[0025] In some embodiments, as seen in Figure 4K, the carrier 418 may comprise a bonding layer 409. In some embodiments, the bonding layer 409 may comprise a dielectric material with at least partially embedded conductive contact features (such as contacts 419, 420). Although not separately shown, the dies 421, 423 can also include a nonconductive or dielectric bonding layer in which the contacts 422, 424 are at least partially embedded. In some embodiments, the first conductive contact 419 and the first conductive contact 420 may be electrically connected through a connector 442, such as a conductive trace at least partially embedded (e.g., fully embedded) in the bonding layer 409. In some embodiments, the connector 442 may be configured similarly to the conductive through vias (TSV) as described above in conjunction with the other embodiments.

[0026] Any of the embodiments described herein, may incorporate the features of any of the other embodiments described herein. For example, the embodiment as seen in Figure 4A may further comprise a connector 442 as seen in Figure 4K.

[0027] In an embodiment, a bonded structure can include a first singulated element comprising a first conductive contact, and a carrier comprising a second conductive contact. The first conductive contact and the second conductive contact can be directly bonded to one another without an intervening adhesive. The first conductive contact can be spaced apart from an outer edge of the first singulated element by an edge exclusion distance of no more than 100 μm . The first conductive contact can comprise an electrically active contact electrically connected to circuitry of the first singulated element. In various embodiments, the edge exclusion distance can be no more than 50 μm , or no more than 10 μm . For example, the edge exclusion distance can be in a range of 1 μm to 100 μm .

[0028] In an embodiment, a bonded structure can include a first singulated element having a first plurality of conductive contacts spaced at a pitch. The first plurality of conductive contacts can include at least one outer conductive contact closest to an outer side edge of the first singulated element. The at least one outer conductive contact can be spaced from the outer side edge by an edge exclusion distance and can comprise an electrically active contact electrically connected to circuitry of the first singulated element. The bonded structure can include a carrier comprising a second plurality of conductive contacts directly bonded to the first plurality of conductive contacts without an intervening adhesive.

[0029] In some embodiments, a ratio of the edge exclusion distance to the pitch between the contact pad of at least one element can be less than 15:1. In some embodiments, the ratio of the edge exclusion distance to the pitch of a group of pads adjacent to the exclusion zone can be less than 10:1, less than 5:1, or less than 2:1. In some embodiments, a ratio of a maximum lateral width of the first singulated element to the edge exclusion distance can be more than 15:1, more than 10:1, more than 5:1, or more than 2:1.

[0030] In various embodiments, a bonded structure can include a carrier having first bonding surface including a first nonconductive region and a first plurality of conductive contacts; and a singulated device die having a second bonding surface including a second nonconductive region and a second plurality of conductive contacts. The second nonconductive region can be directly bonded to the first nonconductive region of the carrier without an adhesive and the second plurality of conductive contacts can be directly bonded to the first plurality of conductive contacts without an adhesive. The singulated device die can include an etched outer side edge extending non-parallel relative to the second bonding surface

and the second plurality of conductive contacts can include at least one outer conductive contact closest to the outer side edge. The at least one outer conductive contact can comprise an electrically active contact electrically connected to circuitry of the singulated device die.

[0031] In some embodiments, an integrated device die can include active circuitry, a bonding surface configured for direct hybrid bonding to another element, and an outer edge extending non-parallel relative to the bonding surface. A first conductive contact can be spaced apart from the outer edge by an edge exclusion distance of no more than 100 μm . The first conductive contact can comprise an electrically active contact electrically connected to the active circuitry. In some embodiments, the edge exclusion distance is no more than 50 μm . In some embodiments, the first conductive contact is electrically connected to a signal line, a power line, or electrical ground. In some embodiments, one or more dummy pads may be disposed in the exclusion zone between the first active conductive contact and an outer edge of the die. In some arrangements, the dummy pad(s) may have smaller maximum lateral dimensions than the first active conductive contact.

[0032] In any of the above embodiments, any of the singulated elements can include an etched outer side which extends non-parallel relative to bonding surface of the singulated die. In some embodiments, the etched outer side extends perpendicular to the bonding surface of the singulated die. In some embodiments, the etched outer side extends at an 85°-90° angle relative to the bonding surface of the singulated die.

[0033] In various embodiments, a bonded structure can include a carrier including a first conductive contact and a second conductive contact, a first singulated element including a third conductive contact directly bonded to the first conductive contact without an adhesive, and a second singulated element including a fourth conductive contact directly bonded to the second conductive contact without an adhesive. In some embodiments, the first and second conductive contacts are spaced apart by a contact spacing of no more than 250 microns.

[0034] In some embodiments, the first and second singulated elements are spaced apart by an element spacing of no more than 10 microns. In some embodiments, the first and second conductive contacts are spaced apart by a contact spacing of between about 0.4 times and 8 times a thickness of at least one of the first and second singulated elements. In some embodiments, the bonded structure can include a carrier and a first and second singulated elements that are direct hybrid bonded. In another embodiment, the contact spacing is less than

about 2 times the thickness of at least one of the first and second singulated elements. In one embodiment, the first and second singulated elements included respective nonconductive regions directly bonded to corresponding nonconductive region(s) of the carrier without an adhesive. In some embodiments, the contact spacing is no more than 200 microns. In some embodiments, the contact spacing is no more than 100 microns. In some embodiments, the contact spacing is no more than 50 microns. In some embodiments, contact spacing is no more than 10 microns. In some embodiments, the contact spacing is no more than 5 microns.

[0035] In some embodiments, the contact spacing is no more than 2 microns. In some embodiments, the contact spacing is in a range of 1 micron to 250 microns. In some embodiments, the contact spacing is in a range of 1 micron to 100 microns. In some embodiments, the contact spacing is in a range of 1 micron to 20 microns. In some embodiments, the element spacing is no more than 20 microns. In some embodiments, the element spacing is no more than 10 microns. In some embodiments, the contact spacing is no more than the thickness of at least one of the first and second singulated elements.

[0036] In various embodiments, a bonded structure can include a carrier including a first conductive contact and a second conductive contact, a first singulated element including a third conductive contact directly bonded to the first conductive contact without an adhesive, and a second singulated element including a fourth conductive contact directly bonded to the second conductive contact without an adhesive. In some embodiments, the third conductive contact comprises an electrically active contact electrically connected to circuitry of the first singulated element. In some embodiments, the third conductive contact is connected to a signal line, a power line, or electrical ground. In some embodiments, the at least one of the first and second singulated elements comprise an integrated device die having active circuitry. In some embodiments, the first singulated element comprises an integrated device die having active circuitry and the second singulated element comprises a passive component. In some embodiments, at least one of the first and second singulated elements are singulated with a reactive ion etching (RIE) process. In some embodiments, a maximum lateral width of at least one of the first and second singulated elements is no more than 4 mm. In some embodiments, a maximum lateral width of at least one of the first and second singulated elements is no more than 2 mm. In some embodiments, an edge exclusion distance between an outer edge of the first singulated element and the third conductive contact is less than 100 microns. In some

embodiments, the edge exclusion distance is no more than 50 microns. In some embodiments, the edge exclusion distance is no more than 10 microns. In some embodiments, the edge exclusion distance is in a range of 1 micron to 100 microns.

[0037] In various embodiments, a bonded structure can include a carrier, a first element directly bonded to the carrier without an adhesive, the first element including a cutout region, and a second singulated element directly bonded to the carrier without an adhesive, the second singulated element disposed at least partially laterally within the cutout region of the first element. In some embodiments, the bonded structure further comprises a third singulated element directly bonded to the carrier without an adhesive, the second singulated element disposed between the first element and the third singulated element. In some embodiments, a third element is directly bonded to the second singulated element. In some embodiments, the bonded structure comprises a conductive via through the second singulated element to connect to the third element. In some embodiments, the contact spacing is no more than a length of the conductive via.

[0038] In various embodiments, a bonded structure can include a first singulated element comprising a first conductive contact and a carrier comprising a second contact pad. In some embodiments, the first conductive contact and the second conductive contact are directly bonded to one another without an intervening adhesive. The first conductive contact can be spaced apart from an outer edge of the first singulated element by an edge exclusion distance of no more than 200 microns. In some embodiments, the first conductive contact comprises an electrically active contact electrically connected to circuitry of the first singulated element. In some embodiments, the edge exclusion distance is between about 10 microns and 100 microns.

[0039] In various embodiments, a bonded structure can include a first singulated element having a first plurality of conductive contacts spaced at a pitch. The first plurality of conductive contacts can include at least one outer conductive contact closest to an outer side edge of the first singulated element. In some embodiments the at least one outer conductive contact is spaced from the outer side edge by an edge exclusion distance and comprises an electrically active contact electrically connected to circuitry of the first singulated element and a carrier which comprises a second plurality of conductive contacts directly bonded to the first plurality of conductive contacts without an intervening adhesive. In some embodiments, the

ratio of the edge exclusion distance to the pitch is between about 10:1 and 50:1. In some embodiments, the ratio of the edge exclusion distance to the pitch is less than about 15:1.

[0040] In another embodiment, a bonded structure can include a first singulated element having a maximum lateral width and include a first plurality of conductive contacts. In some embodiments, the first plurality of conductive contacts includes at least one outer conductive contact closest to an outer side edge of the first singulated element. In some embodiments, the at least one outer conductive contact is spaced from the outer side edge by an edge exclusion distance and comprises an electrically active contact electrically connected to circuitry of the first singulated element; In some embodiments, the bonded structure can include a carrier which comprises a second plurality of conductive contacts directly bonded to the first plurality of conductive contacts without an intervening adhesive. In some embodiments, the ratio of the maximum lateral width to the edge exclusion distance is between about 10:1 and 100:1. In some embodiments, the ratio of the maximum lateral width to the exclusion distance is less than about 50:1.

[0041] In another embodiment, a bonded structure can include a carrier having first bonding surface which includes a first nonconductive region and a first plurality of conductive contacts. In some embodiments, the bonded structure includes a singulated device die having a second bonding surface including a second nonconductive region and a second plurality of conductive contacts. In some embodiments, the second nonconductive region is directly bonded to the first nonconductive region of the carrier without an adhesive and the second plurality of conductive contacts is directly bonded to the first plurality of conductive contacts without an adhesive. In some embodiments, the singulated device die includes an etched outer side edge extending non-parallel relative to the second bonding surface and the second plurality of conductive contacts includes at least five outer conductive contacts closest to the outer side edge, the at least five outer conductive contacts comprising an electrically active contact electrically connected to circuitry of the singulated device die. In some embodiments, the edge exclusion distance is no more than 50 microns. In some embodiments, the edge exclusion distance is no more than 10 microns. In some embodiments, wherein the edge exclusion distance is in a range of 1 micron to 100 microns. In some embodiments, the ratio of the edge exclusion distance to the pitch is less than 10. In some embodiments, the ratio of the edge exclusion distance to the pitch is less than 5. In some embodiments, the edge exclusion distance

to the pitch is less than 2. In some embodiments, the ratio of the maximum lateral width to the edge exclusion distance is less than 10. In some embodiments, the ratio of the maximum lateral width to the edge exclusion distance is less than 5. In some embodiments, the ratio of the maximum lateral width to the edge exclusion distance is less than 2. In some embodiments, the at least one outer conductive contact is electrically connected to a signal line, a power line, or electrical ground.

[0042] In various embodiments, an integrated device die can include active circuitry, a bonding surface configured for direct hybrid bonding to another element, an outer edge extending non-parallel relative to the bonding surface, and a first conductive contact spaced apart from the outer edge by an edge exclusion distance of no more than 100 microns. In some embodiments, the first conductive contact comprises an electrically active contact electrically connected to the active circuitry. In some embodiments, the edge exclusion distance is no more than 50 microns. In some embodiments, the first conductive contact is electrically connected to a signal line, a power line, or electrical ground. An integrated comprising a dummy inactive contact disposed between the first conductive contact and the outer edge of the die.

[0043] In various embodiments, an integrated device die can include active circuitry, a bonding surface configured for direct hybrid bonding to another element, an outer edge extending non-parallel relative to the bonding surface, and a first conductive contact spaced apart from the outer edge by an edge exclusion distance of no more than 100 microns. In some embodiments, the first conductive contact comprises an electrically active contact electrically connected to the active circuitry. In some embodiments, the edge exclusion distance is no more than 50 microns. In some embodiments, the first conductive contact is electrically connected to a signal line, a power line, or electrical ground. An integrated comprising a dummy inactive contact disposed between the first conductive contact and the outer edge of the die.

[0044] In various embodiments, a method for singulating dies includes planarizing a substrate, wherein the substrate comprises a plurality of conductive contacts, applying a protective layer on the substrate, patterning the protective layer on the substrate, transferring the substrate to a dicing frame, and singulating the substrate, via an etching process, into a plurality of singulated elements. In some embodiments, the etching process comprises a dry

etching process, a wet etching process, or a fine dicing blade. In some embodiments, the dry etching process is reactive ion etching. In some embodiments, singulating the substrate is accomplished through a combination of etching processes.

[0045] In various embodiments, the method for singulating dies can further comprise removing the protective layer from the substrate, processing the substrate with a treatment method, and preparing the substrate for direct bonding to another element. In some embodiments, the treatment method comprises ashing, surface activation or nitrogen plasma treatment. In some embodiments, preparing the substrate for direct bonding further comprises cleaning, rinsing, and drying the substrate.

[0046] In various embodiments, a method for creating a bonded structure can include singulating a first and second elements, wherein the first and second element comprise an edge exclusion distance of no more than 100 microns, and bonding the first and second singulated elements to a carrier, wherein the distance between the first and second singulated elements is no more than 10 microns. In some embodiments, bonding the first and second singulated elements to a carrier comprises directly bonding the first and second singulated elements to the carrier without the use of an adhesive. In some embodiments, singulating a first and second elements, comprises singulating the first and second elements using reactive ion etching.

[0047] The skilled artisan will appreciate that features of the above-reference embodiments can be informed, without limitation, by the additional disclosures provided in U.S. Provisional Application No. 63/313,639, the entire contents of which are incorporated by reference herein in its entirety and for all purposes.

Examples of Direct Bonding Methods and Directly Bonded Structures

[0048] Various embodiments disclosed herein relate to directly bonded structures in which two or more elements can be directly bonded to one another without an intervening adhesive. Figures 5A and 5B schematically illustrate a process for forming a directly hybrid bonded structure without an intervening adhesive according to some embodiments. In Figures 5A and 5B, a bonded structure 517 comprises two elements 543 and 544 that can be directly bonded to one another at a bond interface 545 without an intervening adhesive. Two or more microelectronic elements 543 and 544 (such as semiconductor elements, including, for example, integrated device dies, wafers, passive devices, individual active devices such as

power switches, etc.) may be stacked on or bonded to one another to form the bonded structure 517. Conductive features 546a (e.g., contact pads, traces, exposed ends of vias through substrate electrodes or vias) of a first element 543 may be electrically connected to corresponding conductive features 546b of a second element 544. Any suitable number of elements can be stacked in the bonded structure 517. For example, a third element (not shown) can be stacked on the second element 544, a fourth element (not shown) can be stacked on the third element, and so forth. Additionally or alternatively, one or more additional elements (not shown) can be stacked laterally adjacent one another along the first element 543. In some embodiments, the laterally stacked additional element may be smaller than the second element. In some embodiments, the laterally stacked additional element may be two times smaller than the second element.

[0049] In some embodiments, the elements 543 and 544 are directly bonded to one another without an adhesive. In various embodiments, a non-conductive field region that includes a non-conductive or dielectric material can serve as a first bonding layer 509a of the first element 543 which can be directly bonded to a corresponding non-conductive field region that includes a non-conductive or dielectric material serving as a second bonding layer 509b of the second element 104 without an adhesive. The non-conductive bonding layers 509a and 509b can be disposed on respective front sides 547a and 547b of device portions 548a and 548b, such as a semiconductor (e.g., silicon) portion of the elements 543, 544, or back-end-of-line (BEOL) interconnect layers over such semiconductor portions. Active devices and/or circuitry can be patterned and/or otherwise disposed in or on the device portions 548a and 548b. Active devices and/or circuitry can be disposed at or near the front sides 547a and 547b of the device portions 548a and 548b, and/or at or near opposite backsides 549a and 549b of the device portions 548a and 548b. Bonding layers can be provided on front sides and/or back sides of the elements. The non-conductive material can be referred to as a non-conductive bonding region or bonding layer 509a of the first element 543. In some embodiments, the non-conductive bonding layer 509a of the first element 543 can be directly bonded to the corresponding non-conductive bonding layer 509b of the second element 544 using dielectric-to-dielectric bonding techniques. For example, non-conductive or dielectric-to-dielectric bonds may be formed without an adhesive using the direct bonding techniques disclosed at least in U.S. Patent Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of

which are incorporated by reference herein in their entirety and for all purposes. It should be appreciated that in various embodiments, the bonding layers 509a and/or 509b can comprise a non-conductive material such as a dielectric material, such as silicon oxide, or an undoped semiconductor material, such as undoped silicon. Suitable dielectric bonding surface or materials for direct bonding include but are not limited to inorganic dielectrics including silicon, such as silicon oxide, silicon nitride, or silicon oxynitride, or can include carbon, such as silicon carbide, silicon oxycarbonitride, low K dielectric materials, SiCOH dielectrics, silicon carbonitride or diamond-like carbon or a material comprising a diamond surface. Such carbon-containing ceramic materials can be considered inorganic, despite the inclusion of carbon. In some embodiments, the dielectric materials do not comprise polymer materials, such as epoxy, resin or molding materials.

[0050] In some embodiments, the device portions 548a and 548b can have a significantly different coefficients of thermal expansion (CTEs) defining a heterogenous structure. The CTE difference between the device portions 548a and 548b, and particularly between bulk semiconductor, typically single crystal portions of the device portions 548a, 548b, can be greater than 5 ppm or greater than 10 ppm. For example, the CTE difference between the device portions 548a and 548b can be in a range of 5 ppm to 100 ppm, 5 ppm to 40 ppm, 10 ppm to 100 ppm, or 10 ppm to 40 ppm. In some embodiments, one of the device portions 548a and 548b can comprise optoelectronic single crystal materials, including perovskite materials, that are useful for optical piezoelectric or pyroelectric applications, and the other of the device portions 548a, 548b comprises a more conventional substrate material. For example, one of the device portions 548a, 548b comprises lithium tantalate (LiTaO₃) or lithium niobate (LiNbO₃), and the other one of the device portions 548a, 548b comprises silicon (Si), quartz, fused silica glass, sapphire, or a glass. In other embodiments, one of the device portions 548a and 548b comprises a III-V single semiconductor material, such as gallium arsenide (GaAs) or gallium nitride (GaN), and the other one of the device portions 548a and 548b can comprise a non-III-V semiconductor material, such as silicon (Si), or can comprise other materials with similar CTE, such as quartz, fused silica glass, sapphire, or a glass.

[0051] In various embodiments, direct hybrid bonds can be formed without an intervening adhesive. For example, nonconductive bonding surfaces 550a and 550b can be

polished to a high degree of smoothness. The nonconductive bonding surfaces 550a and 550b can be polished using, for example, chemical mechanical polishing (CMP). The roughness of the polished bonding surfaces 550a and 550b can be less than 30 Å rms. For example, the roughness of the bonding surfaces 550a and 550b can be in a range of about 0.1 Å rms to 15 Å rms, 0.5 Å rms to 10 Å rms, or 1 Å rms to 5 Å rms. The bonding surfaces 550a and 550b can be cleaned and exposed to a plasma and/or etchants to activate the surfaces 550a and 550b. In some embodiments, the surfaces 550a and 550b can be terminated with a species after activation or during activation (e.g., during the plasma and/or etch processes). Without being limited by theory, in some embodiments, the activation process can be performed to break chemical bonds at the bonding surfaces 550a and 550b, and the termination process can provide additional chemical species at the bonding surfaces 550a and 550b that improves the bonding energy during direct bonding. In some embodiments, the activation and termination are provided in the same step, e.g., a plasma to activate and terminate the surfaces 550a and 550b. In other embodiments, the bonding surfaces 550a and 550b can be terminated in a separate treatment to provide the additional species for direct bonding. In various embodiments, the terminating species can comprise nitrogen. For example, in some embodiments, the bonding surface(s) 550a, 550b can be exposed to a nitrogen-containing plasma. Further, in some embodiments, the bonding surfaces 550a and 550b can be exposed to fluorine. For example, there may be one or multiple fluorine peaks at or near a bond interface 545 between the first and second elements 543, 544. Thus, in the directly bonded structure 517, the bond interface 545 between two non-conductive materials (e.g., the bonding layers 509a and 509b) can comprise a very smooth interface with higher nitrogen content and/or fluorine peaks at the bond interface 545. Additional examples of activation and/or termination treatments may be found throughout U.S. Patent Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes. The roughness of the polished bonding surfaces 550a and 550b can be slightly rougher (e.g., about 1 Å rms to 30 Å rms, 3 Å rms to 20 Å rms, or possibly rougher) after an activation process.

[0052] In various embodiments, conductive features 546a of the first element 543 can also be directly bonded to corresponding conductive features 546b of the second element 544 without an adhesive (e.g., without solder or other conductive adhesive intervening between the conductive features 546a, 546b). For example, a direct hybrid bonding technique can be

used to provide conductor-to-conductor direct bonds along the bond interface 545 that includes covalently direct bonded non-conductive-to-non-conductive (e.g., dielectric-to-dielectric) surfaces, prepared as described above. In various embodiments, the conductor-to-conductor (e.g., conductive feature 546a to conductive feature 546b) direct bonds and the dielectric-to-dielectric hybrid bonds can be formed using the direct hybrid bonding techniques disclosed at least in U.S. Patent Nos. 9,716,033 and 9,852,988, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes. In direct hybrid bonding embodiments described herein, conductive features are provided within non-conductive bonding layers, and both conductive and nonconductive features are prepared for direct bonding, such as by the planarization, activation and/or termination treatments described above. Thus, the bonding surface prepared for direct hybrid bonding includes both conductive and non-conductive features.

[0053] For example, non-conductive (e.g., dielectric) bonding surfaces 550a, 550b (for example, inorganic dielectric surfaces) can be prepared and directly bonded to one another without an intervening adhesive as explained above. Conductive contact features (e.g., conductive features 546a and 546b which may be at least partially surrounded by non-conductive dielectric field regions within the bonding layers 509a, 509b) may also directly bond to one another without an intervening adhesive. In various embodiments, the conductive features 546a, 546b can comprise discrete pads or traces at least partially embedded in the non-conductive field regions. In some embodiments, the conductive contact features can comprise exposed contact surfaces of through substrate vias (e.g., through silicon vias (TSVs)). In some embodiments, the respective conductive features 546a and 546b can be recessed below exterior (e.g., upper) surfaces (non-conductive bonding surfaces 550a and 550b) of the dielectric field region or non-conductive bonding layers 509a and 509b, for example, recessed by less than 30 nm, less than 20 nm, less than 15 nm, or less than 10 nm, for example, recessed in a range of 2 nm to 20 nm, or in a range of 4 nm to 10 nm. The recess can be at or near the middle or center of the cavity in which the conductive features 546a, 546b are disposed, and, additionally or alternatively, can extend or be disposed along sides of the cavity in which the conductive features 546a, 546b are disposed. In various embodiments, prior to direct bonding, the recesses in the opposing elements can be sized such that the total gap between opposing contact pads is less than 15 nm, or less than 10 nm. The non-conductive bonding layers 509a and 509b can

be directly bonded to one another without an adhesive at room temperature in some embodiments and, subsequently, the bonded structure 517 can be annealed. Upon annealing, the conductive features 546a and 546b can expand and contact one another to form a metal-to-metal direct bond. Beneficially, the use of Direct Bond Interconnect, or DBI®, techniques commercially available from Adeia of San Jose, CA, can enable high density of conductive features 546a and 546b to be connected across the direct bond interface 545 (e.g., small or fine pitches for regular arrays). In some embodiments, the pitch of the conductive features 546a and 546b, such as conductive traces embedded in the bonding surface of one of the bonded elements, may be less than 100 microns or less than 10 microns or even less than 2 microns. For some applications, the ratio of the pitch of the conductive features 546a and 546b to one of the dimensions (e.g., a diameter) of the bonding pad is less than 20, or less than 10, or less than 5, or less than 3 and sometimes desirably less than 2. In other applications, the width of the conductive traces embedded in the bonding surface of one of the bonded elements may range between 0.3 to 20 microns, e.g., in a range of 0.3 to 3 microns. In various embodiments, the conductive features 546a and 546b and/or traces can comprise copper or copper alloys, although other metals may be suitable. For example, the conductive features disclosed herein, such as the conductive features 546a and 546b, can comprise fine-grain metal (e.g., a fine-grain copper).

[0054] Thus, in direct bonding processes, a first element 543 can be directly bonded to a second element 544 without an intervening adhesive. In some arrangements, the first element 543 can comprise a singulated element, such as a singulated integrated device die. In other arrangements, the first element 543 can comprise a carrier or substrate (e.g., a wafer) that includes a plurality (e.g., tens, hundreds, or more) of device regions that, when singulated, form a plurality of integrated device dies. Similarly, the second element 544 can comprise a singulated element, such as a singulated integrated device die. In other arrangements, the second element 104 can comprise a carrier or substrate (e.g., a wafer). The embodiments disclosed herein can accordingly apply to wafer-to-wafer (W2W), die-to-die (D2D), or die-to-wafer (D2W) bonding processes. In W2W processes, two or more wafers can be directly bonded to one another (e.g., direct hybrid bonded) and singulated using a suitable singulation process. After singulation, side edges of the singulated structure (e.g., the side edges of the two bonded elements) may be substantially flush and may include markings indicative of the

common singulation process for the bonded structure (e.g., saw markings if a saw singulation process is used).

[0055] As explained herein, the first and second elements 543 and 544 can be directly bonded to one another without an adhesive, which is different from a deposition process and results in a structurally different interface compared to a deposition. In one application, a width of the first element 543 in the bonded structure is similar to a width of the second element 544. In some other embodiments, a width of the first element 543 in the bonded structure 517 is different from a width of the second element 544. Similarly, the width or area of the larger element in the bonded structure may be at least 10% larger than the width or area of the smaller element. The first and second elements 543 and 544 can accordingly comprise non-deposited elements. Further, directly bonded structures 517, unlike deposited layers, can include a defect region along the bond interface 545 in which nanometer-scale voids (nanovoids) are present. The nanovoids may be formed due to activation of the bonding surfaces 550a and 550b (e.g., exposure to a plasma). As explained above, the bond interface 545 can include concentration of materials from the activation and/or last chemical treatment processes. For example, in embodiments that utilize a nitrogen plasma for activation, a nitrogen peak can be formed at the bond interface 545. The nitrogen peak can be detectable using secondary ion mass spectroscopy (SIMS) techniques. In various embodiments, for example, a nitrogen termination treatment (e.g., exposing the bonding surface to a nitrogen-containing plasma) can replace OH groups of a hydrolyzed (OH-terminated) surface with NH₂ molecules, yielding a nitrogen-terminated surface. In embodiments that utilize an oxygen plasma for activation, an oxygen peak can be formed at the bond interface 545. In some embodiments, the bond interface 545 can comprise silicon oxynitride, silicon oxycarbonitride, or silicon carbonitride. As explained herein, the direct bond can comprise a covalent bond, which is stronger than van Der Waals bonds. The bonding layers 509a and 509b can also comprise polished surfaces that are planarized to a high degree of smoothness.

[0056] In various embodiments, the metal-to-metal bonds between the conductive features 546a and 546b can be joined such that metal grains grow into each other across the bond interface 545. In some embodiments, the metal is or includes copper, which can have grains oriented along the 111 crystal plane for improved copper diffusion across the bond interface 545. In some embodiments, the conductive features 546a and 546b may include

nanotwinned copper grain structure, which can aid in merging the conductive features during anneal. The bond interface 545 can extend substantially entirely to at least a portion of the bonded conductive features 546a and 546b, such that there is substantially no gap between the non-conductive bonding layers 509a and 509b at or near the bonded conductive features 546a and 546b. In some embodiments, a barrier layer may be provided under and/or laterally surrounding the conductive features 546a and 546b (e.g., which may include copper). In other embodiments, however, there may be no barrier layer under the conductive features 546a and 546b, for example, as described in U.S. Patent No. 11,195,748, which is incorporated by reference herein in its entirety and for all purposes.

[0057] Beneficially, the use of the hybrid bonding techniques described herein can enable extremely fine pitch between adjacent conductive features 546a and 546b, and/or small pad sizes. For example, in various embodiments, the pitch p (i.e., the distance from edge-to-edge or center-to-center, as shown in Figure 5A) between adjacent conductive features 546a (or 546b) can be in a range of 0.5 microns to 50 microns, in a range of 0.75 microns to 25 microns, in a range of 1 micron to 25 microns, in a range of 1 micron to 10 microns, or in a range of 1 micron to 5 microns. Further, a major lateral dimension (e.g., a pad diameter) can be small as well, e.g., in a range of 0.25 microns to 30 microns, in a range of 0.25 microns to 5 microns, or in a range of 0.5 microns to 5 microns.

[0058] As described above, the non-conductive bonding layers 509a, 509b can be directly bonded to one another without an adhesive and, subsequently, the bonded structure 517 can be annealed. Upon annealing, the conductive features 546a, 546b can expand and contact one another to form a metal-to-metal direct bond. In some embodiments, the materials of the conductive features 546a, 546b can interdiffuse during the annealing process.

[0059] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” “include,” “including” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word “connected”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,”

“below,” and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Moreover, as used herein, when a first element is described as being “on” or “over” a second element, the first element may be directly on or over the second element, such that the first and second elements directly contact, or the first element may be indirectly on or over the second element such that one or more elements intervene between the first and second elements. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0060] Moreover, conditional language used herein, such as, among others, “can,” “could,” “might,” “may,” “e.g.,” “for example,” “such as” and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments.

[0061] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel apparatus, methods, and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. For example, while blocks are presented in a given arrangement, alternative embodiments may perform similar functionalities with different components and/or circuit topologies, and some blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these blocks may be implemented in a variety of different ways. Any suitable combination of the elements and acts of the various embodiments described above can be combined to provide further embodiments. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A bonded structure comprising:
a carrier including a first conductive contact and a second conductive contact;
a first singulated element including a third conductive contact directly bonded to the first conductive contact without an adhesive; and
a second singulated element including a fourth conductive contact directly bonded to the second conductive contact without an adhesive,
wherein the first and second conductive contacts are spaced apart by a contact spacing of no more than 250 microns.
2. A bonded structure comprising:
a carrier including a first conductive contact and a second conductive contact;
a first singulated element including a third conductive contact directly bonded to the first conductive contact without an adhesive; and
a second singulated element including a fourth conductive contact directly bonded to the second conductive contact without an adhesive,
wherein the first and second singulated elements are spaced apart by an element spacing of no more than 50 microns.
3. A bonded structure comprising:
a carrier including a first conductive contact and a second conductive contact;
a first singulated element including a third conductive contact directly bonded to the first conductive contact without an adhesive; and
a second singulated element including a fourth conductive contact directly bonded to the second conductive contact without an adhesive,
wherein the first and second conductive contacts are spaced apart by a contact spacing of between about 0.4 times and 8 times a thickness of at least one of the first and second singulated elements.
4. The bonded structure of any one of Claims 1 to 3, wherein the first and second singulated elements are spaced apart by an element spacing of no more than 10 microns.
5. The bonded structure of any one of Claims 1 to 4, wherein the carrier and the first and second singulated elements are direct hybrid bonded.

6. The bonded structure of Claim 3, wherein the contact spacing is less than about 2 times the thickness of at least one of the first and second singulated elements.

7. The bonded structure of any one of Claims 1 to 3, wherein the first and second singulated elements included respective nonconductive regions directly bonded to corresponding nonconductive region(s) of the carrier without an adhesive.

8. The bonded structure of any one of Claims 1 to 7, wherein the contact spacing is no more than 200 microns.

9. The bonded structure of any one of Claims 1 to 7, wherein the contact spacing is no more than 100 microns.

10. The bonded structure of any one of Claims 1 to 7, wherein the contact spacing is no more than 50 microns.

11. The bonded structure of any one of Claims 1 to 7, wherein the contact spacing is no more than 10 microns.

12. The bonded structure of any one of Claims 1 to 7, wherein the contact spacing is no more than 5 microns.

13. The bonded structure of any one of Claims 1 to 7, wherein the contact spacing is no more than 2 microns.

14. The bonded structure of any one of Claims 1 to 7, wherein the contact spacing is in a range of 1 micron to 250 microns.

15. The bonded structure of any one of Claims 1 to 7, wherein the contact spacing is in a range of 1 micron to 100 microns.

16. The bonded structure of any one of Claims 1 to 7, wherein the contact spacing is in a range of 1 micron to 20 microns.

17. The bonded structure of any one of Claims 1 to 15, wherein the element spacing is no more than 20 microns.

18. The bonded structure of any one of Claims 1 to 15, wherein the element spacing is no more than 10 microns.

19. The bonded structure of Claim 6, wherein the contact spacing is no more than the thickness of at least one of the first and second singulated elements.

20. The bonded structure of any one of Claims 1 to 19, wherein the third conductive contact comprises an electrically active contact electrically connected to circuitry of the first singulated element.

21. The bonded structure of Claim 20, wherein the third conductive contact is connected to a signal line, a power line, or electrical ground.

22. The bonded structure of any one of Claims 1 to 21, wherein at least one of the first and second singulated elements comprises an integrated device die having active circuitry.

23. The bonded structure of Claim 22, wherein the first singulated element comprises an integrated device die having active circuitry and the second singulated element comprises a passive component.

24. The bonded structure of any one of Claims 1 to 23, wherein at least one of the first and second singulated elements are singulated with a reactive ion etching (RIE) process.

25. The bonded structure of any one of Claims 1 to 24, wherein a maximum lateral width of at least one of the first and second singulated elements is no more than 4 mm.

26. The bonded structure of any one of Claims 1 to 24, wherein a maximum lateral width of at least one of the first and second singulated elements is no more than 2 mm.

27. The bonded structure of any one of Claims 1 to 26, wherein an edge exclusion distance between an outer edge of the first singulated element and the third conductive contact is less than 100 microns.

28. The bonded structure of Claim 27, wherein the edge exclusion distance is no more than 50 microns.

29. The bonded structure of Claim 28, wherein the edge exclusion distance is no more than 10 microns.

30. The bonded structure of any one of Claims 27 to 29, wherein the edge exclusion distance is in a range of 1 micron to 100 microns.

31. The bonding structure of any one of Claims 1 to 3, wherein the second singulated element comprises at least one conductive through substrate via (TSV).

32. A bonded structure comprising:

a carrier;

a first element directly bonded to the carrier without an adhesive, the first element including a cutout region; and

a second singulated element directly bonded to the carrier without an adhesive, the second singulated element disposed at least partially laterally within the cutout region of the first element.

33. The bonded structure of Claim 32, further comprising a third singulated element directly bonded to the carrier without an adhesive, the second singulated element disposed between the first element and the third singulated element.

34. The bonded structure of any one of Claims 1 to 33, further comprising a third element directly bonded to the second singulated element.

35. The bonded structure of Claim 34, further comprising a conductive via through the second singulated element to connect to the third element.

36. The bonded structure of Claim 35, wherein the contact spacing is no more than a length of the conductive via.

37. A bonded structure comprising:

a first singulated element comprising a first conductive contact; and

a carrier comprising a second conductive contact, the first conductive contact and the second conductive contact directly bonded to one another without an intervening adhesive, the first conductive contact spaced apart from an outer edge of the first singulated element by an edge exclusion distance of no more than 200 microns, the first conductive contact comprising an electrically active contact electrically connected to circuitry of the first singulated element.

38. The bonded structure of Claim 37, wherein the edge exclusion distance is between about 10 microns and 100 microns.

39. A bonded structure comprising:

a first singulated element having a first plurality of conductive contacts spaced at a pitch, the first plurality of conductive contacts including at least one outer conductive contact closest to an outer side edge of the first singulated element, the at least one outer conductive contact spaced from the outer side edge by an edge exclusion distance and comprising an electrically active contact electrically connected to circuitry of the first singulated element; and

a carrier comprising a second plurality of conductive contacts directly bonded to the first plurality of conductive contacts without an intervening adhesive,

wherein a ratio of the edge exclusion distance to the pitch is between about 10:1 and 50:1.

40. The bonded structure of Claim 39, wherein the ratio of the edge exclusion distance to the pitch is less than about 15:1.

41. A bonded structure comprising:

a first singulated element having a maximum lateral width and including a first plurality of conductive contacts, the first plurality of conductive contacts including at least one outer conductive contact closest to an outer side edge of the first singulated element, the at least one outer conductive contact spaced from the outer side edge by an edge exclusion distance and comprising an electrically active contact electrically connected to circuitry of the first singulated element; and

a carrier comprising a second plurality of conductive contacts directly bonded to the first plurality of conductive contacts without an intervening adhesive,

wherein a ratio of the maximum lateral width to the edge exclusion distance is between about 10:1 and 100:1.

42. The bonded structure of Claim 41, wherein the ratio of the maximum lateral width to the exclusion distance is less than about 50:1.

43. A bonded structure comprising:

a carrier having a first bonding surface including a first nonconductive region and a first plurality of conductive contacts; and

a singulated device die having a second bonding surface including a second nonconductive region and a second plurality of conductive contacts, the second nonconductive region directly bonded to the first nonconductive region of the carrier without an adhesive and the second plurality of conductive contacts directly bonded to the first plurality of conductive contacts without an adhesive,

wherein the singulated device die includes an etched outer side edge extending non-parallel relative to the second bonding surface and the second plurality of conductive contacts includes at least five outer conductive contacts closest to the outer side edge, the at least five outer conductive contacts comprising an electrically active contact electrically connected to circuitry of the singulated device die.

44. The bonded structure of any one of Claims 37 to 43, wherein the edge exclusion distance is no more than 50 microns.

45. The bonded structure of Claim 44, wherein the edge exclusion distance is no more than 10 microns.

46. The bonded structure of any one of Claims 37 to 45, wherein the edge exclusion distance is in a range of 1 micron to 100 microns.

47. The bonded structure of any one of Claims 37 to 46, wherein the ratio of the edge exclusion distance to the pitch is less than 10.

48. The bonded structure of Claim 47, wherein the ratio of the edge exclusion distance to the pitch is less than 5.

49. The bonded structure of Claim 48, wherein the ratio of the edge exclusion distance to the pitch is less than 2.

50. The bonded structure of any one of Claims 37 to 49, wherein the ratio of the maximum lateral width to the edge exclusion distance is less than 10.

51. The bonded structure of Claim 50, wherein the ratio of the maximum lateral width to the edge exclusion distance is less than 5.

52. The bonded structure of Claim 51, wherein the ratio of the maximum lateral width to the edge exclusion distance is less than 2.

53. The bonded structure of any one of Claims 37 to 52, wherein the at least one outer conductive contact is electrically connected to a signal line, a power line, or electrical ground.

54. An integrated device die comprising:
active circuitry;
a bonding surface configured for direct hybrid bonding to another element;
an outer edge extending non-parallel relative to the bonding surface; and
a first conductive contact spaced apart from the outer edge by an edge exclusion distance of no more than 100 microns, the first conductive contact comprising an electrically active contact electrically connected to the active circuitry.

55. The integrated device die of Claim 54, wherein the edge exclusion distance is no more than 50 microns.

56. The integrated device die of Claim 54 or 55, wherein the first conductive contact is electrically connected to a signal line, a power line, or electrical ground.

57. The integrated device die of Claim 54, further comprising a dummy inactive contact disposed between the first conductive contact and the outer edge of the die.

58. A method for bonding dies comprising:

planarizing a first element, wherein the first element comprises a first plurality of conductive contacts;

planarizing a second element, wherein the second element comprises a second plurality of conductive contacts; and

bonding the first and second elements to a carrier, wherein a first outermost conductive contact of the first plurality of conductive contacts of the first element is spaced apart from a second outermost conductive contact of the second plurality of conductive contacts by a contact spacing of no more than 250 microns.

59. The method of Claim 58, further comprising:

applying a protective layer on the first element;

patterning the protective layer on the first element; and

transferring the first element to a dicing frame.

60. The method of Claim 59, further comprising singulating the first element, via an etching process, into a plurality of singulated elements.

61. The method of Claim 60, wherein the etching process comprises at least one of a dry etching process and a wet etching process.

62. The method of Claim 60, wherein the dry etching process is reactive ion etching (RIE) process.

63. The method of claim 60, wherein singulating the first element is accomplished through a combination of wet and dry etching processes.

64. The method of Claim 60, further comprising:

removing the protective layer from the first element;

processing the first element with a treatment method; and

preparing the first element for direct bonding to another element.

65. The method of Claim 64, wherein the treatment method comprises surface activation.

66. The method of Claim 64, wherein preparing the first element for direct bonding further comprises cleaning, rinsing, and drying the substrate.

67. A method for creating a bonded structure, comprising:

singulating first and second elements, wherein each of the first and second element comprise an edge exclusion distance of no more than 100 microns; and

bonding the first and second singulated elements to a carrier, wherein the distance between the first and second singulated elements is no more than 10 microns.

68. The method of Claim 67, wherein bonding the first and second singulated elements to a carrier comprises directly bonding the first and second singulated elements to the carrier without the use of an adhesive.

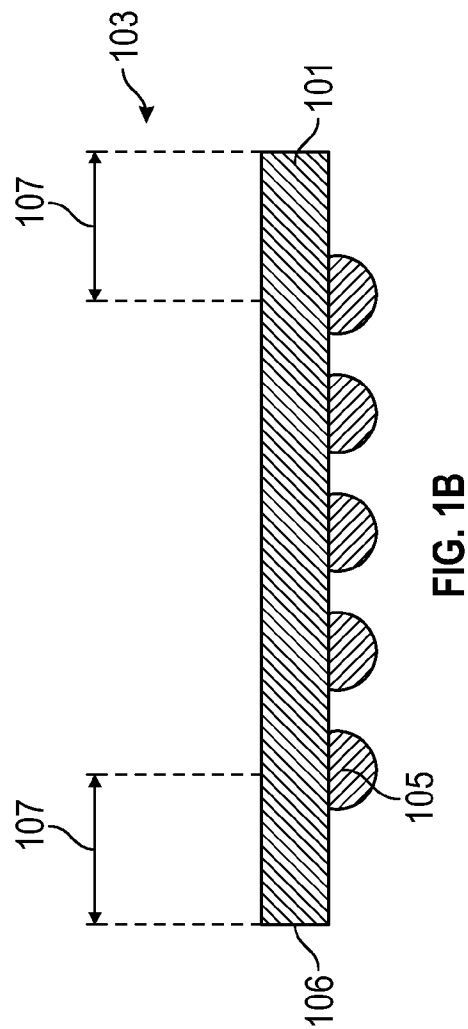
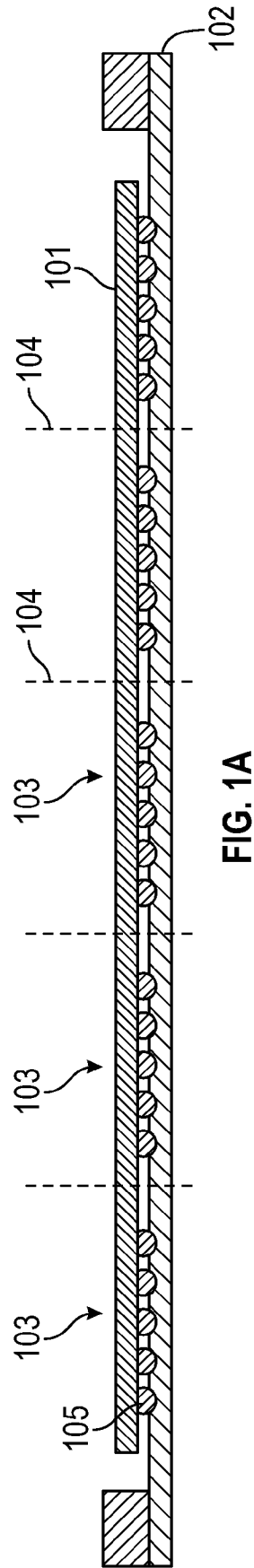
69. The method of Claim 67, wherein singulating a first and second elements, comprises singulating the first and second elements using reactive ion etching.

70. A bonded structure comprising:

a first singulated element comprising a first conductive contact; and

a carrier comprising a second contact pad, the first conductive contact and the second conductive contact directly bonded to one another without an intervening adhesive, the first conductive contact spaced apart from an outer edge of the first singulated element by an edge exclusion distance of no more than 200 microns, the first conductive contact comprising an electrically active contact electrically connected to circuitry of the first singulated element; wherein at least one of the first singulated element and the carrier are packaged in an integrated device package.

71. The bonded structure of Claim 70, wherein the integrated device package comprises of one or more dies at least partially embedded in an encapsulating material.



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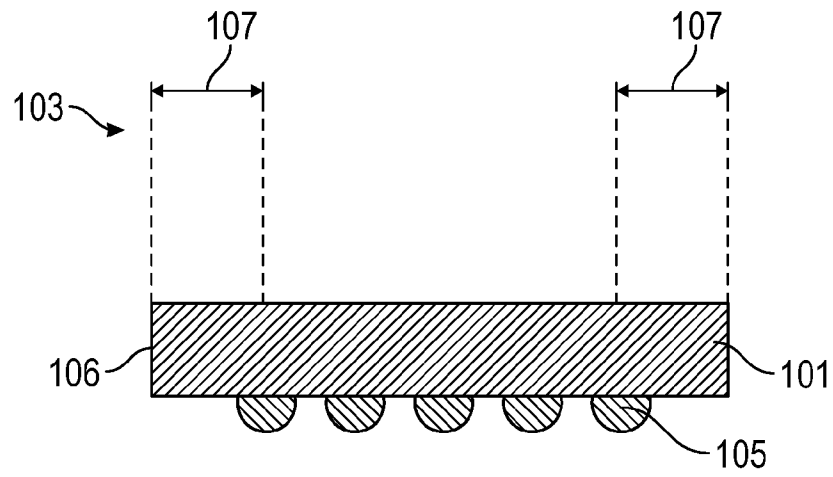


FIG. 1C

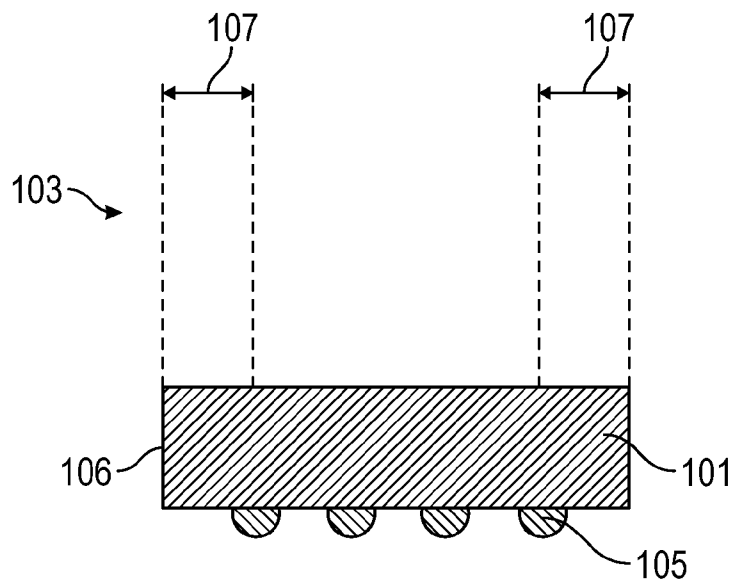


FIG. 1D

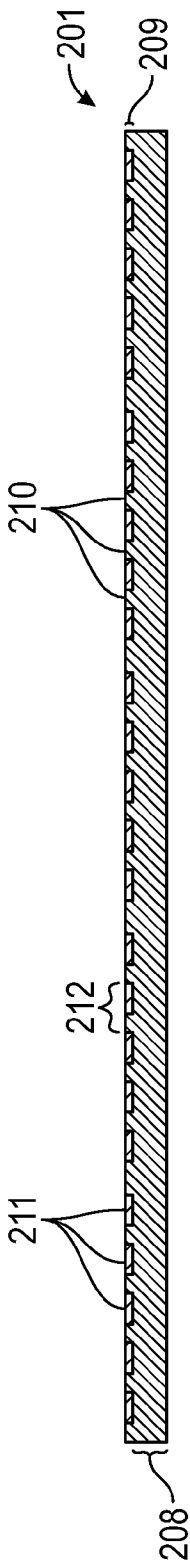


FIG. 2A

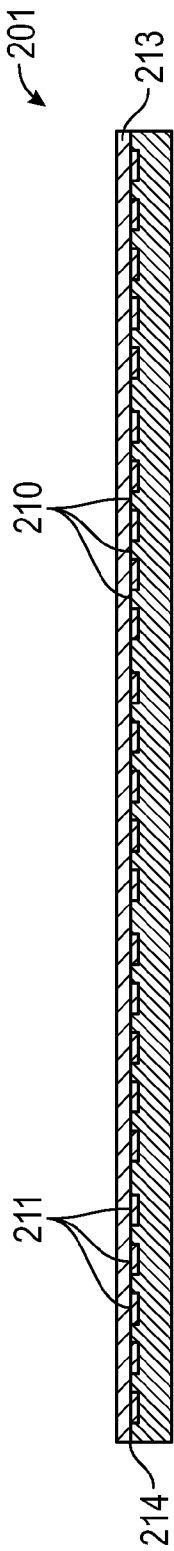


FIG. 2B

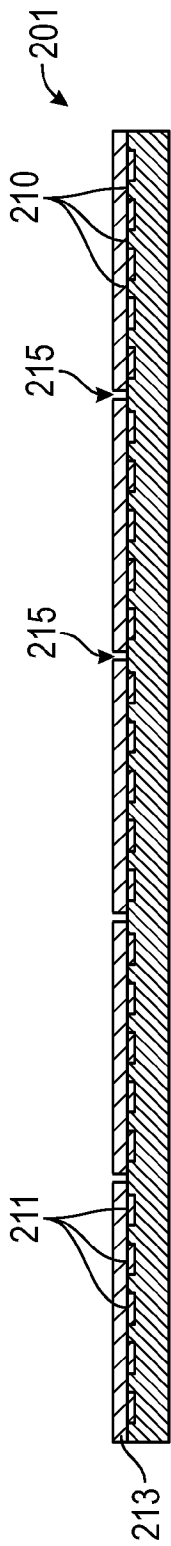


FIG. 2C

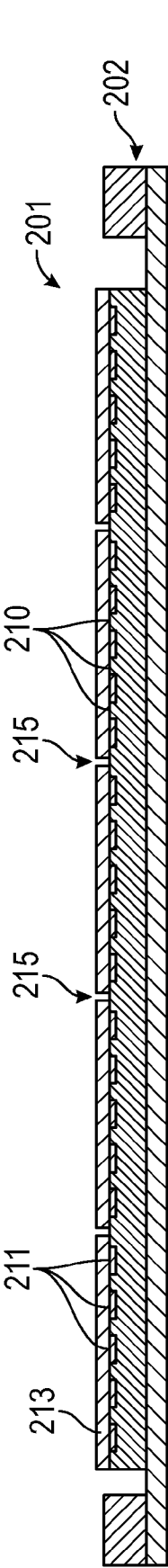


FIG. 2D

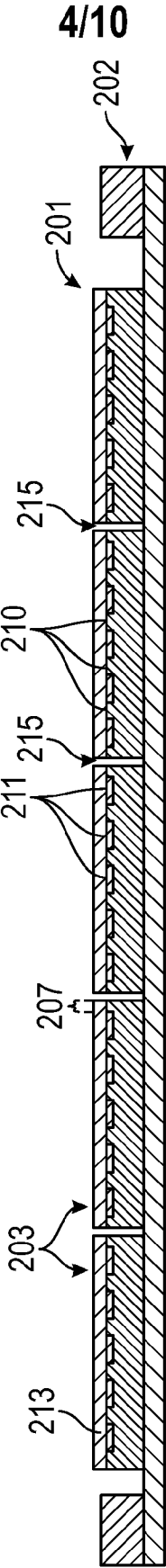


FIG. 2E

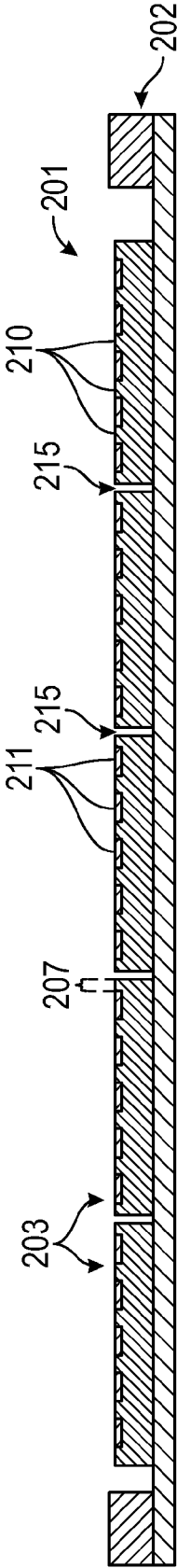


FIG. 2F

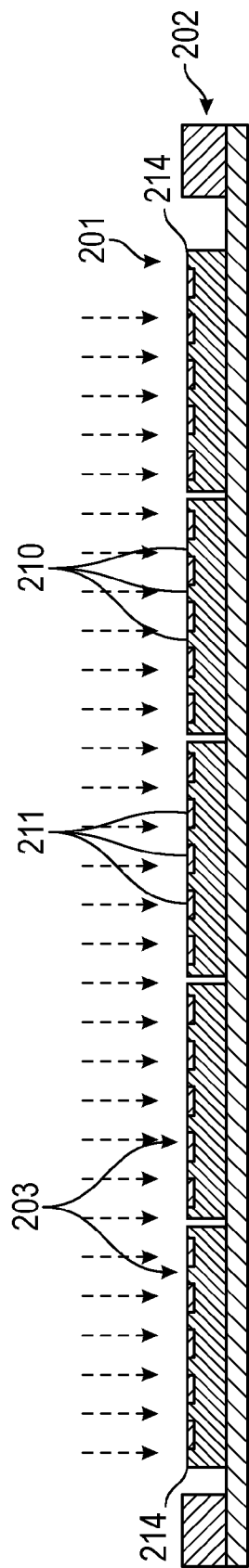


FIG. 2G

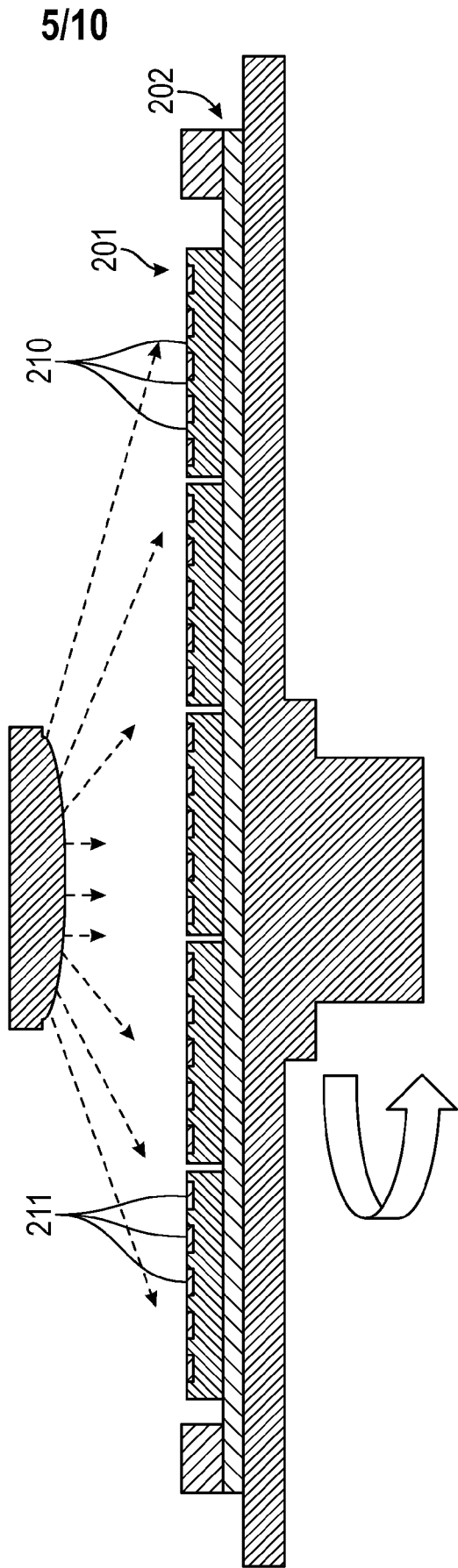


FIG. 2H

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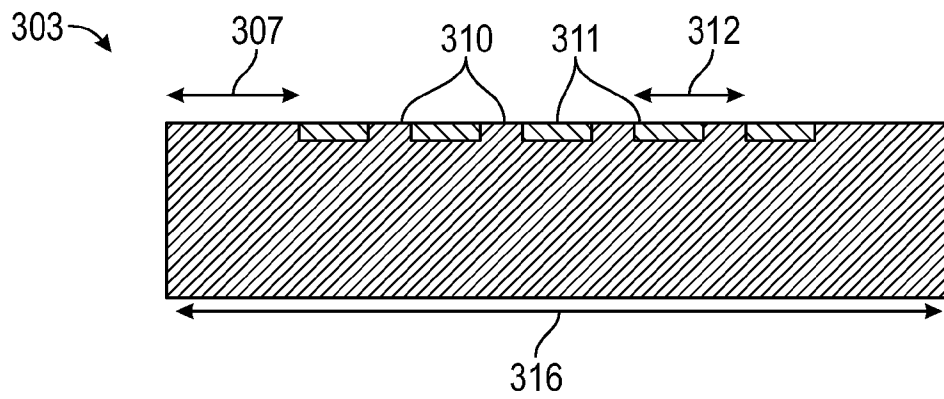


FIG. 3

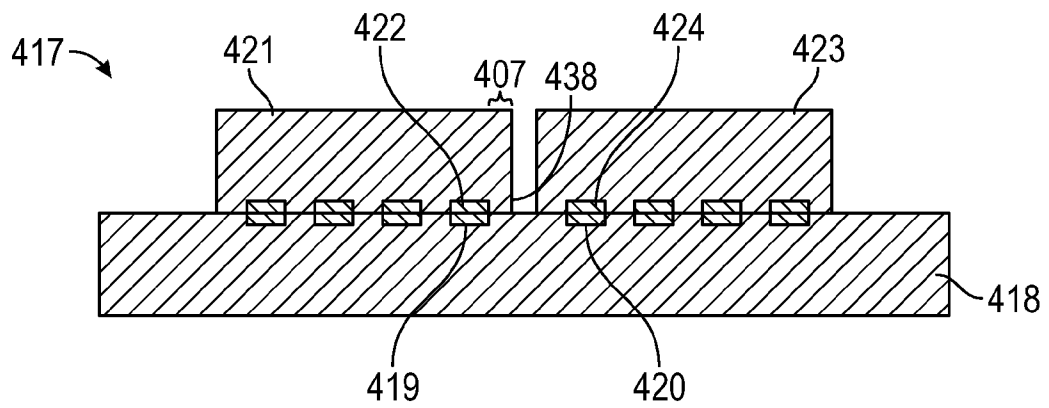


FIG. 4A

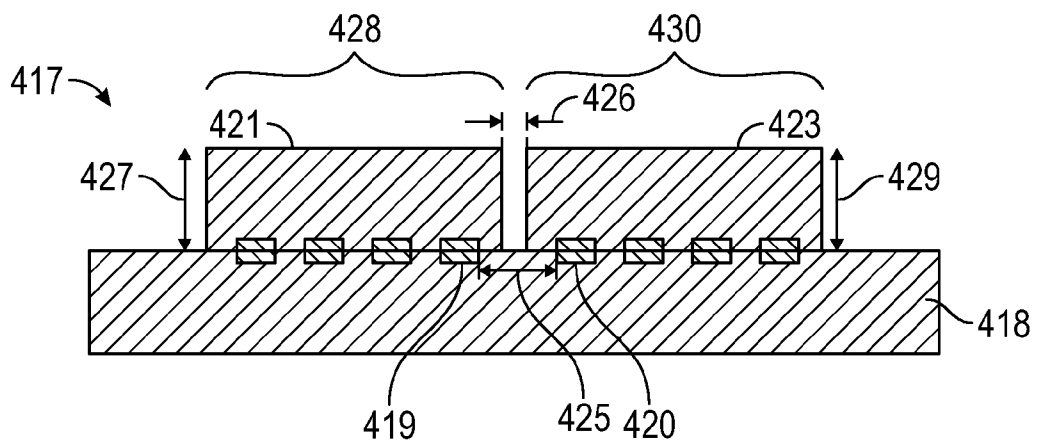


FIG. 4B

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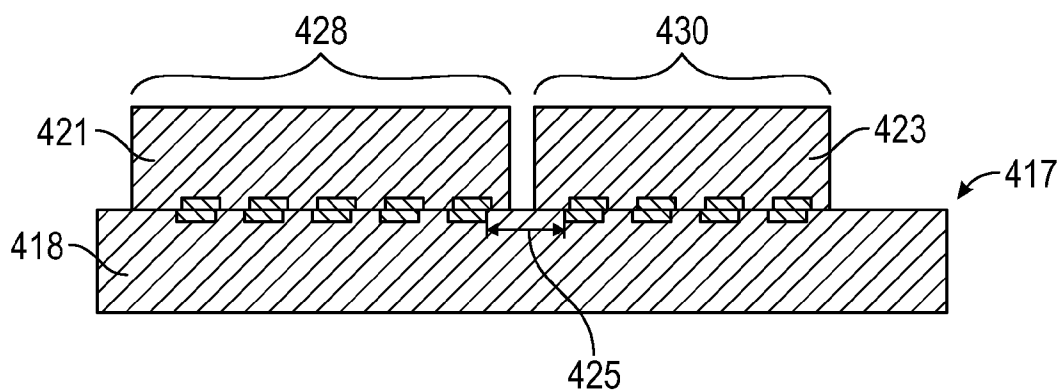


FIG. 4C

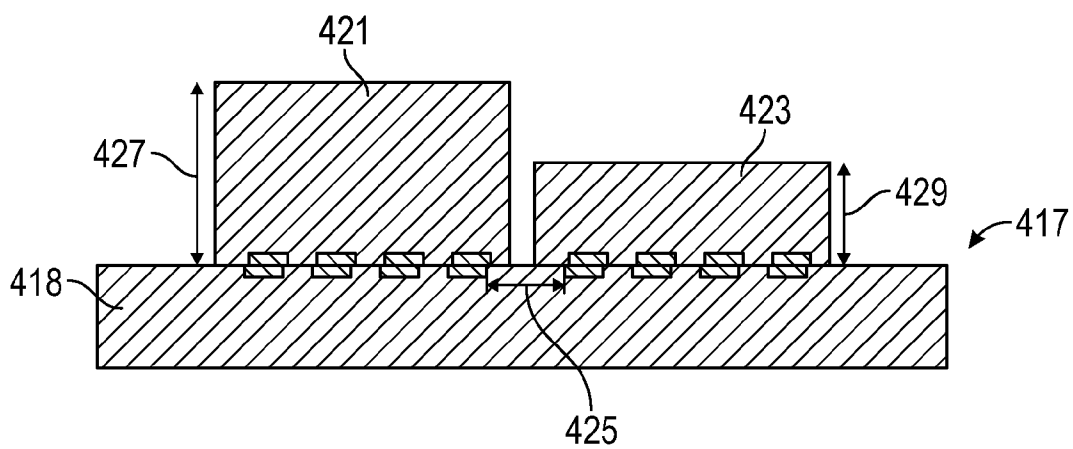


FIG. 4D

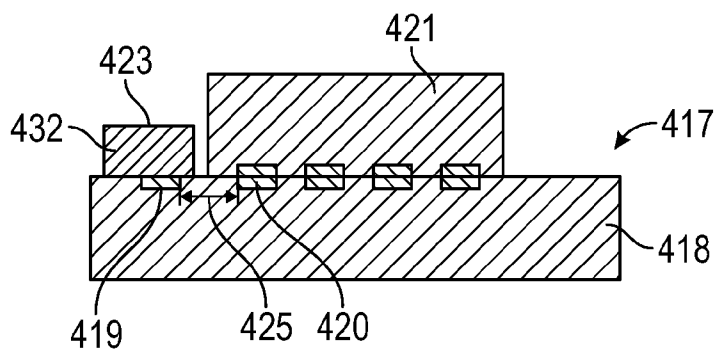


FIG. 4E

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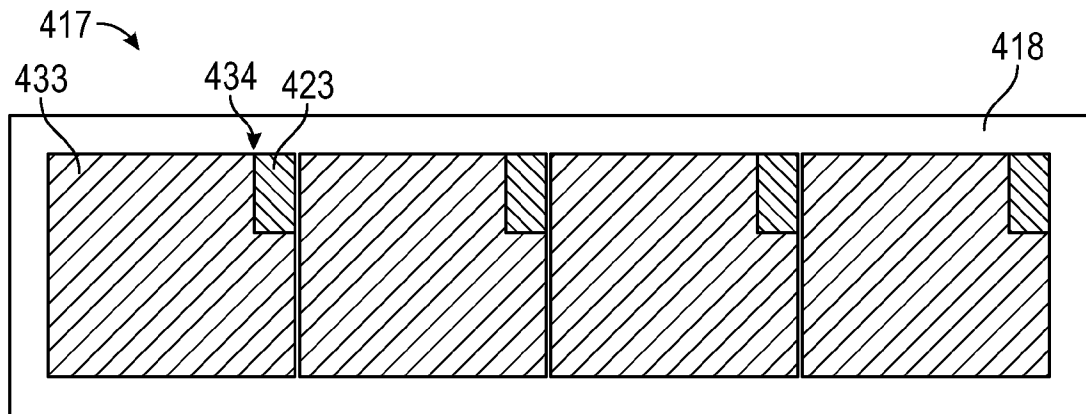


FIG. 4F

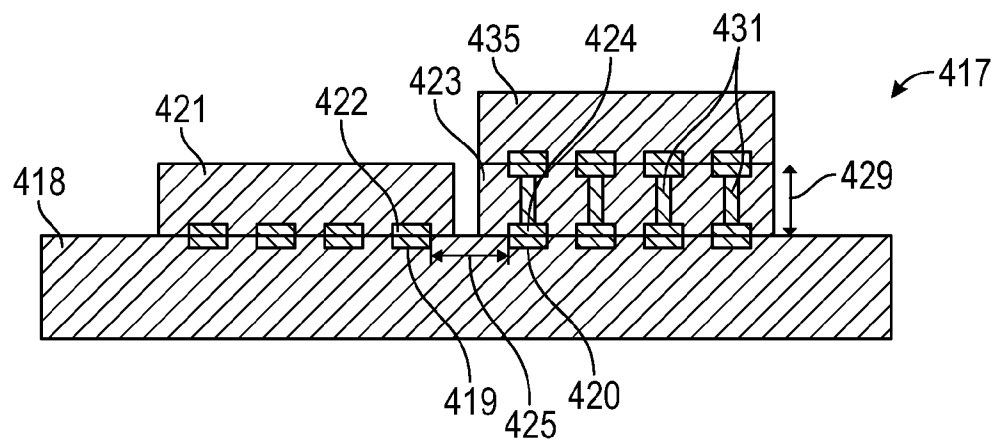


FIG. 4G

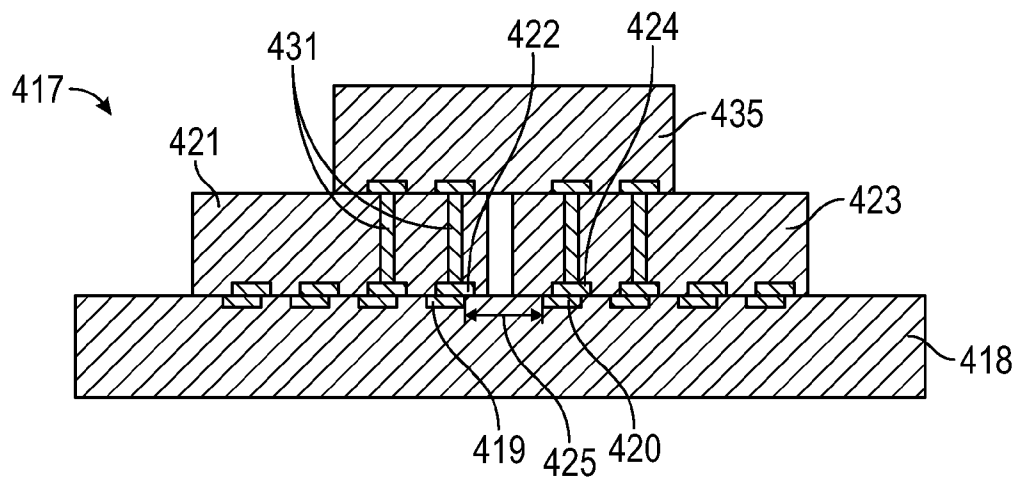


FIG. 4H

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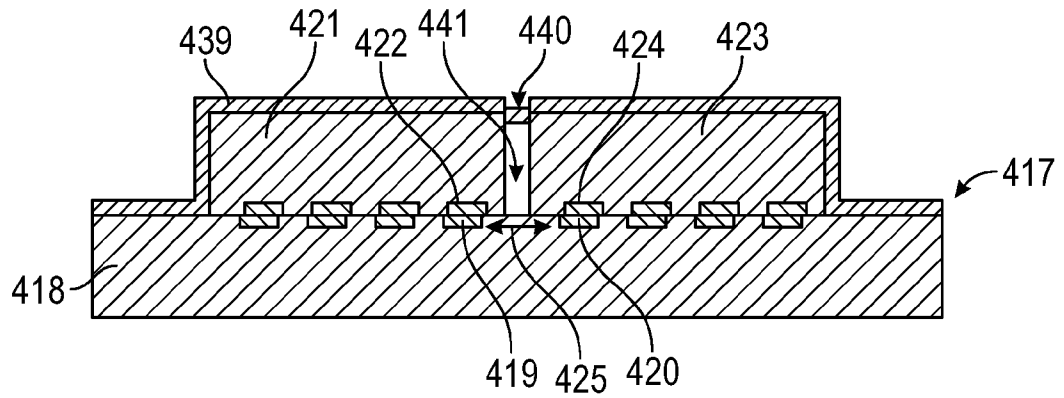


FIG. 4I

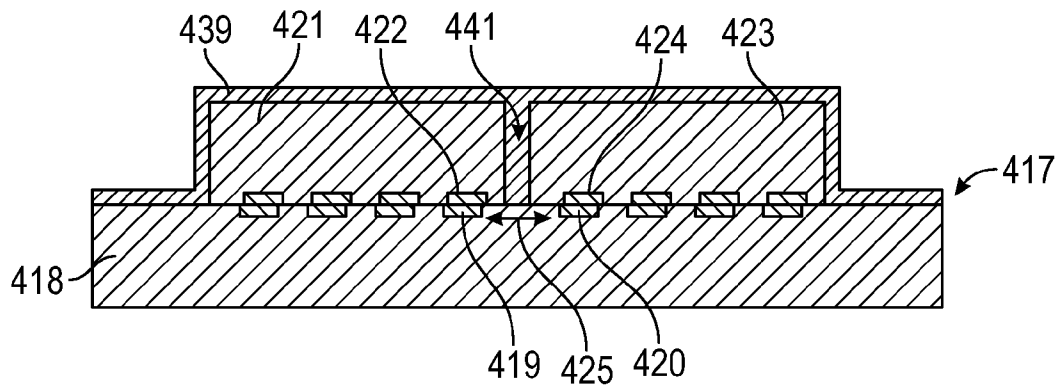


FIG. 4J

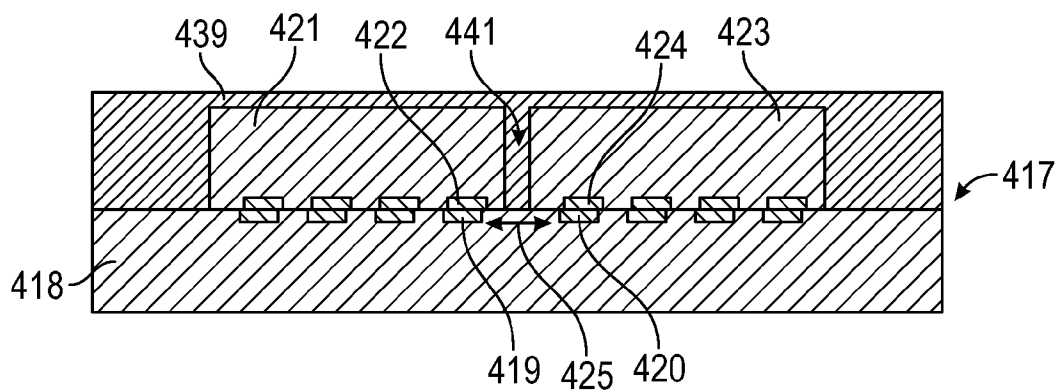


FIG. 4J-2

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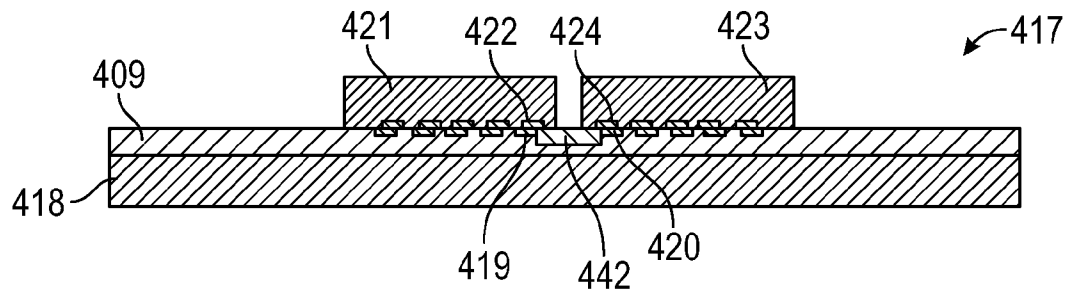


FIG. 4K

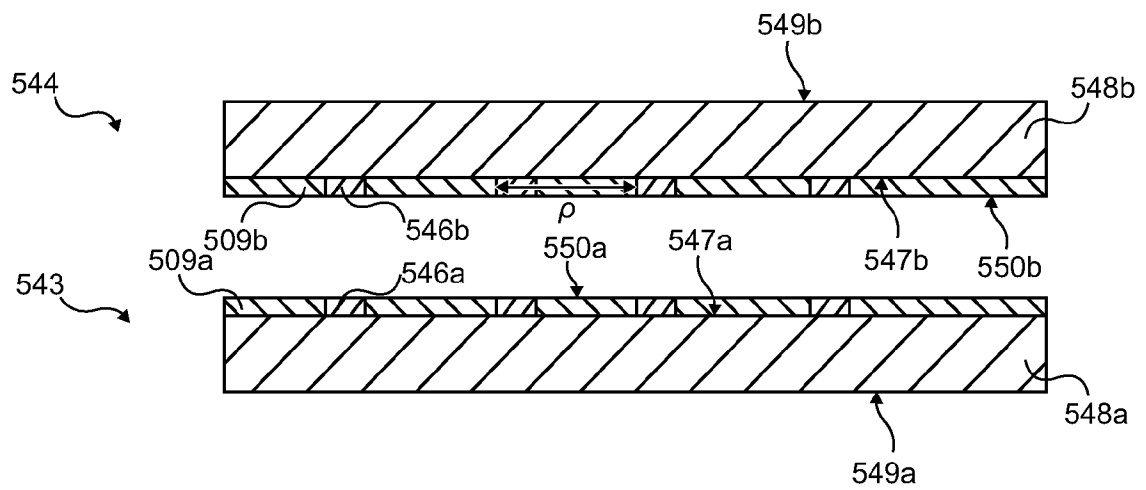


FIG. 5A

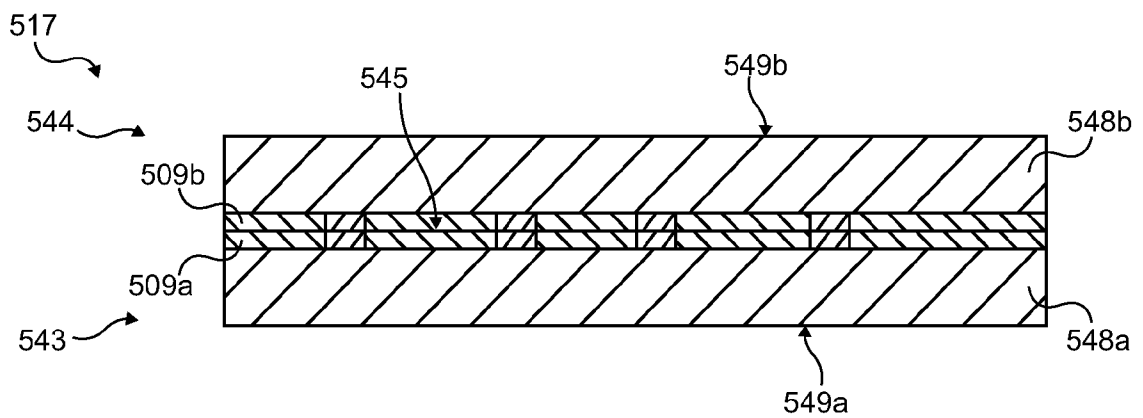


FIG. 5B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2023/063147

A. CLASSIFICATION OF SUBJECT MATTER H01L 23/00(2006.01)i; H01L 25/065(2006.01)i; H01L 23/498(2006.01)i; H01L 23/31(2006.01)i; H01L 25/18(2006.01)i According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L 23/00(2006.01); H01L 21/48(2006.01); H01L 21/56(2006.01); H01L 23/48(2006.01); H01L 23/498(2006.01); H01L 23/538(2006.01); H01L 25/00(2006.01); H01L 25/065(2006.01) Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: bonded structure, directly bonding, carrier, die, edge exclusion distance		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2021-0375850 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 02 December 2021 (2021-12-02) See paragraphs [0003], [0027]-[0075] and figures 1A-1B, 3, 6B.	1-4,6-7,19,31-33,37-45,54-71
Y	CN 111916354 A (UNIMICRON TECHNOLOGY CORP.) 10 November 2020 (2020-11-10) See paragraphs [0088], [0090] and figures 1K-2A.	1-4,6-7,19,31,37-45,54-71
Y	US 2020-0395309 A1 (INTEL CORPORATION) 17 December 2020 (2020-12-17) See paragraph [0034] and figure 2A.	32-33
A	US 2021-0407941 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 30 December 2021 (2021-12-30) See paragraphs [0029]-[0045] and figures 1A-8B.	1-4,6-7,19,31-33,37-45,54-71
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 22 June 2023		Date of mailing of the international search report 22 June 2023
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer PARK, Hye Lyun Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2023/063147

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003-0155640 A1 (SOUPIN YAN et al.) 21 August 2003 (2003-08-21) See paragraphs [0032]-[0036] and figures 4-8.	1-4,6-7,19,31-33,37-45,54-71

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2023/063147

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: **21,23,28-29,35-36,48-49,51-52**
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

Claims 21, 23, 28-29, 35-36, 48-49, 51-52 are regarded to be unclear because the claims refer to multiple dependent claims which do not comply with PCT Rule 6.4(a).

3. ☒ Claims Nos.: **5,8-18,20,22,24-27,30,34,46-47,50,53**
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2023/063147

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2021-0375850	A1	02 December 2021	CN	111742398	A	02 October 2020
				CN	111742398	B	09 July 2021
				CN	113410133	A	17 September 2021
				TW	201937584	A	16 September 2019
				TW	202249073	A	16 December 2022
				TW	I778223	B	21 September 2022
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				US	11037919	B2	15 June 2021
				US	2019-0252364	A1	15 August 2019
				US	2020-0365575	A1	19 November 2020
				WO	2019-160690	A1	22 August 2019
CN	111916354	A	10 November 2020	CN	111916354	B	30 August 2022
US	2020-0395309	A1	17 December 2020	US	11289427	B2	29 March 2022
US	2021-0407941	A1	30 December 2021	CN	116157918	A	23 May 2023
				EP	4173032	A1	03 May 2023
				KR	10-2023-0029960	A	03 March 2023
				TW	202211398	A	16 March 2022
				US	11538781	B2	27 December 2022
				US	11631647	B2	18 April 2023
				US	2022-0122934	A1	21 April 2022
				WO	2022-005846	A1	06 January 2022
US	2003-0155640	A1	21 August 2003	US	6552425	B1	22 April 2003
				US	6734544	B2	11 May 2004