



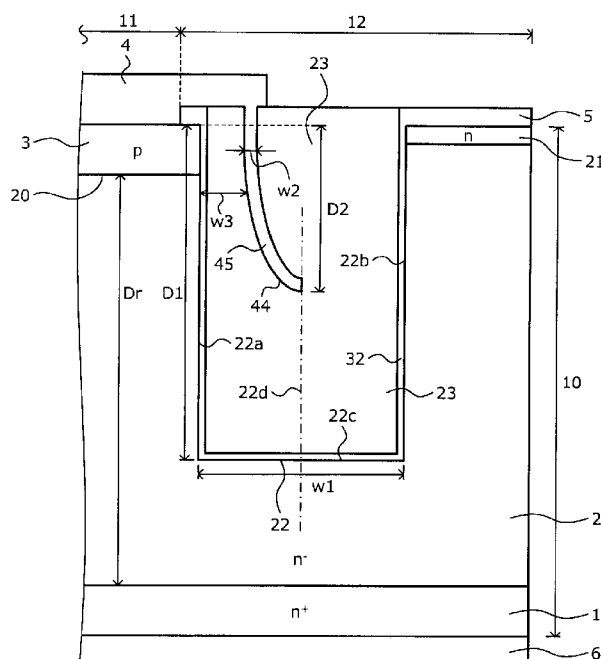
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(54) **Title:** SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE



(57) **Abstract:** At edge termination region (12), a trench (22) is disposed near an interface of an active region (11). Inside the trench (22), an embedded insulating film (23) is embedded, and inside the embedded insulating film (23), a FP (45) long in a direction of depth is disposed. The FP (45) curves outwardly away from an inner side wall (22a) of the trench (22) as a depth from a base front surface increases. At least near a bottom end of the FP (45), a distance (w3) between the FP (45) and the inner side wall (22a) of trench (22) is greater than a width (w2) of the groove (24). The FP (45) is connected to a front surface electrode (4) that extends on the embedded insulating film (23). As a result, breakdown voltage can be enhanced, adverse effects of the surface charge can be reduced, and chip size can be further reduced.

Description

Title of Invention: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Technical Field

[0001] The present invention relates to a semiconductor device and a method of manufacturing the semiconductor device.

Background Art

[0002] To control electric field concentration at the device end (chip end), in one known high voltage structure, a field limiting ring (FLR) that is a floating (floating electric potential) p-type region is disposed in plural in an edge termination region that surrounds the periphery of an active region. In another known high voltage structure, a field plate (FP), which is a metal electrode or a polysilicon (poly-Si) electrode connected to an FLR, is disposed. The FP controls that way that the depletion layer spreads, prevents degradation of the breakdown voltage, and has a function of controlling the surface charge distribution and property changes consequent to the surface charge.

[0003] A structure of the edge termination region of a semiconductor device will be described. Fig. 35 is a cross sectional view of a structure of an edge termination region of a conventional semiconductor device. The conventional semiconductor device depicted in Fig. 35 includes a high voltage structure formed by FLRs 103 and FPs 106, in an edge termination region 112 surrounding a periphery of an active region 111. The active region 111 is a region in which current flows during the ON state. The edge termination region 112 is a region that relaxes the electric field of a substrate front-surface side of an n-type drift region 101 and maintains the breakdown voltage. The FLR 103 is disposed in plural, concentrically surrounding the periphery of the active region 111, in a surface layer of a front surface of an n-type semiconductor substrate (semiconductor chip) 110 that becomes the n-type drift region 101.

[0004] In the edge termination region 112, the front surface of the n-type semiconductor substrate 110 is covered by an interlayer insulating film 107. The FP 106 contacts the FLR 103 via a contact hole that penetrates the interlayer insulating film 107 in a direction of depth. The FP 106 is disposed for each the FLRs 103. Further, the FP 106 extends inwardly (the active region 111 side) or outwardly (the chip end side), or both, on the interlayer insulating film 107. Reference numeral 102 represents a p-type region configuring a pn junction (main junction) with the n-type drift region 101, in the active region 111. Reference numerals 104, 105, and 108 represent a p-type channel stop region, a local oxidation of silicon (LOCOS), and a passivation film, respectively.

- [0005] A principle of operation at the edge termination region 112 where the FLRs 103 are disposed will be described. Fig. 36 is a diagram depicting the principle of operation at the edge termination region of a conventional semiconductor device. In Fig. 36, (a) and (b) respectively depict temporally from the left, transition of electric field distribution and charge distribution corresponding to (c). In Fig. 36, (c) depicts temporally by broken lines 121a and 121b, end positions of a depletion layer 121 extending outwardly when the semiconductor device is OFF. The horizontal axes in Fig. 36 represent a distance r expressing positional relations of parts, in a direction from an inner side toward an outer side. At (a), the vertical axis represents electric field strength E . At (b), the vertical axis represents charge q and an upper quadrant above the horizontal axis represents negative charge N_D while a lower quadrant below the horizontal axis represents positive charge N_A . Further, at (c), the vertical axis represents a depth d of the front surface of the n-type semiconductor substrate 110.
- [0006] When the semiconductor device is OFF and a pn junction (hereinafter, main junction) 120 between the p-type region 102 and the n-type drift region 101 in the active region 111 is reverse biased, the depletion layer 121 is formed along the main junction 120, and extends outwardly accompanying an increase in the reverse biasing. Furthermore, although the electric field strength near an end of the active region 111 (near an end 102a of the p-type region 102) increases ((a) of Fig. 36) accompanying the reverse biasing, near an end of the active region 111, before avalanche breakdown occurs, the depletion layer 121 reaches the innermost FLR 103 (broken line 121a in (c) of Fig. 36). As a result, the p-type region 102 and the innermost FLR 103 punchthrough, suppressing the peak electric field at the end 102a of the p-type region 102.
- [0007] When the depletion layer 121 reaches the innermost FLR 103, holes (positive holes) in the innermost FLR 103 flow to the active region 111 and positive charge N_A is lost (portion indicated by reference numeral 131 in (b) of Fig. 36). To compensate for the lost positive charge N_A of the innermost FLR 103, the depletion layer 121 further extends outwardly (broken line 121b in (c) of Fig. 36). When the reverse biasing is further increased, although the electric field strength increases near an outer end 103a of the inner most FLR 103, before avalanche breakdown occurs at the outer end 103a of the FLR 103, the depletion layer 121 further reaches an outward FLR 103 (not depicted in (c) of Fig. 36). As a result, the FLRs 103 punchthrough, suppressing the peak electric field at the outer end 103a of the innermost FLR 103.
- [0008] Thus, portions contributing to the critical electric field strength are sequentially moved outward to the outer ends 103a of the FLRs 103 such that avalanche breakdown occurs at the outermost FLR 103, whereby the electric field near the end of the active region 111 relaxes, realizing high breakdown voltage. The breakdown voltage of the

semiconductor device is determined by the applied voltage that causes avalanche breakdown at the outermost FLR 103. Further, as described above, since the way the depletion layer 121 extends consequent to the balance of the charge q of the FLRs 103 is determined, the adverse effects of the charge (hereinafter, surface charge) at the surface of the interlayer insulating film 107, the interface of the interlayer insulating film 107 and the n-type semiconductor substrate 110, etc. is remarkable. Therefore, the FPs 106 and the FLRs 103 are connected respectively to reduce the adverse effects of the surface charge.

- [0009] In a device proposed (for example, refer to PLT 1 below) as another semiconductor device equipped with FPs, a trench disposed in the edge termination region is filled with an insulating film and a FP is embedded in a recess disposed in the insulating film. In PLT 1, the depth of the FP in the insulating film is suitably adjusted, whereby a range of the quantity of surface charge allowed under the environment at the time of actual use is set and breakdown voltage that is nearly an ideal breakdown voltage (voltage causing avalanche breakdown in an ideal state when no surface charge is present) is set.

Citation List

Patent Literature

- [0010] PTL 1: Japanese Patent No. 5135663

Summary of Invention

Technical Problem

- [0011] Nonetheless, in the conventional structure depicted in Figs. 35 and 36, the higher the breakdown voltage is, the greater the curvature of the depletion layer 121 becomes and therefore, although more the FLRs 103 have to be disposed, the depletion layer 121 does not extend to the inside of the FLRs 103. Consequently, the FLRs 103 themselves have a region that does not bear the load of the electric field and thus, the regions that do not bear the load of the electric field increase in the edge termination region 112 as the number of the FLRs 103 increases. Further, in a case where the FPs 106 are disposed, a minimum dimension of a width x of the FLRs 103 is rate limited by the accuracy of processing of the FP 106. Therefore, particularly in a high voltage semiconductor device, a problem arises in that the area occupied by the edge termination region 112 increases. In PLT 1, although the area occupied by the edge termination region can be reduced, there is room to further reduce the adverse effects of surface charge and increase the breakdown voltage.
- [0012] To solve the problems associated with the conventional techniques above, one object of the present invention is to provide a semiconductor device and a method of manufacturing semiconductor device that can enhance breakdown voltage, reduce the

adverse effects of surface charge, and further reduce chip size.

Solution to Problem

- [0013] To solve the problems above and achieve an object, a semiconductor device according to the present invention has the following characteristics. A trench is disposed farther outward than an active region and reaches a predetermined depth from a first principal surface of a semiconductor substrate. A pn junction between a second conductivity type region and a first conductivity type region is disposed in a first principal surface side of the semiconductor substrate. The pn junction extends outwardly from the active region and is terminated by the trench. An insulating film is embedded inside the trench. A first field plate is disposed inside the insulating film and is long in a direction of depth. A first electrode contacts the second conductivity type region and the first field plate. A second electrode is disposed in a second principal surface of the semiconductor substrate. A distance between an inner side wall of the trench and the first field plate is greater than a width of the first field plate.
- [0014] The semiconductor device according to the present invention is further characterized in that the first field plate curves away from the inner side wall of the trench as a depth from the first principal surface of the semiconductor substrate increases.
- [0015] The semiconductor device according to the present invention is further characterized in that the distance between the inner side wall of the trench and the first field plate toward a second principal surface side of semiconductor substrate is greater than the width of the first field plate.
- [0016] The semiconductor device according to the present invention is further characterized in that a depth of the first field plate is deeper than the pn junction and shallower than the trench, from the first principal surface of the semiconductor substrate.
- [0017] The semiconductor device according to the present invention is further characterized in that the depth of the first field plate is 30% or more and 70% or less of a depth of the trench.
- [0018] The semiconductor device according to the present invention further includes a second field plate that is disposed inside the insulating film and that is long in the direction of depth. The second field plate is further characterized in that the second field plate is disposed farther outward than the first field plate and away from the first field plate.
- [0019] The semiconductor device according to the present invention is further characterized in that the second field plate curves away from an outer side wall of the trench as a depth from the first principal surface of the semiconductor substrate increases.
- [0020] The semiconductor device according to the present invention is further characterized in that a depth of the second field plate is greater than a depth of the first field plate.

- [0021] The semiconductor device according to the present invention is further characterized in that the semiconductor substrate is configured by the first conductivity type region, the second conductivity type region, and a supporting substrate. The second conductivity type region contacts the first electrode disposed in the first principal surface of the semiconductor. The supporting substrate contacts the second electrode disposed in the second principal surface of the semiconductor substrate. The first conductivity type region is between the second conductivity type region and the supporting substrate. The trench, from the pn junction, reaches a depth that is 30% or more of a thickness of the first conductivity type region and less than the thickness of the first conductivity type region.
- [0022] The semiconductor device according to the present invention is further characterized in that a width of the trench is 30% or more and 60% or less of a depth of the trench.
- [0023] Further, to solve the problems above and achieve an object, a method of manufacturing a semiconductor device according to the present invention has the following characteristics. A first process of forming in a first principal surface side of a semiconductor substrate, a pn junction between a second conductivity type region and a first conductivity type region such that the pn junction extend outwardly from an active region is performed. Next, a second process of forming farther outward than the active region, a trench that reaches a predetermined depth from the first principal surface of the semiconductor substrate and that terminates the pn junction is performed. Next, a third process of embedding inside the trench, an insulating film so as to leave a groove having a U-shaped cross sectional shape is performed. Next, a fourth process of forming a metal film along the groove is performed. Next, a fifth process of selectively removing the metal film to leave, as a first field plate, a remaining portion of the metal film at an inner side wall of the groove is performed. Next, a sixth process of further embedding inside the trench, the insulating film so as to cover the first field plate is performed.
- [0024] The method of manufacturing a semiconductor device according to the present invention further includes a process of forming a reflection preventing film on the metal film, after the fourth process and before the fifth process. The fifth process is further characterized in that the fifth process includes a process applying a resist film on the reflection preventing film. Next, a process of luminously exposing the resist film and forming a resist mask that covers a forming region of the first field plate is performed. Next, a process of etching using the resist mask as a mask to leave, as the first field plate, the remaining portion of the metal film at the inner side wall of the groove is performed.
- [0025] The method of manufacturing a semiconductor device according to the present invention is further characterized in that in the fifth process, a remaining portion of the

metal film, away from the first field plate, is left at an outer side wall of the groove as a second field plate.

- [0026] According to the described invention, the electric field near the end of the active region can be relaxed. As a result, breakdown voltage on the same order as the theoretical value of the maximum breakdown voltage that can be obtained by the main junction of the active region can be obtained. Further, the field plate disposed inside the insulating film has a function of shielding the surface charge. In addition, since no FLR is disposed in the edge termination region farther outward than the active region, the width of the edge termination region can be greatly reduced compared to a conventional structure in which FLRs are disposed.

Advantageous Effects of Invention

- [0027] The semiconductor device and the method of manufacturing semiconductor device according to the present invention enable enhancement of the breakdown voltage, reduction of the adverse effects of surface charge, and further reduction of chip size.

Brief Description of Drawings

- [0028] [fig.1]Fig. 1 is a cross sectional view of a structure of an edge termination region of a semiconductor device according to a first embodiment.
- [fig.2]Fig. 2 is a cross sectional view of the semiconductor device according to the first embodiment, during manufacture.
- [fig.3]Fig. 3 is a cross sectional view of the semiconductor device according to the first embodiment, during manufacture.
- [fig.4]Fig. 4 is a cross sectional view of the semiconductor device according to the first embodiment, during manufacture.
- [fig.5]Fig. 5 is a cross sectional view of the semiconductor device according to the first embodiment, during manufacture.
- [fig.6]Fig. 6 is a cross sectional view of the semiconductor device according to the first embodiment, during manufacture.
- [fig.7]Fig. 7 is a cross sectional view of the semiconductor device according to the first embodiment, during manufacture.
- [fig.8]Fig. 8 is a cross sectional view of the semiconductor device according to the first embodiment, during manufacture.
- [fig.9]Fig. 9 is a cross sectional view of the semiconductor device according to the first embodiment, during manufacture.
- [fig.10]Fig. 10 is a graph depicting the relationship between trench depth of first examples and breakdown voltage.
- [fig.11]Fig. 11 is a graph depicting the relationship between second examples and breakdown voltage.

[fig.12]Fig. 12 is a graph depicting the relationship between groove depth of third examples and breakdown voltage.

[fig.13]Fig. 13 is a graph depicting breakdown charge of a fourth example.

[fig.14A]Fig. 14A is a cross sectional view of a structure of the semiconductor device according to a second embodiment.

[fig.14B]Fig. 14B is a cross sectional view of the structure of the semiconductor device according to the second embodiment.

[fig.15]Fig. 15 is a cross sectional view of the semiconductor device according to the second embodiment, during manufacture.

[fig.16]Fig. 16 is a cross sectional view of the semiconductor device according to the second embodiment, during manufacture.

[fig.17]Fig. 17 is a cross sectional view of the semiconductor device according to the second embodiment, during manufacture.

[fig.18]Fig. 18 is a cross sectional view of the semiconductor device according to the second embodiment, during manufacture.

[fig.19]Fig. 19 is a cross sectional view of the semiconductor device according to the second embodiment, during manufacture.

[fig.20]Fig. 20 is a cross sectional view of the semiconductor device according to the second embodiment, during manufacture.

[fig.21A]Fig. 21A is a cross sectional view of a structure of the semiconductor device according to a third embodiment.

[fig.21B]Fig. 21B is a cross sectional view of the structure of the semiconductor device according to the third embodiment.

[fig.22]Fig. 22 is a cross sectional view of the semiconductor device according to the third embodiment, during manufacture.

[fig.23]Fig. 23 is a cross sectional view of the semiconductor device according to the third embodiment, during manufacture.

[fig.24]Fig. 24 is a cross sectional view of the semiconductor device according to the third embodiment, during manufacture.

[fig.25]Fig. 25 is a cross sectional view of the semiconductor device according to the third embodiment, during manufacture.

[fig.26]Fig. 26 is a diagram of static characteristics of a fifth example.

[fig.27]Fig. 27 is a diagram of dynamic characteristics of the fifth example.

[fig.28]Fig. 28 is a diagram of dynamic characteristics of a sixth example.

[fig.29]Fig. 29 is a cross sectional view of a structure of the semiconductor device according to a fourth embodiment.

[fig.30]Fig. 30 is a cross sectional view of the semiconductor device according to the fourth embodiment, during manufacture.

[fig.31]Fig. 31 is a cross sectional view of the semiconductor device according to the fourth embodiment, during manufacture.

[fig.32]Fig. 32 is a cross sectional view of the semiconductor device according to the fourth embodiment, during manufacture.

[fig.33]Fig. 33 is a cross sectional view of the semiconductor device according to the fourth embodiment, during manufacture.

[fig.34]Fig. 34 is a cross sectional view of a structure of the semiconductor device according to a fifth embodiment.

[fig.35]Fig. 35 is a cross sectional view of a structure of an edge termination region of a conventional semiconductor device.

[fig.36]Fig. 36 is a diagram depicting a principle of operation at the edge termination region of a conventional semiconductor device.

Description of Embodiments

[0029] Preferred embodiments of a semiconductor device and a method of manufacturing the semiconductor device according to the present invention will be described in detail with reference to the accompanying drawings. In the present description and accompanying drawings, layers and regions prefixed with n or p mean that majority carriers are electrons or holes. Additionally, + or - appended to n or p means that the impurity concentration is higher or lower, respectively, than layers and regions without + or -. In the description of the embodiments below and the accompanying drawings, identical constituent elements will be given the same reference numerals and will not repeatedly be described.

[0030] (First embodiment)

A structure of an edge termination region of the semiconductor device according to a first embodiment will be described. Fig. 1 is a cross sectional view of a structure of the edge termination region of the semiconductor device according to the first embodiment. Fig. 1 depicts the structure from a vicinity of an interface of an active region 11 and an edge termination region 12 to the chip end (similarly for Figs. 2 to 9, 14 to 25, and 29 to 34). The semiconductor device according to the first embodiment and depicted in Fig. 1 has in the edge termination region 12 that surrounds a periphery of the active region 11, a high voltage structure that is formed by an insulating film (hereinafter, embedded insulating film) 23 embedded inside a trench 22 and a field plate (FP) 25 embedded inside the embedded insulating film 23. The active region 11 is a region in which current flows in the ON state.

[0031] More specifically, in the active region 11, on a front surface of a semiconductor base (semiconductor substrate (semiconductor chip)) 10, a p-type region 3 is selectively disposed. The semiconductor base 10 is an epitaxial substrate formed by epitaxially

growing on a front surface of an n⁺-type supporting substrate 1, an n-type semiconductor layer that becomes an n-type drift region 2. The surface of an n-type drift region 2 side of the semiconductor base 10 is assumed as a front surface (base front surface) and a surface of an n⁺-type supporting substrate 1 side of the semiconductor base 10 (back surface of the n⁺-type supporting substrate 1) is assumed as a back surface (base back surface). The front surface of the semiconductor base 10 is covered by an interlayer insulating film 5. A front surface electrode 4 contacts the p-type region 3 via a contact hole that penetrates the interlayer insulating film 5 in a direction of depth. The front surface electrode 4 extends outwardly (a chip end side) on the interlayer insulating film 5 and the embedded insulating film 23. A back surface electrode 6 is disposed in the entire back surface of the semiconductor base 10.

[0032] When a diode, for example, is formed in the active region 11, the n⁺-type supporting substrate 1, the p-type region 3, the front surface electrode 4, and the back surface electrode 6 are a cathode region, an anode region, an anode electrode, and a cathode electrode, respectively. Further, when a metal oxide semiconductor field effect transistor (MOSFET), for example, is formed in the active region 11, the n⁺-type supporting substrate 1, the p-type region 3, the front surface electrode 4, and the back surface electrode 6 are a drain region, base region, source electrode, and a drain electrode, respectively. Fig. 1 depicts among one or more unit cells (element functional units) arranged in the semiconductor base 10, the p-type region 3 configuring an outermost unit cell.

[0033] In the edge termination region 12, at the chip end, an n-type channel stopper region 21 is disposed in a surface layer of the front surface of the semiconductor base 10. The n-type channel stopper region 21 is exposed at a chip side surface and an outer side wall 22b of the trench 22 described hereinafter. Further, the n-type channel stopper region 21 is covered by the interlayer insulating film 5. The interlayer insulating film 5 is, for example, a low temperature oxide (LTO) film, etc. The n-type channel stopper region 21 may be covered by, for example, a passivation film (not depicted) of a silicon nitride (SiN_x) film and the like.

[0034] The trench 22 is disposed at a depth D1 that does not reach the n⁺-type supporting substrate 1 in a direction of depth from the base front surface. The trench 22 is preferably disposed at a position near the interface with the active region 11. Further, the trench 22 is disposed to have a planar layout surrounding a periphery of the active region 11. At an inner side wall 22a (the active region 11 side) of the trench 22, the p-type region 3 that extends from the active region 11 is exposed and contacts the embedded insulating film 23. In other words, an outer end of a pn junction (hereinafter, main junction) 20 between the p-type region 3 that is outermost in the active region 11 and the n-type drift region 2 terminates at the trench 22 and does not substantially

curve. Therefore, electric field concentration at the outer end of the main junction 20 of the active region 11 does not occur. When the depth D1 and a width w1 of the trench 22 are optimized, breakdown voltage of the same level as the theoretical value of the maximum breakdown voltage obtained by the main junction 20 of the active region 11 can be obtained.

[0035] The depth D1 of the trench 22, for example, is favorably 30% or more of a thickness Dr of the n-type drift region 2 ($30\% \leq D1/Dr < 100\%$), and is preferably 50% or more and 80% or less of the thickness Dr of the n-type drift region 2, whereby high voltage breakdown can be achieved ($50\% \leq D1/Dr \leq 80\%$). The width w1 of the trench 22, irrespective of the voltage breakdown rating, is about 30% or more and 60% or less of the depth D1 of the trench 22, whereby high voltage breakdown can be achieved ($30\% \leq w1/D1 \leq 60\%$). The depth D1 of the trench 22 is a depth from the front surface of the semiconductor base 10. The thickness Dr of the n-type drift region 2 is a length from the interface of the p-type region 3 and the n-type drift region 2, to an interface of the n-type drift region 2 and the n⁺-type supporting substrate 1.

[0036] More specifically, for example, in the case of breakdown voltage of 600V, the thickness Dr of the n-type drift region 2 is about 50μm. Therefore, the depth D1 of the trench 22 is about 35μm ($D1/Dr = 70\%$), and the width w1 of the trench 22 is about 15μm ($w1/D1 \approx 43\%$). For example, in a case of breakdown voltage of 1200V, the thickness Dr of the n-type drift region 2 is about 140μm. Therefore, the depth D1 of the trench 22 is about 70μm ($D1/Dr = 50\%$), and the width w1 of the trench 22 is about 31μm ($w1/D1 \approx 44\%$).

[0037] The insulating film (embedded insulating film) 23 is embedded inside the trench 22. The insulating material of the embedded insulating film 23 may be, for example, Spin on Glass (SOG), Benzocyclobutene (BCB), etc. Inside the embedded insulating film 23, a groove 24 is disposed to a depth D2 that does not reach a bottom 22c of the trench 22, in a direction of depth from the base front surface. The groove 24, for example, is disposed at a position (hereinafter, center position of the trench 22) 22d that is substantially 1/2 of the width w1 of the trench 22, and has a planar layout that surrounds the periphery of the active region 11. The FP 25 is embedded inside the groove 24. In other words, the FP 25 is disposed inside the embedded insulating film 23 to have a length in a direction of depth (vertical direction).

[0038] The depth D2 (hereinafter, the depth of the FP 25) of the groove 24 is deeper than the depth of the p-type region 3. Further, the depth D2 of the groove 24, for example, is favorably about 30% or more and 70% or less of the depth D1 of the trench 22 ($30\% \leq D2/D1 \leq 70\%$), and preferably, about 40% or more and 60% or less the depth D1 of the trench 22, whereby high breakdown voltage can be achieved ($40\% \leq D2/D1 \leq 60\%$). More specifically, for example, in the case of breakdown voltage

of 600V, as described above, since the depth D1 of the trench 22 is about 35 μ m, the depth D2 of the groove 24 is about 15 μ m ($D2/D1 \approx 43\%$). For example, in the case of withstand voltage of 1200V, as described above, since the depth D1 of the trench 22 is about 70 μ m, the depth D2 of the groove 24 is about 40 μ m ($D2/D1 = 57\%$). The depth D2 of the groove 24 is a depth from the front surface of the semiconductor base 10, to the bottom of the groove 24.

[0039] The width w2 of the groove 24 is sufficiently narrow with respect to the width w1 of the trench 22 and, for example, is about 1 μ m. A distance w3 between the FP 25 and the inner side wall 22a of the trench 22 is wider than the width w2 of the groove 24 ($w3 > w2$). The wider the distance w3 is between the FP 25 and the inner side wall 22a of the trench 22, the greater the electric field load can be increased at a portion of the embedded insulating film 23, between the inner side wall 22a of the trench 22 and the FP 25. As a result, the electric field near an end of the active region 11 (interface of the active region 11 and the edge termination region 12) can be relaxed, enabling the breakdown voltage to be enhanced.

[0040] Thus, by disposing the FP 25 inside the embedded insulating film 23, electric field distribution near the FP 25 is modulated. As a result, similar to a case of a super-junction (SJ) structure, an effect can be obtained in that during reverse biasing, the breakdown voltage can be maintained. Therefore, with respect to the main junction 20 of the active region 11, even higher breakdown voltage can be realized. A super-junction structure is a structure where the drift layer is a parallel pn layer in which n-type regions and p-type regions are alternately disposed in a horizontal direction (direction parallel to the substrate primary surface of the substrate) repeatedly. Further, since charge (surface charge) at an interface of the interlayer insulating film 5 and the semiconductor base 10, the surface of the interlayer insulating film 5, etc. is shielded by the FP 25, property changes with respect to the surface charge are reduced.

[0041] Further, disposal of the FP 25 that is long in a vertical direction enables a length (width) L1 of the edge termination region 12 to be greatly reduced as compared to the conventional structure equipped with the FLR 103 (refer to Fig. 36). For example, in the case of breakdown voltage of 600V, the length L1 of the edge termination region of the present invention is about 30 μ m in contrast to about 250 μ m for a length L100 of the edge termination region of the conventional structure. For example in the case of breakdown voltage of 1200V, the length L1 of the edge termination region of the present invention is about 60 μ m in contrast to about 500 μ m for the length L100 of the edge termination region of the conventional structure.

[0042] The FP 25 is connected to the front surface electrode 4 extending on the embedded insulating film 23. More specifically, the front surface electrode 4 extends outwardly so as to cover entirely an end (end of the base front surface side) on the FP 25.

Preferably, the front surface electrode 4 covers a top end of the FP 25 entirely and further extends slightly outward. The reason for this is that during patterning of the front surface electrode 4, the top end of the FP 25 can be prevented from being removed by etching.

- [0043] The method of manufacturing the semiconductor device according to the first embodiment will be described taking the production (manufacture) of a diode as an example. Figs. 2 to 9 are cross sectional views of the semiconductor device according to the first embodiment, during manufacture. As depicted in Fig. 2, in the front surface of the n⁺-type supporting substrate 1 becoming the cathode region, an n-type semiconductor layer that becomes the n-type drift region 2 is epitaxially grown. As a result, the semiconductor base (semiconductor wafer) 10 is formed where the n-type drift region 2 is epitaxially grown on the n⁺-type supporting substrate 1.
- [0044] Next, a process combining photolithography, impurity implantation, and resist mask removal is repeatedly performed under different conditions, and a predetermined region is selectively formed on the front surface side (surface of the n-type drift region 2 side) of the semiconductor base 10. The predetermined region is the n-type channel stopper region 21, an anode region (the p-type region 3) configuring an element structure of the active region 11, and the like. Next, in the entire front surface of the semiconductor base 10, an LTO film, for example, is formed as the interlayer insulating film 5. Next, impurities implanted inside the semiconductor base 10 are activated by heat treatment.
- [0045] As depicted in Fig. 3, by photolithography and etching, a resist mask (not depicted) is formed in which a portion corresponding to a forming region of the trench 22 is opened. Next, using the resist mask as a mask, the interlayer insulating film 5 is patterned. Next, after the resist mask is removed, the interlayer insulating film 5 is used as a mask to perform etching and the trench 22 is formed having the depth D1 and the width w1. Here, the trench 22 is formed to penetrate in a direction of depth, an outer end 3a (refer to Fig. 2) of the outermost p-type region 3 and an inner end 21a of the n-type channel stopper region 21 (refer to Fig. 2).
- [0046] Next, as depicted in Fig. 4, after a sacrificial oxide film 31 is formed along interior walls of the trench 22, the sacrificial oxide film 31 is removed. As a result, an interface state between a semiconductor region exposed after sacrificial oxidation of the interior walls of the trench 22 and an LTO film 32 formed at a subsequent process can be reduced. Next, as depicted in Fig. 5, the LTO film 32 is deposited (formed), for example, along the interior walls of the trench 22 and the base front surface. Next, defects in the LTO film 32 are reduced by heat treatment. The thickness of the interlayer insulating film 5 becomes thick consequent to deposition of the LTO film 32.
- [0047] By making the interlayer insulating film 5 thick, adverse effects of the surface charge

can be reduced during operation of the semiconductor device. The surface charge is the charge at the interface of the interlayer insulating film 5 and the semiconductor base 10, in the surface of the interlayer insulating film 5, etc. Further, the interlayer insulating film 5 becomes a polishing stopper film to stop polishing when the embedded insulating film 23 formed at a subsequent process is polished and planarized.

Therefore, by making the interlayer insulating film 5 thick, the process margin when the embedded insulating film 23 is polished can be increased, enabling the embedded insulating film 23 to be prevented from becoming thinner than a predetermined thickness.

[0048] Next, as depicted in Fig. 6, the embedded insulating film 23 is deposited along the interior walls of the trench and the base front surface. Here, the interior of the trench 22 is not completely embedded with the embedded insulating film 23 and the embedded insulating film 23 is embedded so as to leave inside the trench 22, the groove 24 of the depth D2 and the width w2 and having a cross sectional shape that is substantially linear. More specifically, for example, insulating material of the embedded insulating film 23 suffices to be applied to the base front surface by a depositing method or spin coat method. Next, the embedded insulating film 23 is hardened by heat treatment (curing).

[0049] Next, as depicted in Fig. 7, the FP 25 formed by, for example, an aluminum (Al) film is deposited on the embedded insulating film 23 so as to be embedded inside the groove 24. Next, as depicted in Fig. 8, the FP 25 and the embedded insulating film 23 are polished until the interlayer insulating film 5 is exposed. As a result, the FP 25 remains only inside the groove 24 of the embedded insulating film 23. Next, as depicted in Fig. 9, the interlayer insulating film 5 is patterned, a contact hole is formed, and the p-type region 3 is exposed by the contact hole.

[0050] Next, after forming the front surface electrode 4, which is formed by an aluminum film, on the entire base front surface so as to be embedded in the contact hole, the front surface electrode 4 is patterned. Here, the front surface electrode 4 is left so as to cover entirely the active region 11 and at a portion extending outward, to at least cover entirely the top end the FP 25. The back surface electrode 6 is formed on the entire back surface (the back surface of the n⁺-type supporting substrate 1) of the semiconductor base 10. Thereafter, the semiconductor wafer is diced into chips (dicing), forming singular units, whereby the semiconductor device depicted in Fig. 1 is completed.

[0051] The relationship between the depth D1 of the trench 22 and breakdown voltage was verified. Fig. 10 is a graph depicting the relationship between trench depth of first examples and breakdown voltage. In Fig. 10, the horizontal axis represents the depth (trench depth) D1 of the trench 22 and the vertical axis represents breakdown voltage

of the semiconductor device when the main junction 20 of the active region 11 is reverse biased. Samples (hereinafter, first examples) for which the depth D1 of the trench 22 differed were produced according to the method of manufacturing the semiconductor device according to the first embodiment described above. In each of the first examples, the width (trench width) w1 of the trench 22 was 15 μ m. The depth D2 of the groove 24 (in Fig. 10, indicated as the FP depth D2) was 15 μ m.

[0052] For the first examples, the results of breakdown voltage measurement for each semiconductor device are depicted in Fig. 10. Further, in Fig. 10, theoretical value (=683V) of the maximum breakdown voltage that can be obtained by the main junction 20 of the active region 11 of the first examples and breakdown voltage that is 95% of theoretical value ($\approx$ 649V) are respectively depicted by dotted-dashed horizontal lines. From the results depicted in Fig. 10, it was confirmed that the deeper the depth D1 of the trench 22 is, the higher the breakdown voltage is. Further, it was confirmed that by setting the depth D1 of the trench 22 to 35 μ m or greater, high breakdown voltage can be achieved that is greater than or equal to the maximum breakdown voltage theoretically obtainable by the main junction 20 of the active region 11.

[0053] Next, the relationship between the width w1 of the trench 22 and breakdown voltage was verified. Fig. 11 is a graph depicting the relationship between second examples and breakdown voltage. In Fig. 11, the horizontal axis represents the width (trench width) w1 of the trench 22 and the vertical axis represents breakdown voltage of the semiconductor device when the main junction 20 of the active region 11 is reverse biased. Samples (hereinafter, second examples) for which the width w1 of the trench 22 differed were produced according to the method of manufacturing the semiconductor device according to the first embodiment described above. In each of the second examples, the depth (trench depth) D1 of the trench 22 was 35 μ m. The depth D2 of the groove 24 (in Fig. 11, indicated as FP depth D2) was 15 μ m.

[0054] For the second examples, the results of breakdown voltage measurement for each semiconductor device are depicted in Fig. 11. Further, in Fig. 11, theoretical value (=683V) of the maximum breakdown voltage that can be obtained by the main junction 20 of the active region 11 of the second examples and breakdown voltage that is 95% of theoretical value ($\approx$ 649V) are respectively depicted by dotted-dashed horizontal lines. From the results depicted in Fig. 11, it was confirmed that the wider the width w1 of the trench 22 is, the higher the breakdown voltage is. Further, it was confirmed that by setting the width w1 of the trench 22 to 15 μ m or greater, high breakdown voltage can be achieved that is greater than or equal to the maximum breakdown voltage theoretically obtainable by the main junction 20 of the active region 11.

[0055] Next, the relationship between the depth D2 of the groove 24 (the depth of the FP 25) and breakdown voltage was verified. Fig. 12 is a graph depicting the relationship

between groove depth of third examples and breakdown voltage. In Fig. 12, the horizontal axis represents the depth D2 of the groove 24 (in Fig. 12, indicated as FP depth D2) and the vertical axis represents breakdown voltage of the semiconductor device when the main junction 20 of the active region 11 is reverse biased. Samples (hereinafter, third examples) for which the depth D2 of the groove 24 differed were produced according to the method of manufacturing the semiconductor device according to the first embodiment described above. In each of the third examples, the width (trench width) w1 of the trench 22 was 15 μ m. The depth (trench depth) D1 of the trench 22 was 35 μ m.

[0056] For the third examples, the results of breakdown voltage measurement for each semiconductor device are depicted in Fig. 12. Further, in Fig. 12, theoretical value (=683V) of the maximum breakdown voltage that can be obtained by the main junction 20 of the active region 11 of the second examples and breakdown voltage that is 95% of the theoretical value ($\approx$ 649V) are respectively depicted by dotted-dashed horizontal lines. From the results depicted in Fig. 12, it was confirmed that the deeper the depth D2 of the groove 24 is, the higher the breakdown voltage is. Further, it was confirmed that by setting the depth D2 of the groove 24 to 15 μ m or greater, high breakdown voltage can be achieved that is greater than or equal to the maximum breakdown voltage theoretically obtainable by the main junction 20 of the active region 11.

[0057] Next, breakdown charge by the presence/absence of the FP 25 was verified. Fig. 13 is a graph depicting breakdown charge of a fourth example. In Fig. 13, the horizontal axis represents surface charge density and the vertical axis represents breakdown voltage of the semiconductor device when the main junction 20 of the active region 11 is reverse biased. A Sample (hereinafter, fourth example) was produced according to the method of manufacturing the semiconductor device according to the first embodiment described above. In the fourth example, the width (trench width) w1 of the trench 22 was 17 μ m. The depth (trench depth) D1 of the trench 22 was 40 μ m and the depth D2 of the groove 24 (in Fig. 13, indicated as FP depth D2) was 17 μ m.

[0058] For the fourth example, surface charge density was varied and semiconductor device the results of breakdown voltage measurement for each semiconductor device are depicted in Fig. 13. Fig. 13 further depicts breakdown voltage of a semiconductor device (hereinafter, comparison example) in which the FP in the edge termination region is not disposed, when surface charge density is varied. The width of the edge termination region of the comparison example was the same as that of the fourth example. From the results depicted in Fig. 13, it was confirmed that in the comparison example, the more positive charge increases, the greater breakdown voltage decreases. In contrast, it was confirmed that in the fourth example, irrespective of surface charge density, the breakdown voltage was about the same.

[0059] As described above, according to the first embodiment, by disposing the trench of a wide width in the edge termination region, embedding the embedded insulating film, and terminating at an interior wall of the trench, the end of the main junction of the active region, electric field near the end of the active region can be relaxed. As a result, breakdown voltage can be obtained that is greater than or equal to the maximum breakdown voltage theoretically obtainable by the main junction of the active region. Further, since no FLR is disposed in the edge termination region, the width of the edge termination region can be greatly reduced as compared to the conventional structure in which FLRs are disposed. Further, according to the first embodiment, by disposing inside the embedded insulating film, the FP that is sufficiently narrower than the trench width and long in a vertical direction, the electric field distribution can be modulated to contain inside the embedded insulating film, locations where electric field concentrates. As a result, breakdown voltage can be obtained that is greater than or equal to the maximum breakdown voltage theoretically obtainable by the main junction of the active region. Further, according to the first embodiment, by disposing the FP inside the embedded insulating film, tolerance of overvoltage can be increased. Therefore, when overvoltage is applied, current occurring consequent to avalanche breakdown equally flows in the active region. Further, the FP disposed inside the embedded insulating film has a function of shielding surface charge. Consequently, adverse effects of the surface charge can be reduced. Therefore, breakdown voltage and breakdown charge can be enhanced.

[0060] The semiconductor base 10 of the present embodiment is not limited to the n⁺-type supporting substrate 1 and epitaxial substrate. For example, the semiconductor base 10 may be a bulk wafer cut from an ingot. The ingot for the bulk wafer may be manufactured by a float zone (FZ) method, a Czochralski (CZ) process, or a magnetic Czochralski (MCZ) process. The semiconductor base 10 may be, for example, a bulk wafer that has been thinned by grinding the back surface side thereof. In this case, the n-type drift region 2 may be of the same impurity concentration as the bulk wafer. An n-type high impurity concentration layer corresponding to the n⁺-type supporting substrate 1 may be formed by introducing an n-type dopant (phosphorus, arsenic, etc.) into the ground surface by ion implantation, etc., and thermal annealing, etc. A thinning process of the semiconductor base 10 may be performed after formation of surface structures such as the FP, the embedded insulating film, and the trench of the present embodiment.

[0061] (Second embodiment)

A structure of the semiconductor device according to a second embodiment will be described. Figs. 14A and 14B are cross sectional views of a structure of the semiconductor device according to the second embodiment. The semiconductor device

according to the second embodiment differs from the semiconductor device according to the first embodiment in that the distance w_3 between a FP 45 and the inner side wall 22a of the trench 22 progressively increases with the depth from the base front surface. In other words, the FP 45 curves outwardly away from the inner side wall 22a of the trench 22 as the depth from the base front surface increases.

[0062] More specifically, the FP 45, similar to the first embodiment, is embedded inside a groove 44 disposed in the embedded insulating film 23. Both side walls 44a, 44b of the groove 44 curve away from the inner side wall 22a of the trench 22 as the depth from the base front surface increases. At least near a bottom end of the FP 45, the distance w_3 between the FP 45 and the inner side wall 22a of the trench 22 is greater than the width w_2 of the groove 44. Although the electric field strength of the embedded insulating film increases with the depth from the base front surface, at a portion where the electric field strength near the bottom end of the FP 45 is high, the thickness (the width in a horizontal direction) of the embedded insulating film 23 becomes thick, and the effect of relaxing the electric field at this thickened portion of the embedded insulating film 23 becomes enhanced.

[0063] Further, disposal of the FP 45 enables electric field distribution to be obtained such that corresponding to the curve of the FP 45, locations where electric field concentrates are moved farther outward within the interior the embedded insulating film 23. In other words, the FP 45 has a function of modulating the electric field distribution such that locations where electric field concentrates are contained inside the embedded insulating film 23. The farther outward the locations where electric field concentrates are positioned inside the embedded insulating film 23, the greater the breakdown voltage is enhanced by relaxing the electric field of the portion of the n-type drift region 2, along the inner side wall 22a of the trench 22.

[0064] More specifically, an angle θ_1 of the base front surface and a tangent passing through an inner corner portion 44d of a bottom 44c of the groove 44 is 0 degrees or greater and less than 90 degrees ($0 \text{ degrees} \leq \theta_1 < 90 \text{ degrees}$). The inner corner portion 44d of the bottom 44c of the groove 44 is positioned at the center position 22d of the trench 22 (i.e., corresponding to a case where $\theta_1 = 0 \text{ degrees}$: refer to Fig. 14A), or, farther inward than the center position 22d of the trench 22 (i.e., corresponding to a case where $0 \text{ degrees} < \theta_1 < 90 \text{ degrees}$: refer to Fig. 14B). The inner corner portion 44d of the bottom 44c of the groove 44 is an intersecting line of the bottom 44c of the groove 44 and the inner side wall 44a.

[0065] Preferably, the FP 45 curves outwardly to an extent enabling the electric field strength of the portion of the n-type drift region 2, along the inner side wall 22a of the trench 22 to be lower than the electric field strength near the main junction 20 of the active region 11. For example, the angle θ_1 of the base front surface and the tangent

passing through the inner corner portion 44d of the bottom 44c of the groove 44 is favorably 20 degrees or greater and 70 degrees or less ($20 \text{ degrees} \leq \theta_1 \leq 70 \text{ degrees}$) and is preferably, 30 degrees or greater and 60 or less ($30 \text{ degrees} \leq \theta_1 \leq 60 \text{ degrees}$). A case where $\theta_1 = 90$ degrees is a state where the side wall of the groove is not curved and corresponds to the first embodiment.

[0066] The depth D2 of the groove 44 is identical to that of the first embodiment. In the second embodiment, the depth D2 of the groove 44 is a length in a vertical direction, from the front surface of the semiconductor base 10, to the inner corner portion 44d of the bottom 44c of the groove 44. The width w2 of the groove 44 is substantially constant from the base front surface to the bottom 44c of the groove 44. The end of the front surface electrode 4 is preferably positioned farther inward than a position of the bottom end of the FP 45 (end on base back surface side) in a horizontal direction. The reason for this is that when the front surface electrode 4 extends farther outward than the position of the bottom end of the FP 45 in a horizontal direction, electric field distribution is adversely affected by the FP 45. The bottom end of the FP 45 is a portion of the FP 45 at the inner corner portion 44d of the bottom 44c of the groove 44.

[0067] The method of manufacturing the semiconductor device according to the second embodiment will be described. Figs. 15 to 20 are cross sectional views during manufacture of the semiconductor device according to the second embodiment. Similar to the first embodiment, the n⁺-type supporting substrate 1 is prepared and processes from epitaxial growth of the n-type drift region 2 to deposition of the LTO film 32 are sequentially performed (refer to Figs. 2 to 5). Next, as depicted in Fig. 15, the embedded insulating film 23 is deposited along the base front surface and along the inner wall of the trench 22. Here, the interior of the trench 22 is not completely embedded with the embedded insulating film 23 and the embedded insulating film 23 is embedded so as to leave a groove 51 having a cross sectional shape that is substantially a U-shape inside the trench 22. The groove 51 later becomes the groove 44 in which the FP 45 is embedded. Therefore, the groove 51 is left at the depth D2 from the interface of the p-type region 3 and the n-type drift region 2.

[0068] More specifically, by a spin coat method, the insulating material of the embedded insulating film 23 is applied to the base front surface while rotating the semiconductor base 10 about an axis. Here, adjustment of the thickness of the embedded insulating film 23 by adjusting the rotating speed of the stage on which the semiconductor base 10 is placed, enables the cross sectional shape (slope of the side wall) of the groove 51 and the depth D2 to be adjusted. An application-type insulating material that is viscous and has high fluidity such as SOG and BCB described above is used as the insulating material of the embedded insulating film 23. The reason for this is that with insulating material deposited by a deposition method, etc., the groove 51 cannot be left to have a

cross section that is substantially a U-shape.

- [0069] Next, as depicted in Fig. 16, after hardening of the embedded insulating film 23 by heat treatment, a metal film 52 that becomes the FP 45 is deposited along the inner wall of the groove 51. The metal film 52 is, for example, an aluminum film. The aluminum film easily reflects irradiated light for luminous exposure during photolithography to form a resist mask used for patterning the metal film 52. Therefore, next, the metal film 52 is covered by a metal film (hereinafter, reflection preventing film) that prevents reflection. The reflection preventing film may be, for example, a deposited metal film of a titanium-tungsten (TiW) film and a silicon nitride (SiN) film, sequentially deposited.
- [0070] Next, for example, a resist film is applied onto the reflection preventing film by a deposition method or a spray coat method. Application of the resist film by a spray coat method enables the resist film to be formed along the reflection preventing film. Next, the resist film is patterned (luminous exposure of resist film) by photolithography and a resist mask that covers the forming region of the FP 45 is formed. When the resist film is luminously exposed, in an opening of the resist film, the reflection preventing film is luminously exposed; and the lower layer thereof, the metal film 52, is not luminously exposed. Therefore, unintended luminous exposure of a portion (a portion to be left as the resist mask) of the resist film by light that is irradiated for luminous exposure and reflected by the metal film 52 does not occur.
- [0071] Next, as depicted in Fig. 17, etching is performed using the resist mask (not depicted) as a mask, and the metal film 52 and the reflection preventing film (not depicted) are patterned. For example, a portion of the metal film 52, from a portion covering an outer side wall 51b of the groove 51 outward, is removed, and a portion from a portion covering an inner side wall 51a of the groove 51 inward, is left. The metal film 52 left on the inner side wall 51a of the groove 51 becomes the FP 45. Next, the resist mask is removed, followed by the reflection preventing film. The reason for removing the reflection preventing film is that a contact unit (contact) of the FP 45, contacting the front surface electrode 4 is preferably formed by the same metal material as the front surface electrode 4.
- [0072] Next, as depicted in Fig. 18, after completely embedding the interior of the trench 22 with the embedded insulating film 23, the embedded insulating film 23 is hardened by heat treatment. As a result, the groove 44 in which the FP 45 is embedded is formed. Next, as depicted in Fig. 19, the FP 45 and the embedded insulating film 23 are polished until the interlayer insulating film 5 is exposed. Next, as depicted in Fig. 20, photolithography and etching are performed to pattern the interlayer insulating film 5 and form a contact hole, exposing the p-type region 3. Thereafter, similar to the first embodiment, formation of the front surface electrode 4 and the processes thereafter are

sequentially performed, whereby the semiconductor device depicted in Fig. 14A is completed.

[0073] As described above, according to the second embodiment, effects similar to those of the first embodiment can be achieved. Further, according to the second embodiment, by curving the FP inside the embedded insulating film outward as the depth from the base front surface increases, the electric field near the lower end of the FP can be relaxed. As a result, electric field concentration of a portion of the n-type drift region, along the inner side wall of the trench can be reduced and the breakdown voltage can be further enhanced.

[0074] (Third embodiment)

A structure of the semiconductor device according to a third embodiment will be described. Figs. 21A and 21B are cross sectional views of a structure of the semiconductor device according to the third embodiment. Fig. 21B depicts an enlarge view of a portion of Fig. 21A. The semiconductor device according to the third embodiment differs from the semiconductor device according to the second embodiment in that inside the embedded insulating film 23, on an outer side of the FP (hereinafter, a first FP) 45, a FP (hereinafter, second FP) 47 is further disposed. The second FP 47 curves inwardly away from the outer side wall 22b of the trench 22 as the depth from the base front surface increases. The second FP 47 is separate from and not electrically connected to the first FP 45. The second FP 47 is electrically connected to the n-type channel stopper region 21.

[0075] Disposal of the second FP 47 enables electric field distribution to be obtained such that corresponding to the curve of the second FP 47, locations where electric field concentrates are moved farther inward within the interior of the embedded insulating film 23. As a result, distribution in which locations where electric field concentrates protrude farther outward than the embedded insulating film 23 can be suppressed. In other words, the second FP 47 has a function of suppressing extension of the depletion layer that extends outwardly from the main junction 20 of the active region 11 and a function of adjusting the electric field distribution such that locations where electric field concentrates are contained inside the embedded insulating film 23. As a result, concentration of the electric field in the n-type channel stopper region 21 is suppressed, enabling the occurrence of avalanche breakdown at the n-type channel stopper region 21 to be prevented.

[0076] More specifically, the second FP 47 is embedded inside a groove (hereinafter, second groove) 46 disposed in the embedded insulating film 23. The second groove 46 is disposed to have a planar layout surrounding a periphery of a groove (hereinafter, first groove) 44 in which the first FP 45 is embedded. Both side walls 46a, 46b of the second groove 46 curve away from the outer side wall 22b of the trench 22 as the

depth from the base front surface increases. With respect to a central line passing through the center position 22d of the trench 22, for example, the second groove 46 may curve to be substantially symmetrical to the first groove 44.

[0077] The angle θ_1 of the base front surface and a tangent passing through the inner corner portion 44d of the bottom 44c of the first groove 44 is greater than 0 degrees and less than 90 degrees ($0 \text{ degrees} < \theta_1 < 90 \text{ degrees}$). The inner corner portion 44d of the bottom 44c of the first groove 44 is positioned farther inward than the center position 22d of the trench 22. The angle θ_1 of the base front surface and the tangent passing through the inner corner portion 44d of the bottom 44c of the groove 44 is similar to that in the second embodiment.

[0078] An angle θ_2 of the base front surface and a tangent that passes through an outer corner portion 46d of a bottom 46c of the second groove 46 is greater than 0 degrees and less than 90 ($0 \text{ degrees} < \theta_2 < 90 \text{ degrees}$). The outer corner portion 46d of the bottom 46c of the second groove 46 is an intersecting line of the bottom 46c of the second groove 46 and the outer side wall 46b. The outer corner portion 46d of the bottom 46c of the second groove 46 is positioned farther outward than the center position 22d of the trench 22.

[0079] In other words, the bottom 44c of the first groove 44 and the bottom 46c of the second groove 46 do not contact. A distance w_5 between the inner corner portion 44d of the bottom 44c of the first groove 44 and the outer corner portion 46d of the bottom 46c of the second groove 46, for example, preferably satisfies expression (1) with respect to breakdown voltage V_B of the semiconductor device and dielectric breakdown voltage V_C of the embedded insulating film 23. The dielectric breakdown voltage V_C of the embedded insulating film 23, for example, is about $2 \times 10^6 \text{ V/cm}$.

[0080] $w_5[\text{cm}] \geq V_B[\text{V}] / V_C[\text{V/cm}]$ (1)

[0081] From expression (1), when the breakdown voltage V_B of the semiconductor device is, for example, 1000V, the distance w_5 between the inner corner portion 44d of the bottom 44c of the first groove 44 and the outer corner portion 46d of the bottom 46c of the second groove 46 is about $5 \mu\text{m}$. A width w_4 of the second groove 46 is substantially constant from the base front surface to the bottom 46c of the second groove 46. The width w_4 of the second groove 46 may be substantially equivalent to the width w_2 of the first groove 44 ($w_4 = w_2$).

[0082] The depth D_2 of the groove 44 is identical to that in the second embodiment. A depth D_3 of the second groove 46 can be varied and is favorably a depth that enables the occurrence of avalanche breakdown at the n-type channel stopper region 21 to be prevented and that enables modulation of the electric field distribution to an extent that a depletion layer 63 (refer to Fig. 28) that extends outwardly from the main junction 20 of the active region 11 does not reach the chip end. The depth D_3 of the second groove

46 is a length in a vertical direction from the front surface of the semiconductor base 10, to the outer corner portion 46d of the bottom 46c of the second groove 46. Figs. 21A and 21B depict a case where the depth D2 of the first groove 44 and the depth D3 of the second groove 46 are substantially the same.

[0083] The second FP 47 extends on the embedded insulating film 23 and is electrically connected to the n-type channel stopper region 21. More specifically, a stopper electrode 4a is connected to the n-type channel stopper region 21 and covers entirely or at least a portion of the n-type channel stopper region 21 (end on the base front surface side). Furthermore, the stopper electrode 4a extends inwardly from an outer side of the semiconductor substrate so as to cover a portion on the embedded insulating film 23. The second FP 47, at an upper portion, is connected to the stopper electrode 4a. The second FP 47 may be connected farther outward than an inner end of the stopper electrode 4a. Such configuration enables adverse effects of external charge on potential distribution inside the embedded insulating film 23 to be minimized.

[0084] The method of manufacturing the semiconductor device according to the third embodiment will be described. Figs. 22 to 25 are cross sectional views during manufacture of the semiconductor device according to the third embodiment. Similar to the second embodiment, first, the n⁺-type supporting substrate 1 is prepared and processes from epitaxial growth of the n-type drift region 2 to deposition of the metal film 52 and the reflection preventing film are sequentially performed (refer to Figs. 2 to 5, 15, and 16). In the third embodiment, the groove 51 disposed inside the trench 22 becomes the first and the second grooves 44, 46; and the metal film 52 formed along the groove 51 becomes the first and the second FPs 45, 47.

[0085] Next, as depicted in Fig. 22, photolithography and etching are performed to pattern the metal film 52 and the reflection preventing film (not depicted), and the portions of the metal film 52 to become the first and the second FPs 45, 47 are left. Next, the resist mask and the reflection preventing film are removed and subsequently, as depicted in Fig. 23, after the interior of the trench 22 is completely embedded with the embedded insulating film 23, the embedded insulating film 23 is hardened by heat treatment. As a result, the first and the second grooves 44, 46 in which the first and the second FPs 45, 47 are respectively embedded are formed.

[0086] Next, as depicted in Fig. 24, the first and the second FPs 45, 47 and the embedded insulating film 23 are polished until the interlayer insulating film 5 is exposed. Next, as depicted in Fig. 25, photolithography and etching are performed to pattern the interlayer insulating film 5 and form a contact hole, exposing the p-type region 3 and the n-type channel stopper region 21. Thereafter, similar to the second embodiment, formation of the front surface electrode 4 and the processes thereafter are sequentially performed, whereby the semiconductor device depicted in Figs. 21A and 21B is

completed. In the semiconductor device according to the third embodiment, the stopper electrode 4a is formed concurrently with a process of forming the front surface electrode 4 or at a process after formation of the front surface electrode 4.

[0087] As described above, according to the third embodiment, effects similar to those of the first and the second embodiments can be achieved. Further, according to the third embodiment, disposal of the second FP that curves inwardly as the depth from the base front surface increases enables electric field distribution to be obtained that contains locations where electric field concentrates, to be in a portion between the first and the second FPs of the embedded insulating films. As a result, the occurrence of avalanche breakdown farther outward than the embedded insulating film can be suppressed.

[0088] Dynamic characteristics of the FPs 45, 47 were verified. Fig. 26 is a diagram of static characteristics of a fifth example. Fig. 27 is a diagram of dynamic characteristics of the fifth example. Fig. 28 is a diagram of dynamic characteristics of a sixth example. A diode (hereinafter, fifth example: refer to Figs. 14A and 14B) in which the FP 45 that curves outwardly is embedded inside the embedded insulating film 23 was produced according to the method of manufacturing the semiconductor device according to the second embodiment described above. A state (static state) of a depletion layer 61 that extends outwardly from the main junction 20 of the active region 11 during a steady state of the fifth example is depicted in Fig. 26; and a state (dynamic state) of a depletion layer 62 that extends from the main junction 20 of the active region 11 when high dV/dt is applied is depicted in Fig. 27.

[0089] Further, a diode (hereinafter, sixth example: refer to Figs. 21A and 21B) in which inside the embedded insulating film 23, the first FP 45 that curves outwardly and the second FP 47 that curves inwardly are disposed sequentially from an inner side, was produced according to the method of manufacturing the semiconductor device according to the third embodiment described above. A state (dynamic state) of the depletion layer 63 that extends outwardly from the main junction 20 of the active region 11 when high dV/dt is applied is depicted in Fig. 28. High dV/dt is high voltage (noise) needed for high speed switching and voltage fluctuation dV/dt corresponding to switching time may be great.

[0090] From the results depicted in Fig. 26, it was confirmed that during the steady state of the fifth example, the depletion layer 61 that extends outwardly from the main junction 20 of the active region 11 can be stopped at a state along the outer side wall 22b of the trench 22. The reason for this is that in a portion of the n-type drift region 2, along the outer side wall 22b of the trench 22, electrons are induced and an n-type region 61a that is formed by these induced electrons is formed. The n-type region 61a functions as a channel stopper and has a function of modulating the electric field distribution such that locations where electric field concentrates are contained inside the embedded in-

insulating film 23.

[0091] From the results depicted in Fig. 27, during high dV/dt application to the fifth example, the depletion layer 62 that extends outwardly from the main junction 20 of the active region 11 spreads toward the chip end side to a greater extent than during the steady state. The reason for this is that in a portion of the n-type drift region 2, along the outer side wall 22b of the trench 22, before the n-type region 61a (refer to Fig. 26) is formed, the depletion layer 62 spreads to the chip end side. In this case, depending on the magnitude of the high dV/dt , there is a risk of distribution in which locations where electric field concentrates protrude farther outward than the embedded insulating film 23 and a risk of avalanche breakdown at the n-type channel stopper region 21.

[0092] From the results depicted in Fig. 28, in the sixth example, it was confirmed that even during high dV/dt application, the depletion layer 63 that extends outwardly from the main junction 20 of the active region 11 can be stopped at a state along the outer side wall 22b of the trench 22. As a result, the second FP 47 of the sixth example is confirmed to have the same function as the n-type region 61a (refer to Fig. 26) that is consequent to induced electrons in the portion along the outer side wall 22b of the trench 22 during the steady state.

[0093] (Fourth embodiment)

A structure of the semiconductor device according to a fourth embodiment will be described. Fig. 29 is a cross sectional view of a structure of the semiconductor device according to the fourth embodiment. The semiconductor device according to the fourth embodiment differs from the semiconductor device according to the third embodiment in that the depth of a second FP 49 is greater than the depth of the first FP 45. In other words, the depth D3 of a second groove 48 in which the second FP 49 is embedded is deeper than the depth D2 of the first groove 44 in which the first FP 45 is embedded. Configuration other than the depth D3 of the second groove 48 of the semiconductor device according to the fourth embodiment is identical to that of the semiconductor device according to the third embodiment.

[0094] The method of manufacturing the semiconductor device according to the fourth embodiment will be described. Figs. 30 to 33 are cross sectional views during manufacture of the semiconductor device according to the fourth embodiment. Similar to the first embodiment, first, the n⁺-type supporting substrate 1 is prepared and processes from epitaxial growth of the n-type drift region 2 to deposition of the LTO film 32 are sequentially performed (refer to Figs. 2 to 5). Next, as depicted in Fig. 30, the embedded insulating film 23 is deposited along the inner walls of the base front surface and the trench 22. Here, the embedded insulating film 23 is embedded so as to leave a groove 71 having a cross sectional shape that is substantially a U-shape inside the

trench 22. The groove 71 later becomes the second groove 48 in which the second FP 49 is embedded. Therefore, the groove 71 is left at the depth D3 from the front surface of the semiconductor base 10.

- [0095] Next, the embedded insulating film 23 is hardened by heat treatment and subsequently, a metal film 72 that becomes the second FP 49 is deposited along the inner wall of the groove 71. Next, similar to the formation of the first FP of the second embodiment, after the metal film 72 is covered by the reflection preventing film (not depicted), photolithography and etching are performed to pattern the metal film 72 and the reflection preventing film, and a portion of the metal film 72 to become the second FP 49 is left. Next, the resist mask and the reflection preventing film are removed.
- [0096] Next, as depicted in Fig. 31, the embedded insulating film 23 is deposited inside the trench 22 so as to cover the second FP 49. Here, the embedded insulating film 23 is embedded so as to leave a groove 73 having a cross sectional shape that is substantially a U-shape inside the trench 22. The groove 73 later becomes the first groove 44 in which the first FP 45 is embedded. Therefore, the groove 73 is left at the depth D2 from the front surface of the semiconductor base 10.
- [0097] Next, the embedded insulating film 23 is hardened by heat treatment and a metal film 74 that becomes the first FP 45 is deposited along the inner wall of the groove 73. Next, similar to the second embodiment, after the metal film 74 is covered by the reflection preventing film (not depicted), photolithography and etching are performed to pattern the metal film 74 and the reflection preventing film, and a portion of the metal film 74 to become the first FP 45 is left. Next, the resist mask and the reflection preventing film are removed.
- [0098] Next, as depicted in Fig. 32, after the inside of the trench 22 is completely embedded with the embedded insulating film 23, the embedded insulating film 23 is hardened by heat treatment. As a result, the first and the second grooves 44, 48 in which the first and the second FPs 45, 49 are respectively embedded are formed. The embedding of the embedded insulating film 23 described above suffices to use a spin coat method, similar to the second embodiment.
- [0099] Next, as depicted in Fig. 33, the first and the second FPs 45, 49 and the embedded insulating film 23 are polished until the interlayer insulating film 5 is exposed. Next, photolithography and etching are performed to pattern the interlayer insulating film 5 and form a contact hole, exposing the p-type region 3 and the n-type channel stopper region 21. Thereafter, similar to the first embodiment, formation of the front surface electrode 4 and the processes thereafter are sequentially performed, whereby the semiconductor device depicted in Fig. 29 is completed. In the semiconductor device according to the fourth embodiment, the stopper electrode 4a is formed concurrently with a process of forming the front surface electrode 4 or at a process after formation

of the front surface electrode 4.

[0100] As described above, according to the fourth embodiment, effects similar to those of the first to the third embodiments can be achieved. Further, according to the fourth embodiment, by making the depth of the second FP deep, electric field distribution that contains locations where electric field concentrates, to be inside the embedded insulating film can be more assuredly obtained.

[0101] (Fifth embodiment)

A structure of the semiconductor device according to the fifth embodiment will be described. Fig. 34 is a cross sectional view of the structure of the semiconductor device according to the fifth embodiment. The semiconductor device according to the fifth embodiment differs from the semiconductor device according to the second embodiment in that an n-type region 81 is disposed in a portion of the n-type drift region 2, along the outer side wall 22b of the trench 22.

[0102] The n-type region 81 is disposed to be exposed to the outer side wall 22b of the trench 22. Further, the n-type region 81 is connected to the n-type channel stopper region 21. The n-type region 81 has a function identical to the n-type region 61a (refer to Fig. 26) of the semiconductor device according to the second embodiment and formed by inducted electrons at the end of the depletion layer 61 during the steady state.

[0103] The method of manufacturing the semiconductor device according to the fifth embodiment, for example, suffices to form the n-type region 81 at the outer side wall 22b of the trench 22 by oblique ion implantation after formation of the trench 22 and before sacrificial oxidation of the inner wall of the trench 22 in the method of manufacturing the semiconductor device according to the second embodiment. Oblique ion implantation is ion implantation performed from an oblique direction relative to the base front surface.

[0104] The manufacturing method described in the fifth embodiment may be applied to the first embodiment.

[0105] As described above, according to the fifth embodiment, disposal of the n-type region in a portion of the n-type drift region, along the outer side wall of the trench enables effects similar to those of the first to the fourth embodiments to be achieved.

[0106] In the description, various design modifications can be made without departing from the spirit of the present invention and in the described embodiments, for example, dimensions, impurity concentration, etc. of components can be set according to required specifications. Further, in the described embodiments, although description is given taking a diode, a MOSFET, etc. as an example, the invention is further applicable to insulated gate bipolar transistors (IGBT). In this case, in place of the n⁺-type supporting substrate, a p⁺-type supporting substrate is used.

- [0107] Even in the case of an IGBT, the semiconductor base 10 may be a bulk wafer cut from an ingot. The ingot for the bulk wafer may be manufactured by a float zone (FZ) method, a Czochralski (CZ) process, or a magnetic Czochralski (MCZ) process. The semiconductor base 10 may be, for example, a bulk wafer that has been thinned by grinding the back surface side thereof. In this case, the n-type drift region 2 may be of the same impurity concentration as the bulk wafer. A p-type high impurity concentration layer corresponding to a p⁺-type supporting substrate may be formed by introducing a p-type dopant (boron, aluminum, etc.) into the ground surface by ion implantation, etc., and thermal annealing, etc. A thinning process of the semiconductor base 10 may be performed after formation of surface structures such as the FP, the embedded insulating film, and the trench of the present embodiment. Further, in each of the embodiments described above, other than silicon and germanium, the semiconductor base may be a wide bandgap semiconductor base such as silicon carbide (SiC), gallium nitride (GaN), and diamond.
- [0108] In the third and the fourth embodiments, even in cases where the second FP has a cross sectional shape that is substantially linear, modulation is possible such that electric field distribution is obtained that contains locations where electric field concentrates, to be farther inward within the interior of the embedded insulating film. Further, in the embodiments, although description is given taking a case where an epitaxial substrate is used that is a semiconductor substrate on which a semiconductor layer is epitaxial grown, without limitation hereto, for example, a doping region formed by ion implanting inside a semiconductor substrate, all regions configuring the device, may be used. Further, in the embodiments, although a first conductivity type is assumed to be an n-type and a second conductivity type is assumed to be a p-type, the present invention is further applicable when the first conductivity type is assumed to be a p-type and the second conductivity type is assumed to be an n-type.

Industrial Applicability

- [0109] As described, the semiconductor device and the method of manufacturing the semiconductor device according to the present invention is useful for various semiconductor devices in which a high voltage structure is disposed in an edge termination region.

Reference Signs List

- [0110] 1 n⁺-type supporting substrate
 2 n-type drift region
 3 p-type region
 3a outer end
 4 front surface electrode

5 interlayer insulating film
6 back surface electrode
10 semiconductor base
11 active region
12 edge termination region
20 main junction of active region
21 n-type channel stopper region
22 trench
22a, 22b side wall of trench
22c bottom of trench
22d center position of trench
23 embedded insulating film
24, 44, 46, 48, 51, 71, 73 groove
25, 45, 47, 49 FP
31 sacrificial oxide film
32 LTO film
44a, 44b, 46a, 46b, 51a, 51b side wall of groove
44c, 46c bottom of groove
44d, 46d bottom corner portion of groove
52, 72, 74 metal film
61 to 63 depletion layer
61a, 81 n-type region
D1 depth of trench
D2, D3 depth of groove
w1 width of trench
w2, w4 width of groove
w3 distance between FP and inner side wall of trench
w5 distance between bottom corner portions inside groove
 $\theta 1$ angle between base front surface and tangent passing through inner corner portion of bottom of groove
 $\theta 2$ angle between base front surface and tangent passing through outer corner portion of bottom of groove

Claims

- [Claim 1] A semiconductor device comprising:
a trench disposed farther outward than an active region and reaching a predetermined depth from a first principal surface of a semiconductor substrate;
a pn junction between a second conductivity type region and a first conductivity type region, and disposed in a first principal surface side of the semiconductor substrate, the pn junction extends outwardly from the active region and is terminated by the trench;
an insulating film embedded inside the trench;
a first field plate disposed inside the insulating film and long in a direction of depth;
a first electrode contacting the second conductivity type region and the first field plate; and
a second electrode disposed in a second principal surface of the semiconductor substrate, wherein
a distance between an inner side wall of the trench and the first field plate is greater than a width of the first field plate.
- [Claim 2] The semiconductor device according to claim 1, wherein
the first field plate curves away from the inner side wall of the trench as a depth from the first principal surface of the semiconductor substrate increases.
- [Claim 3] The semiconductor device according to claim 2, wherein
the distance between the inner side wall of the trench and the first field plate toward a second principal surface side of semiconductor substrate is greater than the width of the first field plate.
- [Claim 4] The semiconductor device according to claim 1, wherein
a depth of the first field plate is deeper than the pn junction and shallower than the trench, from the first principal surface of the semiconductor substrate.
- [Claim 5] The semiconductor device according to claim 4, wherein
the depth of the first field plate is 30% or more and 70% or less of a depth of the trench.
- [Claim 6] The semiconductor device according to claim 1 and further comprising
a second field plate disposed inside the insulating film and long in the direction of depth, wherein
the second field plate is disposed farther outward than the first field

- plate and away from the first field plate.
- [Claim 7] The semiconductor device according to claim 6, wherein the second field plate curves away from an outer side wall of the trench as a depth from the first principal surface of the semiconductor substrate increases.
- [Claim 8] The semiconductor device according to claim 6, wherein a depth of the second field plate is greater than a depth of the first field plate.
- [Claim 9] The semiconductor device according to claim 1, wherein the semiconductor substrate is configured by the second conductivity type region that contacts the first electrode disposed in the first principal surface of the semiconductor, a supporting substrate that contacts the second electrode disposed in the second principal surface of the semiconductor substrate, and the first conductivity type region between the second conductivity type region and the supporting substrate, and the trench, from the pn junction, reaches a depth that is 30% or more of a thickness of the first conductivity type region and less than the thickness of the first conductivity type region.
- [Claim 10] The semiconductor device according to any one among claims 1 to 9, wherein a width of the trench is 30% or more and 60% or less of a depth of the trench.
- [Claim 11] A method of manufacturing a semiconductor device, the method comprising:
a first process of forming in a first principal surface side of a semiconductor substrate, a pn junction between a second conductivity type region and a first conductivity type region, the pn junction extending outwardly from an active region;
a second process of forming farther outward than the active region, a trench that reaches a predetermined depth from the first principal surface of the semiconductor substrate and that terminates the pn junction;
a third process of embedding inside the trench, an insulating film so as to leave a groove having a U-shaped cross sectional shape;
a fourth process of forming a metal film along the groove;
a fifth process of selectively removing the metal film to leave, as a first field plate, a remaining portion of the metal film at an inner side wall of

the groove; and

a sixth process of further embedding inside the trench, the insulating film so as to cover the first field plate.

[Claim 12]

The method according to claim 11 and further comprising a process of forming a reflection preventing film on the metal film, after the fourth process and before the fifth process, wherein the fifth process includes

a process applying a resist film on the reflection preventing film,

a process of luminously exposing the resist film and forming a resist mask that covers a forming region of the first field plate, and

a process of etching using the resist mask as a mask to leave, as the first field plate, the remaining portion of the metal film at the inner side wall of the groove.

[Claim 13]

The method according to claim 11, wherein

in the fifth process, a remaining portion of the metal film, away from the first field plate, is left at an outer side wall of the groove as a second field plate.

AMENDED CLAIMS

received by the International Bureau on 13 January 2017 (13.01.2017)

[Claim 1] (amended) A semiconductor device comprising:
a trench disposed farther outward than an active region and reaching a predetermined depth from a first principal surface of a semiconductor substrate;
a pn junction between a second conductivity type region and a first conductivity type region, and disposed in a first principal surface side of the semiconductor substrate, the pn junction extends outwardly from the active region and is terminated by the trench;
an insulating film embedded inside the trench;
a first field plate disposed inside the insulating film and long in a direction of depth;
a first electrode contacting the second conductivity type region and the first field plate; and
a second electrode disposed in a second principal surface of the semiconductor substrate, wherein
a distance between an inner side wall of the trench and the first field plate is greater than a width of the first field plate,
the first field plate curves away from the inner side wall of the trench as a depth from the first principal surface of the semiconductor substrate increases.

[Claim 2] (cancelled)

[Claim 3] The semiconductor device according to claim 2, wherein

the distance between the inner side wall of the trench and the first field plate toward a second principal surface side of semiconductor substrate is greater than the width of the first field plate.

[Claim 4] The semiconductor device according to claim 1, wherein

a depth of the first field plate is deeper than the pn junction and shallower than the trench, from the first principal surface of the semiconductor substrate.

[Claim 5] The semiconductor device according to claim 4, wherein

the depth of the first field plate is 30% or more and 70% or less of a depth of the trench.

[Claim 6] The semiconductor device according to claim 1 and further comprising

a second field plate disposed inside the insulating film and long in the direction of depth, wherein

the second field plate is disposed farther outward than the first field plate and away from the first field plate.

[Claim 7] The semiconductor device according to claim 6, wherein

the second field plate curves away from an outer side wall of the trench as a depth from the first principal surface of the semiconductor substrate increases.

[Claim 8] The semiconductor device according to claim 6, wherein

a depth of the second field plate is greater than a depth of the first field plate.

[Claim 9] The semiconductor device according to claim 1, wherein

the semiconductor substrate is configured by
the second conductivity type region that contacts the first electrode disposed in the first principal surface of the semiconductor,

a supporting substrate that contacts the second electrode disposed in the second principal surface of the semiconductor substrate, and

the first conductivity type region between the second

conductivity type region and the supporting substrate, and the trench, from the pn junction, reaches a depth that is 30% or more of a thickness of the first conductivity type region and less than the thickness of the first conductivity type region.

[Claim 10] The semiconductor device according to any one among claims 1 to 9, wherein

a width of the trench is 30% or more and 60% or less of a depth of the trench.

[Claim 11] (amended) A method of manufacturing a semiconductor device, the method comprising:

a first process of forming in a first principal surface side of a semiconductor substrate, a pn junction between a second conductivity type region and a first conductivity type region, the pn junction extending outwardly from an active region;

a second process of forming farther outward than the active region, a trench that reaches a predetermined depth from the first principal surface of the semiconductor substrate and that terminates the pn junction;

a third process of embedding inside the trench, an insulating film so as to leave a groove having a U-shaped cross sectional shape;

a fourth process of forming a metal film along the groove;

a fifth process of selectively removing the metal film to leave, as a first field plate, a remaining portion of the metal film at an inner side wall of the groove; and

a sixth process of further embedding inside the trench, the insulating film so as to cover the first field plate, wherein

the first field plate curves away from the inner side wall of the trench as a depth from the first principal surface

of the semiconductor substrate increases.

[Claim 12] The method according to claim 11 and further comprising

a process of forming a reflection preventing film on the metal film, after the fourth process and before the fifth process, wherein

the fifth process includes

a process applying a resist film on the reflection preventing film,

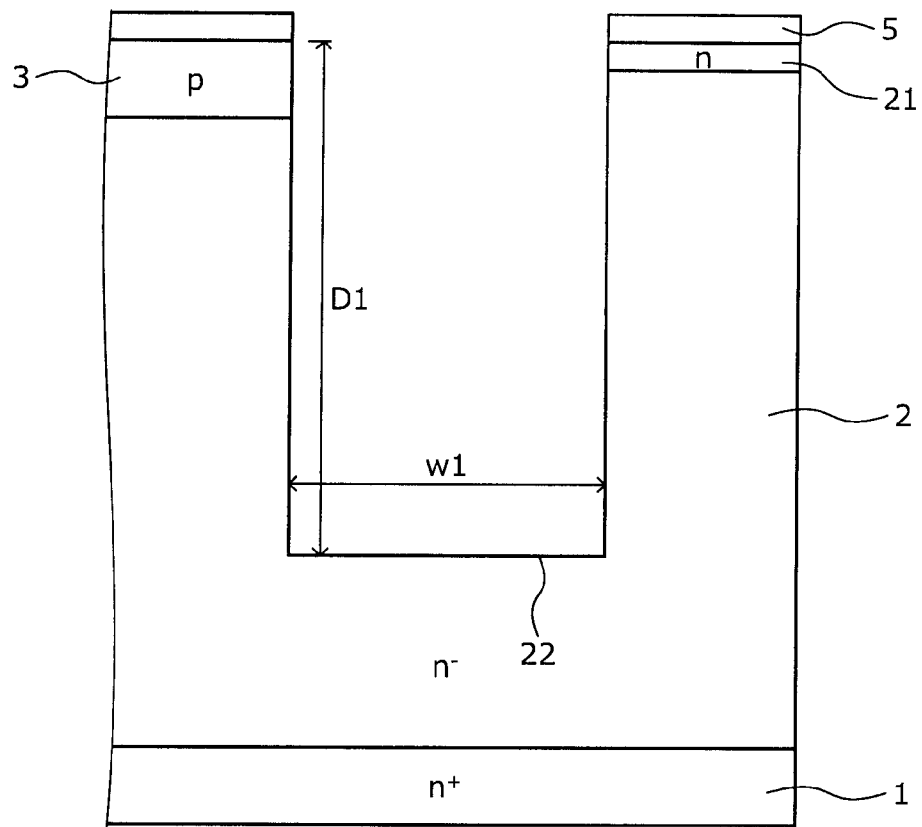
a process of luminously exposing the resist film and forming a resist mask that covers a forming region of the first field plate, and

a process of etching using the resist mask as a mask to leave, as the first field plate, the remaining portion of the metal film at the inner side wall of the groove.

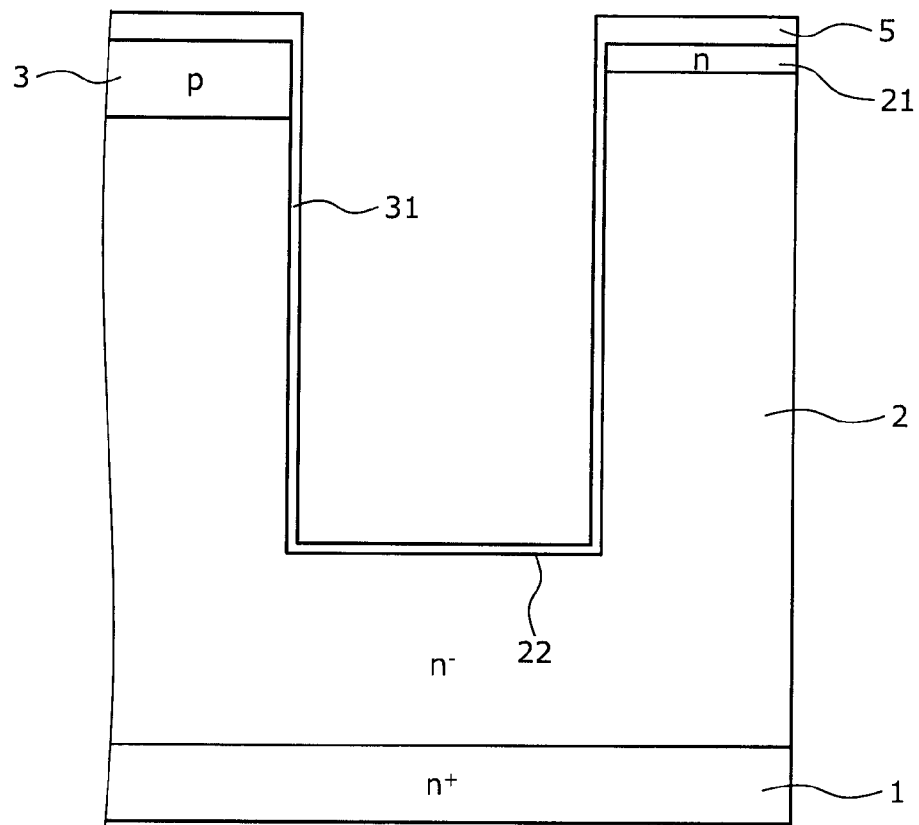
[Claim 13] The method according to claim 11, wherein

in the fifth process, a remaining portion of the metal film, away from the first field plate, is left at an outer side wall of the groove as a second field plate.

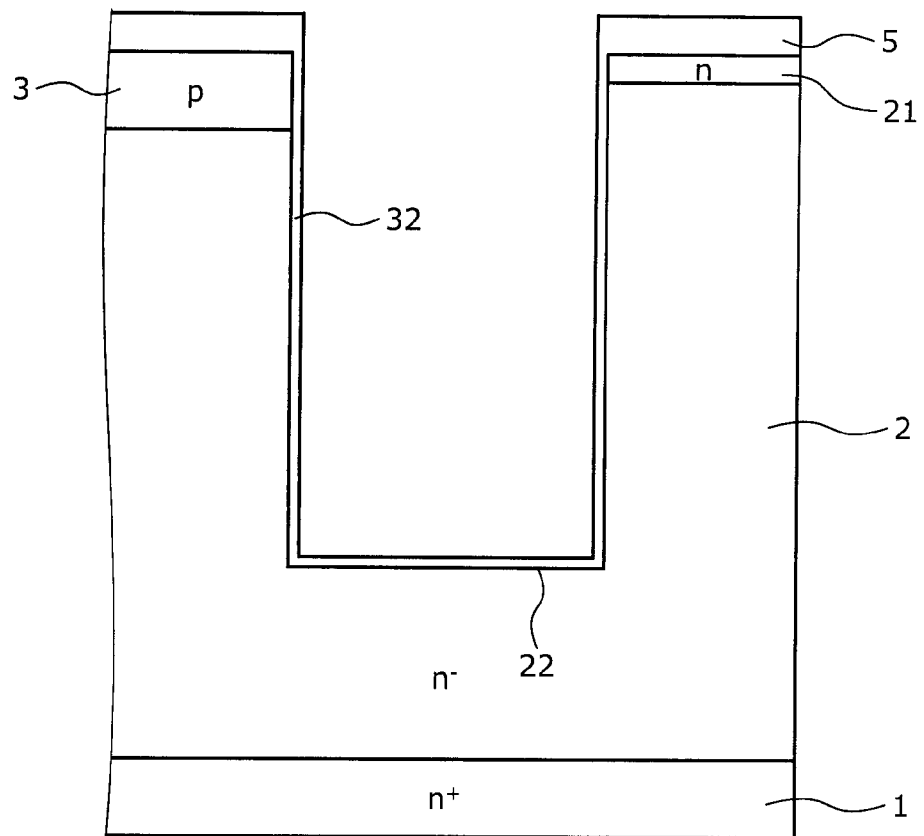
[Fig. 3]



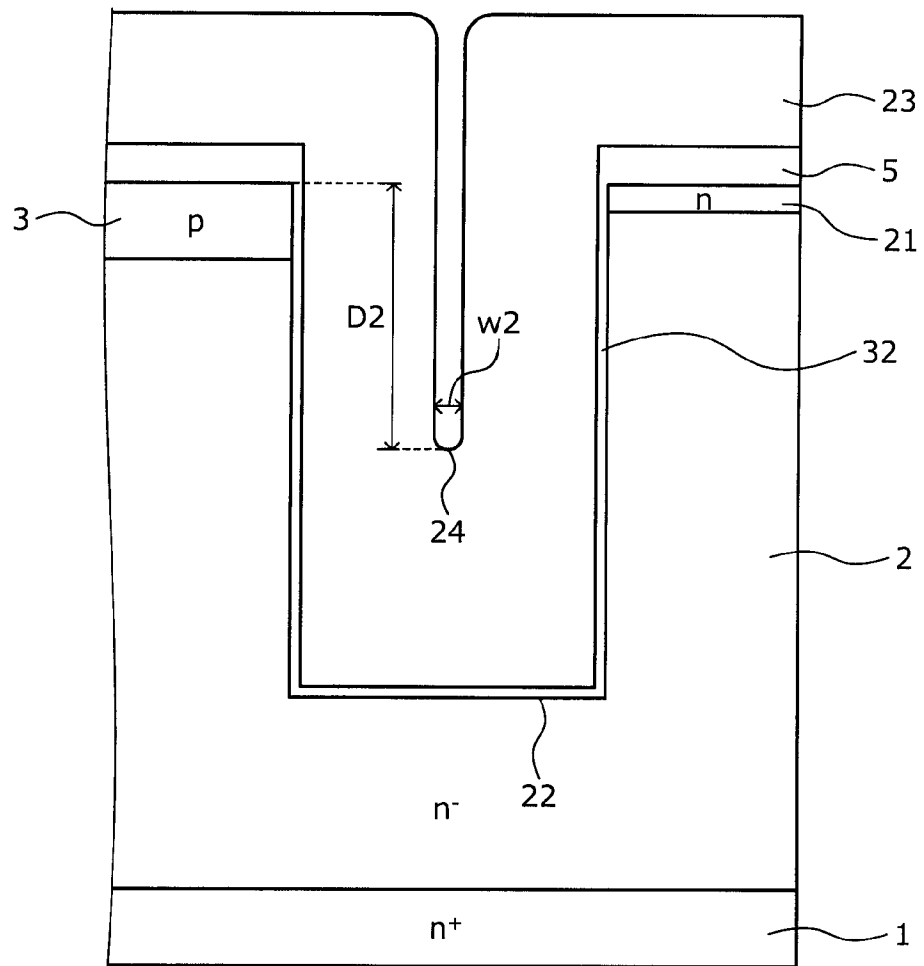
[Fig. 4]



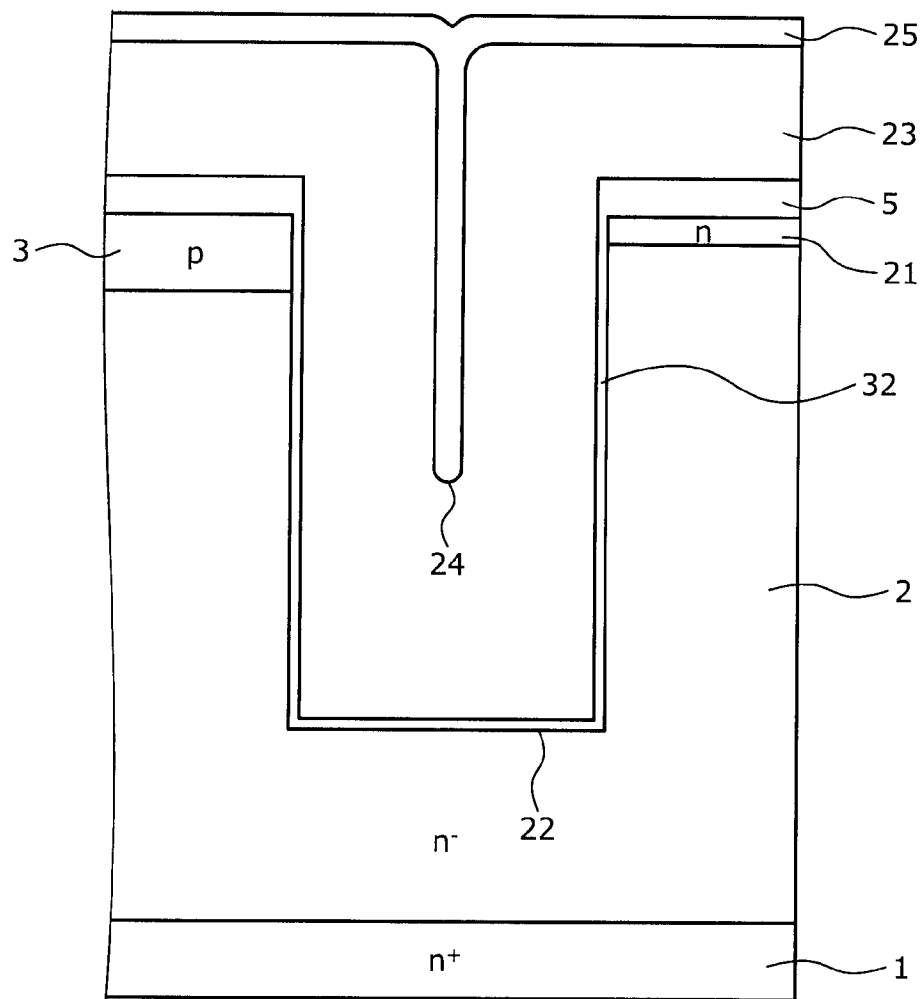
[Fig. 5]



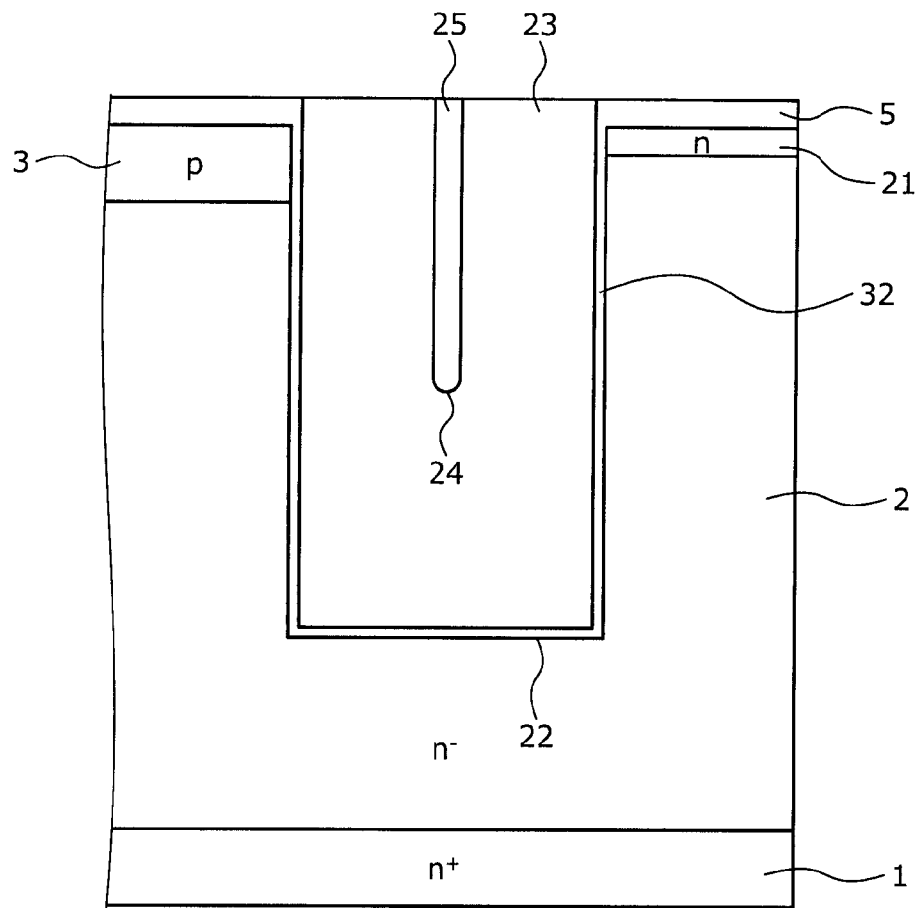
[Fig. 6]



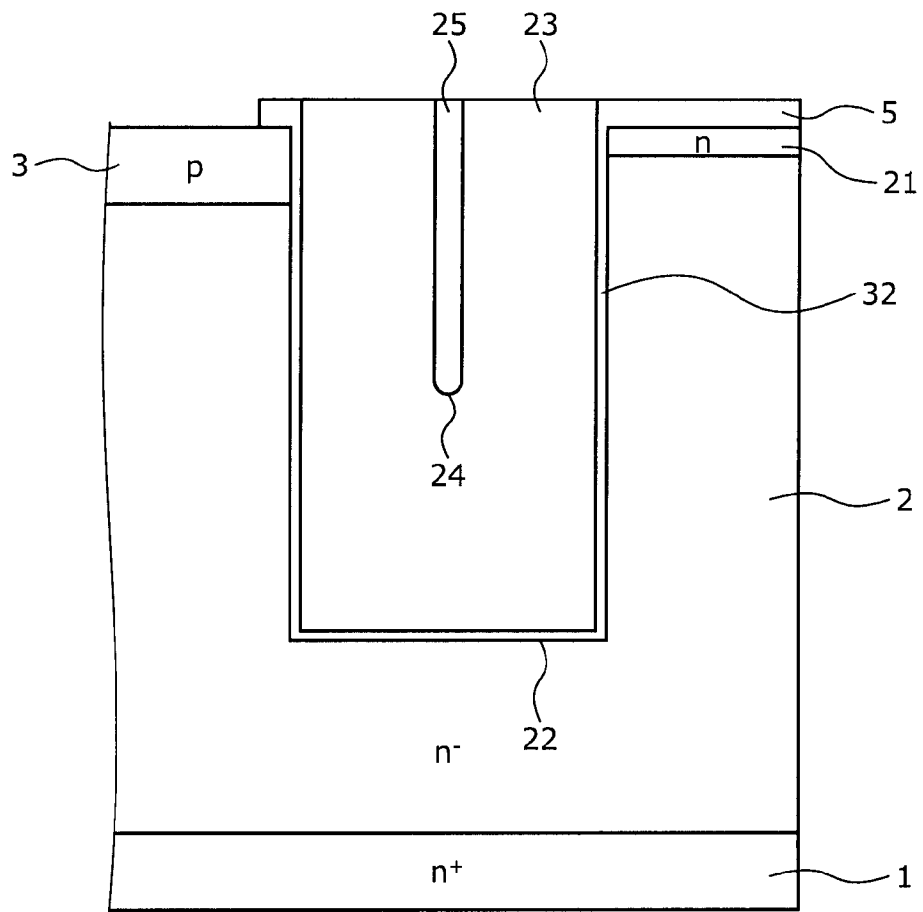
[Fig. 7]



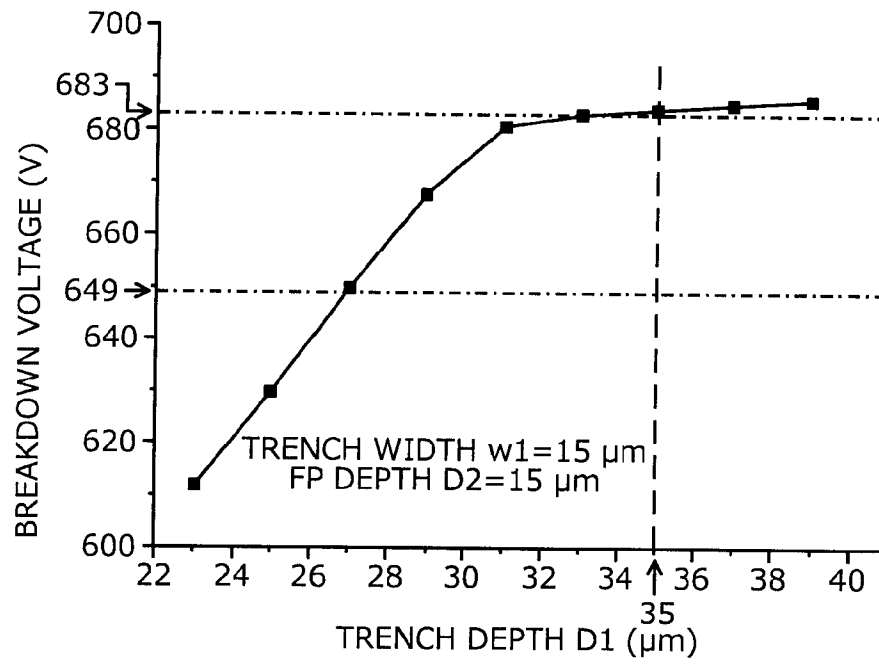
[Fig. 8]



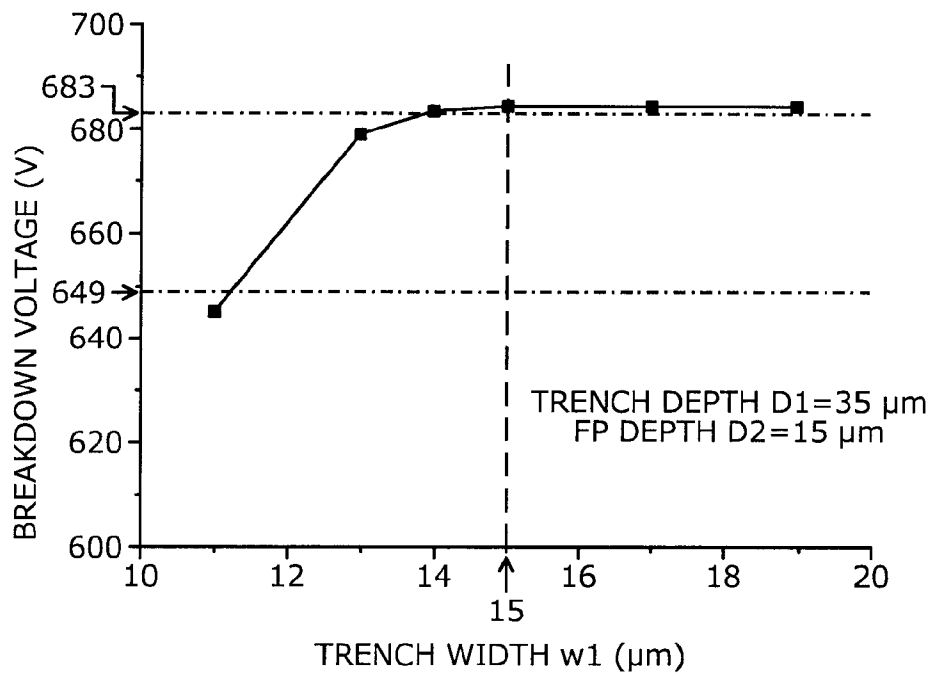
[Fig. 9]



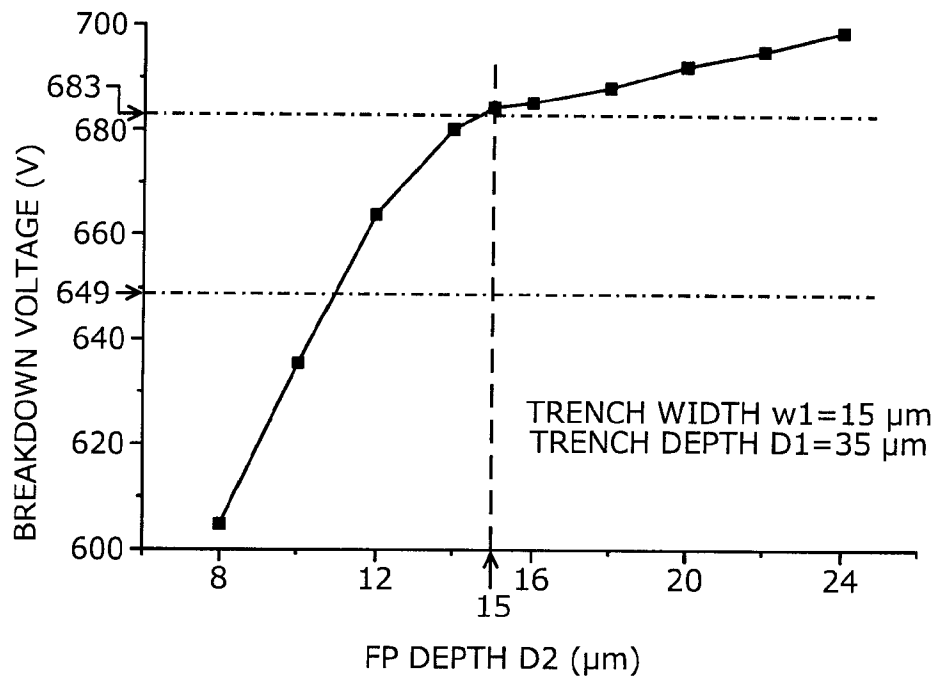
[Fig. 10]



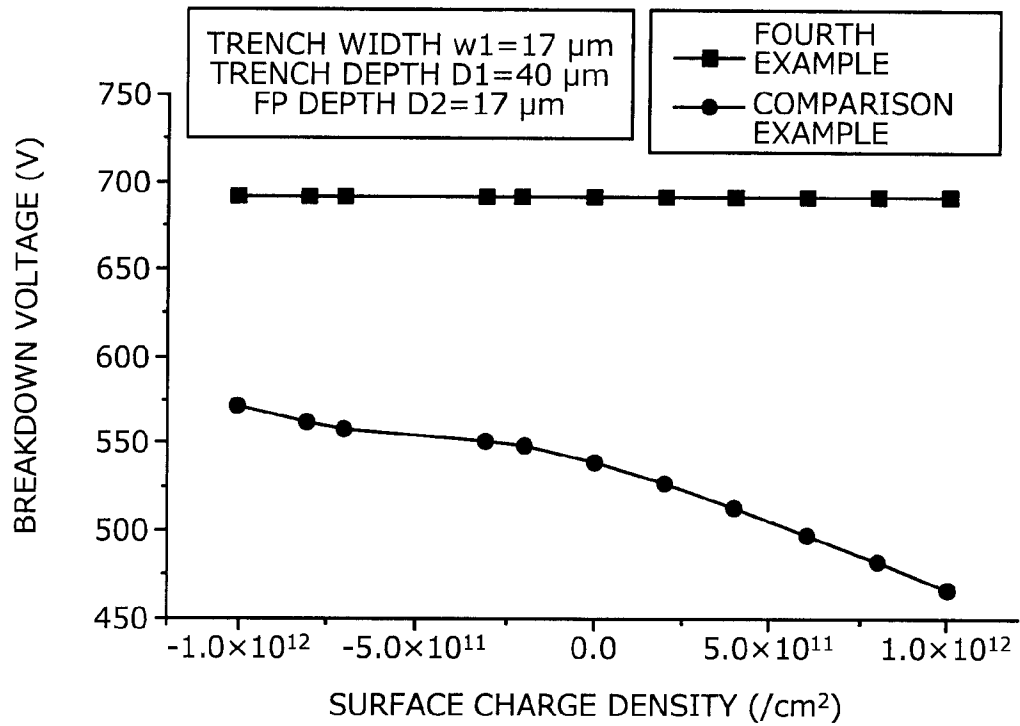
[Fig. 11]



[Fig. 12]



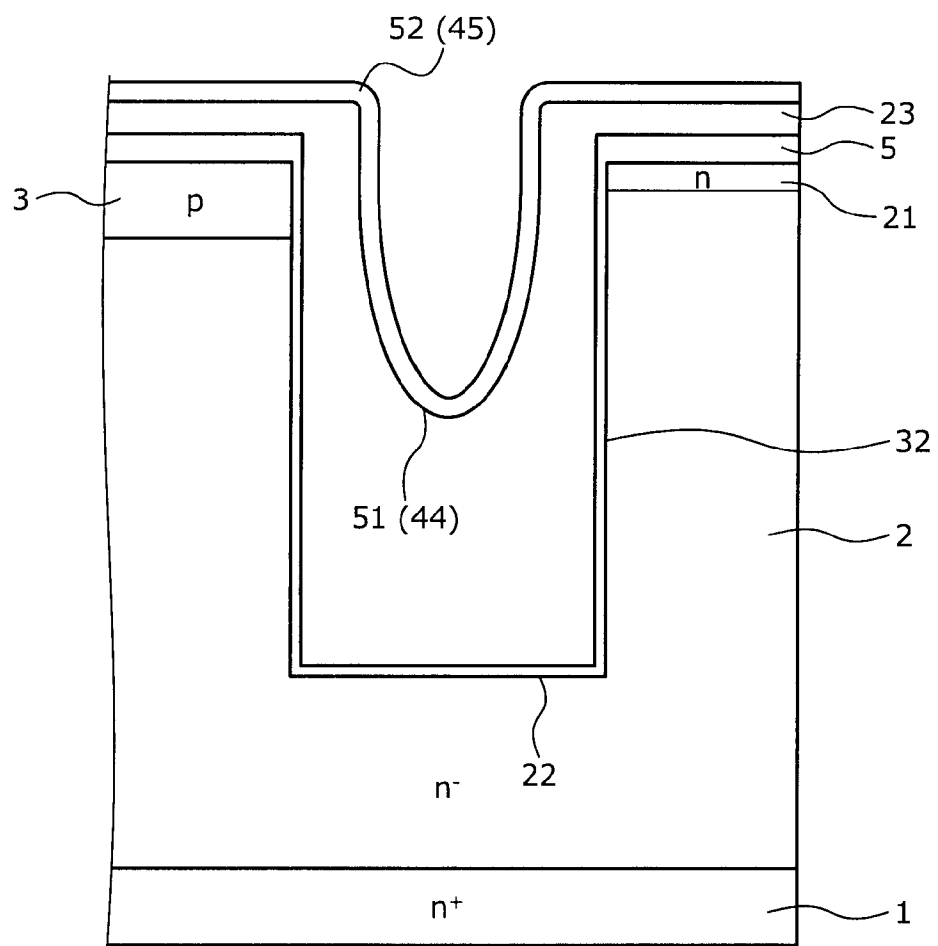
[Fig. 13]



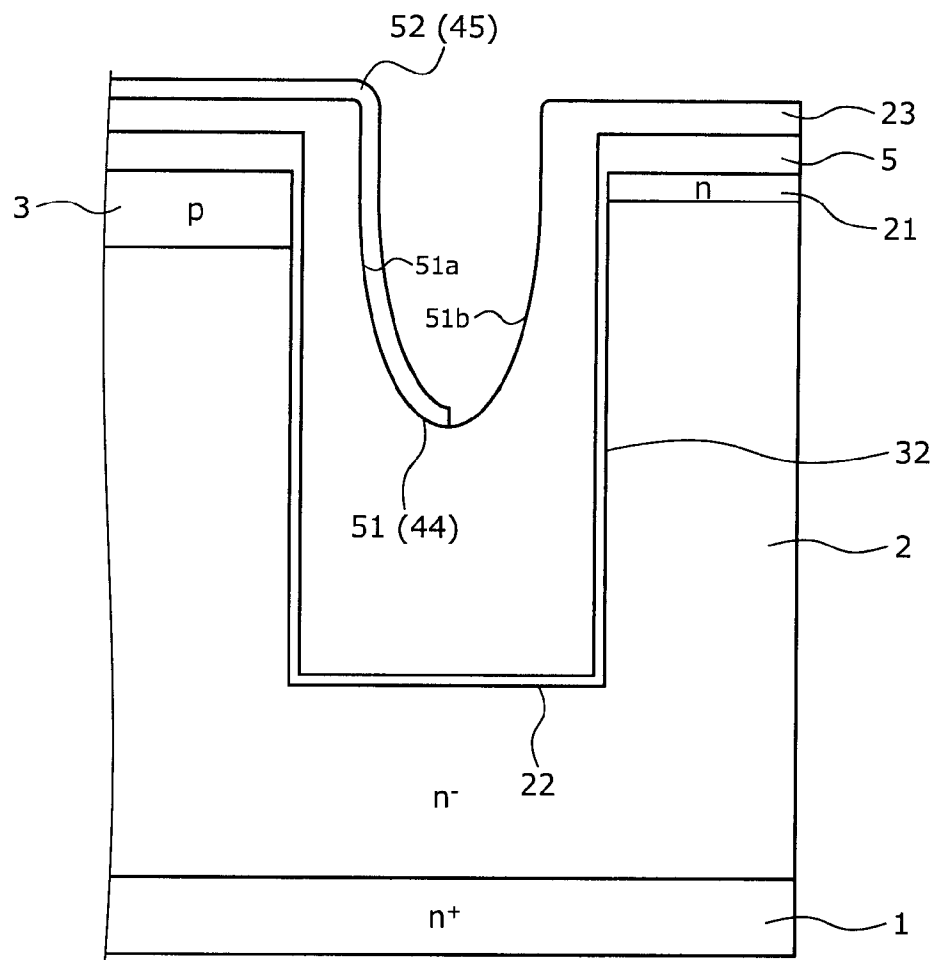
[illegible]

A cross-sectional view of a semiconductor device. The structure consists of several layers and regions. On the left, a p-type region (3) is on top of an n⁻ region (20). A layer (4) is on top of the p-type region. To the right of the p-type region is a vertical layer (22). Further right is a curved layer (44a, 44b, 44c, 44d) that meets a vertical dashed line. To the right of this curved layer is a large n⁻ region (2). Above the n⁻ region (2) is a thin n-type layer (5) and a layer (21). A layer (23) is on top of the n⁻ region (2). A layer (32) is at the bottom of the n⁻ region (2). An angle $\theta 1$ is indicated between a horizontal dashed line and the curved layer (44c).

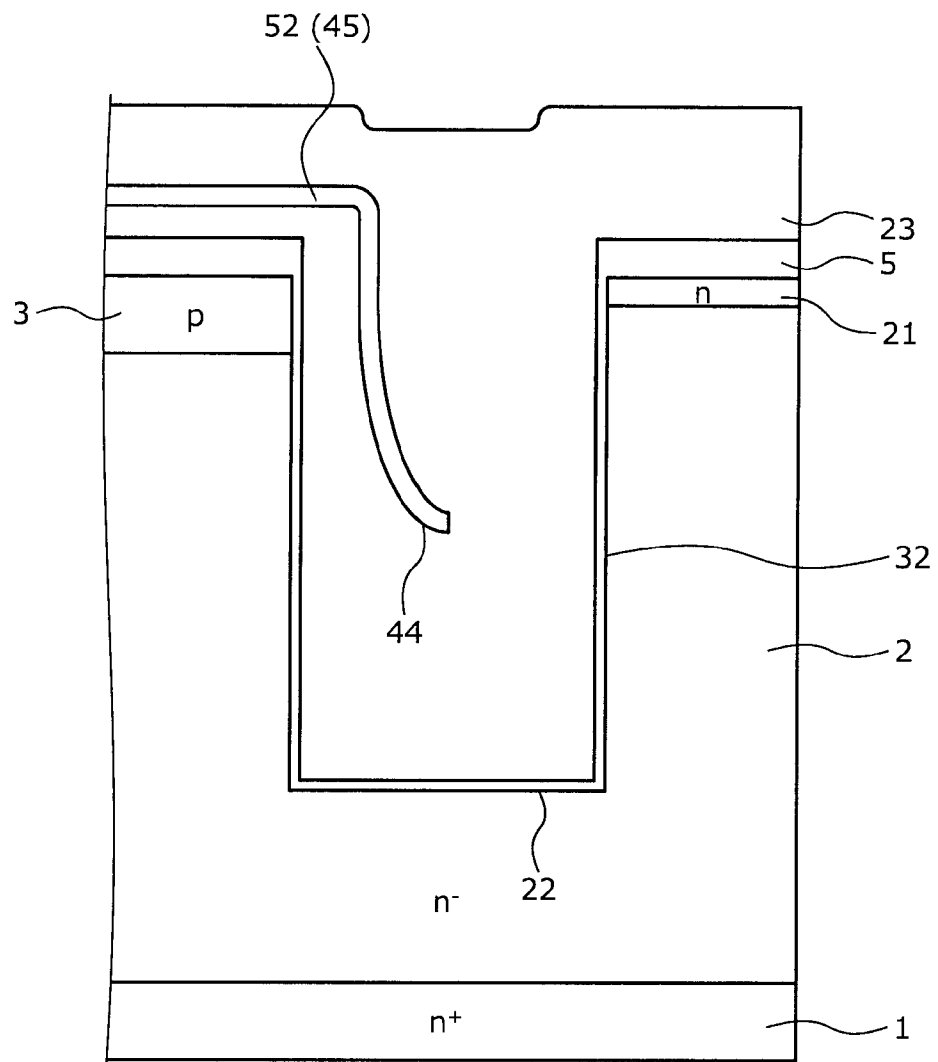
[Fig. 16]



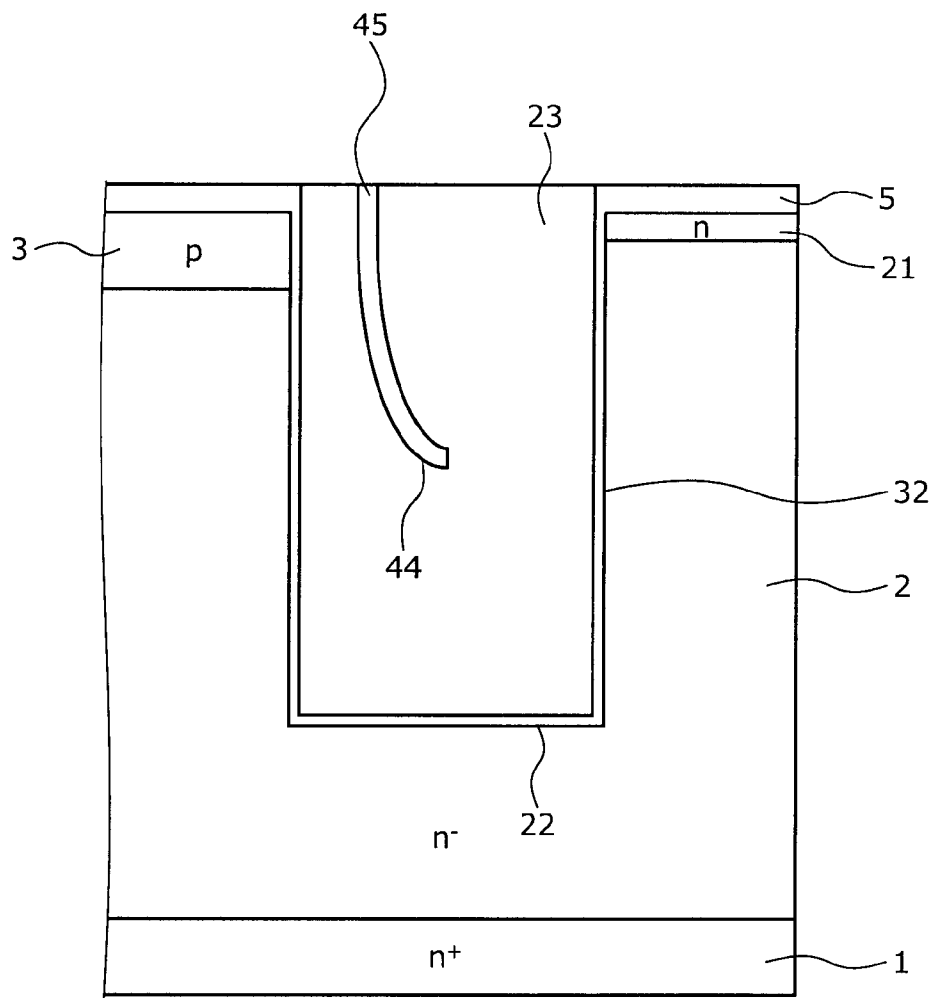
[Fig. 17]



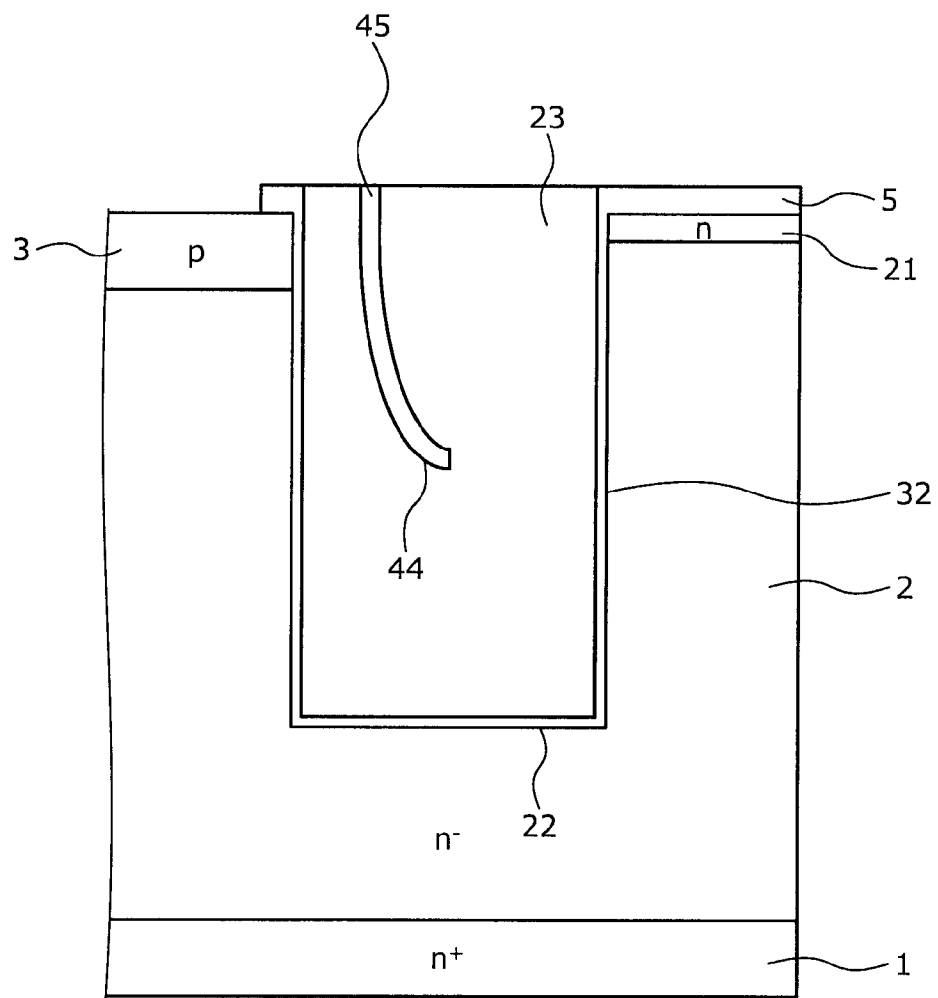
[Fig. 18]



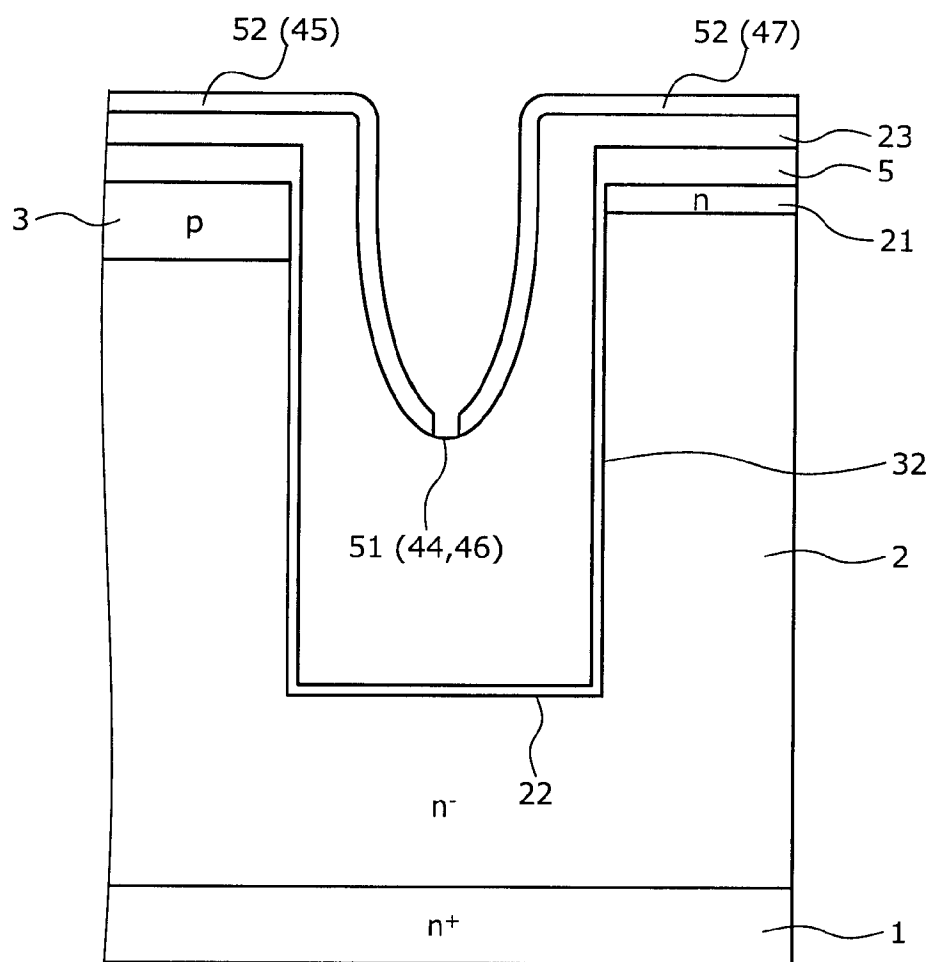
[Fig. 19]



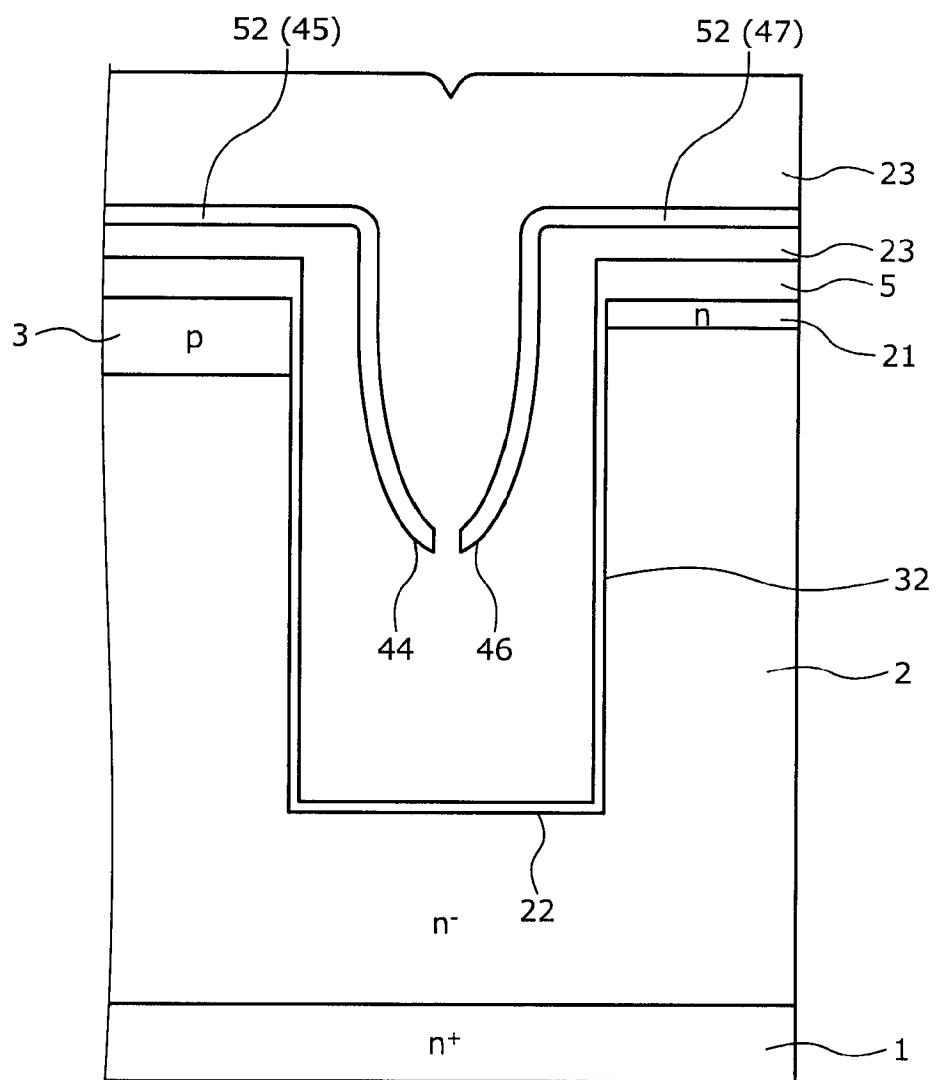
[Fig. 20]



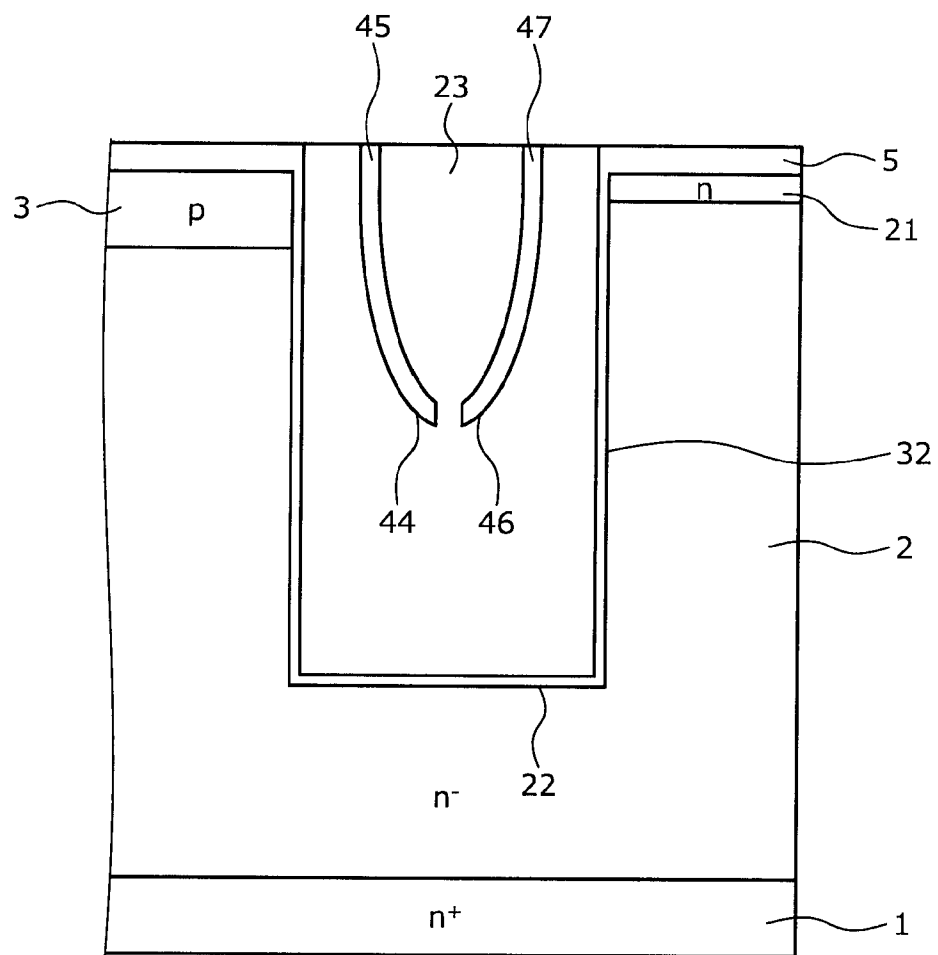
[Fig. 22]



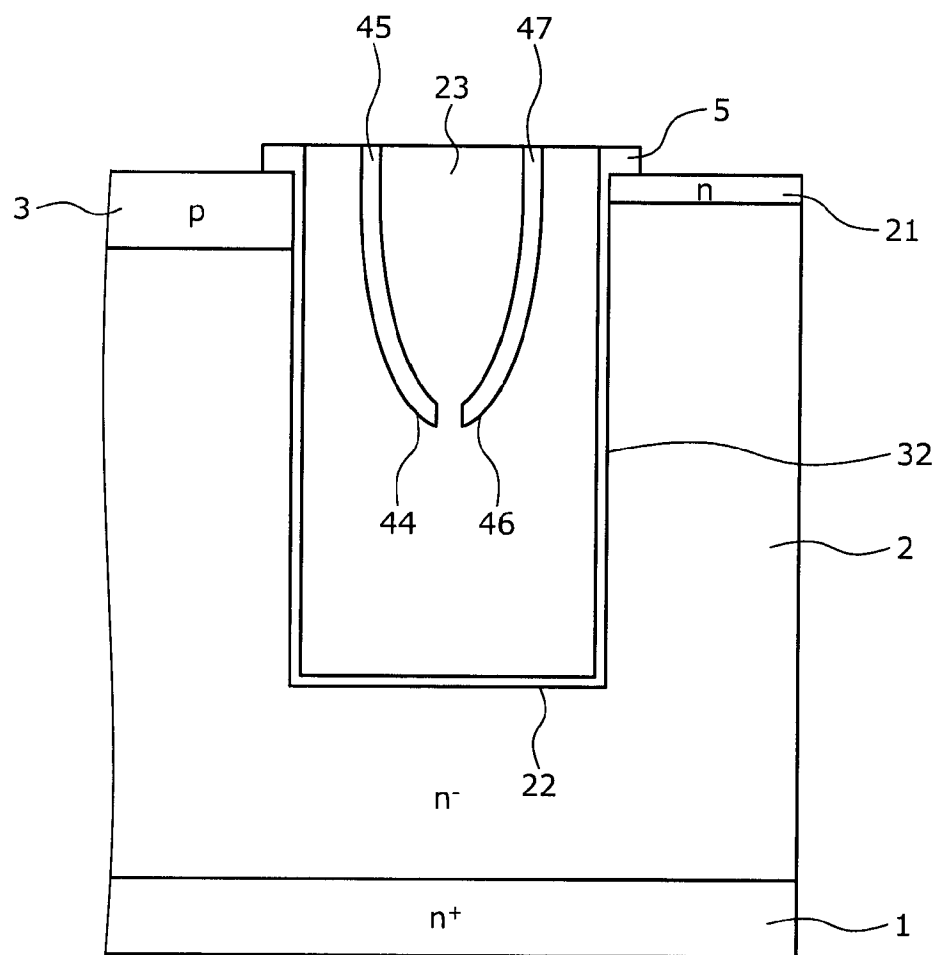
[Fig. 23]



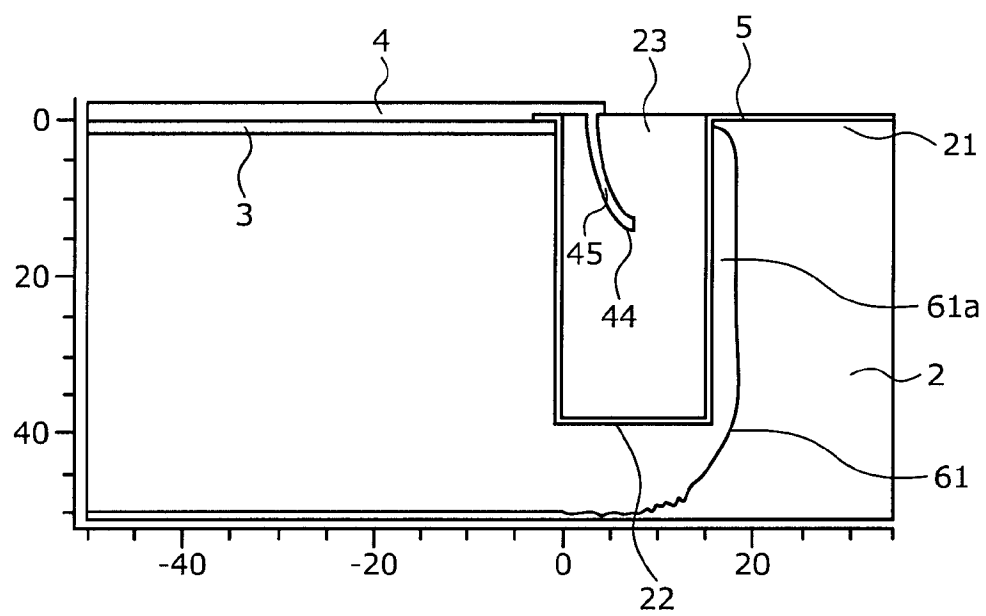
[Fig. 24]



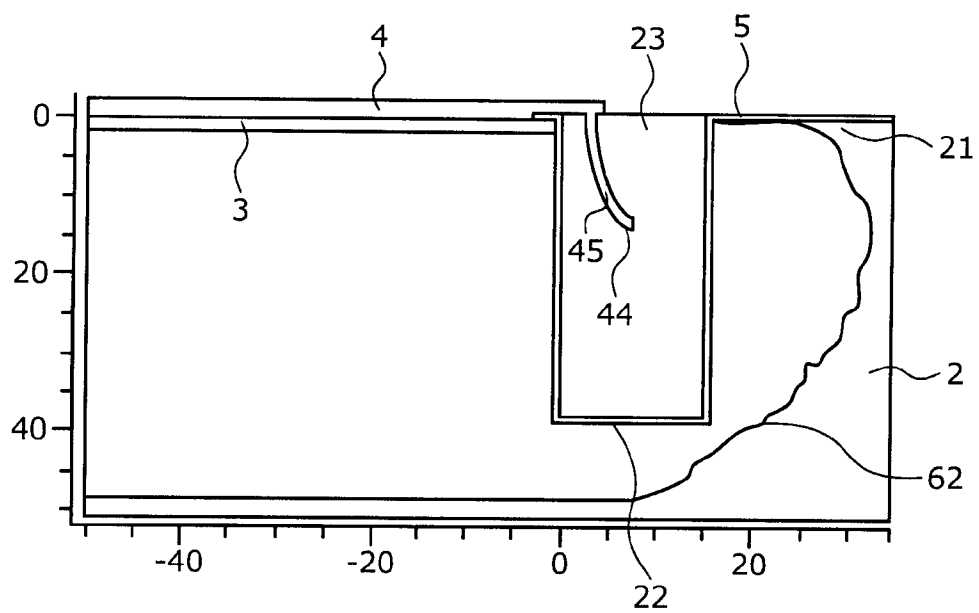
[Fig. 25]



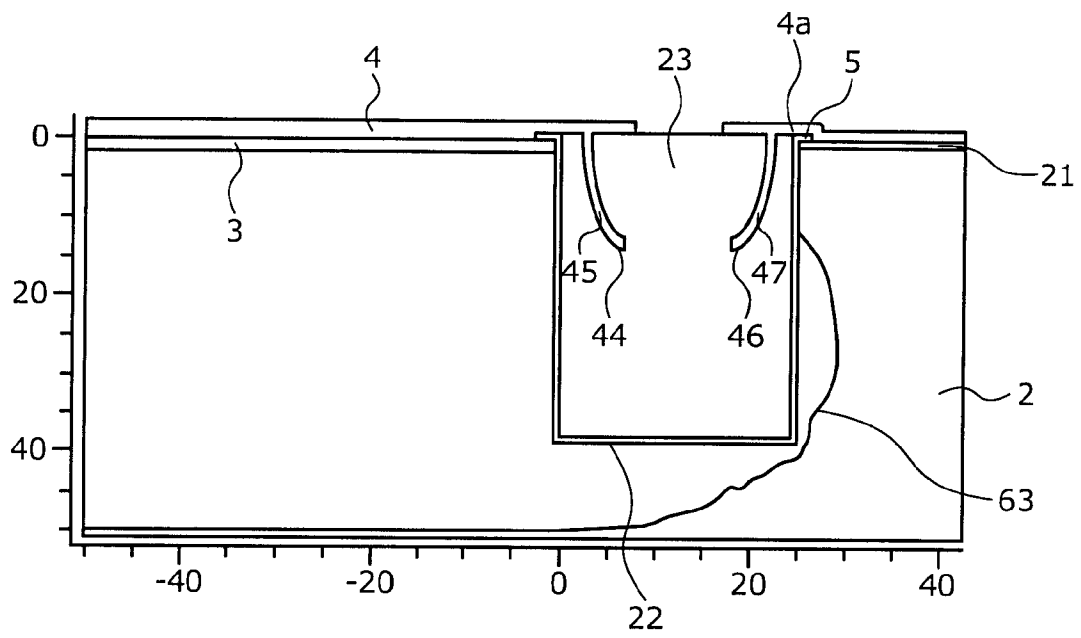
[Fig. 26]



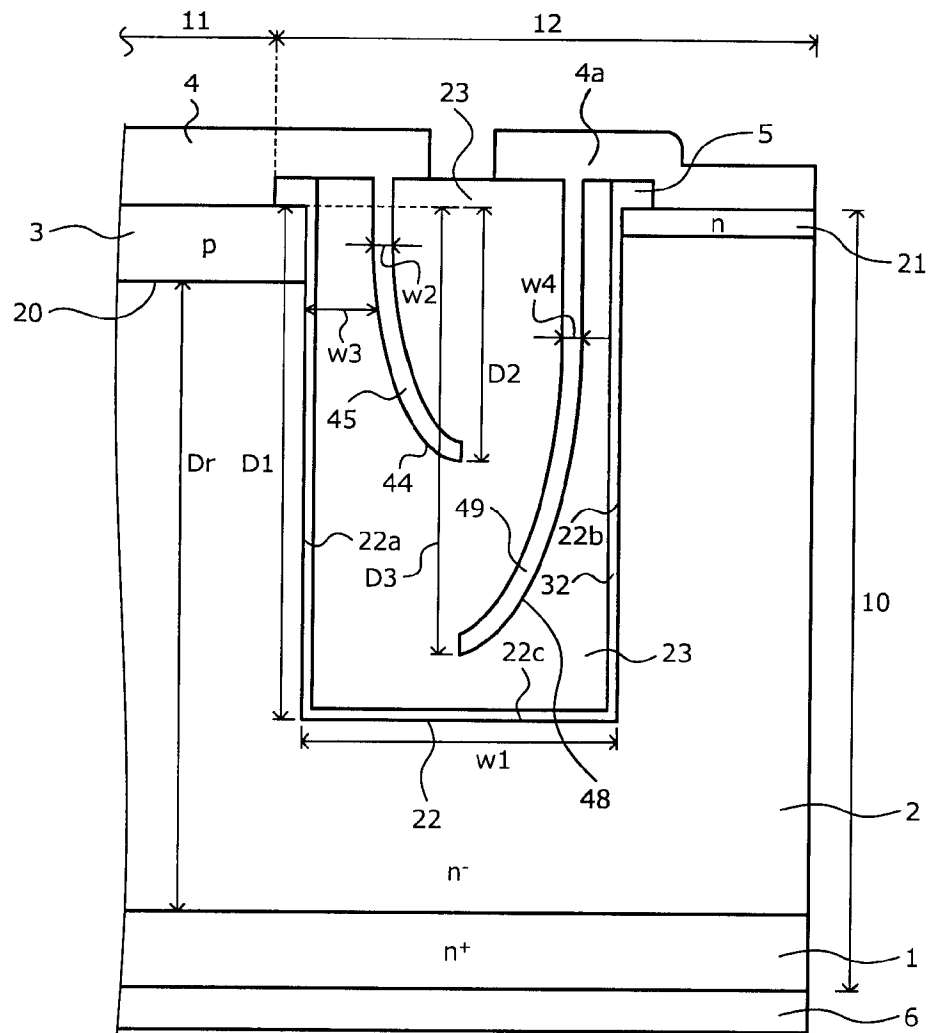
[Fig. 27]



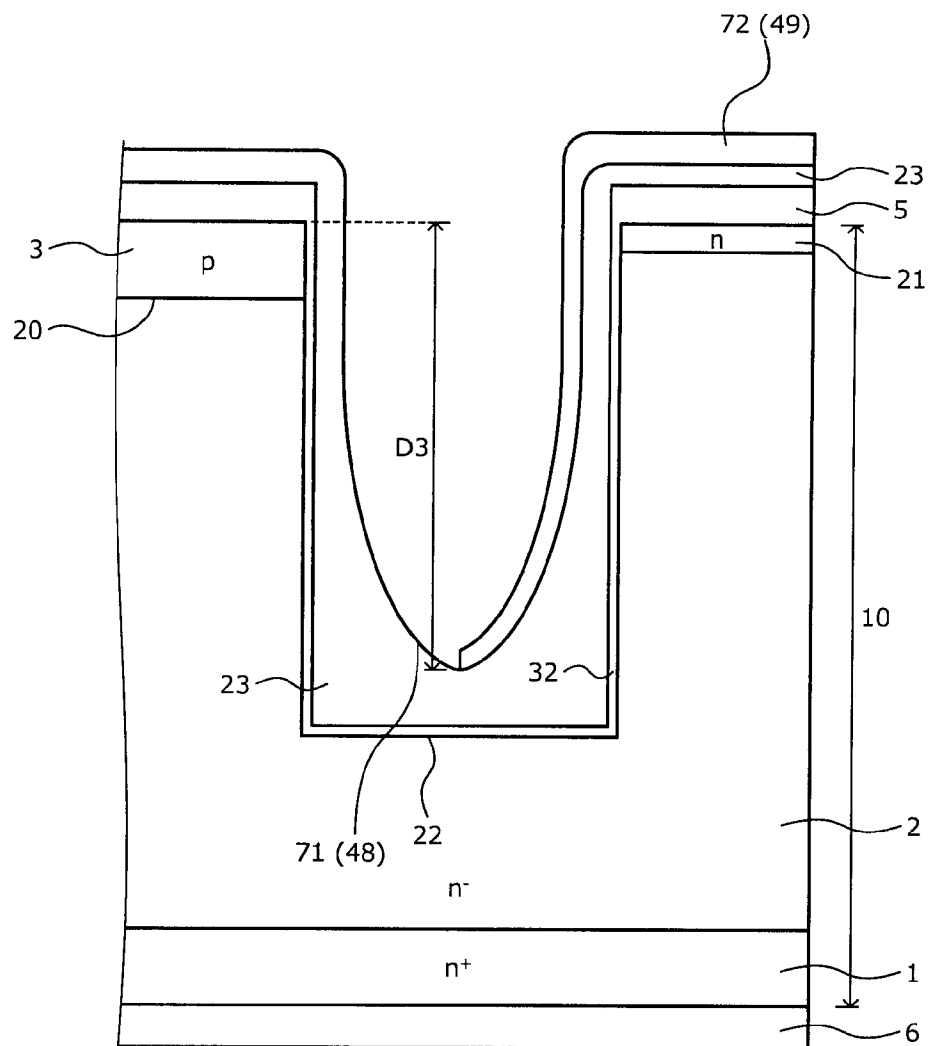
[Fig. 28]



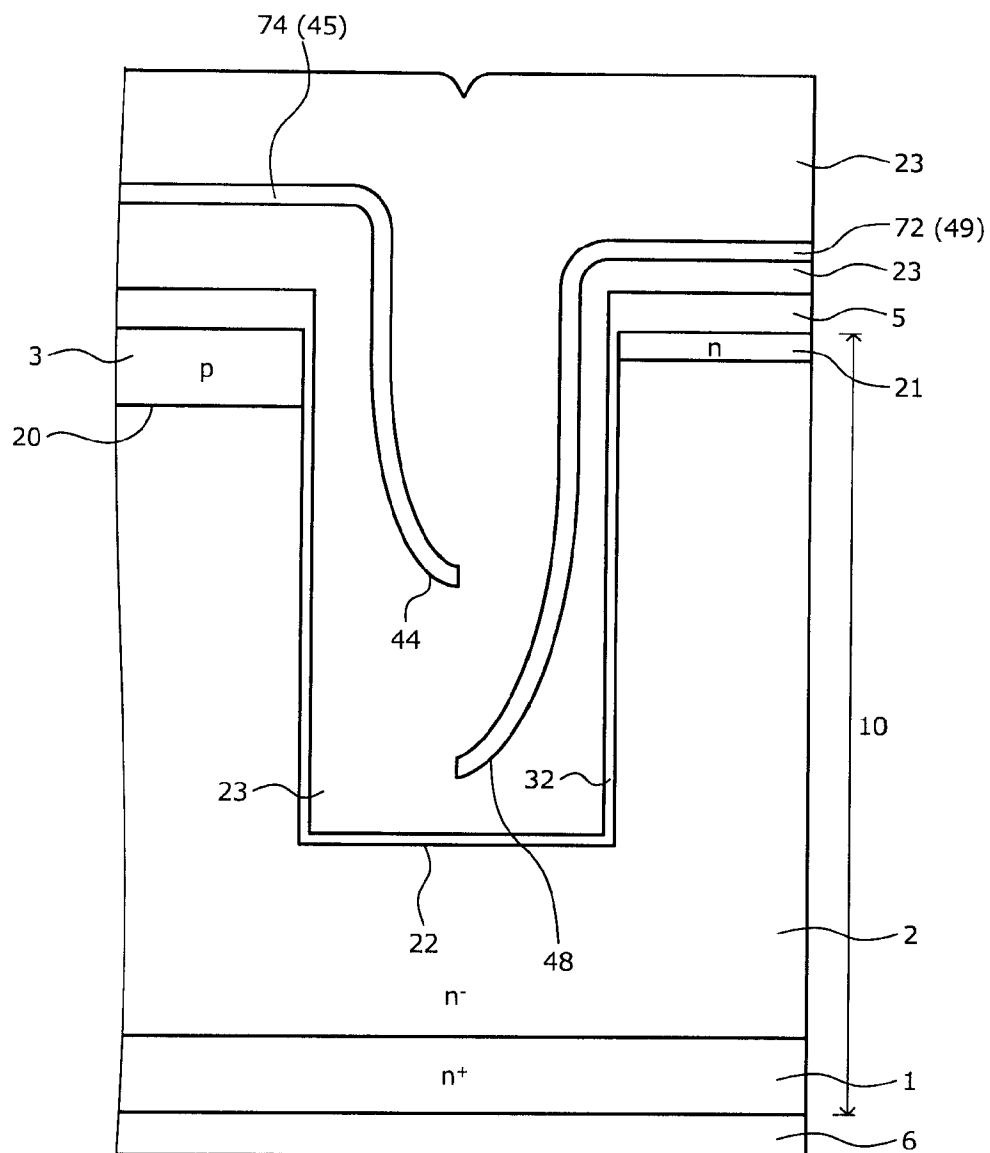
[Fig. 29]



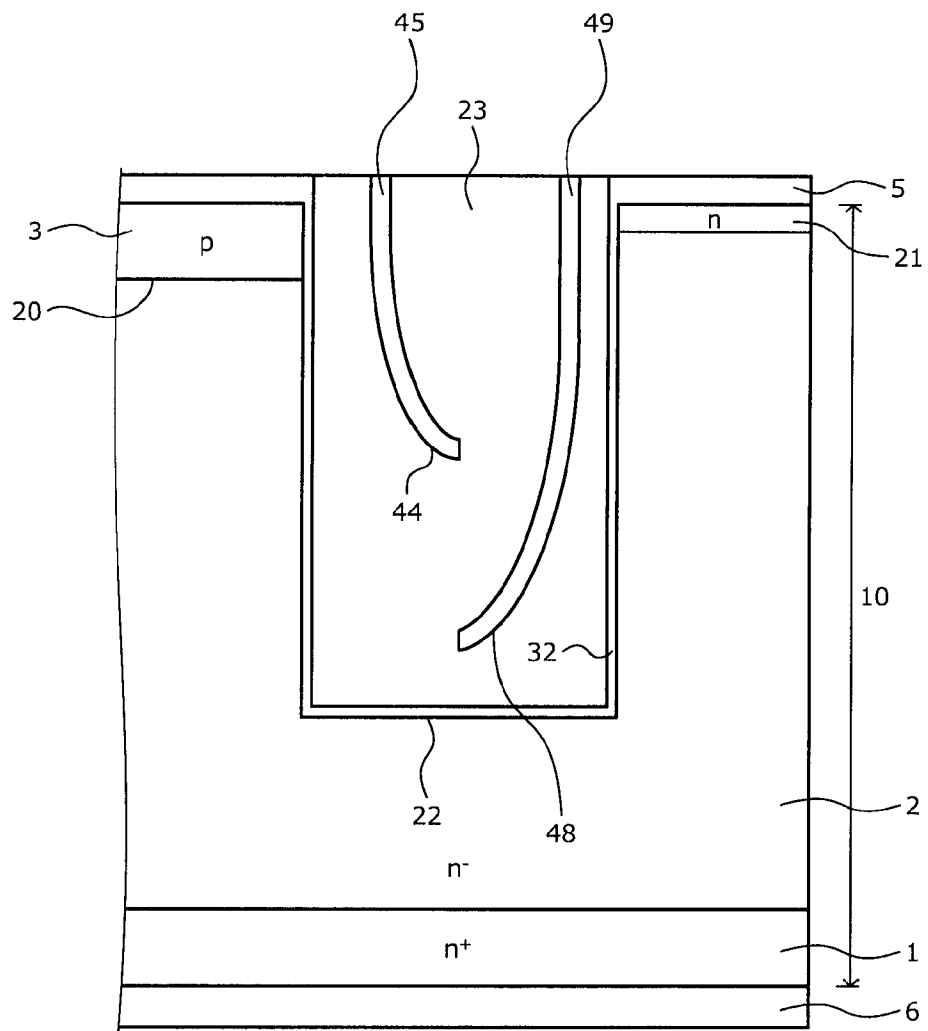
[Fig. 30]



[Fig. 32]



[Fig. 33]



[illegible]

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2016/001056

A. CLASSIFICATION OF SUBJECT MATTER Int.Cl. H01L29/06 (2006.01) i, H01L29/78 (2006.01) i According to International Patent Classification (IPC) or to both national classification and IPC				
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) Int.Cl. H01L29/06, H01L29/78 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Published examined utility model applications of Japan 1922-1996 Published unexamined utility model applications of Japan 1971-2016 Registered utility model specifications of Japan 1996-2016 Published registered utility model applications of Japan 1994-2016 Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)				
C. DOCUMENTS CONSIDERED TO BE RELEVANT				
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
Y A	US 2005/0167749 A1 (DONALD RAY DISNEY) 2005.08.04, paragraphs 0055-0086, figures 5, 7-9 & JP 2006-216927 A & US 2003/0047768 A1 & EP 1689001 A2	1, 4, 5, 9-12 2, 3, 6-8, 13		
Y A	JP 2006-120807 A (FUJI ELECTRONICS HOLDINGS, INC.) 2006.05.11, paragraphs 0009-0013, figures 1, 2 (No Family)	1, 4, 5, 9-12 2, 3, 6-8, 13		
Y A	US 8872257 B1 (KABUSHIKI KAISHA TOSHIBA) 2014.09.28, column 6 line 40 - column 7 line 3, figure 5 & JP 2014-229705 A & US 2015/0008510 A1 & US 2015/0318392 A1	9, 10 2, 3, 6-8, 13		
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.				
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