



- (51) **International Patent Classification:**
G06F 13/16 (2006.01) *G06F 12/08* (2006.01)
- (21) **International Application Number:**
PCT/US2014/042513
- (22) **International Filing Date:**
16 June 2014 (16.06.2014)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (71) **Applicant:** HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. [US/US]; 11445 Compaq Center Drive W., Houston, Texas 77070 (US).
- (72) **Inventors:** RAMAKRISHNAN, Senthil Kumar; 11311 Chinden Blvd., Boise, Idaho 83714 (US). COHEN, Eugene; 11311 Chinden Blvd., Boise, Idaho 83714 (US).
- (74) **Agents:** HARTMANN II, Kenneth R et al.; Intellectual Property Administration, 3404 E. Harmony Road Mail Stop 35, Fort Collins, Colorado 80528 (US).
- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,

DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to the identity of the inventor (Rule 4.17(i))

Published:

— with international search report (Art. 21(3))

(54) **Title:** CACHE COHERENCY FOR DIRECT MEMORY ACCESS OPERATIONS

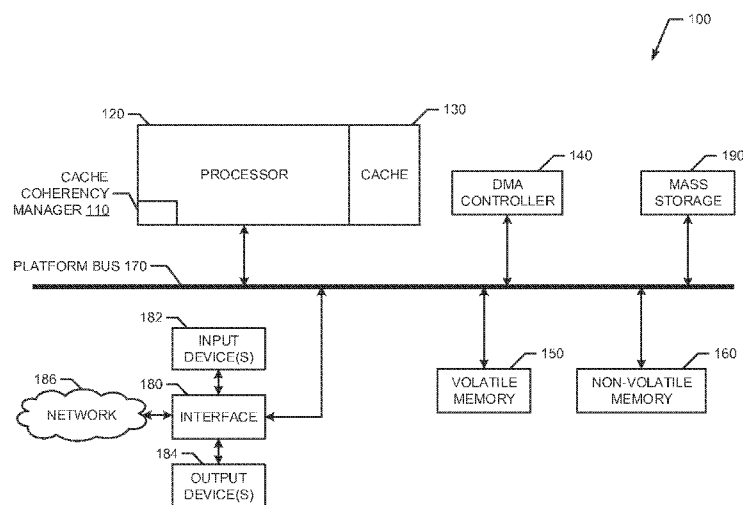


FIG. 1

(57) **Abstract:** Methods, apparatus, systems and articles of manufacture are disclosed to maintain cache coherency. Examples disclosed herein involve, in response to receiving, from a direct memory access controller, an interrupt associated with a direct memory access operation, handling the interrupt based on a parameter of the direct memory access operation, wherein the direct memory access controller is to execute the direct memory access operation.

Cache Coherency for Direct Memory Access Operations

BACKGROUND

[0001] Processing systems, also known as processor platforms, commonly include a processor or central processing unit (CPU), a memory (e.g. a volatile memory, a non-volatile memory, a main memory, a mass storage device, etc.), and a cache among many other system components and/or hardware (e.g. interface cards, input/output (I/O) devices or peripherals, etc.). The CPU and the cache may be collocated on a same semiconductor chip or device. The CPU may locally store data from the memory into the cache.

[0002] Direct memory access (DMA) is a feature of processing systems found in many computing devices (e.g., personal computers, tablet computers, mobile devices, etc.). DMA operations allow certain hardware components (e.g., DMA controllers), interface cards, peripherals, etc. of a processing system to access a memory of the processing system independently of the CPU. The CPU may initiate a DMA operation, and a DMA controller executes the DMA operation, while the CPU continues other operations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 is a block diagram of an example processor platform including an example cache coherency manager implemented in accordance with the teachings of this disclosure.

[0004] FIG. 2A illustrates an example software layer diagram representative of software layers of a processor of the processor platform of FIG. 1 including the cache coherency manager in a driver software layer of the processor.

[0005] FIG. 2B illustrates another example software layer diagram representative of software layers of another processor of the processor platform of FIG. 1 including the cache coherency manager in a firmware layer of the processor.

[0006] FIG. 3 is a block diagram of an example cache coherency manager constructed in accordance with the teachings of this disclosure.

[0007] FIG. 4 illustrates a flow diagram of example events and example messages in the processor platform of FIG. 1 to handle a direct memory access operation requested by an application/driver module in accordance with the teachings of this disclosure.

[0008] FIG. 5 illustrates a flow diagram of example events and example messages in the processor platform of FIG. 1 to handle a direct memory access operation identified by a direct memory access controller in accordance with the teachings of this disclosure.

[0009] FIG. 6 is a flowchart representative of example machine readable instructions that may be executed to implement the cache coherency manager of FIG. 1.

[0010] FIG. 7 is a flowchart representative of example machine readable instructions that may be executed to implement a portion of the example machine readable instructions of FIG. 6 to implement the cache coherency manager of FIG. 1.

[0011] FIG. 8 is a flowchart representative of an example process and/or machine readable instructions executed by a direct memory access controller associated with the cache coherency manager of FIG. 1.

DETAILED DESCRIPTION

[0012] Example methods, systems, and articles of manufacture disclosed herein involve maintaining cache coherency across direct memory access (DMA) operations. Examples disclosed herein involve a cache coherency manager to handle an interrupt received from a DMA controller to maintain cache coherency. The cache coherency manager may handle the interrupt by flushing and/or

invalidating a cache of a processor system based on a parameter (e.g., a direction) of the DMA operation.

[0013] In previous techniques, when a DMA operation is set up, a DMA controller receives parameters of the DMA operation. For example, an application setting up the DMA operation may send a source address, a destination address, and a number of bytes of data of the DMA operation to the DMA controller. In these previous techniques, the DMA controller would then begin executing the DMA operation by writing to a hardware register of the DMA controller. Such previous techniques may frequently cause cache coherency issues as locations of memory of the DMA operations (e.g., the destination address) may correspond to data in a cache associated with the memory (i.e., the cache and the memory are components of a processor system). Accordingly, following the DMA operations, the cache data may no longer appropriately match corresponding data in memory, resulting in a lack of cache coherency.

[0014] Cache coherency is desirable in processor systems to prevent errors and/or system failures. For example, if data in a cache does not match or suitably match corresponding data in a memory, processors may access improper versions of data and/or non-existent data. Accordingly, as used herein, maintaining cache coherency refers to a technique to ensure that cache data properly matches corresponding memory data. As used herein, flushing a cache involves writing back data from the cache to a main memory device. As used herein, invalidating a cache and/or a location in a cache involves removing/clearing data from the cache and/or location in the cache, respectively. As used herein, the phrase, "associated with," refers to the presence of a relationship (e.g., communicative, hierarchical, parametric, etc.) between at least two elements or components. As used herein, an interrupt refers to a message, prompt, or other instrument used for communication between components of a system. As used herein, software is computer readable instructions stored on a tangible computer readable medium (e.g., a storage device or storage disc) that are executable by a processor.

[0015] Examples disclosed herein involve, in response to receiving an interrupt associated with a direct memory access operation from a direct memory

access controller, handling the interrupt based on a parameter of the direct memory access operation, wherein the direct memory access controller is to execute the direct memory access operation. An example system disclosed herein includes a hardware direct memory access controller and a software cache coherency manager and/or a cache coherency manager in system firmware to maintain cache coherency. An example method includes determining that a direct memory access operation is to be executed, generating an interrupt corresponding to the direct memory access operation, and sending the interrupt to a cache coherency manager to maintain cache coherency.

[0016] FIG. 1 is a block diagram of an example processor system 100 of a machine including a cache coherency manager 110 implemented in accordance with the teachings of this disclosure. The processor system 100 includes a processor 120, a cache 130, a direct memory access (DMA) controller 140, a volatile memory 150, a non-volatile memory 160, a platform bus 170, an interface circuit 180, and a mass storage device 190. In the illustrated example of FIG. 1, the processor 120 includes the cache coherency manager 110 constructed in accordance with the teachings of this disclosure. The cache coherency manager 110 handles interrupts associated with DMA operations detected and/or received by the DMA controller 140. The cache coherency manager 110 may handle received interrupts to maintain cache coherency by flushing and/or invalidating all or part of a cache depending on at least one parameter (e.g., a direction, an address, etc.) of the DMA operation. Accordingly, the cache coherency manager 110 maintains cache coherency between the cache 130 and at least one of the volatile memory 150 or non-volatile memory 160. In other words, the cache coherency manager 110 ensures that data in the cache 130 suitably matches (e.g., is a corresponding copy of) corresponding data in the volatile memory 150 and/or non-volatile memory 160 (and vice versa). The processor 120 of FIG. 1 may be collocated on a same device (e.g., a same semiconductor chip) as the cache 130.

[0017] The processor 120 of FIG. 1 is hardware that executes software and/or computer readable instructions of the processor system 100. For example, the processor 120 may be implemented by at least one integrated

circuit, logic circuit, microprocessor, or controller from any desired family or manufacturer. More specifically, the processor 120 may be an ARM processor, an x86 processor, an MIPS core processor, or any other type of processor. The processor 120 of FIG. 1 may include a central processing unit (CPU) of the processor system 100 with a hardware processing core, a memory controller, and/or other software, firmware, or hardware components.

[0018] In the illustrated example of FIG. 1, the platform bus 170 facilitates communication between the processor 120, the DMA controller 140, the volatile memory 150, the non-volatile memory 160, the interface circuit 180, and/or the mass storage device 190. The example DMA controller 140 of FIG. 1 is hardware implemented by at least one integrated circuit, logic circuit, microprocessor, or controller from any desired family or manufacturer. In some examples, the DMA controller 140 may be implemented by a plurality of individual DMA controllers with the same or similar capabilities as those disclosed herein in connection with the DMA controller 140. In some examples, the DMA controller 140 may be implemented by DMA controller(s) collocated with peripheral(s) of the processor system 100. For example, each of the input device(s) 182, the output device(s) 184, the interface 180, the mass storage 190, etc. may include a DMA controller similar to the DMA controller 140. For ease of readability, the DMA controller 140 may be used herein to refer to any DMA controller collocated with a peripheral of the processor system 100.

[0019] The example DMA controller 140 of FIG. 1 monitors for (e.g., identifies, detects, etc.) attempted or initiated DMA operations within the processor system 100. For example, the DMA controller 140 may determine (e.g., via a data request) that an application and/or driver module being executed by the processor 120 is initiating a DMA operation. In another example, the DMA controller 140 may determine that the interface circuit 180 and/or the mass storage device 190 is attempting a DMA operation involving the volatile memory 150. In some examples, the DMA controller 140 may be initially setup (e.g., upon startup) for designated DMA operations (e.g., for scatter/gather operations). In some such examples, the DMA controller 140 may monitor for and/or detect

DMA operations based on certain regions of memory targeted by the DMA operations and/or hardware attempting the DMA operations.

[0020] The example DMA controller 140 of FIG. 1 generates interrupts for determined DMA operations and/or sends the interrupts to the cache coherency manager 110. The generated interrupts may include parameters (e.g., a direction, a source address, a destination address, a byte size, etc.) of the DMA operations. Furthermore, the DMA controller 140 of FIG. 1 executes the DMA operations by accessing the memory accordingly. The DMA controller 140 of FIG. 1 may execute the DMA operations before and/or after the cache coherency manager 110 maintains cache coherency in accordance with the teachings of this disclosure.

[0021] In examples disclosed herein, the DMA controller 140 of FIG. 1 may send the interrupt to the cache coherency manager 110 before and/or after executing the DMA operation. The example interrupt may be a trigger message to indicate that the DMA operation is to be executed in the processor system 100. In some examples where the processor 120 supports multiple interrupt lines, a specific interrupt line may be designated for interrupts sent between the DMA controller 140 and the cache coherency manager 110. In examples in which the processor 120 does not support multiple interrupt lines, the DMA controller 140 may demultiplex interrupt parameters (e.g., source/destination addresses, direction, size, etc.) to a designated location (e.g., a set of register locations of the DMA controller 140 and/or a memory location the volatile memory 150 and/or non-volatile memory 160).

[0022] Timing for when the DMA controller 140 in the example of FIG. 1 sends an interrupt to the cache coherency manager 110 may depend on a parameter (e.g., a direction, a size, an address, etc.) of the DMA operation. For example, if the DMA operation (e.g., a read) is from a memory (e.g., the volatile memory 150 or the non-volatile memory 160) to a peripheral (e.g., the interface circuit 180, the storage device 190, an application/driver module being executed by the processor 120, etc.) the interrupt may be sent to the cache coherency manager 110 so that the cache coherency manager 110 may flush a cache (e.g., the cache 130) associated with the memory. As another example, if the DMA

operation is from a peripheral to a memory, the DMA controller 140 may send the interrupt after the DMA controller 140 executes the DMA operations so that the cache coherency manager 110 may invalidate a cache associated with the memory or a cache location corresponding to a memory location of the DMA operation.

[0023] The example cache 130 is a local storage circuit that may be collocated on a same device (e.g., a semiconductor chip) as the example processor 120. In the illustrated example of FIG. 1, the processor 120 can perform faster read and/or write operations when accessing data in the cache 130 than when accessing data in the volatile memory 150 and/or in the non-volatile memory 160 via the platform bus 170. Accordingly, the processor 120 may load data from the volatile memory 150 and/or the non-volatile memory 160 into the cache 130 so that the processor 120 can access the data relatively faster using the cache 130. When data is modified in the cache 130, write back operations are used to perform the same modifications on the corresponding data in the volatile memory 150 and/or the non-volatile memory 160 so that the data in the cache 130 and corresponding data in the volatile memory 150 or corresponding data in the non-volatile memory 160 are the same or similar. Without such write back operations, errors or system failures may occur as the storage devices 150 and 160 would not have an accurate and/or current version of the most recent data updated in the cache 130. Because DMA operations may involve data in the cache 130, the cache coherency manager 110 handles interrupts associated with DMA operations to ensure that data in the cache 130 is valid to avoid such errors and/or system failures.

[0024] The example volatile memory 150 of FIG. 1 is any volatile memory storage device that stores data when powered, but loses memory state when power is removed. For example, the volatile memory 150 may be implemented by Synchronous Dynamic Random Access Memory (SDRAM), Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), RAMBUS Dynamic Random Access Memory (RDRAM) and/or any other type of volatile memory. The non-volatile memory 160 is any non-volatile memory storage

device (e.g., phase-change memory, memristor memory, etc.) that is capable of storing data when powered and when not powered.

[0025] The interface circuit 180 of FIG. 1 may be implemented by any type of interface standard, such as an Ethernet interface, a universal serial bus (USB), a Peripheral Component Interconnect (PCI) express interface, etc. The example interface circuit 180 may include an advance extensible interface (AXI) controller, a PCI controller, a PCIe controller, an Infiniband, etc. to facilitate a bridge to the platform bus 170 from any peripheral of the processor system 100. In the illustrated example, at least one input device 182 is connected to the interface circuit 180. The input device(s) 182 permit(s) a user to enter data and commands into the processor core 130. The input device(s) 182 can be implemented by, for example, an audio sensor, a microphone, a camera (still or video), a keyboard, a button, a mouse, a touchscreen, a track-pad, a trackball, isopoint and/or a voice recognition system. At least one output device 184 is also connected to the interface circuit 180 of the illustrated example of FIG. 1. The output devices 184 can be implemented, for example, by display devices (e.g., a light emitting diode (LED), an organic light emitting diode (OLED), a liquid crystal display, a cathode ray tube display (CRT), a touchscreen, a tactile output device, a light emitting diode (LED), a printer and/or speakers). The interface circuit 180 of the illustrated example, thus, typically includes a graphics driver card, a graphics driver chip or a graphics driver processor. In some examples, at least one of the interface circuit 180, the input device(s), or the output device(s) 184 may include a DMA controller (e.g., the DMA controller 140).

[0026] The interface circuit 180 of the illustrated example also includes a communication device such as a transmitter, a receiver, a transceiver, a modem and/or network interface card to facilitate exchange of data with external machines (e.g., computing devices of any kind) via a network 186 (e.g., an Ethernet connection, a digital subscriber line (DSL), a telephone line, coaxial cable, a cellular telephone system, etc.). Accordingly, the interface circuit 180 may facilitate communication with the network 186. As such, the interface circuit 180 may initiate DMA operations involving the volatile memory 150 and/or the

non-volatile memory 160 from at least one of the input device(s) 182, the output device(s) 184, or the network 186.

[0027] The processor system 100 in the illustrated example of FIG. 1 also includes at least one mass storage device 190 for storing software and/or data. Examples of such mass storage devices 190 include floppy disk drives, hard drive disks, compact disk drives, Blu-ray disk drives, RAID systems, and digital versatile disk (DVD) drives. In some examples, the mass storage devices 190 may be implemented using the non-volatile memory 150. In some examples, the mass storage device 190 may include a DMA controller (e.g., the DMA controller 140).

[0028] The processor system 100 of FIG. 1 may be, for example, a server, a personal computer, a mobile device (e.g., a cell phone, a smart phone, a tablet such as an iPad™), a personal digital assistant (PDA), an Internet appliance, a DVD player, a CD player, a digital video recorder, a Blu-ray player, a gaming console, a personal video recorder, a set top box, or any other type of computing device.

[0029] As mentioned above, the processor 120 of FIG. 1 includes the cache coherency manager 110. In some examples, the cache coherency manager 110 is implemented by a program and/or software (e.g., computer readable instructions) executed by the processor 120 and/or implemented by firmware of the processor 120. FIGS. 2A and 2B illustrate software layers 200 of the processor 120 comprising the cache coherency manager 110. The software layers 200 of FIGS. 2A and 2B include an application layer 210, a driver layer 220, and a firmware layer 230. In some examples, other layers (e.g. operating system (OS), basic input/output system (BIOS), hardware abstraction layer (HAL), etc.) may be included. The application layer 210 may include application software for programs executed by the processor 120. The driver layer 220 includes driver software for driving and/or managing peripherals (e.g., input/output devices, interface circuits, printers, storage devices etc.) associated with the processor 120 and/or in communication with the processor system 100. The firmware layer 230 may include software stored within the processor 120 for running and/or managing the processor system 100 (e.g., a board/platform

service package (BSP). In the illustrated example of FIG. 2A, the cache coherency manager 110 is located in the driver layer 220. Accordingly, computer readable instructions to implement the cache coherency manager 110 of FIG. 2A may be installed and/or stored as a driver or within driver software in the processor 120. In the illustrated example of FIG. 2B, computer readable instructions to implement the cache coherency manager 110 of FIG. 2B may be installed and stored as firmware (e.g., in the BSP) of the processor 120. In some examples, the cache coherency manager 110 may be implemented by computer readable instructions within and/or across multiple software layers of the processor 120 (e.g., both the driver layer 220 and the firmware layer 230).

[0030] FIG. 3 is a block diagram of an example cache coherency manager 110 that may be used to implement the cache coherency manager 110 of FIGS. 1, 2A, and/or 2B. As previously mentioned, the cache coherency manager 110 handles interrupts from the DMA controller 140 to maintain cache coherency in the processor system 100. In the illustrated example of FIG. 3, the cache coherency manager 110 includes an interrupt manager 310, a cache flusher 320, and a cache invalidator 330. The interrupt manager 310 of FIG. 3 receives interrupts (e.g., messages, prompts, etc.) from the DMA controller 140 of FIG. 1. The example interrupt manager 310 may then analyze the interrupt to identify parameter(s) (e.g., a direction) of a DMA operation that is to be executed by the DMA controller 140. Based on the identified parameter(s) the interrupt manager 310 may then instruct the cache flusher 320 to flush the cache 130 and/or the cache invalidator 330 to invalidate the cache 130. In some examples, when the interrupt manager 310 determines that a direction of a DMA operation is from a memory to a peripheral, the interrupt manager 310 instructs the cache flusher 320 to flush the cache 130. In examples in which the interrupt manager 330 determines that the direction of a DMA operation is from a peripheral to a memory, the interrupt manager 310 instructs the cache invalidator 330 to invalidate the cache 130 and/or a location of the cache 130 corresponding to a memory location of the DMA operation.

[0031] The cache flusher 320 of FIG. 3 flushes the cache 130 by writing back data to corresponding locations in the volatile memory 150 and/or the non-

volatile memory 160. In some examples, after flushing the cache 130, the cache flusher 320 may instruct the cache invalidator 330 to invalidate the cache 130 or portions of the cache 130. Accordingly, when the cache flusher 320 of the cache coherency manager 110 flushes the cache 130, cache coherency is maintained by ensuring that the most updated data is in the volatile memory 150 and/or the non-volatile memory 160 before performing a DMA operation (e.g., a DMA operation from a memory to a peripheral).

[0032] The cache invalidator 330 of FIG. 3 invalidates the cache 130 by clearing data from the cache 130. In some examples, the cache invalidator 330 only clears a portion of the cache 130. For example, the cache invalidator 330 may identify a cache location corresponding to a memory location of a DMA operation (e.g., a location corresponding to an address identified by the interrupt manager 310), and clears the data from the cache location. Accordingly, when the cache invalidator 330 clears the data from the cache 130, cache coherency is maintained by removing data that is not up to date with the volatile memory 150 and/or the non-volatile memory 160 before and/or after performing a DMA operation (e.g., a DMA operation from a peripheral to a memory). Furthermore, if the processor 120 is to access data from the memory location of the DMA operation at a later time, because corresponding data is no longer stored in the cache 130, the processor 120 may load the data from the memory location of the volatile memory 150 and/or non-volatile memory 160, which is the most updated data.

[0033] The cache coherency manager 110 of FIG. 3 may communicate with the DMA controller 140 to indicate that the interrupt has been handled. For example, the interrupt manager 310 may send an interrupt completion message or prompt to the DMA controller 140 indicating the interrupt has been cleared. Accordingly, in some examples, once the interrupt completion message (interrupt cleared message) has been received, the DMA controller 140 may then execute the DMA operation while maintaining cache coherency in the processor system 100.

[0034] While an example manner of implementing the cache coherency manager 110 of FIG. 1 is illustrated in FIG. 3, at least one of the elements,

processes and/or devices illustrated in FIG. 3 may be combined, divided, re-arranged, omitted, eliminated and/or implemented in any other way. Further, the interrupt manager 310, the cache flusher 320, the cache invalidator 330, and/or, more generally, the example cache coherency manager 110 of FIG. 3 may be implemented by hardware (e.g., the processor 120), software, firmware and/or any combination of hardware, software, and/or firmware. Thus, for example, any of the interrupt manager 310, the cache flusher 320, the cache invalidator 330, and/or, more generally, the example cache coherency manager 110 could be implemented by at least one of an analog or digital circuit, a logic circuit, a programmable processor (e.g., the processor 120), an application specific integrated circuit (ASIC), a programmable logic device (PLD), a field programmable logic device (FPLD), and/or a field programmable gate array (FPGA). At least one of the interrupt manager 310, the cache flusher 320, the cache invalidator 330 is/are hereby expressly defined to include a tangible computer readable storage device or storage disk, such as a memory, storing the software and/or firmware. Further still, the example cache coherency manager 110 of FIG. 3 may include at least one element, process, and/or device in addition to, or instead of, those illustrated in FIG. 3, and/or may include more than one of any or all of the illustrated elements, processes and devices.

[0035] FIG. 4 illustrates a flow diagram of events and messages in the processor platform of FIG. 1 to handle a DMA operation requested by an application/driver module in accordance with the teachings of this disclosure. The messages in the illustrated example of FIGS. 4 and 5 are exchanged between a driver module 400, 500, the DMA controller 140 of FIG. 1, and the cache coherency manager 110 of FIG. 1. The events and/or messages in each of the examples of FIGS. 4 and 5 are in chronological order from (1) – (8). In other examples, the events and/or messages may be the same but the order of events and/or messages (1) – (8) may be different (and vice versa).

[0036] In FIG. 4, the example driver module 400 may be a driver module (and/or an application module) being executed by the processor 120 of FIG. 1. At event (1) of FIG. 4, the driver module 400 begins a DMA operation to access data from the memory (e.g., a read). For example, at event (1), the driver

module 400 may attempt a DMA operation without involving the DMA controller 140 or the driver module 400 may send a request to the DMA controller 140. In message (2) of FIG. 4, the DMA controller 140 may detect the DMA operation initiated by the driver module 400 (denoted by an arrow directed toward the driver module 400) and/or may receive a request to setup the DMA operation from the driver module 400 (denoted by an arrow directed toward the DMA controller 140).

[0037] In FIG. 4, in message (3) the DMA controller 140 sends a DMA interrupt to the cache coherency manager 110. At event (4), the cache coherency manager 110 handles the DMA interrupt to maintain cache coherency. Based on the direction of the DMA operation going from the memory to the peripheral (i.e., the driver module 400), the cache coherency manager 110, at event (4), may handle the interrupt by flushing the cache 130. In message (5), the cache coherency manager 110 indicates to the DMA controller 140 that the DMA interrupt has been cleared after handling the DMA interrupt.

[0038] At event (6) of FIG. 4, the DMA controller 140 executes the DMA operation by retrieving the data from the memory and providing the data to the driver module 400 requesting the data). In message (7) and (8) of FIG. 4, the DMA controller 140 indicates to the cache coherency manager 110 and the driver module 400, respectively, that the DMA operation is complete.

[0039] FIG. 5 illustrates a flow diagram of events and messages in the processor platform of FIG. 1 to handle a DMA operation identified/detected by the DMA controller 140 in accordance with the teachings of this disclosure. In the example of FIG. 5, at event (1) a DMA operation occurs in the processor system 100. The example DMA operation of FIG. 5 is a scatter/gather operation in which data arriving via the network 186 of FIG. 1 is to be DMA-ed to the volatile memory 150 based on the driver module 500 providing DMA setup instructions to the DMA controller 140.

[0040] At event (2) of FIG. 5, the DMA controller 140 identifies and/or detects the event (e.g., the DMA controller 140 detects the attempted DMA operation from the interface circuit 180 to the volatile memory 150 via the platform bus 170). At event (3), the DMA controller executes the DMA operation

by writing the network data to the volatile memory 150. In message (4), the DMA controller 140 sends an interrupt to the cache coherency manager 110.

[0041] At event (5) of FIG. 5, the cache coherency manager 110 handles the interrupt by invalidating the cache 130 (based on the direction of the DMA operation being from a peripheral (the interface circuit 180) to memory (the volatile memory 150)). In message (6), the cache coherency manager 110 indicates to the DMA controller 140 that the DMA interrupt has been cleared after handling the DMA interrupt. In messages (7) and (8) of FIG. 5, the DMA controller 140 indicates that the DMA operation is complete to the cache coherency manager 110 and the driver module 500, respectively.

[0042] Flowcharts representative of example machine readable instructions for implementing the cache coherency manager 110 of FIGS. 1, 2A, 2B, 3, 4, and/or 5 are shown in FIGS. 6 and 7. In this example, the machine readable instructions comprise a program/process for execution by the processor 120 of FIG. 1. The program/process may be embodied in computer readable instructions stored on a tangible computer readable storage medium such as a CD-ROM, a floppy disk, a hard drive, a digital versatile disk (DVD), a Blu-ray disk, or a memory associated with the processor 120, but the entire program/process and/or parts thereof could alternatively be executed by a device other than the processor 120 and/or embodied in firmware of the processor 120 or dedicated hardware associated the processor 120. Further, although the example program is described with reference to the flowcharts illustrated in FIGS. 6 and 7, many other methods of implementing the example cache coherency manager 110 may alternatively be used. For example, the order of execution of the blocks may be changed, and/or some of the blocks described may be changed, eliminated, or combined.

[0043] The example process 600 of FIG. 6 begins with an initiation of the cache coherency manager 110 (e.g., upon startup of the processor system 100, upon installation of the cache coherency manager 110 within processor 120, upon execution by the processor 120, etc.). At block 610, the interrupt manager 310 determines whether an interrupt associated with a DMA operation is received. If an interrupt has not been received, the interrupt manager 310

continues to monitor for receipt of an interrupt (control returns loops at block 610). If the interrupt manager 310 determines that an interrupt has been received, the cache coherency manager 110, at block 620, handles the DMA interrupt based on a parameter of the DMA operation. After block 620 of FIG. 6, the process ends.

[0044] The example process 620 of FIG. 7, which may be used to implement block 620 of FIG. 6, begins with an initiation of the cache coherency manager 110. At block 710 of FIG. 7, the interrupt manager 310 determines if a direction of the DMA operation is from a memory to a peripheral. For example, at block 710, the interrupt manager 310 may identify a direction parameter from the received interrupt to determine the direction of the DMA operation. For example, a direction of the DMA operation may be based on whether the operation is a read or write operation. If the interrupt manager 310 determines that the direction of the DMA operation is from a memory of the processor system 100 (e.g., the volatile memory 150 or the non-volatile memory 160) to a peripheral of the processor system 100 (e.g., an application or driver executed by the processor 120, the interface circuit 180, the input device(s) 182, the output device(s) 184, the network 186, the mass storage device 190, etc.), at block 720, the cache flusher 320 flushes the cache 130.

[0045] If, at block 710, the interrupt manager 310 determines that the direction of the DMA operation is not from a memory of the processor system 100 to a peripheral of the processor system 100 (e.g., it is from a peripheral to a memory), control advances to block 730. At block 730 of the example of FIG. 7, the cache invalidator 330 invalidates a location of the cache 130 corresponding to a memory location of the DMA operation in the volatile memory 150 and/or the non-volatile memory 150. For example, at block 730, the cache invalidator 330 may determine a memory location from an address parameter of the DMA operation. After block 720 or 730, the interrupt manager 310 clears the interrupt by sending a message to the DMA controller 140 indicating that the interrupt was handled. After block 740, the process 620 of FIG. 7 ends.

[0046] A flowchart representative of a process and/or example machine readable instructions for implementing the DMA controller 140 of FIG. 1 is shown

in FIG. 8. In this example, the process and/or machine readable instructions are executed by the DMA controller 140. The program/process may be embodied in software stored on a tangible computer readable storage medium such as a CD-ROM, a floppy disk, a hard drive, a digital versatile disk (DVD), a Blu-ray disk, or a memory associated with the DMA controller 140, but the entire program/process and/or parts thereof could alternatively be executed by a device other than the DMA controller 140 and/or embodied in firmware or dedicated hardware. Further, although the example program/process is described with reference to the flowchart illustrated in FIG. 8, many other methods of implementing the example DMA controller 140 may alternatively be used. For example, the order of execution of the blocks may be changed, and/or some of the blocks described may be changed, eliminated, or combined.

[0047] The process 800 of FIG. 8 begins with an initiation of the DMA controller 140 (e.g., upon startup of the processor system 100, upon startup of the DMA controller 140, upon installation of the DMA controller 140, etc.). At block 810, the DMA controller 140 determines that a DMA operation is to be executed. For example, at block 810, the DMA controller 140 may monitor for and/or detect an attempted DMA to the volatile memory 150 and/or the non-volatile memory 150 over the platform bus 170 of FIG. 7. As another example, the DMA controller 140 may receive requests to execute DMA operations from peripherals (e.g., applications/drivers executing on the processor 120, the interface circuit 180, the mass storage device 190, etc.).

[0048] At block 820, the DMA controller generates an interrupt corresponding to the DMA operation. For example, the generated interrupt may indicate parameters of the DMA operation. Example parameters may include a direction of the DMA operation, a source address, a destination address, a size of the DMA operation, a data format (byte, word, etc.) of the DMA operation, etc.). At block 830, the DMA controller 140 sends the interrupt to the cache coherency manager 110. Accordingly, the cache coherency manager 110, in accordance with the teachings of this disclosure, may maintain cache coherency within the processor system for the DMA operation of block 810. After block 830, the process 800 ends.

[0049] As mentioned above, the example processes of FIGS. 6, 7, and/or 8 may be implemented using coded instructions (e.g., computer and/or machine readable instructions) stored on a tangible computer readable storage medium such as a hard disk drive, a flash memory, a read-only memory (ROM), a compact disk (CD), a digital versatile disk (DVD), a cache, a random-access memory (RAM) and/or any other storage device or storage disk in which information is stored for any duration (e.g., for extended time periods, permanently, for brief instances, for temporarily buffering, and/or for caching of the information). As used herein, the term tangible computer readable storage medium is expressly defined to include any type of computer readable storage device and/or storage disk and to exclude propagating signals and to exclude transmission media. As used herein, "tangible computer readable storage medium" and "tangible machine readable storage medium" are used interchangeably. Additionally or alternatively, the example processes of FIGS. 6, 7, and/or 8 may be implemented using coded instructions (e.g., computer and/or machine readable instructions) stored on a non-transitory computer and/or machine readable medium such as a hard disk drive, a flash memory, a read-only memory, a compact disk, a digital versatile disk, a cache, a random-access memory and/or any other storage device or storage disk in which information is stored for any duration (e.g., for extended time periods, permanently, for brief instances, for temporarily buffering, and/or for caching of the information). As used herein, the term non-transitory computer readable medium is expressly defined to include any type of computer readable storage device and/or storage disk and to exclude propagating signals and to exclude transmission media. As used herein, when the phrase "at least" is used as the transition term in a preamble of a claim, it is open-ended in the same manner as the term "comprising" is open ended.

[0050] From the foregoing, it will be appreciated that the above disclosed methods, apparatus and articles of manufacture involve maintaining cache coherency of a processor system using a cache coherency manager. In examples disclosed herein, a DMA controller generates and sends an interrupt to the cache coherency manager to maintain cache coherency by flushing and/or

invalidating a cache of the processor system. In some examples, the cache coherency manager may be implemented via software executed by a processor and/or by firmware of a processor.

[0051] Although certain example methods, apparatus and articles of manufacture have been disclosed herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the claims of this patent.

What Is Claimed Is:

1. A non-transitory computer readable storage medium comprising instructions that, when executed, cause a processor to at least:
in response to receiving, from a direct memory access controller, an interrupt associated with a direct memory access operation, handle the interrupt via the processor to maintain cache coherency based on a parameter of the direct memory access operation, the interrupt generated by the direct memory access controller and comprising the parameter,
wherein the direct memory access controller is to execute the direct memory access operation.
2. The non-transitory computer readable storage medium of claim 1, wherein the instructions, when executed cause the processor to:
handle the interrupt by flushing a cache associated with the direct memory access operation when the parameter comprises a direction of the direct memory access operation from a memory of the system to a peripheral communicatively coupled with the system.
3. The non-transitory computer readable storage medium of claim 1, wherein the instructions, when executed cause the processor to:
handle the interrupt by invalidating a location of a cache corresponding to a memory location of the direct memory access operation when the parameter of comprises a direction of the direct memory access operation is from a peripheral communicatively coupled with the system to a memory of the system.
4. The non-transitory computer readable storage medium of claim 1, wherein firmware of the processor comprises the instructions.
5. The non-transitory computer readable storage medium of claim 1, the instructions comprise a first software layer of a processor and the direct memory

access operation was initiated by a module running on a second software layer of the processor.

6. A system comprising:
 - a direct memory access controller to:
 - determine that a direct memory access operation is to be executed;
 - generate an interrupt indicating that the direct memory access operation is to be executed; and
 - send the interrupt to a cache coherency manager of a processor;
 - and
 - the processor comprising the cache coherency manager to handle the interrupt based on a parameter of the direct memory access operation.
7. The system of claim 6, wherein the parameter of the direct memory access operation is a direction of the direct memory access operation.
8. The system of claim 6, wherein the cache coherency manager is to handle the interrupt by flushing a cache of the system when the parameter comprises a direction of the direct memory access operation from a memory of the system to a peripheral communicatively coupled with the system.
9. The system of claim 6, wherein the cache coherency manager is to handle the interrupt by invalidating a location of a cache corresponding to a memory location of the direct memory access operation when the parameter comprises a direction of the direct memory access operation from a peripheral of the system to a memory of the system.
10. The system of claim 6, wherein the cache coherency manager is a portion of system firmware, the system firmware comprising computer readable instructions to run a processor platform of the system.

11. A method comprising:
 - determining, via a hardware direct memory access controller, that a direct memory access operation is to be executed;
 - generating, via the hardware direct memory access controller, an interrupt corresponding to the direct memory access operation; and
 - sending, via the hardware direct memory access controller, the interrupt to a cache coherency manager of a processor, the cache coherency manager to handle the interrupt to maintain cache coherency.
12. The method of claim 11, wherein determining that the direct memory access operation is to be executed comprises receiving a data request from a first software layer of a processor.
13. The method of claim 12, wherein a second software layer of the processor comprises the cache coherency manager, the first software layer being different from the second software layer.
14. The method of claim 11, wherein the interrupt indicates that the cache coherency manager is to flush a cache associated with a memory associated with the direct memory access operation when a direction of the direct memory access operation is from the memory to a peripheral.
15. The method of claim 11, wherein the interrupt indicates that the cache coherency manager is to invalidate a cache location corresponding a location of a memory associated with the direct memory access operation when a direction of the direct memory access operation is from a peripheral to the memory.

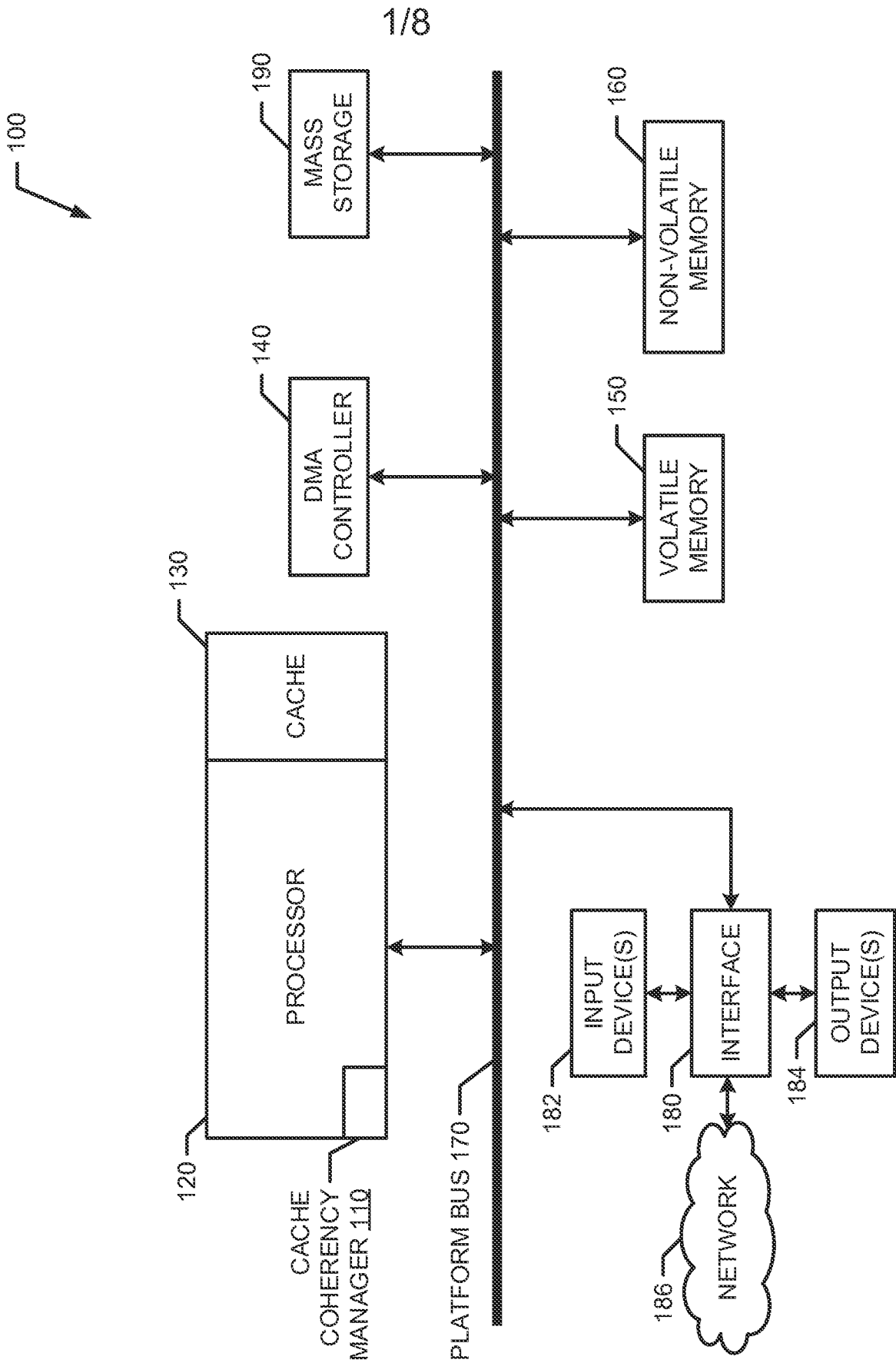


FIG. 1

2/8

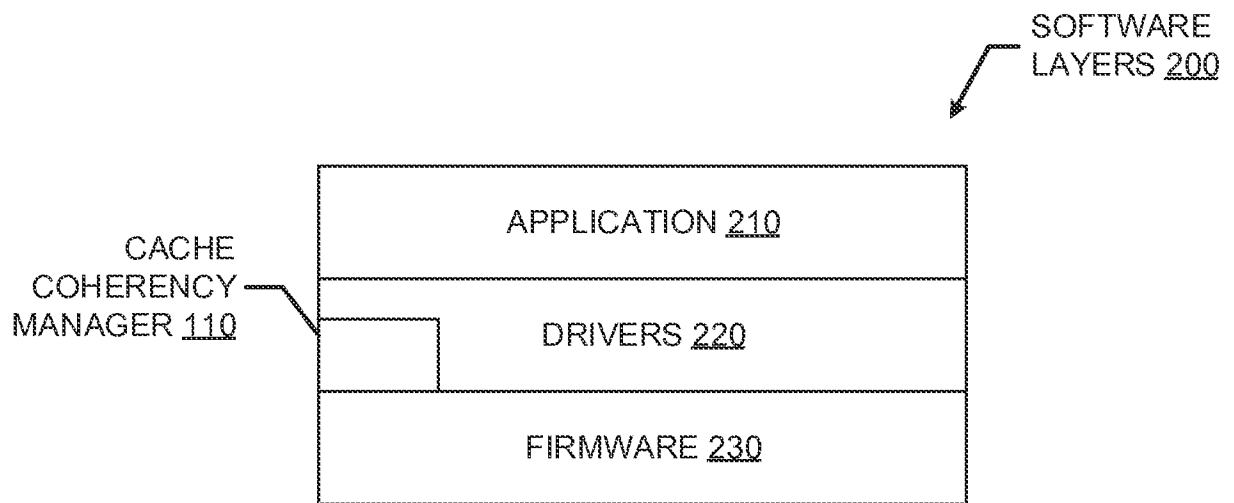


FIG. 2A

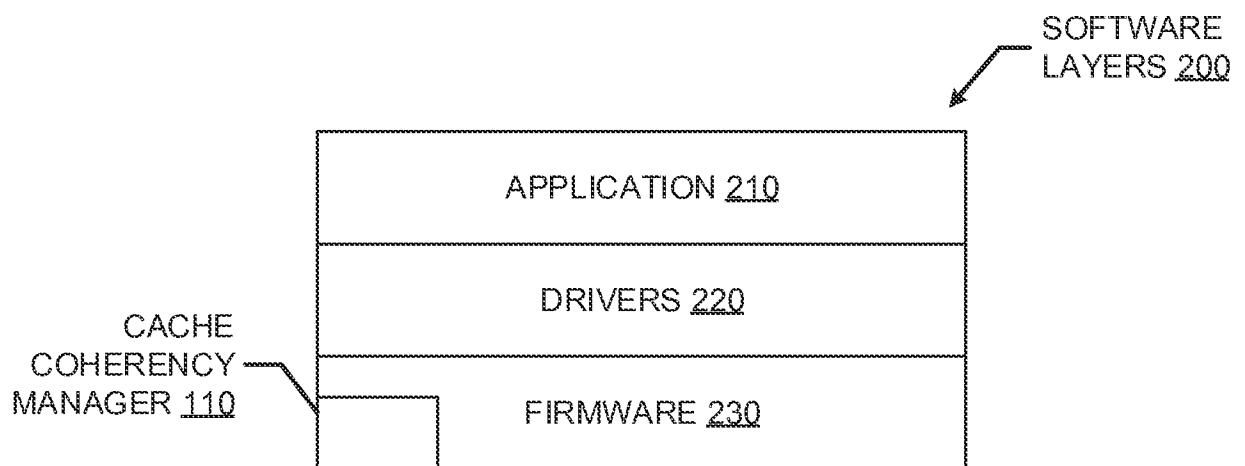


FIG. 2B

3/8

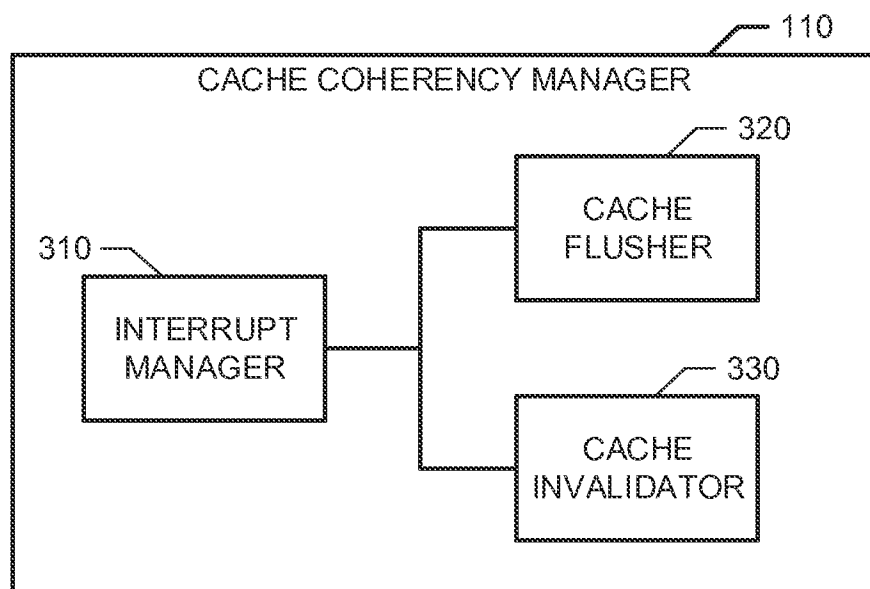


FIG. 3

4/8

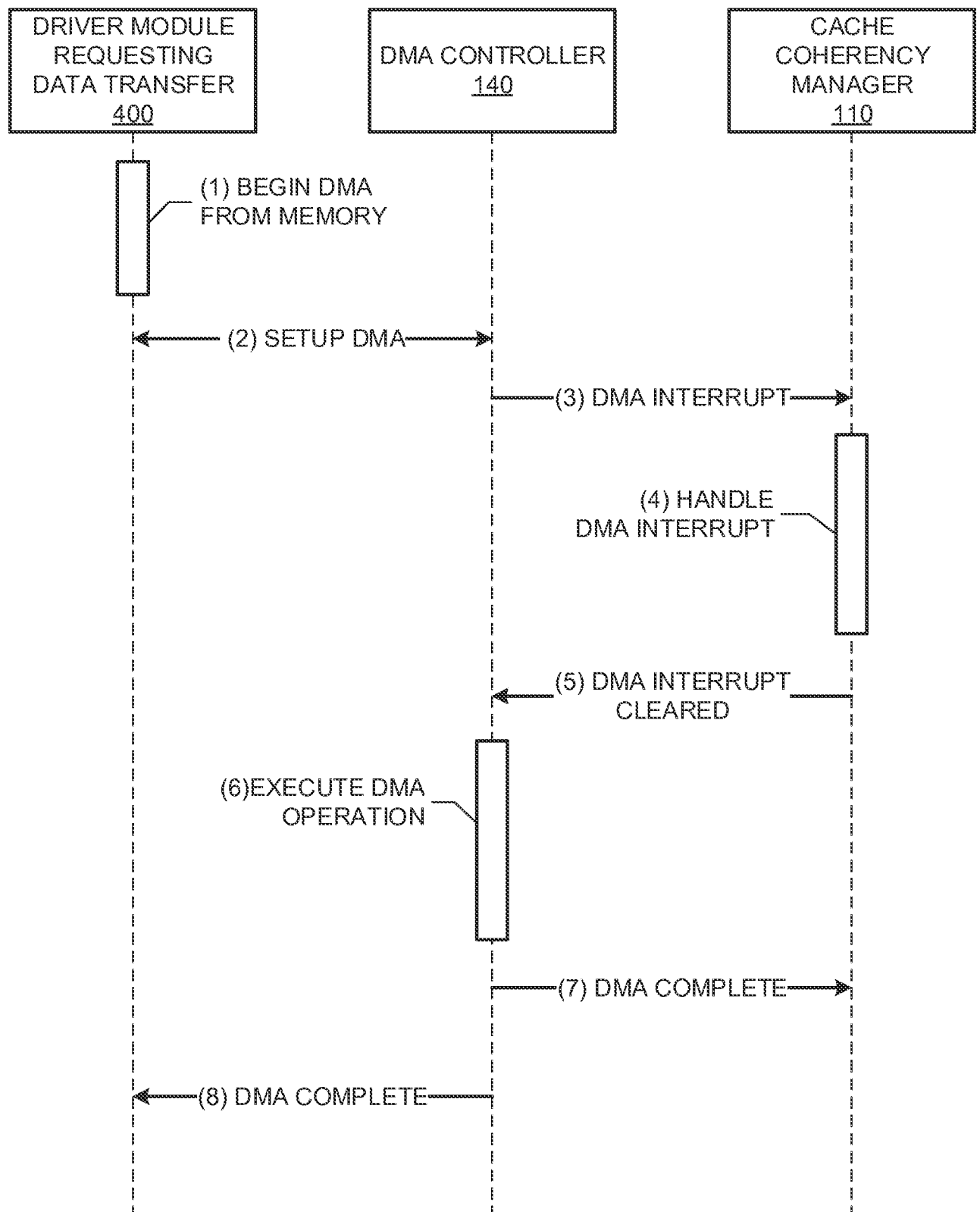


FIG. 4

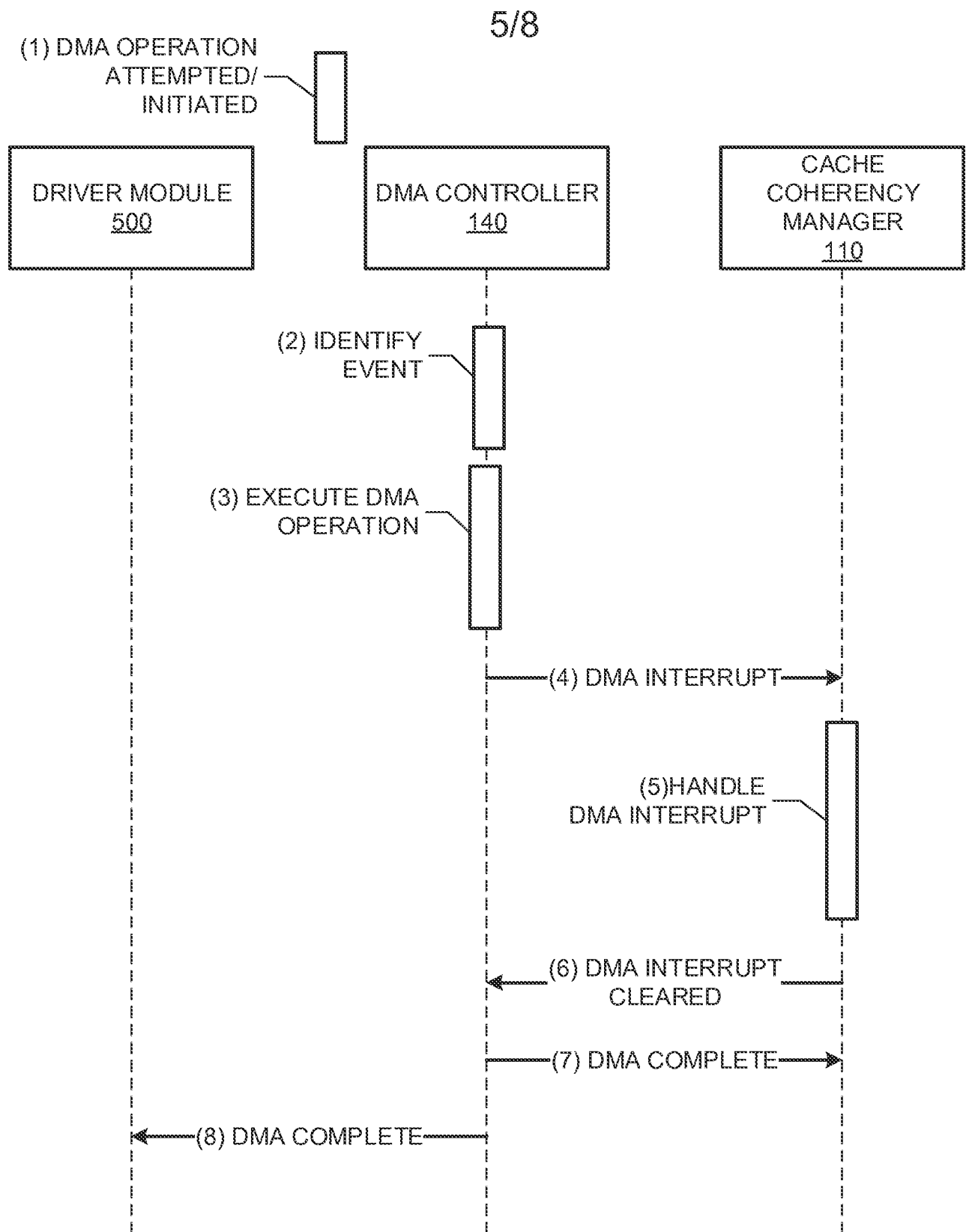


FIG. 5

6/8

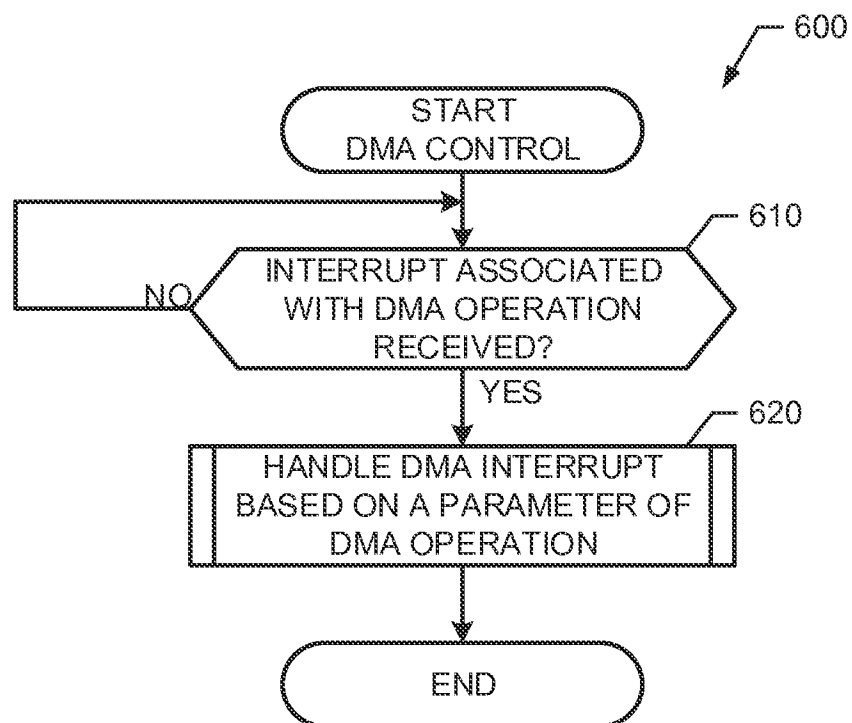


FIG. 6

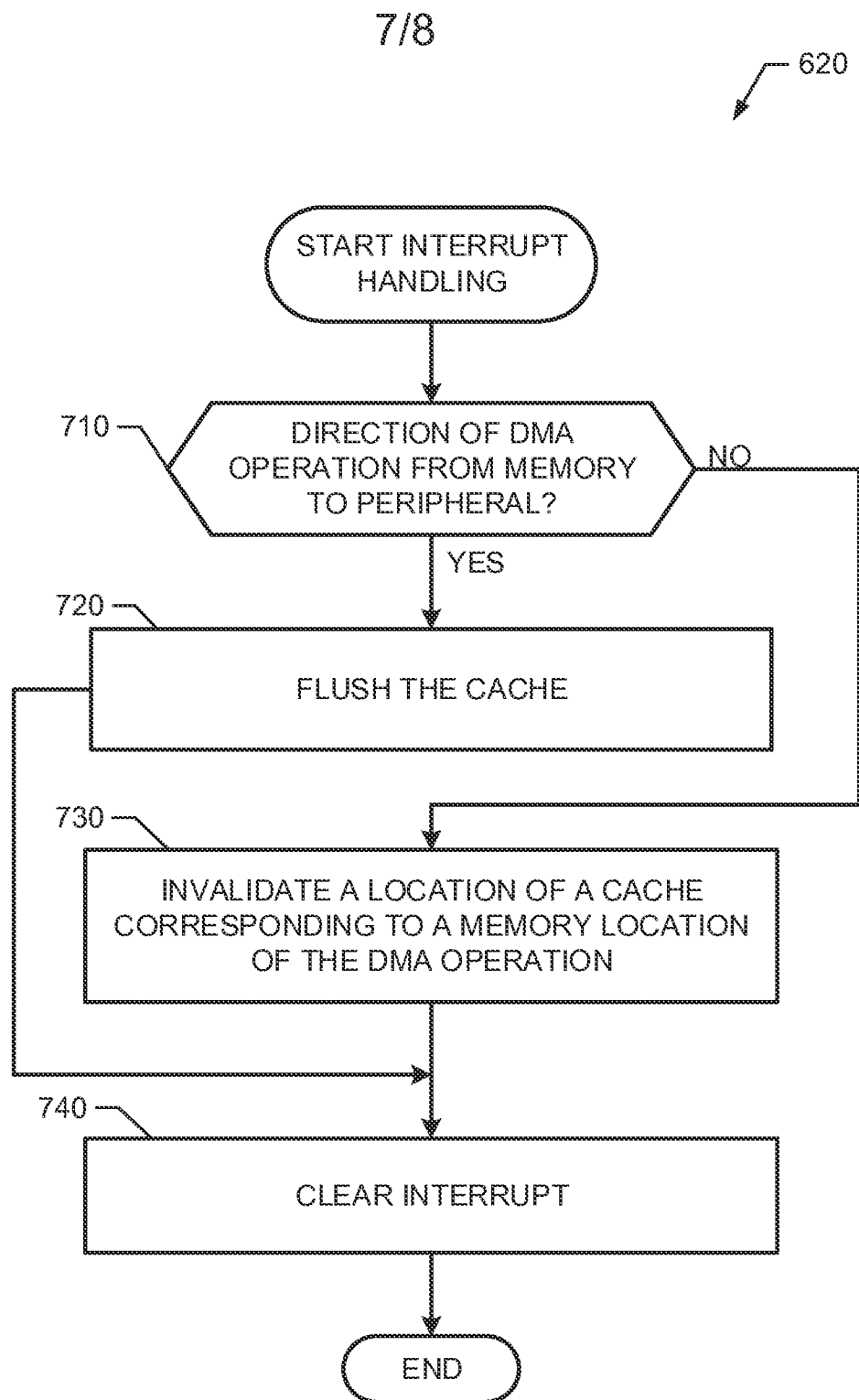


FIG. 7

8/8

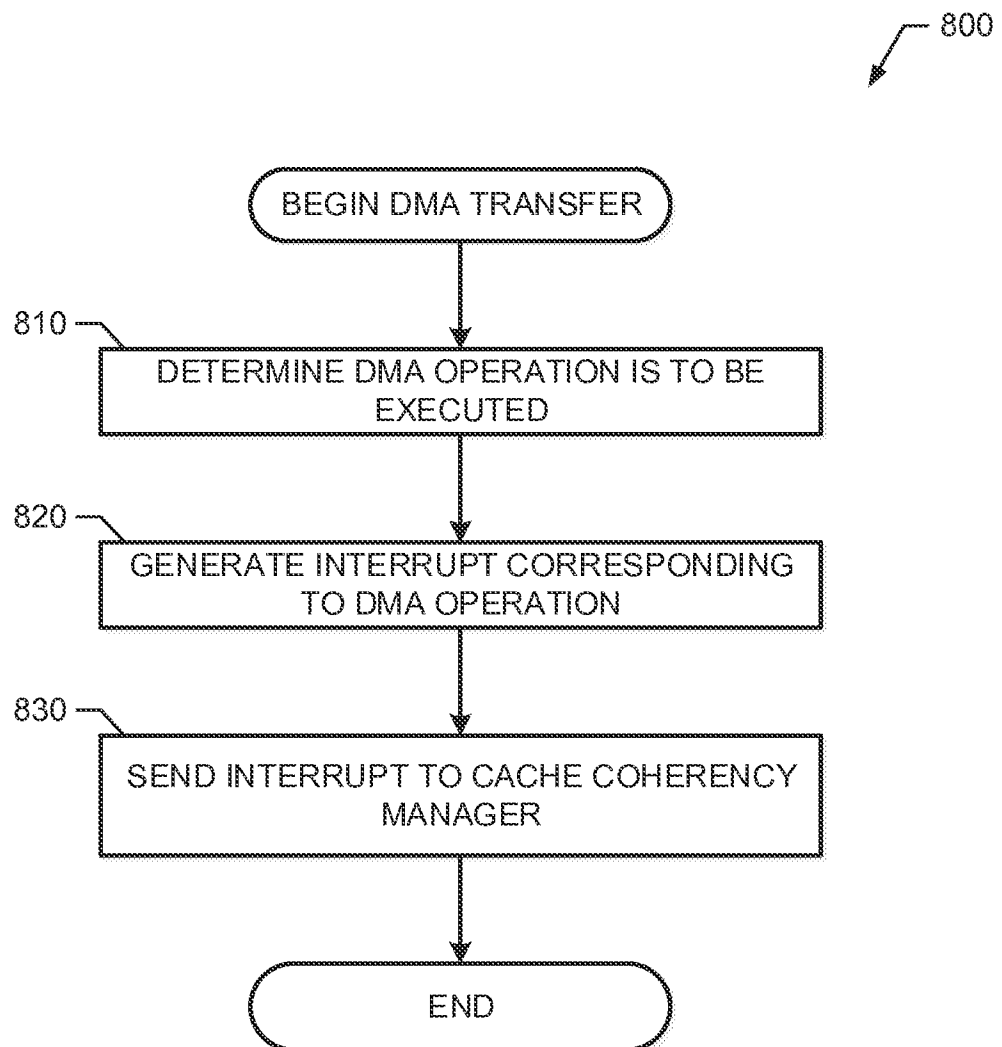


FIG. 8

A. CLASSIFICATION OF SUBJECT MATTER**G06F 13/16(2006.01)i, G06F 12/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 13/16; G06F 12/00; G06F 13/28; G06F 12/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: cache coherency, dma operation, dma, interrupt, and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,664,149 A (MARVIN WAYNE MARTINEZ, JR. et al.) 02 September 1997 See column 1, line 15; column 6, lines 31-33; column 8, lines 33-42; column 9, lines 38-42; claims 1 and 4-5; and figure 3a.	1-4, 6-11, 14-15
A		5, 12-13
Y	US 2005-0216610 A1 (CHARLES RAY JOHNS et al.) 29 September 2005 See paragraph [0016]; claim 1; and figure 1.	1-4, 6-11, 14-15
A	US 2003-0023783 A1 (RAVI KUMAR ARIMILLI et al.) 30 January 2003 See paragraphs [0008], [0013], [0017], and [0029]-[0038]; and figure 1.	1-15
A	EP 0644491 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 12 April 2000 See paragraphs [0001] and [0017]-[0018]; and figure 1.	1-15
A	WO 2005-121966 A2 (FREESCALE SEMICONDUCTOR, INC.) 22 December 2005 See page 8, lines 3-6; page 22, line 4 - page 25, line 18; and figure 5.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 February 2015 (27.02.2015)

Date of mailing of the international search report

27 February 2015 (27.02.2015)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea

Facsimile No. ++82 42 472 3473

Authorized officer

NHO, Ji Myong

Telephone No. +82-42-481-8528



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/042513

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 05664149 A	02/09/1997	EP 0600626 A1 JP 07-168763 A US 5524234 A US 5664149 A US 5860111 A	08/06/1994 04/07/1995 04/06/1996 02/09/1997 12/01/1999
US 2005-0216610 A1	29/09/2005	CN 1673980 A JP 2005-276199 A TW I334540 B US 7657667 B2	28/09/2005 06/10/2005 11/12/2010 02/02/2010
US 2003-0023783 A1	30/01/2003	US 6785776 B2	31/08/2004
EP 0644491 B1	12/04/2000	AT 191803 T CA 2125218 A1 DE 69423938 D1 DE 69423938 T2 EP 0644491 A1 ES 2144488 T3 JP 07-105090 A JP 2642064 B2 KR 10-1997-0007271 B1 US 5526512 A	15/04/2000 21/03/1995 18/05/2000 12/10/2000 22/03/1995 16/06/2000 21/04/1995 20/08/1997 07/05/1997 11/06/1996
WO 2005-121966 A2	22/12/2005	AT 458222 T CN 101617298 A CN 101617298 B DE 602004025556 D1 EP 1605360 A1 EP 1605360 B1 JP 2008-502069 A KR 10-2007-0017551 A US 2008-0301371 A1 WO 2005-121966 A3	15/03/2010 30/12/2009 21/03/2012 01/04/2010 14/12/2005 17/02/2010 24/01/2008 12/02/2007 04/12/2008 22/06/2006