Title: STACKABLE IC PACKAGE WITH TOP AND BOTTOM INTERCONNECT

Abstract: Consistent with an example embodiment, there is a stackable IC package (218) that comprises a die (206) having a first major surface and a second major surface (212). The first and second major (212) surfaces are joined by opposed pairs of longitudinal (208) and lateral sides (210). A conductive pattern (202) is electrically coupled to the first major surface of the die. The conductive pattern (202) extends past the longitudinal sides of the die and is folded back (204) in a direction (214) generally toward the die. The conductive pattern defines a first portion approximately co-planar with the first major surface of the die and a second portion approximately co-planar with the second major surface of the die. The first and second portions are electrically connectable to another stackable IC package. A support material (216) fixedly supports the conductive pattern (202) relative to the die (206) and supports the first and second portions of the conductive pattern is a spaced, generally parallel relationship to one another.
STACKABLE IC PACKAGE WITH TOP AND BOTTOM INTERCONNECT

The present invention relates generally to stackable IC packages, and more particularly to stackable IC packages with top and bottom interconnect.

Miniaturization in IC packaging and “System in Package” are driving forces for packaging solutions with stackable packages. Stackable packages are volumetrically efficient, consisting of two or more IC packages that are interconnected in a single component, a “chip-stack”, which is mountable to a printed circuit board using the “footprint” typically used for a single package device, such as for instance a packaged IC.

The IC packages must, in addition to being formed into a stack, be electrically interconnected to each other in a desired manner. One of the current solutions is the “Match-X” approach from the Fraunhofer Institute in Germany. The Match-X concept consists of the stacking of substrates, with electronic components, on top of each other with solder balls as interconnect between the different substrates. Match-X is discussed in an article titled, “Stackable System-On-Packages with Integrated Components,” in the IEEE Transactions on Advanced Packaging, (Vol. 27, No. 2, May 2004) of Becker et al.

Similarly, US Patent No. 6,426,240 issued to Isaak on July 30, 2002, discloses a stackable flex circuit chip package including a flexible substrate having a conductive pattern disposed thereon. These references are incorporated by reference in their entirety. In the assembled condition, the flexible substrate supports a first side of an integrated circuit chip, wraps around opposite parallel edges of the integrated circuit chip, and is attached to at least a portion of a second side of the integrated circuit chip that is opposite the first side. The conductive pattern defines portions along both the first side and the second side of the integrated circuit, which are electrically connectable to another stackable IC package.

However, in both of these prior art approaches it is a disadvantage that additional substrate layers are used as carrier, which increases the size of the IC package.

There is a need to provide a stackable IC package that overcomes at least some of the above-mentioned limitations of the prior art.

The present invention has been found useful in the drive for miniaturization in integrated circuit packages and system-in-package in finding packaging solutions with stackable packages.

In an example embodiment, there is a method of assembling a stackable IC package with top and bottom interconnect. The method comprises providing a die comprising first
and second opposing longitudinal sides, first and second major surfaces, and a plurality of contacts arrayed on the first major surface. A flexible substrate comprising a conductive pattern and having first and second end portions is provided. The plurality of contacts of the die is electrically coupled to the conductive pattern. The flexible substrate is folded along at least a known line relative to at least one of the longitudinal sides of the die to dispose at least one of the first and second end portions in a planar arrangement opposing a plane of the second major surface of the die and on a side thereof opposite the first major surface of the die for electrical connection to a second stackable IC package. A support material between the flexible substrate and the die for supporting the conductive pattern relative to the die is provided. By removing at least a portion of the flexible substrate, the conductive pattern is exposed.

In another example embodiment, there is a stackable IC package that comprises a die having a first major surface and a second major surface joined by opposed pairs of longitudinal and lateral sides. A conductive pattern electrically couples to the first major surface of the die. The conductive pattern extends past the longitudinal sides of the die and folds back in a direction generally toward the die. The conductive pattern thereby defines a first portion which is approximately co-planar with the first major surface of the die and a second portion which is approximately co-planar with the second major surface of the die; the first and second portions each being electrically connectable to another stackable IC package. A support material fixedly supports the conductive pattern relative to the die, and supports the first and second portions of the conductive pattern in spaced, generally parallel relationship one to the other.

In another example embodiment according to the present invention there is a stackable IC package. The IC package comprises a die having a first major surface and a second major surface joined by opposed pairs of longitudinal and lateral sides; a distance between the first major surface and the second major surface defines a thickness of the die. A conductive pattern electrically couples to the first major surface of the die and has a thickness that is small relative to the thickness of the die. The conductive pattern extends past the longitudinal sides of the die and folds back in a direction generally toward the die; the conductive pattern thereby defines a first portion which is approximately co-planar with the first major surface of the die and a second portion which is approximately co-planar with the second major surface of the die. The first and second portions each are electrically connectable to another stackable IC package. A support material fixedly supports the
conductive pattern relative to the die, for electrically isolating the conductive pattern and the
surface of the die where the support material is disposed therebetween, and for supporting
the first and second portions of the conductive pattern in a spaced, generally parallel
relationship one to the other.

The above summaries of the present invention are not intended to represent each
disclosed embodiment, or every aspect, of the present invention. Other aspects and example
embodiments are provided in the figures and the detailed description that follows.

The invention may be more completely understood in consideration of the following
detailed description of various embodiments of the invention in connection with the
accompanying drawing, in which:

FIG. 1 is a simplified flow diagram of a method of assembling a stackable IC
package with top and bottom interconnect, according to an embodiment of the instant
invention;

FIG. 2A is a top perspective view of a temporary substrate including a conductive
pattern, for use in assembling a stackable IC package with top and bottom interconnect;
FIG. 2B is a top perspective view of a die attached to the temporary substrate of
FIG. 2A;

FIG. 2C is a top perspective view showing the folded temporary substrate and die;
FIG. 2D is a top perspective view showing the folded temporary substrate filled with
an epoxy support material;

FIG. 2E is a top perspective view showing a stackable IC package with top and
bottom interconnect, subsequent to removal of the temporary substrate;

FIG. 3 is a cross-sectional view of a stackable IC package with top and bottom
interconnect, according to an embodiment of the instant invention; and,

FIG. 4 is a cross-sectional view of a chip-stack assembled using stackable IC
packages according to an embodiment of the instant invention.

The following description is presented to enable a person skilled in the art to make
and use the invention, and is provided in the context of a particular application and its
requirements. Various modifications to the disclosed embodiments will be readily apparent
to those skilled in the art, and the general principles defined herein may be applied to other
embodiments and applications without departing from the spirit and the scope of the
invention. Thus, the present invention is not intended to be limited to the embodiments
disclosed, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

Referring to FIG. 1, shown is a simplified flow diagram of a method of assembling a stackable IC package with top and bottom interconnect, according to an embodiment of the instant invention. A die is provided at 10, the die having first and second opposing longitudinal sides, first and second opposing lateral sides, first and second major surfaces, and a plurality of contacts arrayed on the first major surface. A flexible substrate, having a conductive pattern disposed along one side thereof, is provided at 15. The flexible substrate includes a sacrificial layer; in an example embodiment, the flexible substrate is an Al or Cu substrate. At 20, the die is mounted onto the temporary substrate and is electrically coupled to the conductive pattern via the plurality of contacts. Electrical coupling is achieved using techniques that are well known in the art, such as for instance. For example, the interconnect can be made by wire bonding or ultrasonic flip-chip bonding. The use of glue or glue film is also possible. At 25, the flexible substrate is folded along an imaginary line adjacent to each of the longitudinal sides of the die, to dispose the first and second end portions opposed to each other in a co-planar arrangement above the second major surface of the die for electrical connection to a second stackable IC package. Subsequent to folding, a support material is provided between the flexible substrate and the die at 30. The support material is preferably an epoxy, which is cured and hardened for supporting the conductive pattern relative to the die. Finally, the flexible substrate is removed at 35 so as to expose the conductive pattern.

In another example embodiment, the flexible substrate is folded along an imaginary line parallel to each of the longitudinal sides of the die, so as to facilitate manufacturing of the stackable IC packages. Of course, optionally the conductive pattern is disposed along the one side of the flexible substrate so as to support folding of the flexible substrate along imaginary lines that are other than parallel to each of the longitudinal sides of the die. Preferably, such folding is accomplished in an automated manner using, for instance, a moulding machine as is known in the art. For example, trim and form tools and the like may be used to shape the leads of semiconductor packages, such as DILs.

According to the method described supra with reference to FIG. 1, the temporary substrate is folded in one direction only. Specifically, the temporary substrate is folded along an imaginary line adjacent to each of the longitudinal sides of the die. In another example embodiment, the temporary substrate is folded in two directions. In particular, the
temporary substrate optionally is folded along an imaginary line adjacent and parallel to each of the longitudinal sides of the die or along an imaginary line adjacent and parallel to each of the lateral sides of the die.

Referring now to FIG. 2A, shown is a top perspective view of a temporary substrate 200, including a conductive pattern 202, for use in assembling a stackable IC package with top and bottom interconnect. The temporary substrate 200 is fabricated using materials that support folding or bending of the temporary substrate without breakage. For instance, the flexible substrate 200 is an Al-Cu substrate. Opposite end portions of the temporary substrate 200 are identified in FIG. 2a using the reference numeral 204. The conductive pattern 202 is formed in a known manner. The thick ranges from about 3μm to about 30μm. The conductive pattern may be made by electroplating and can consist of a stack-like structure of 1μm gold followed by 2μm nickel and 10μm copper. Depending on the particular interconnect method, additional layers of for example, gold or solder may be included.

Referring now to FIG. 2B, shown is a top perspective view of a die 206 that is attached to the temporary substrate 200 of FIG. 2A. For the sake of simplicity, only one package with a single die 206 is shown. However, in practice a substrate with multiple positions, where each position contains a single IC or a more complex SiP with IC's and discrete components, optionally is used. The die 206 includes first and second opposing longitudinal sides 208, first and second opposing lateral sides 210, a not illustrated first major surface and a second major surface 212, and a plurality of not illustrated contacts arrayed on the first major surface. In FIG. 2B, the first major surface is the “lower surface” of the die 206 and the second major surface 212 is the “upper surface” of the die 206. The die 206 is electrically coupled to the conductive pattern 202 via the plurality of contacts, in a known manner.

Referring now to FIG. 2C, shown is a top perspective view showing the folded temporary substrate 200 and die 206. In particular, the flexible substrate 200 is folded along an imaginary line 214 that is parallel to each of the opposite end portions 204 of the die 206, to dispose the opposite end portions 204 opposed to each other in a co-planar arrangement above the second major surface 212 of the die 206 in FIG. 2C. The opposite end portions 204 are disposed for electrical connection to a second stackable IC package. In another example embodiment, the flexible substrate 200 is folded along a not illustrated imaginary line that is not parallel to each of the opposite end portions 204 of the die 206.
Referring now to FIG. 2D, shown is a top perspective view showing the folded temporary substrate 200, with the opposite end portions 204 opposed to each other in a co-planar arrangement, filled with an epoxy support material 216. The epoxy support material 216 fills the voids between conductive tracks of the conductive pattern 202, and then is cured in a known manner.

Referring now to FIG. 2E, shown is a top perspective view showing a stackable IC package 218 with top interconnects 220 and not illustrated bottom interconnects, subsequent to removal of the flexible substrate. The epoxy support material 216 supports the conductive pattern 202, including the top interconnects 220 and the bottom interconnects, relative to the die after the flexible substrate has been removed. Advantageously, the flexible substrate 200 is removed prior to stacking the stackable IC packages into a stack. Since the flexible substrate 200 is not required to carry the conductive pattern, the stackable IC package 218 as shown, in FIG. 2e supports a minimum stack size.

Referring now to FIG. 3, shown is a cross-sectional view of a stackable IC package with top and bottom interconnect, according to an embodiment of the instant invention. As shown in FIG. 3, the epoxy support material 216 supports the conductive pattern 202, including the top interconnects 220 and the bottom interconnects 222, relative to the die 206. In addition, the epoxy support material 216 supports the top interconnects 220 adjacent to the longitudinal sides 208 of the die in a co-planar arrangement above the second major surface 212 of the die 206.

Referring now to FIG. 4, shown is a cross-sectional view of a chip-stack assembled using stackable IC packages according to an embodiment of the instant invention. In FIG. 4, three stackable IC packages according to an embodiment of the instant invention are shown. In another example embodiment, the chip stack includes two or more than three stackable IC packages according to an embodiment of the instant invention. In the chip stack, the top interconnects 220 of a first stackable IC package are electrically coupled to the bottom interconnects of an adjacent stackable IC package. Electrical coupling is achieved using any suitable procedure that is known in the art for this purpose. Some non-limiting examples include gluing, soldering or use of adhesive strips.

Optionally, each stackable IC package in the chip stack shown at FIG. 4 has the same function. Further optionally, each stackable IC package in the chip stack may have a different electrical function.
Optionally, the stackable IC package, according to an embodiment of the instant invention, is used as a single package with on top "odd" components such as for instance a loudspeaker, coil, or microphone. Further optionally, a plurality of stackable IC package is assembled into a stack, wherein the stack acts as for instance, a system-in-package (SiP).

The above description has used the specific and non-limiting example of a flip-chip. Optionally, wire bonding is possible since only the lateral ends of the flexible substrate are bent and folded. Other examples may include a chip with a microprocessor upon which through application of the present invention may have memory chips stacked thereon.

While the present invention has been described with reference to several particular example embodiments, those skilled in the art will recognize that many changes may be made thereto without departing from the spirit and scope of the present invention, which is set forth in the following claims.
CLAIMS

What is claimed is:

1. A method (100) of assembling a stackable IC package with top and bottom interconnect, comprising: providing a die (10) comprising first and second opposing longitudinal sides, first and second major surfaces, and a plurality of contacts arrayed on the first major surface; providing a flexible substrate (15, 20) comprising a conductive pattern and having first and second end portions; electrically coupling the plurality of contacts of the die to the conductive pattern; folding the flexible substrate (25) along at least a known line relative to at least one of the longitudinal sides of the die to dispose at least one of the first and second end portions in a planar arrangement opposing a plane of the second major surface of the die and on a side thereof opposite the first major surface of the die for electrical connection to a second stackable IC package; providing a support material (30) between the flexible substrate and the die for supporting the conductive pattern relative to the die; and, exposing the conductive pattern (35) by removing at least a portion of the flexible substrate.

2. The method as recited in claim 1, wherein folding comprises, folding the flexible substrate along at least two known lines relative to each of the longitudinal sides of the die to dispose the first and second end portions opposed to each other in a co-planar arrangement opposing a plane of the second major surface and on a side thereof opposite the first major surface of the die for electrical connection to a second stackable IC package.

3. The method as recited in claim 1 wherein the at least a known line comprises an imaginary line adjacent to at least one of the longitudinal sides of the die.

4. The method as recited in claim 2 wherein the at least a known line comprises an imaginary line adjacent to at least one of the longitudinal sides of the die.

5. The method as recited in any of claims 1, 2, 3, or 4, wherein the known line is parallel to at least one of the longitudinal sides of the die.

6. The method as recited in any of claims 1 through 5, wherein removing at least a portion of the flexible substrate comprises removing all of the flexible substrate on the support material.

7. The method as recited in any of claims 1 through 6, wherein removing at least a portion of the flexible substrate comprises removing all of the flexible substrate on
an opposing side of a plane of the second major surface of the die relative to the first major surface of the die.

8. The method as recited in any of claims 1 through 7, wherein removing at least a portion of the flexible substrate comprises other than removing a portion of the flexible substrate joining a surface of the flexible substrate on opposing sides of the first major surface of the die and of a plane of the second major surface of the die.

9. The method as recited in any of claims 1 through 8, comprising removing all of the flexible substrate on an opposing side of the first major surface of the die relative to the second major surface of the die.

10. The method as recited in any of claims 1 through 9, wherein the support material is an epoxy material and comprising curing the epoxy material prior to exposing the conductive pattern.

11. The method as recited in any of claims 1 through 10, wherein the flexible substrate is folded such that the first and second end portions other than oppose a portion of the second major surface of the die.

12. A stackable IC package(218), comprising: a die (206) having a first major surface and a second major surface (212) joined by opposed pairs of longitudinal(208) and lateral (210) sides; a conductive pattern (202) electrically coupled to the first major surface of the die, the conductive pattern extending past the longitudinal sides (208) of the die and folded back (204) in a direction generally toward the die, the conductive pattern thereby defining a first portion which is approximately co-planar with the first major surface of the die and a second portion which is approximately co-planar with the second major surface of the die, the first and second portions each being electrically connectable to another stackable IC package; and, a support material (216) for fixedly supporting the conductive pattern relative to the die, and for supporting the first and second portions of the conductive pattern (202) in spaced, generally parallel relationship one to the other.

13. A stackable IC package as recited in claim 12, wherein the support material is an epoxy material.

14. A stackable IC package as recited in claims 12 or 13, wherein the conductive pattern is supported by a flexible substrate, the flexible substrate on an outside surface of the conductive pattern.
15. A stackable IC package as recited in any of claims 12 or 13, wherein the conductive pattern is partially supported by a flexible substrate, the flexible substrate (200) being removed from a portion of the conductive pattern.

16. A stackable IC package as recited in any of claims 12 through 15, wherein the conductive pattern is disposed along a periphery of the stackable IC package about the second major surface of the die.

17. A stackable IC package as recited in any of claims 12 through 16, wherein the support material is electrically insulating for providing electrical insulation between stackable IC packages when stacked except in areas wherein the conductive pattern of one stackable IC package is in contact with the conductive pattern of a second other stackable IC package when stacked.

18. A stackable IC package as recited in any of claims 12 through 17, comprising a second stackable IC package comprising: a second die having a first major surface and a second major surface joined by opposed pairs of longitudinal and lateral sides; another conductive pattern electrically coupled to the first major surface of the second die, the conductive pattern extending past the longitudinal sides of the second die and folded back in a direction generally toward the second die, the conductive pattern thereby defining a first portion which is approximately co-planar with the first major surface of the second die and a second portion which is approximately co-planar with the second major surface of the second die, the first and second portions each being electrically coupled to the conductive pattern; and, a support material for fixedly supporting the second conductive pattern relative to the second die, and for supporting the first and second portions of the second conductive pattern in spaced, generally parallel relationship one to the other.

19. A stackable IC package as recited in any of claims 11 through 17 absent a flexible support layer disposed on a second major surface of the die.

20. A stackable IC package (218), comprising: a die (206) having a first major surface and a second major surface (212) joined by opposed pairs of longitudinal (208) and lateral sides (210), a distance between the first major surface and the second major surface defining a thickness of the die; a conductive pattern (202) electrically coupled to the first major surface of the die and having a thickness that is small relative to the thickness of the die, the conductive pattern extending past the longitudinal sides (208) of the die and folded back in a direction (204) generally toward the die (206), the conductive pattern thereby defining a first portion which is approximately co-planar with the first major surface of the
die and a second portion which is approximately co-planar with the second major surface (212) of the die, the first and second portions each being electrically connectable to another stackable IC package; and, a support material for fixedly supporting the conductive pattern relative to the die, for electrically isolating the conductive pattern and the surface of the die where the support material is disposed therebetween, and for supporting the first and second portions of the conductive pattern in spaced, generally parallel relationship one to the other.

21. A stackable IC package as recited in claim 20, wherein a total thickness of the stackable IC package is approximately the sum of the thickness of the die plus twice the thickness of the conductive pattern.

22. A stackable IC package as recited in claims 21 or 20, wherein the thickness of the conductive pattern is in the range of about 3μm to about 30μm.
**INTERNATIONAL SEARCH REPORT**

**International application No**

PCT/IB2006/051946

**A. CLASSIFICATION OF SUBJECT MATTER**

INV. H01L25/10 H01L23/31 H01L23/498

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

**Electronic data base consulted during the international search (name of data base and, where practical, search terms used)**

EP0–Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
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<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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* Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
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