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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Blvd., Santa Clara, California 95054 (US).

(72) Inventors: **MANIPATRUNI, Sasikanth**; 6993 NE Ronler Way, #1817, Hillsboro, Oregon 97124 (US). **NIKONOV, Dmitri E.**; 16569 SW Whitetail Lane, Beaverton, Oregon 97007 (US). **YOUNG, Ian A.**; 3181 NW 114th Terrace, Portland, Oregon 97229 (US).

(74) Agent: **MUGHAL, Usman A.**; Green, Howard & Mughal, LLP, c/o CPA Global, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).

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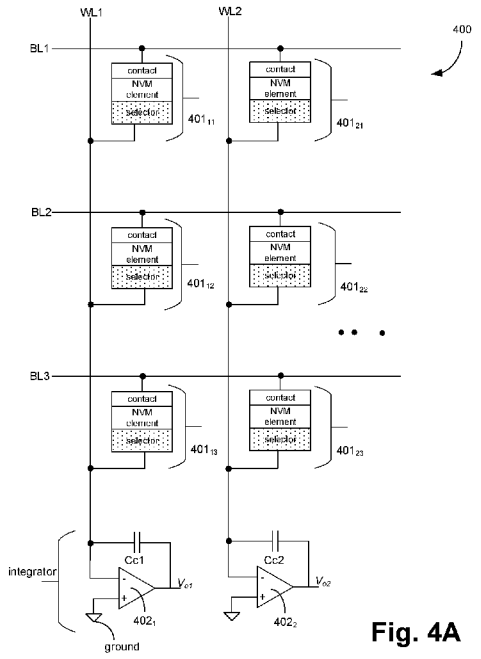


Fig. 4A

(57) **Abstract**: Described is an apparatus which comprises: a first word-line; a first bit-line; a second bit-line; a first resistive memory cell having a first terminal coupled to the first bit-line and a second terminal coupled to the first word-line; a second resistive memory cell having a first terminal coupled to the second bit-line and a second terminal coupled to the first word-line; and a first integrator coupled to the first word-line.

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APPARATUS AND METHOD OF IN-MEMORY COMPUTATION USING NON-VOLATILE ARRAYS

BACKGROUND

[0001] In modern image, speech, and pattern recognition operations, comparison and/or matching of real-valued vectors is often required. Machine learning algorithms are used in various applications such as embedded-sensor networks and computer vision. The operation of pattern recognition can be used for classification in machine learning. Pattern recognition is also used for multimedia applications such as object detection or speech recognition. Computation in pattern recognition is a repetitive process and requires regular memory accesses, and as such, consumes significant energy.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0003] **Fig. 1A** illustrates a scheme of an analog in-memory pattern matching with the use of Resistive Random Access Memory (RRAM) elements, in accordance with some embodiments.

[0004] **Fig. 1B** illustrates a plot indicating dependence of resistance of a RRAM element on a number of switching pulses.

[0005] **Figs. 2A-B** illustrate resistive memory bit-cells for use in the scheme of **Fig. 1A**, in accordance with some embodiments.

[0006] **Fig. 3** illustrates a non-volatile (NV) Phase Change Memory (PCM) element for use in the resistive memory bit-cell of **Figs. 2A-B**, in accordance with some embodiments.

[0007] **Fig. 4A** illustrates an array of NV PCM bit-cells which are operable for in-memory pattern matching, in accordance with some embodiments of the disclosure.

[0008] **Fig. 4B** illustrates the array of **Fig. 4A** showing programming of an NV PCM bit-cell, in accordance with some embodiments of the disclosure.

[0009] **Fig. 4C** illustrates the array of **Fig. 4A** showing computation of a dot product for a row of the array, in accordance with some embodiments of the disclosure.

[0010] **Fig. 5** illustrates a flowchart of a method for determining a dot product of input voltages and conductances using the array of **Fig. 4A**, in accordance with some embodiments of the disclosure.

[0011] **Fig. 6A** illustrates an array of NV PCM bit-cells which are operable for in-memory pattern matching, in accordance with some embodiments of the disclosure.

[0012] **Fig. 6B** illustrates the array of **Fig. 6A** showing programming of an NV PCM bit-cell, in accordance with some embodiments of the disclosure.

[0013] **Fig. 6C** illustrates the array of **Fig. 6A** showing computation of dot product for a row of the array, in accordance with some embodiments of the disclosure.

[0014] **Fig. 7** illustrates a flowchart of a method for determining a dot product of input voltages and conductances using the array of **Fig. 6A**, in accordance with some embodiments of the disclosure.

[0015] **Fig. 8** illustrates a smart device or a computer system or a SoC (System-on-Chip) with the scheme of analog in-memory pattern matching with the use of resistive memory elements, according to some embodiments.

DETAILED DESCRIPTION

[0016] Various embodiments describe an apparatus and method of in-memory computation using non-volatile memory arrays. Pattern matching may be done by computing of the dot product of an input data 'D' and a memorized pattern "P_n" which are real-valued vectors of length 'm'. The dot product can be expressed as:

$$D \cdot P_n = \sum_{j=1}^{m} D_j P_{n,j}$$

[0017] The dot product of the input 'D' and the memorized value P_n is a measure of the similarity of the input data to the memorized data, in accordance with some embodiments. In some embodiments, the memorized patterns P_n are encoded as conductances G in analog memory elements (e.g., phase change memory elements placed in an array). In some embodiments, the input vector is encoded as a set of voltages V on a bus with a pulse duration of t. Then, the charge Q accumulated on a word-line capacitor is expressed as:

$$Q_n = t \sum_{j=1}^{m} V_j G_{n,j}$$

[0018] Alternatively, in some embodiments, voltages can be kept constant and the input pattern can be encoded by the duration of the pulse. Then the charge Q accumulated on a word-line capacitor is expressed as:

$$Q_n = V \sum_{j=1}^{m} t_j G_{n,j}$$

[0019] In some embodiments, a scheme (e.g., apparatus and method) is provided for such computation to be performed naturally and in parallel, without the need for reading the memory, fetching the data to a processor, and writing the result back to the memory. As such, in-memory computation may be performed at much faster pace than any known scheme.

[0020] One known scheme uses Static Random Access Memory (SRAM) array in which data is written into the SRAM memory as 4-bit binary numbers (i.e., data is recorded in binary form such that four bits are used per number). Computations in such a scheme are made by engineering the duration of word-line pulses to eight, four, two, and one times the unit time, according to the order of bits in a 4-bit number. That variation is in addition to the duration or voltage variation between the 4-bit elements of the vector. After applying the word-lines with different pulse durations, an analog-to-digital (A2D) conversion of the memorized data is performed followed by comparison logic. These circuits (e.g., A2D and comparator logic) further delay the process of in-memory computation. Further to ensure stability with respect to within-die variations, SRAM cells are made large in size to perform the in-memory computation. Large SRAM means more space and power consumption.

[0021] In some embodiments, instead of four or more SRAM cells with multiple transistors, one resistive memory element is used, which makes for a denser memory. In some embodiments, the resistive memory element may have a selection transistor. In some embodiments, the selection function is incorporated within the resistive memory element.

[0022] In some embodiments, the resistive memory element is non-volatile in nature, and so compared to the SRAM bit-cells, there is no need to initialize the memory cells before in-memory calculations are performed. In some embodiments, the computation (in this example, the dot product) is performed in-memory and there is no need for A2D conversion of the memorized data and no need for results of the comparator logic. The scheme of the various embodiments is a low power scheme. For example, circuits for providing various signals of precise pulse durations on word-lines are not needed in the various embodiments.

[0023] In the following description, numerous details are discussed to provide a more thorough explanation of the embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0024] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0025] Throughout the specification, and in the claims, the term "connected" means a direct connection, such as electrical, mechanical, or magnetic connection between the things that are connected, without any intermediary devices. The term "coupled" means a direct or indirect connection, such as a direct electrical, mechanical, or magnetic connection between the things that are connected or an indirect connection, through one or more passive or active intermediary devices. The term "circuit" or "module" may refer to one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" may refer to at least one current signal, voltage signal, magnetic signal, or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0026] The terms "substantially," "close," "approximately," "near," and "about," generally refer to being within +/- 10% of a target value (unless specifically specified). Unless otherwise specified the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0027] For the purposes of the present disclosure, phrases "A and/or B" and "A or B" mean (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C). The terms "left," "right," "front," "back," "top," "bottom," "over," "under," and the like in the

description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions.

[0028] For purposes of the embodiments, the transistors in various circuits and logic blocks described here are metal oxide semiconductor (MOS) transistors or their derivatives, where the MOS transistors include drain, source, gate, and bulk terminals. The transistors and/or the MOS transistor derivatives also include Tri-Gate and FinFET transistors, Gate All Around Cylindrical Transistors, Tunneling FET (TFET), Square Wire, or Rectangular Ribbon Transistors, ferroelectric FET (FeFETs), or other devices implementing transistor functionality like carbon nanotubes or spintronic devices. MOSFET symmetrical source and drain terminals i.e., are identical terminals and are interchangeably used here. A TFET device, on the other hand, has asymmetric Source and Drain terminals. Those skilled in the art will appreciate that other transistors, for example, Bi-polar junction transistors (BJT PNP/NPN), BiCMOS, CMOS, etc., may be used without departing from the scope of the disclosure.

[0029] **Fig. 1A** illustrates scheme 100 of an analog in-memory pattern matching with the use of resistive memory elements, in accordance with some embodiments. In some embodiments, scheme 100 comprises resistive random access memory (RRAM) 101, Row Decoder 102, Column Decoder 103, and Logic 104 which is operable to cause RRAM 101 to perform in-memory pattern matching operation. In some embodiments, RRAM 101 comprises an array (e.g., rows and columns) of RRAM bit-cells 101a. In some embodiments, a column of the array is accessible by activating or selecting a word-line. This function may be performed by Column Decoder 103.

[0030] In some embodiments, a row of the array is accessible by activating or selecting a bit-line. This function may be performed by Row Decoder 102. As such, Row Decoder 102 and Colum Decoder 103 can select a RRAM bit-cell 101a. In some embodiments, RRAM bit-cells may be programmed one at a time. One way to program the RRAM bit-cells is to change their resistance(s). So as not to obscure various embodiments, the RRAM bit-cells are phase change memory (PCM) based bit-cells. However, the embodiments are not limited to PCM bit-cells, and other types of RRAM may be used for fast in-memory computations. For example, magnetic RAM (spin transfer torque RAM or spin Hall effect RAM), ferroelectric RAM, ferroelectric tunnel junction RAM, conductive oxide RAM, conductive bridge RAM may be used as bit-cells.

[0031] **Fig. 1B** illustrates plot 120 indicating the dependence of resistance of RRAM element 101a of **Fig. 1A** on a number of switching pulses. Here, the x-axis is a number of

switching pulses applied to the RRAM bit-cell, while the y-axis is the resistance in Ohms. Plot 120 illustrates that the ability to switch the resistance of a PCM element over a large range by using different number of switching pulses. In this example, the resistance of RRAM bit-cell 101a can be set to a range of values (e.g., sixteen distinguishable levels of resistance). RRAM bit-cell 101a also retains its conductance between the applications of setting pulses even if the power to RRAM 101 is switched off. As such, the RRAM of the various embodiments is a non-volatile memory.

[0032] In some embodiments, Logic 104 is operable to perform pattern matching by computing the dot product of an input data vector D and a memorized pattern P_n both real-valued vectors of length m. The dot product is expressed as:

$$D \cdot P_n = \sum_{j=1}^{m} D_j P_{n,j}$$

[0033] The dot product of the input D and the memorized value P_n is a measure of the similarity of the input data to the memorized data, in accordance with some embodiments. In some embodiments, the memorized patterns P_n are encoded as conductances G in the analog memory elements (e.g., RRAM cell 101a). In some embodiments, the input vector is encoded via Row and Column Decoders 102 and 103 as a set of voltages V on a bus with a pulse duration of t. Then, the charge Q accumulated on a word-line capacitor is expressed as:

$$Q_n = t \sum_{j=1}^{m} V_j G_{n,j}$$

[0034] In some embodiments, the dot product is calculated per row or column (e.g., per vector) of the memory array. In some embodiments, upon determining the dot products of two vectors (e.g., by selecting a row or a column), Euclidian distance between the two vectors is determined using the dot products. Euclidean distance or Euclidean metric is the "ordinary" (i.e., straight-line) distance between two points in a Euclidean space.

[0035] **Figs. 2A-B** illustrate resistive memory bit-cells 200 and 220, respectively, for use in the scheme of **Fig. 1A**, in accordance with some embodiments. It is pointed out that those elements of **Figs. 2A-B** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0036] With reference to **Fig. 2A**, in some embodiments, resistive memory bit-cell 200 comprises a bit-line (BL), a word-line (WL), a select-line (SL), a select transistor M_{select}, non-volatile resistive memory (NVM) element 201, and contacts 202 and 203 (e.g., metal

contacts such as Cu contacts). In some embodiments, the WL is coupled to the source terminal of the select transistor M_{select} while the SL is coupled to the gate terminals of the select transistor M_{select}. In some embodiments, SL is coupled to ground. While the embodiment of **Fig. 2A** is described with reference to an n-type select transistor M_{select}, the bit-cell can also be designed using a p-type select transistor.

[0037] In some embodiments, NVM element 201 is a PCM element. In some embodiments, PCM element 201 stores data by altering the state of the matter from which PCM element 201 is fabricated. For example, the structure of the material of PCM element 201 can change rapidly back and forth between amorphous and crystalline on a microscopic scale. In the amorphous or disordered phase, the material has high electrical resistance. In the crystalline or ordered phase, the resistance of the material is reduced. This allows electrical current to be switched on and off, representing digital high and low states.

[0038] The switching between amorphous and crystalline states is typically induced by heating through optical pulses or electrical (Joule) heating. The optical and electronic properties can vary considerably between the amorphous and crystalline phases, and this combination of optical and electrical contrast and repeated switching allows data storage. In some embodiments, to program PCM element 201, select transistor M_{select} is turned on via SL and then BL is activated to pass current through PCM element 201 to cause its material to change its state. In some embodiments, PCM element 201 has the ability to achieve a number of particular intermediary states. As such, PCM element 201 has the ability to hold multiple bits in a single cell.

[0039] With reference to **Fig. 2B**, in some embodiments, resistive memory bit-cell 220 comprises BL, WL, NVM element 201, contact 202, and selector 223. In this case, instead of having the select transistor M_{select}, the selection function is integrated with NVM element 201 as selection layer 223 (or selector 223). As sufficient voltage is applied between the BL and WL, and hence across the selection layer 223, its conductance decreases and it enables current to be conducted through the cell. At the same time in other cells of the array with smaller voltage drop, conductance is low and current is not conducted.

[0040] In some embodiments, the selector layer 223 is a material possessing a metal-insulator transition (also known as Mott insulator), for example transition metal oxides, like VO_2, ZnO, TiO_2, TaO_x. In some embodiments, chalcogenide materials (e.g., GeSe, $GeTe_6$,) or composite layers such as Si-As-Te can serve as selectors. In some embodiments, a semiconductor diode can perform the role of selector 223.

[0041] **Fig. 3** illustrates NV-PCM element 300/201 for use in the resistive memory bit-cells of **Figs. 2A/B**, in accordance with some embodiments. It is pointed out that those elements of **Fig. 3** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0042] In some embodiments, NV-PCM element 300/201 includes, top electrode 202 (e.g., TiN), heating element 301 (e.g., TiN), active area 302, phase change material 303 (e.g., chalcogenide material), embedded in substrate 304 (e.g., SiO_2), and bottom electrode 203/223/305 (e.g., W) coupled together as shown. Chalcogenide material are formed of elements in Group 16 in the periodic table: sulfur, selenium and tellurium. In some embodiments, the chalcogenide material includes one of: AgInSbTe (Silver-Indium-Antimony-Tellurium) or GeSbTe (Germanium-Antimony-Tellurium or GST). In some embodiments, NV-PCM element 300/201 includes layers of TiN, GST, and W.

[0043] **Fig. 4A** illustrates array 400 of NV PCM bit-cells which are operable for in-memory pattern matching, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 4A** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. So as not to obscure the embodiments, **Fig. 4A** is described with reference to **Fig. 2B**.

[0044] Referring back to **Fig 4A**, in this example, for illustration purposes, two columns are shown with three cells each. However, it is understood that an array of memory has more than two columns and more than three rows, in general. The first column has NV PCM bit-cells 401_{11}, 401_{12}, and 401_{13}. The second column has NV PCM bit-cells 401_{21}, 401_{22}, and 401_{23}. In some embodiments, the first column shares WL1 which is coupled to the selector layers 223 of each NV PCM bit-cell of the first column, while the second column shares WL2 which is coupled to the selector layers 223 of each NV PCM bit-cell of the second column of array 400.

[0045] In some embodiments, the each row shares a bit-line. For example, the first row having cells 401_{11} and 401_{21} share BL1; the second row having cells 401_{12} and 401_{22} share BL2, and the third row having cells 401_{13} and 401_{23} shares BL3. The bit-lines are coupled to contact 202 of each NV PCM bit-cell, in accordance with some embodiments.

[0046] In some embodiments, amplifiers are coupled to each WL. For example, amplifier 402_1 is coupled WL1. Even in the absence of amplifier 402_1, the resistive network gives a useful approximation to calculating the dot product of the two vectors. Here, the

input voltages are V_i, memorized conductances are G_i, the voltage on the capacitor C (e.g., Cc1) is V, and the charge is Q. The capacitor is initialized with zero voltage and equivalently zero charge $Q(0)=0$, $V(0)=0$. The approximate nominal charge, which corresponds to the dot product is expressed as:

$$Q_{nom} = t \sum_{i}^{m} V_i G_i$$

[0047] The current through each cell is expressed as:

$$I_i = G_i(V_i - V)$$

[0048] The accumulated charge obeys the differential equation expressed as:

$$\frac{dQ}{dt} = \sum_{i} G_i(V_i - V) = I_s - \frac{G_s}{C} Q$$

where I_s is the current through the NVM element, and where the sum of currents at $t=0$ (when $V=0$) and the sum of conductances are expressed as:

$$I_s = \sum_{i} G_i V_i$$

$$G_s = \sum_{i} G_i$$

[0049] The solution of the differential equation with zero initial charge $Q(0)=0$ is expressed as:

$$Q = (1 - e^{\left(-\frac{tG_s}{C}\right)}) \frac{CI_s}{G_s}$$

[0050] Or in other words, it is proportional to the nominal charge Q_{nom} (i.e., the dot product), and expressed as:

$$Q = Q_{nom}(1 - e^{-x}) \frac{1}{x} = Q_{nom} F(x)$$

[0051] Where the variable x depends merely on the memorized pattern, but not the input pattern:

$$x = \frac{tG_s}{C}$$

In other words $Q(0) = Q_{nom}(0)$ and the error factor F(x) grows with time.

[0052] In some embodiments, when multiple input patterns are compared with the same memorized patters, the factor $F(x)$ does not matter. In some embodiments, for specific set of memorized patterns (e.g., Gabor filters) which are normalized, then G_s is the same. As such, the same input pattern can be compared with the same memorized pattern.

[0053] For typical values of 32 bit-cells where the resistance of a single bit-cell is 100kOhm and the pulse duration is 5ps,

$$x = \frac{5e-12 \times 32 \times 1e-5}{20e-15} = 0.08$$

[0054] In one example, the error introduced by the factor $F(x)$ is less than 6%, which is equal to the error of a 4-bit approximate digital calculation of the known SRAM based scheme. When x is not small, and the factor $F(x)$ can be calibrated out by applying the same voltage V_c to all inputs (e.g., using different pulse duration t'), then the calibration charge is expressed as:

$$Q_c = cV_c(1 - e^{-x'})$$

$$x' = \frac{t'G_s}{C}$$

which is merely a function of the sum of conductances G_s (i.e., the pertinent memorized pattern). For not too large of x', the calibration charge is approximately proportional to the sum of conductances:

$$Q_c \approx G_s V_c t'$$

In some embodiments, an additional analog memory cell is coupled to the word-line which will contain the calibration factor $1/F(x)$ set based on the calibration charge Q_c.

[0055] In some embodiments, array 400, which is capable of in-memory computation, comprises NV PCM bit-cells and an integrator for each column. In some embodiments, the first integrator integrates the charge collected at the end of WL1 via capacitor Cc1. In some embodiments, a first terminal of capacitor Cc1 is coupled to WL1 and a second terminal of capacitor Cc1 is coupled to a first output V_{o1}. In some embodiments, the first integrator comprises a first amplifier 402_1 having a first input (e.g., negative input) coupled to the first terminal of Cc1 and a second input (e.g., positive input) coupled to ground. In some embodiments, the output of the first integrator is coupled to V_{o1}. Here, labels for signal names and nodes are interchangeably used. For example, V_{o1} may refer to node V_{o1} or voltage V_{o1} depending on the context of the sentence.

[0056] In some embodiments, the second integrator integrates the charge collected at the end of WL2 via capacitor Cc2. In some embodiments, a first terminal of capacitor Cc2 is coupled to WL2 and a second terminal of capacitor Cc2 is coupled to a second output V_{o2}. In some embodiments, the second integrator comprises a second amplifier 402_2 having a first input (e.g., a negative input) coupled to the first terminal of Cc2 and a second input (e.g., a

positive input) coupled to ground. In some embodiments, the output of the second integrator is coupled to V_{o2}.

[0057] To perform in-memory dot product computation, first, the NV PCMs are programmed to store a logic state, in accordance with some embodiments. Then, different voltages are applied to the bit-lines for a selected column (e.g., selected WL), and the dot product is computed for that selected column. **Fig. 4B** illustrates the programming aspect while **Fig. 4C** illustrates the dot computation aspect of the various embodiments.

[0058] **Fig. 4B** illustrates array 420 (same as array 400 of **Fig. 4A)** showing programming of an NV PCM bit-cell, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 4B** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0059] In some embodiments, the NV-PCM based bit-cell is programmed one bit-cell at time. In this example, bit-cell 401_{12} is being programmed. To program bit-cell 401_{12}, all word-lines except for WL1 are set to ground (i.e., WL1=1 and WL2=0) and all bit-lines except for BL2 are set to ground (i.e., BL2=1, BL1=BL3=0), in accordance with some embodiments. In this example, BL2 is set to logic high (e.g., 1V). As such, bit-cell 401_{12} is selected. In some embodiments, depending on the applied voltage on BL2, NV-PCM element 201 is programmed (e.g., its resistance is programmed).

[0060] **Fig. 4C** illustrates array 430 (same as array 400 of **Fig. 4A)** showing computation of dot product for a row (or column) of the array, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 4C** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0061] In some embodiments, to perform the in-memory computation process, a column of array 430 is selected and voltages (e.g., Vr1, Vr2, Vr3, etc.) are applied on the BLs. In this example, all WLs are set to ground except for the one for which the dot product is being computed (i.e., WL2=0 while WL1 is un-driven). In some embodiments, WL1 is floated while WL2 is ground to perform dot product of the column controlled by WL1. In some embodiments, WL1 is floated by causing the WL driver (not shown) that drives WL1 to be in a tri-state/floating condition (e.g., high impedance non-driving state). In this example, BL1 is charged to Vr1, BL2 is charged to Vr2, and BL3 is charged to Vr3. In some embodiments, the column-wise dot products can be computed independently in parallel. In some embodiments, all world lines WL remain un-driven.

[0062] In some embodiments, the overall charge is accumulated on WL1 (which is being floated in this case) and this charge is transferred to capacitor Cc1 by charge redistribution and detected as voltage V_{o1}, in accordance with some embodiments. In some embodiments, the read voltage V (e.g., Vr1, Vr2, Vr3, etc. which are applied to the BLs) is smaller than the threshold voltage for the phase-change element 201 in order to not disturb the memorized data. So as not to obscure the embodiments, the sense amplifier for reading and the associated multiplexers coupled to the BLs are not shown.

[0063] Due to the property of operational transconductance amplifier 402_1 in this scheme, the output voltage V_{o1} is proportional to the current conducted through all elements of the word (e.g., column with floating WL1). The output voltage V_{o1} is proportional to:

$$V_{o1} \sim t \sum_{j=1}^{m} Vr_j G_{n,j}$$

[0064] The following section provides some technical basis for the scheme of various embodiments regarding in-memory computation using resistive memories.

[0065] **Fig. 5** illustrates flowchart 500 of a method for determining a dot product of input voltages and conductance using array 400 of **Fig. 4A**, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 5** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0066] Although the blocks in the flowchart with reference to **Fig. 5** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/blocks may be performed in parallel. Some of the blocks and/or operations listed in **Fig. 5** are optional in accordance with certain embodiments. The numbering of the blocks presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur. Additionally, operations from the various flows may be utilized in a variety of combinations.

[0067] At block 501, WL1 is selected. For example, WL1 is set to -1 as described with reference to **Fig. 4B**. As such, the first column which is controlled by WL1 is selected. Referring back to **Fig. 5**, at block 502, BL2 is selected. For example, BL2 is set to 1. By selecting BL2, the bit-cell coupled to BL2 and WL1 is selected. At block 503, BL1 and other bit-lines (other than BL2) are unselected. For example, BL1 and BL3 are set to zero.

[0068] At block 504, a second resistive memory cell 401_{12} having a first terminal coupled to BL2 and a second terminal coupled to WL1 is programmed. For example, a

current is passed through the second resistive memory cell 401_{12} to cause its phase to change. As such, resistance of the second resistive memory cell 401_{12} is adjusted.

[0069] At block 505, a first voltage (e.g., Vr1) voltage is applied to BL1 as described with reference to **Fig. 4C**, where BL1 is coupled to a first terminal of a first resistive memory cell 401_{11}. Likewise, a second voltage (e.g., Vr2) is applied to BL2, where BL2 is coupled to a first terminal of the second resistive memory cell 401_{12}. The second resistive memory cell 401_{12} has a second terminal coupled to the WL1. A third voltage (e.g., Vr3) is applied to BL3, where BL3 is coupled to a first terminal of a third resistive memory cell 401_{13}. The third resistive memory cell 401_{13} has a third terminal coupled to the WL1. The first, second, third voltages may be the same voltages or different voltages (or a combination of both), in accordance with some embodiments.

[0070] At block 506, a dot product is determined of a sum of the first, second, and third voltages (i.e., Vr1, Vr2, and Vr3) applied to the first, second, and third bit-lines, respectively, and conductance of the first, second, and third resistive memory cells. In some embodiments, the WL1 is floated while other word-lines are set to 0V. In some embodiments, the above process is repeated for each column, and dot products of each vector (i.e., bit-cells of a column) is determined.

[0071] **Fig. 6A** illustrates array 600 of NV PCM bit-cells which are operable for in-memory pattern matching, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 6A** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. So as not to obscure the embodiments, **Fig. 6A** is described with reference to **Fig. 2A**.

[0072] Referring back to **Fig 6A**, in this example, for illustration purposes, two columns are shown with three cells each. However, it is understood that an array of memory has more than two columns and more than three rows, in general. The first column has NV PCM bit-cells 601_{11}, 601_{12}, and 601_{13}. The second column has NV PCM bit-cells 601_{21}, 601_{22}, and 601_{23}. In some embodiments, the first column shares WL1 which is coupled to the source terminals of the select transistors of the first column, while the second column shares WL2 which is coupled to the source terminals of the select transistors of the second column.

[0073] In some embodiments, a first select line (SL1) is coupled to the gate terminals of the select transistors of the first column. In some embodiments, a second select line (SL2) is coupled to the gate terminals of the select transistors of the second column. In some embodiments, the each row shares a bit-line. For example, the first row having cells 601_{11}

and 601_{21} share BL1; the second row having cells 601_{12} and 601_{22} share BL2, and the third row having cells 601_{13} and 601_{23} shares BL3.

[0074] In some embodiments, array 600, which is capable of in-memory computation, comprises NV PCM bit-cells and an integrator for each column. In some embodiments, the first integrator integrates the charge collected at the end of WL1 via capacitor Cc1. In some embodiments, a first terminal of capacitor Cc1 is coupled to WL1 and a second terminal of capacitor Cc1 is coupled to a first output V_{o1}. In some embodiments, the first integrator comprises first amplifier 402_1 having a first input (e.g., negative input) coupled to the first terminal of Cc1 and a second input (e.g., positive input) coupled to ground. In some embodiments, the output of the first integrator is coupled to V_{o1}. Here, labels for signal names and nodes are interchangeably used. For example, V_{o1} may refer to node V_{o1} or voltage V_{o1} depending on the context of the sentence.

[0075] In some embodiments, the second integrator integrates the charge collected at the end of WL2 via capacitor Cc2. In some embodiments, a first terminal of capacitor Cc2 is coupled to WL2 and a second terminal of capacitor Cc2 is coupled to a second output V_{o2}. In some embodiments, the second integrator comprises a second amplifier 402_2 having a first input (e.g., a negative input) coupled to the first terminal of Cc2 and a second input (e.g., a positive input) coupled to ground. In some embodiments, the output of the second integrator is coupled to V_{o2}.

[0076] To perform in-memory dot product computation, first, the NV PCMs are programmed to store a logic state, in accordance with some embodiments. Then, different voltages are applied to the bit-lines for a selected column (e.g., selected WL), and the dot product is computed for that selected column. **Fig. 6B** illustrates the programming aspect while **Fig. 6C** illustrates the dot computation aspect of the various embodiments.

[0077] **Fig. 6B** illustrates array 620 (same as array 600 of **Fig. 6A)** showing programming of an NV PCM bit-cell, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 6B** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0078] In some embodiments, the NV-PCM based bit-cell is programmed one bit-cell at time. In this example, bit-cell 601_{12} is being programmed. To program bit-cell 601_{12}, all select lines except for SL1 is set to ground (i.e., SL1=1), all bit-lines except for BL2 is set to ground (i.e., BL2=1), and word-lines are grounded (e.g., WL1=WL2=0), in accordance with some embodiments. In this example, SL1 and BL2 are set to logic high (e.g., 1V). As such,

bit-cell 601_{12} is selected and the select transistor M_{select} is turned on. In some embodiments, depending on the applied voltage on BL2, NV-PCM element 201 is programmed (e.g., its resistance is programmed).

[0079] **Fig. 6C** illustrates array 630 (same as array 600 of **Fig. 6A)** showing computation of dot product for a row of the array, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 6C** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0080] In some embodiments, to perform the in-memory computation process, a column of array 630 is selected and voltages (e.g., Vr1, Vr2, Vr3, etc.) are applied on the BLs. In this example, all WLs are set to ground except for the one for which the dot product is being computed (e.g., WL2=0 while WL1 is un-driven), and select lines are set to ground except for the one for which the dot product is being computed (e.g., SL2=0; SL1=1 turned high to turn on the select transistors). In some embodiments, WL1 is floated while WL2 is set to ground. In some embodiments, WL1 is floated by causing the WL driver (not shown) that drives WL1 to be in a tri-state condition (e.g., high impedance non-driving state). In this example, BL1 is charged to Vr1, BL2 is charged to Vr2, and BL3 is charged to Vr3. In some embodiments, the column-wise dot products can be computed independently in parallel. In some embodiments, all select lines are turned to high voltage (e.g., SL=1) and all world lines WL remain un-driven.

[0081] The overall charge is accumulated on WL1 (which is being floated in this case) and this charge is transferred to capacitor Cc1 and detected as voltage V_{o1}, in accordance with some embodiments. In some embodiments, the read voltage V (e.g., Vr1, Vr2, Vr3, etc. which are applied to the BLs) is smaller than the threshold voltage for the phase-change element 201 in order to not disturb the memorized data. So as not to obscure the embodiments, the sense amplifier for reading and the associated multiplexers coupled to the BLs are not shown. As discussed with reference to **Fig. 4C**, here, output Vo1 also indicates the dot product.

[0082] **Fig. 7** illustrates flowchart 700 of a method for determining a dot product of input voltages and conductance using the array of **Fig. 6A**, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 7** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0083] Although the blocks in the flowchart with reference to **Fig. 7** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/blocks may be performed in parallel. Some of the blocks and/or operations listed in **Fig. 7** are optional in accordance with certain embodiments. The numbering of the blocks presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur. Additionally, operations from the various flows may be utilized in a variety of combinations.

[0084] At block 701, SL1 is selected (e.g., SL1=1). As such, the first column which is controlled by WL1 is selected. At block 702, BL2 is selected. For example, BL2 is set to 1. By selecting BL2, the bit-cell coupled to BL2, SL1, and WL1 is selected. At block 703, BL1 and other bit-lines (other than BL2) are unselected. For example, BL1 and BL3 are set to zero. BL1 and other bit-lines (other than BL2) are unselected. For example, BL1 and BL3 are set to zero. SL2 and other select-lines (other than SL2) are unselected. For example, SL2 is set to zero. Word-lines (WLs) are unselected (e.g., WL1 and WL2 are set to ground). As such, in this example, bit-cell 601_{12} is selected while other bit-cells are unselected.

[0085] At block 704, a second resistive memory cell 601_{12} having a first terminal coupled to BL2 and a second terminal coupled to WL1 via the source terminal of M_{select}, and coupled to SL1 via the gate terminal of M_{select}, is programmed. For example, a current is passed through the second resistive memory cell 601_{12} to cause its phase to change. As such, resistance of the second resistive memory cell 601_{12} is adjusted.

[0086] At block 705, a first voltage (e.g., Vr1) voltage is applied to BL1, where BL1 is coupled to a first terminal of a first resistive memory cell 601_{11}. Likewise, a second voltage (e.g., Vr2) is applied to BL2, where BL2 is coupled to a first terminal of the second resistive memory cell 601_{12}. The second resistive memory cell 601_{12} has a second terminal coupled to the WL1. A third voltage (e.g., Vr3) is applied to BL3, where BL3 is coupled to a first terminal of a third resistive memory cell 601_{13}. The third resistive memory cell 601_{13} has a third terminal coupled to the WL1. The first, second, third voltages may be the same voltages or different voltages (or a combination of both).

[0087] At block 706, a dot product is determined of a sum of the first, second, and third voltages (i.e., Vr1, Vr2, and Vr3) applied to the first, second, and third bit-lines, respectively, and conductance of the first, second, and third resistive memory cells. In some embodiments, the WL1 is floated while other word-lines are set to 0V while the select lines are set to high. In some embodiments, the above process is repeated for each column, and dot products of each vector (i.e., bit-cells of a column) is determined.

[0088] In some embodiments, flowcharts 500 and 700 of **Fig. 5** and **Fig. 7**, respectively, are performed or controlled by a program software or instructions. Program software code/instructions associated with flowchart 500 and executed to implement embodiments of the disclosed subject matter may be implemented as part of an operating system or a specific application, component, program, object, module, routine, or other sequence of instructions or organization of sequences of instructions referred to as "program software code/instructions," "operating system program software code/instructions," "application program software code/instructions," or simply "software" or firmware embedded in processor. In some embodiments, the program software code/instructions associated with flowcharts 500/700.

[0089] In some embodiments, the program software code/instructions associated with flowcharts 500/700 are stored in a computer executable storage medium and executed by Processor or Logic 104. Here, computer executable storage medium is a tangible machine readable medium that can be used to store program software code/instructions and data that, when executed by a computing device, causes one or more processors to perform a method(s) as may be recited in one or more accompanying claims directed to the disclosed subject matter.

[0090] The tangible machine readable medium may include storage of the executable software program code/instructions and data in various tangible locations, including for example ROM, volatile RAM, non-volatile memory and/or cache and/or other tangible memory as referenced in the present application. Portions of this program software code/instructions and/or data may be stored in any one of these storage and memory devices. Further, the program software code/instructions can be obtained from other storage, including, e.g., through centralized servers or peer to peer networks and the like, including the Internet. Different portions of the software program code/instructions and data can be obtained at different times and in different communication sessions or in the same communication session.

[0091] The software program code/instructions (associated with flowcharts 500/700 and other embodiments) and data can be obtained in their entirety prior to the execution of a respective software program or application by the computing device. Alternatively, portions of the software program code/instructions and data can be obtained dynamically, e.g., just in time, when needed for execution. Alternatively, some combination of these ways of obtaining the software program code/instructions and data may occur, e.g., for different applications, components, programs, objects, modules, routines or other sequences of

instructions or organization of sequences of instructions, by way of example. Thus, it is not required that the data and instructions be on a tangible machine readable medium in entirety at a particular instance of time.

[0092] Examples of tangible computer-readable media include but are not limited to recordable and non-recordable type media such as volatile and non-volatile memory devices, read only memory (ROM), random access memory (RAM), flash memory devices, floppy and other removable disks, magnetic storage media, optical storage media (e.g., Compact Disk Read-Only Memory (CD ROMS), Digital Versatile Disks (DVDs), etc.), among others. The software program code/instructions may be temporarily stored in digital tangible communication links while implementing electrical, optical, acoustical or other forms of propagating signals, such as carrier waves, infrared signals, digital signals, etc. through such tangible communication links.

[0093] In general, tangible machine readable medium includes any tangible mechanism that provides (i.e., stores and/or transmits in digital form, e.g., data packets) information in a form accessible by a machine (i.e., a computing device), which may be included, e.g., in a communication device, a computing device, a network device, a personal digital assistant, a manufacturing tool, a mobile communication device, whether or not able to download and run applications and subsidized applications from the communication network, such as the Internet, e.g., an iPhone®, Galaxy®, Blackberry® Droid®, or the like, or any other device including a computing device. In one embodiment, processor-based system is in a form of or included within a PDA (personal digital assistant), a cellular phone, a notebook computer, a tablet, a game console, a set top box, an embedded system, a TV (television), a personal desktop computer, etc. Alternatively, the traditional communication applications and subsidized application(s) may be used in some embodiments of the disclosed subject matter.

[0094] While various embodiments use labels such as WL and BL, these labels can be switched along with their functions. For example, WL in the described figures can be BL and BL in the described figures can be WL. As such, relabeling various nodes of the described figures do not change the essence of the embodiments. Likewise, the terms describing an array, such as columns and rows of an array, can be interchangeably used. For example, the term column can refer to a row and the term row can refer to a column without changing the essence of the embodiments.

[0095] **Fig. 8** illustrates a smart device or a computer system or a SoC (System-on-Chip) with the scheme of analog in-memory pattern matching with the use of resistive

memory elements, according to some embodiments. It is pointed out that those elements of **Fig. 8** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0096] **Fig. 8** illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. In some embodiments, computing device 1600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 1600.

[0097] In some embodiments, computing device 1600 includes first processor 1610 with the scheme of analog in-memory pattern matching with the use of resistive memory elements, according to some embodiments discussed. Other blocks of the computing device 1600 may also include the scheme of analog in-memory pattern matching with the use of resistive memory elements, according to some embodiments. The various embodiments of the present disclosure may also comprise a network interface within 1670 such as a wireless interface so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0098] In some embodiments, processor 1610 (and/or processor 1690) can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 1600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0099] In some embodiments, computing device 1600 includes audio subsystem 1620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into computing device 1600, or connected to the computing device 1600. In one embodiment, a user interacts with the computing device 1600 by providing audio commands that are received and processed by processor 1610.

[00100] In some embodiments, computing device 1600 comprises display subsystem 1630. Display subsystem 1630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 1600. Display subsystem 1630 includes display interface 1632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1632 includes logic separate from processor 1610 to perform at least some processing related to the display. In one embodiment, display subsystem 1630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[00101] In some embodiments, computing device 1600 comprises I/O controller 1640. I/O controller 1640 represents hardware devices and software components related to interaction with a user. I/O controller 1640 is operable to manage hardware that is part of audio subsystem 1620 and/or display subsystem 1630. Additionally, I/O controller 1640 illustrates a connection point for additional devices that connect to computing device 1600 through which a user might interact with the system. For example, devices that can be attached to the computing device 1600 might include microphone devices, speaker or stereo systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[00102] As mentioned above, I/O controller 1640 can interact with audio subsystem 1620 and/or display subsystem 1630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 1600. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 1630 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 1640. There can also be additional buttons or switches on the computing device 1600 to provide I/O functions managed by I/O controller 1640.

[00103] In some embodiments, I/O controller 1640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the computing device 1600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[00104] In some embodiments, computing device 1600 includes power management 1650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 1660 includes memory devices for storing information

in computing device 1600. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 1660 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 1600. In some embodiments, Memory subsystem 1660 includes the scheme of analog in-memory pattern matching with the use of resistive memory elements.

[00105] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 1660) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 1660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[00106] In some embodiments, computing device 1600 comprises connectivity 1670. Connectivity 1670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 1600 to communicate with external devices. The computing device 1600 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[00107] Connectivity 1670 can include multiple different types of connectivity. To generalize, the computing device 1600 is illustrated with cellular connectivity 1672 and wireless connectivity 1674. Cellular connectivity 1672 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 1674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication. In some embodiments, Connectivity 1670 includes parallel sensing arrays as described with reference to **Figs. 10-13**.

[00108] In some embodiments, computing device 1600 comprises peripheral connections 1680. Peripheral connections 1680 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 1600 could both be a peripheral device ("to" 1682) to other computing devices, as well as have peripheral devices ("from" 1684) connected to it. The computing device 1600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 1600. Additionally, a docking connector can allow computing device 1600 to connect to certain peripherals that allow the computing device 1600 to control content output, for example, to audiovisual or other systems.

[00109] In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 1600 can make peripheral connections 1680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[00110] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[00111] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[00112] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[00113] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[00114] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[00115] For example, an apparatus is provided which comprises: a first word-line; a first bit-line; a second bit-line; a first resistive memory cell having a first terminal coupled to the first bit-line and a second terminal coupled to the first word-line; a second resistive memory cell having a first terminal coupled to the second bit-line and a second terminal coupled to the first word-line; and a first integrator coupled to the first word-line. In some embodiments, first and second resistive memory cells are phase-change memory (PCM) cells. In some embodiments, the PCM cells includes chalcogenide material. In some embodiments, the chalcogenide material includes one of: AgInSbTe or GeSbTe. In some embodiments, the PCM cells include layers of TiN, GeSbTe (GST), and W.

[00116] In some embodiments, the first integrator comprises: a capacitor having a first terminal coupled to the first word-line and a second terminal coupled to a first output node. In some embodiments, the first integrator comprises: an amplifier having a first input coupled to the first word-line and a second input coupled to ground, and an output coupled to the first output node. In some embodiments, the first integrator has an output which is to indicate a

dot product of a sum of voltages applied to the first and second bit-lines and conductance of the first and second resistive memory cells.

[00117] In some embodiments, the apparatus comprises: a second word-line; a third resistive memory cell having a first terminal coupled to the first bit-line and a second terminal coupled to the second word-line; a fourth resistive memory cell having a first terminal coupled to the second bit-line and a second terminal coupled to the second word-line; and a second integrator coupled to the second word-line. In some embodiments, the third and fourth resistive memory cells are phase-change memory cells. In some embodiments, the second integrator comprises: a capacitor having a first terminal coupled to the second word-line and a second terminal coupled to a second output node.

[00118] In some embodiments, the second integrator comprises: an amplifier having a first input coupled to the second word-line and a second input coupled to ground, and an output coupled to the second output node. In some embodiments, the second integrator has an output which is to indicate a dot product of a sum of voltages applied to the third and fourth bit-lines and conductance of the third and fourth resistive memory cells.

[00119] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, the processor having an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[00120] In another example, a method is provided which comprises: selecting a first word-line; selecting a first bit-line; unselecting the second bit-line; programming a first resistive memory cell having a first terminal coupled to the first bit-line and a second terminal coupled to the first word-line; applying a first voltage to the first bit-line; applying a second voltage to the second bit-line, where the second bit-line is coupled to a first terminal of a second resistive memory cell, the second resistive memory cell having a second terminal coupled to the first word-line; and determining a dot product of a sum of the first and second voltages applied to the first and second bit-lines, respectively, and conductance of the first and second resistive memory cells.

[00121] In some embodiments, selecting the first word-line comprises applying a negative voltage to the first word-line. In some embodiments, selecting the first bit-line comprises applying a positive voltage to the first bit-line. In some embodiments, unselecting the second bit-line comprises applying a ground voltage to the second bit-line. In some embodiments, programming the first resistive memory cell comprises adjusting resistance of the first resistive memory cell. In some embodiments, determining the dot product

comprises: floating the first word-line; and integrating charge on the first word-line in response to floating it, wherein the charge is provided by the first and second resistive memory cells. In some embodiments, the method comprises programming the second resistive memory cell. In some embodiments, the programming the first and second resistive memory cells occurs sequentially.

[00122] In another example, a machine readable storage media is provided having machine readable storage instructions that, when executed, cause one or more machines to perform an operation according to the method described above.

[00123] In another example, an apparatus is provided which comprises: means for selecting a first word-line; means for selecting a first bit-line; means for unselecting the second bit-line; means for programming a first resistive memory cell having a first terminal coupled to the first bit-line and a second terminal coupled to the first word-line; means for applying a first voltage to the first bit-line; means for applying a second voltage to the second bit-line, where the second bit-line is coupled to a first terminal of a second resistive memory cell, the second resistive memory cell having a second terminal coupled to the first word-line; and means for determining a dot product of a sum of the first and second voltages applied to the first and second bit-lines, respectively, and conductance of the first and second resistive memory cells.

[00124] In some embodiments, the means for selecting the first word-line comprises means for applying a negative voltage to the first word-line. In some embodiments, the means for selecting the first bit-line comprises means for applying a positive voltage to the first bit-line. In some embodiments, the means for unselecting the second bit-line comprises means for applying a ground voltage to the second bit-line. In some embodiments, the means for programming the first resistive memory cell comprises means for adjusting resistance of the first resistive memory cell. In some embodiments, the means for determining the dot product comprises: means for floating the first word-line; and means for integrating charge on the first word-line in response to floating it, wherein the charge is provided by the first and second resistive memory cells. In some embodiments, the apparatus means for programming the second resistive memory cell. In some embodiments, the means for programming the first and second resistive memory cells occurs sequentially.

[00125] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, the processor having an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[00126] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:

a first word-line;

a first bit-line;

a second bit-line;

a first resistive memory cell having a first terminal coupled to the first bit-line and a second terminal coupled to the first word-line;

a second resistive memory cell having a first terminal coupled to the second bit-line and a second terminal coupled to the first word-line; and

a first integrator coupled to the first word-line.

2. The apparatus of claim 1, wherein first and second resistive memory cells are phase-change memory (PCM) cells.

3. The apparatus of claim 2, wherein the PCM cells includes chalcogenide material.

4. The apparatus of claim 3, wherein the chalcogenide material includes one of: AgInSbTe or GeSbTe,

5. The apparatus of claim 2, wherein the PCM cells include layers of TiN, GeSbTe (GST), and W.

6. The apparatus of claim 1, wherein the first integrator comprises: a capacitor having a first terminal coupled to the first word-line and a second terminal coupled to a first output node.

7. The apparatus of claim 6, wherein the first integrator comprises: an amplifier having a first input coupled to the first word-line and a second input coupled to ground, and an output coupled to the first output node.

8. The apparatus of claim 1, wherein the first integrator has an output which is to indicate a dot product of a sum of voltages applied to the first and second bit-lines and conductance of the first and second resistive memory cells.

9. The apparatus of claim 1, comprises:

a second word-line;

a third resistive memory cell having a first terminal coupled to the first bit-line and a second terminal coupled to the second word-line;

a fourth resistive memory cell having a first terminal coupled to the second bit-line and a second terminal coupled to the second word-line; and

a second integrator coupled to the second word-line.

10. The apparatus of claim 9, wherein the third and fourth resistive memory cells are phase-change memory cells.

11. The apparatus of claim 9, wherein the second integrator comprises: a capacitor having a first terminal coupled to the second word-line and a second terminal coupled to a second output node.

12. The apparatus of claim 11, wherein the second integrator comprises: an amplifier having a first input coupled to the second word-line and a second input coupled to ground, and an output coupled to the second output node.

13. The apparatus of claim 9, wherein the second integrator has an output which is to indicate a dot product of a sum of voltages applied to the third and fourth bit-lines and conductance of the third and fourth resistive memory cells.

14. A method comprising:

selecting a first word-line;

selecting a first bit-line;

unselecting the second bit-line;

programming a first resistive memory cell having a first terminal coupled to the first bit-line and a second terminal coupled to the first word-line;

applying a first voltage to the first bit-line;

applying a second voltage to the second bit-line, where the second bit-line is coupled to a first terminal of a second resistive memory cell, the second resistive memory cell having a second terminal coupled to the first word-line; and

determining a dot product of a sum of the first and second voltages applied to the first and second bit-lines, respectively, and conductance of the first and second resistive memory cells.

15. The method of claim 14, wherein selecting the first word-line comprises applying a negative voltage to the first word-line.

16. The method of claim 14, wherein selecting the first bit-line comprises applying a positive voltage to the first bit-line.

17. The method of claim 14, wherein unselecting the second bit-line comprises applying a ground voltage to the second bit-line.

18. The method of claim 14, wherein programming the first resistive memory cell comprises adjusting resistance of the first resistive memory cell.

19. The method of claim 14, wherein determining the dot product comprises:

floating the first word-line; and

integrating charge on the first word-line in response to floating it, wherein the charge is provided by the first and second resistive memory cells.

20. The method of claim 14 comprises programming the second resistive memory cell.

21. The method of claim 14, wherein programming the first and second resistive memory cells occurs sequentially.

22. A system comprising:

a memory;

a processor coupled to the memory, the processor having an apparatus according to any one of apparatus claims 1 to 13; and

a wireless interface for allowing the processor to communicate with another device.

23. Machine readable storage media having machine readable storage instructions that, when executed, cause one or more machines to perform an operation according to any one of method claims 14 to 21.

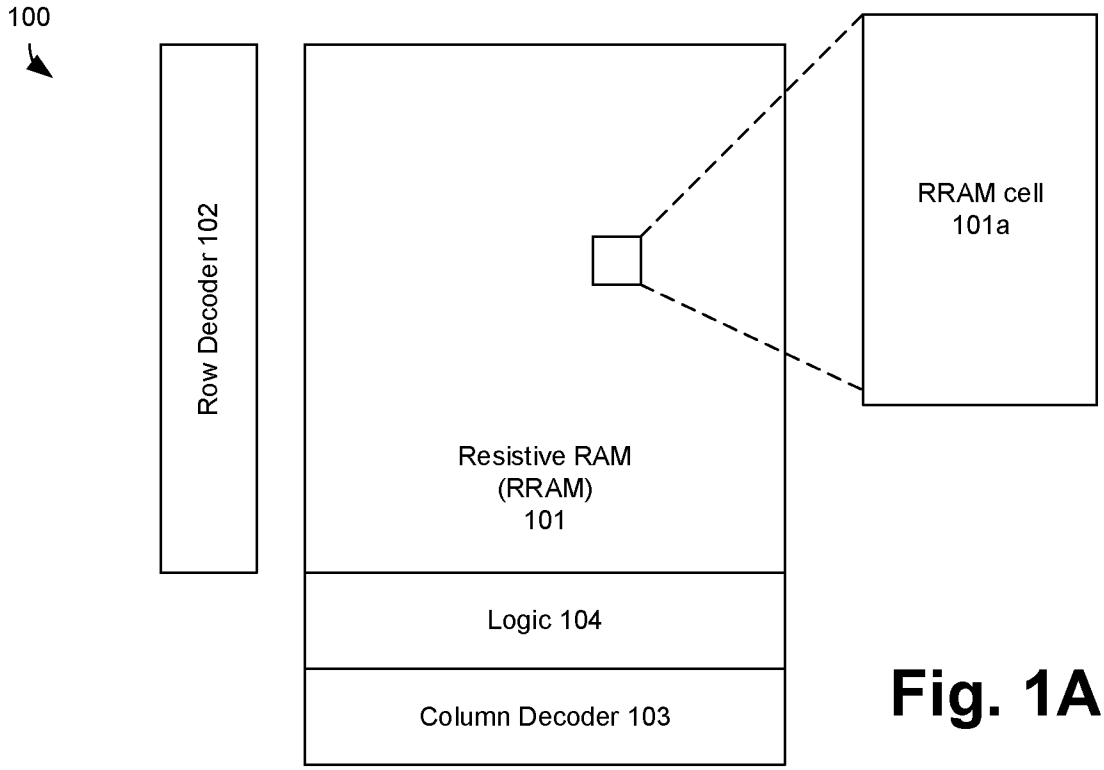

100
Row Decoder 102
Resistive RAM
(RRAM)
101
RRAM cell
101a
Logic 104
Column Decoder 103

Fig. 1A

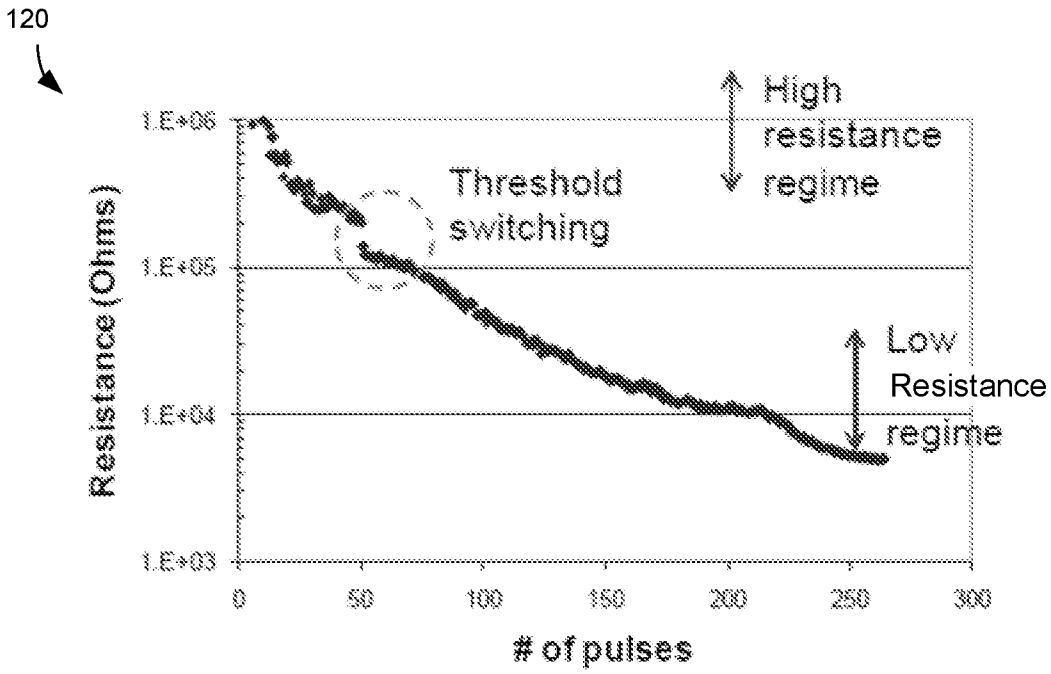

120
High
resistance
regime
Threshold
switching
Low
Resistance
regime
Resistance (Ohms)
1.E+06
1.E+05
1.E+04
1.E+03
0
50
100
150
200
250
300
# of pulses

Fig. 1B

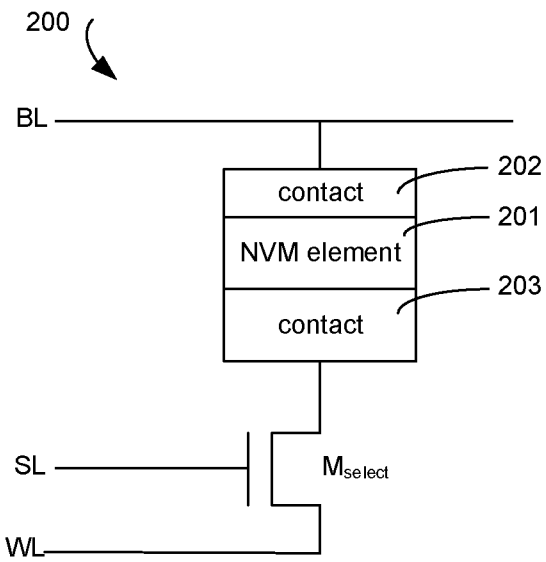


Fig. 2A

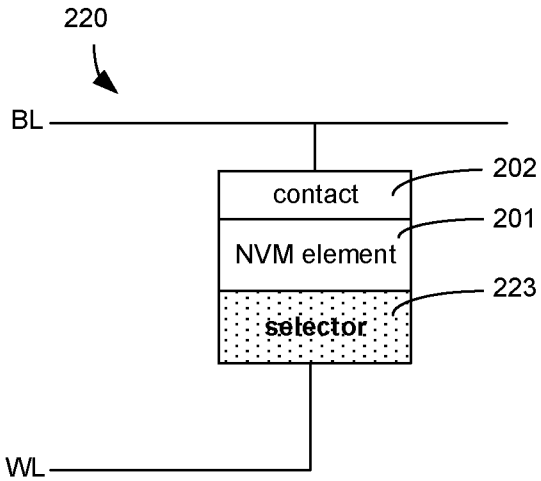


Fig. 2B

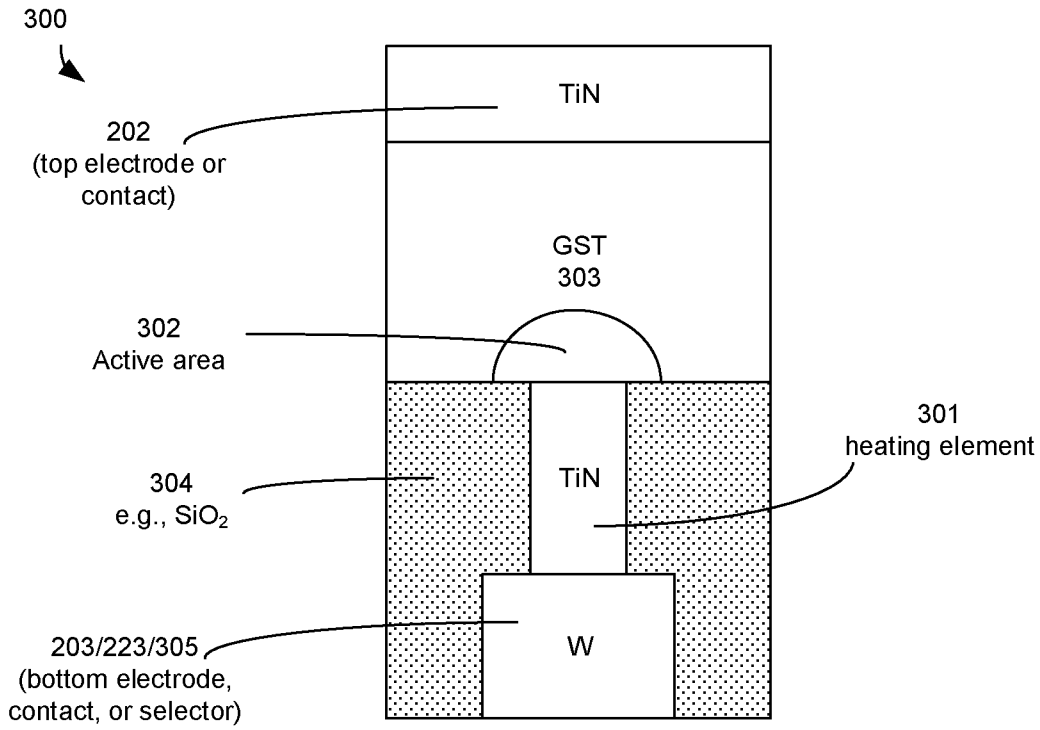


Fig. 3

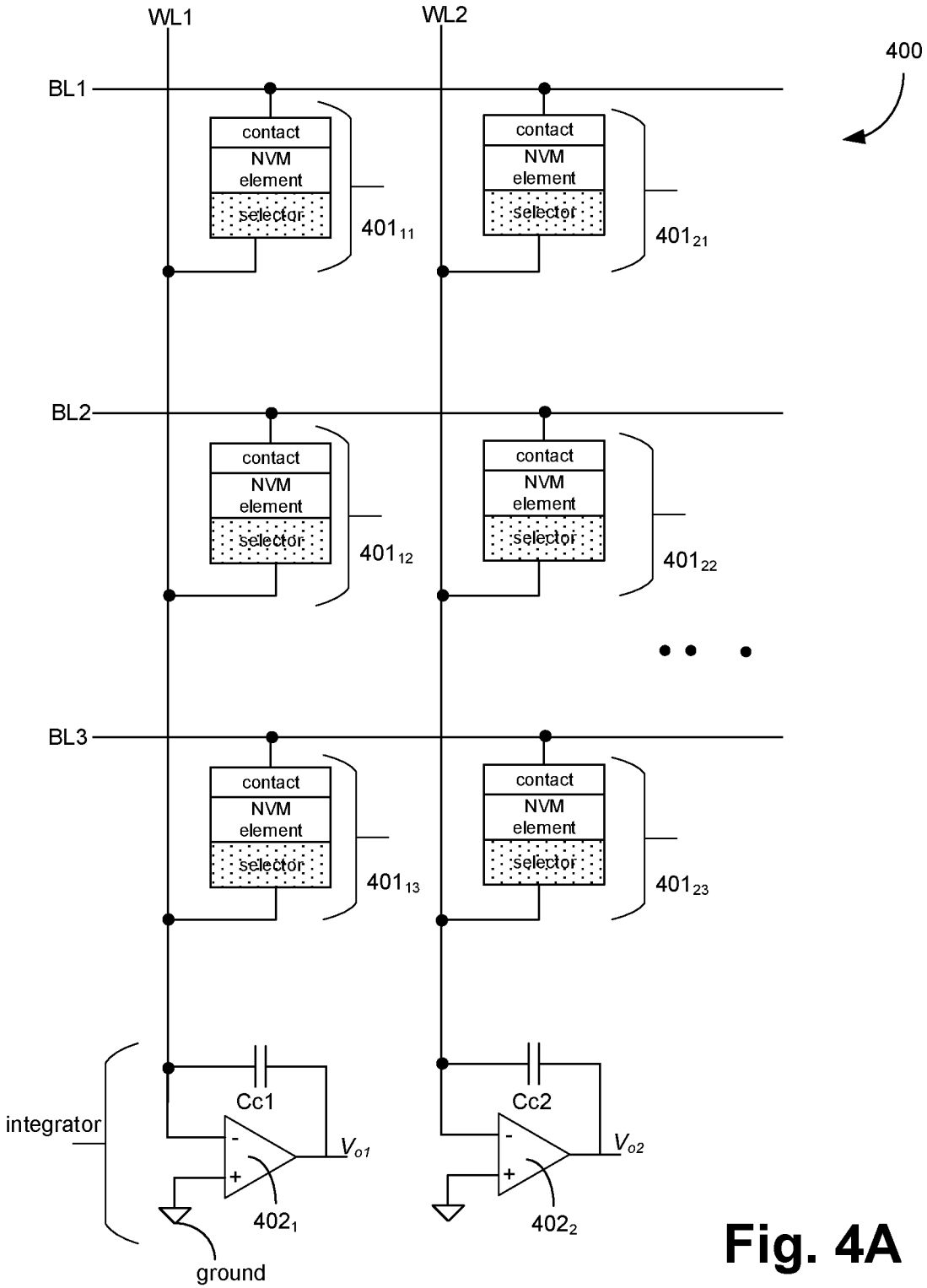

WL1
WL2
400
BL1
BL2
BL3
contact
NVM element
selector
401_{11}
401_{21}
401_{12}
401_{22}
401_{13}
401_{23}
integrator
Cc1
Cc2
V_{o1}
V_{o2}
402_1
402_2
ground

Fig. 4A

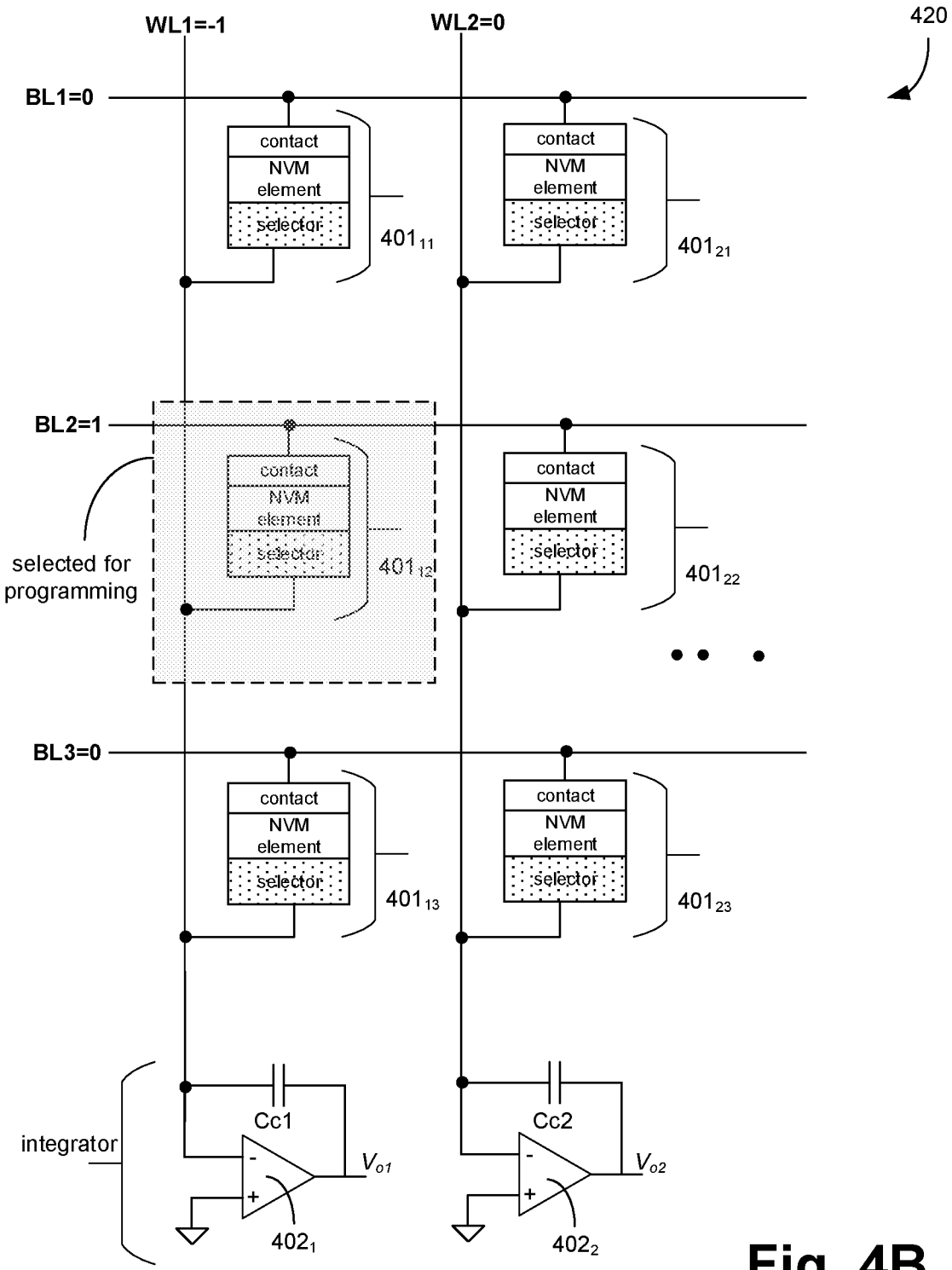

WL1=-1
WL2=0
420
BL1=0
BL2=1
BL3=0
contact
NVM element
selector
401_{11}
401_{21}
401_{12}
401_{22}
401_{13}
401_{23}
selected for programming
integrator
Cc1
Cc2
V_{o1}
V_{o2}
402_1
402_2

Fig. 4B

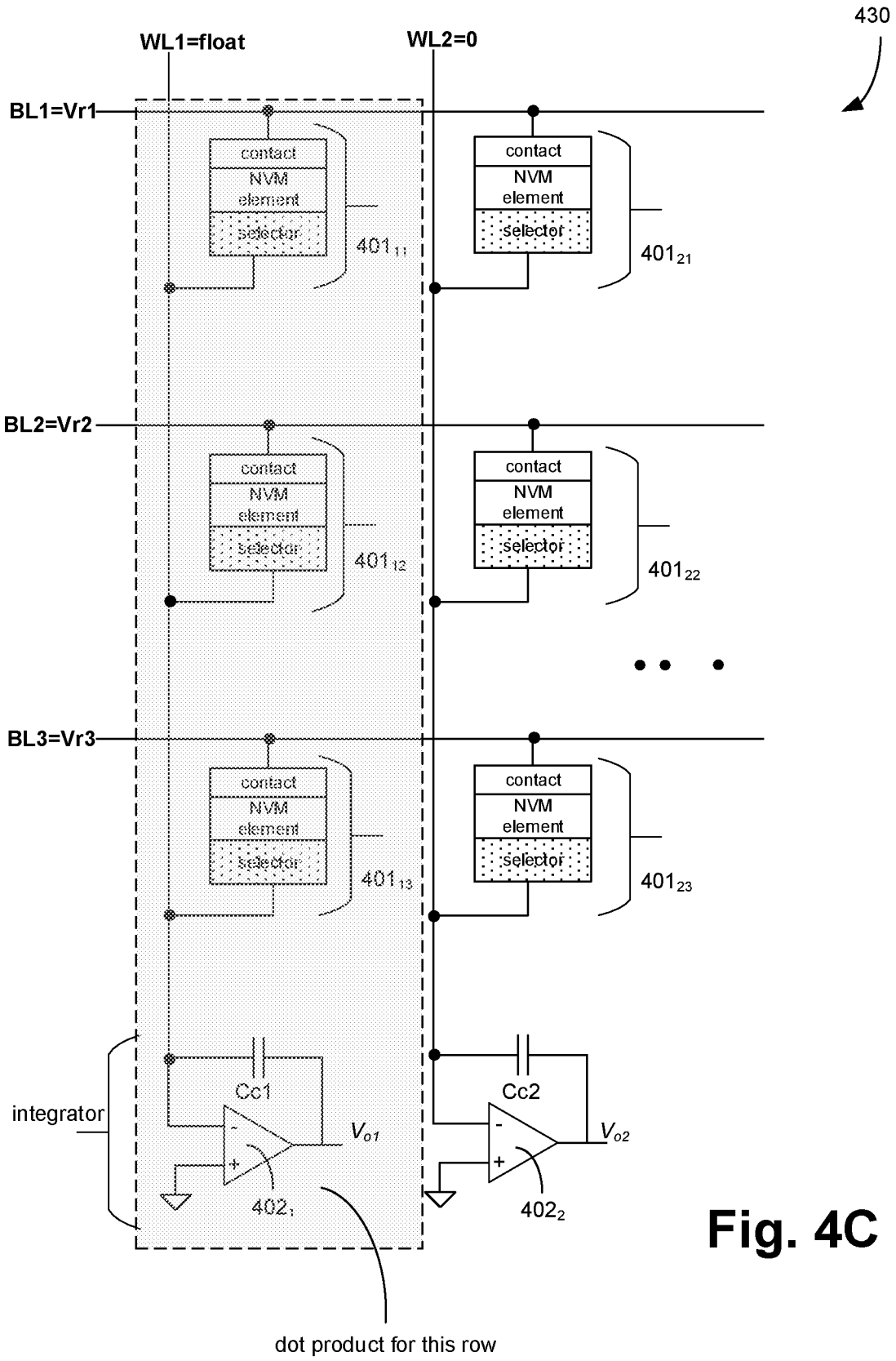

430
WL1=float
WL2=0
BL1=Vr1
BL2=Vr2
BL3=Vr3
contact
NVM element
selector
401 11
401 21
401 12
401 22
401 13
401 23
integrator
Cc1
Cc2
Vo1
Vo2
402 1
402 2
dot product for this row

Fig. 4C

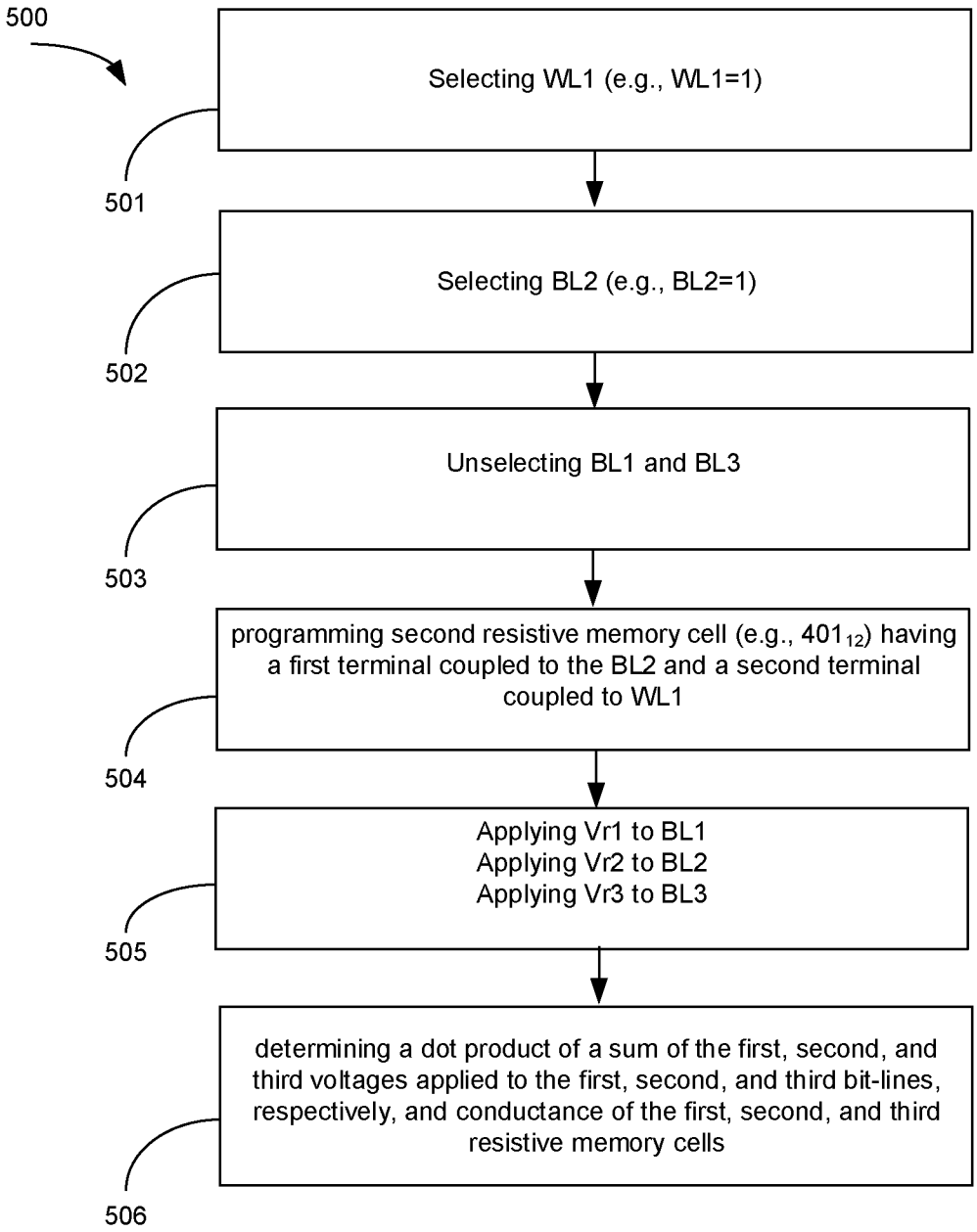

500
Selecting WL1 (e.g., WL1=1)
501
Selecting BL2 (e.g., BL2=1)
502
Unselecting BL1 and BL3
503
programming second resistive memory cell (e.g., 401$_{12}$) having a first terminal coupled to the BL2 and a second terminal coupled to WL1
504
Applying Vr1 to BL1
Applying Vr2 to BL2
Applying Vr3 to BL3
505
determining a dot product of a sum of the first, second, and third voltages applied to the first, second, and third bit-lines, respectively, and conductance of the first, second, and third resistive memory cells
506

Fig. 5

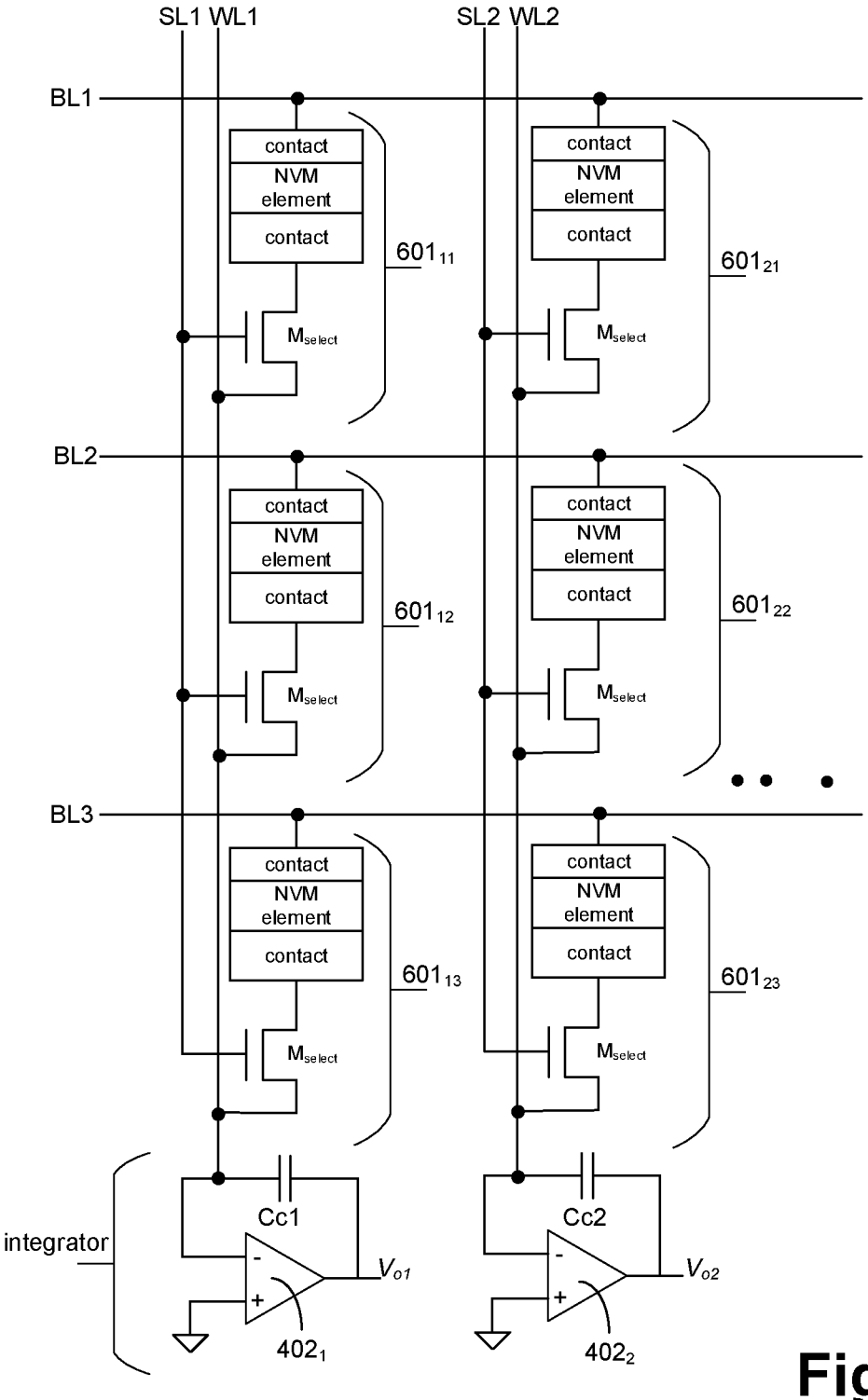

SL1 WL1
SL2 WL2
600
BL1
BL2
BL3
contact
NVM element
contact
601_{11}
601_{21}
601_{12}
601_{22}
601_{13}
601_{23}
M_{select}
integrator
Cc1
Cc2
V_{o1}
V_{o2}
402_1
402_2

Fig. 6A

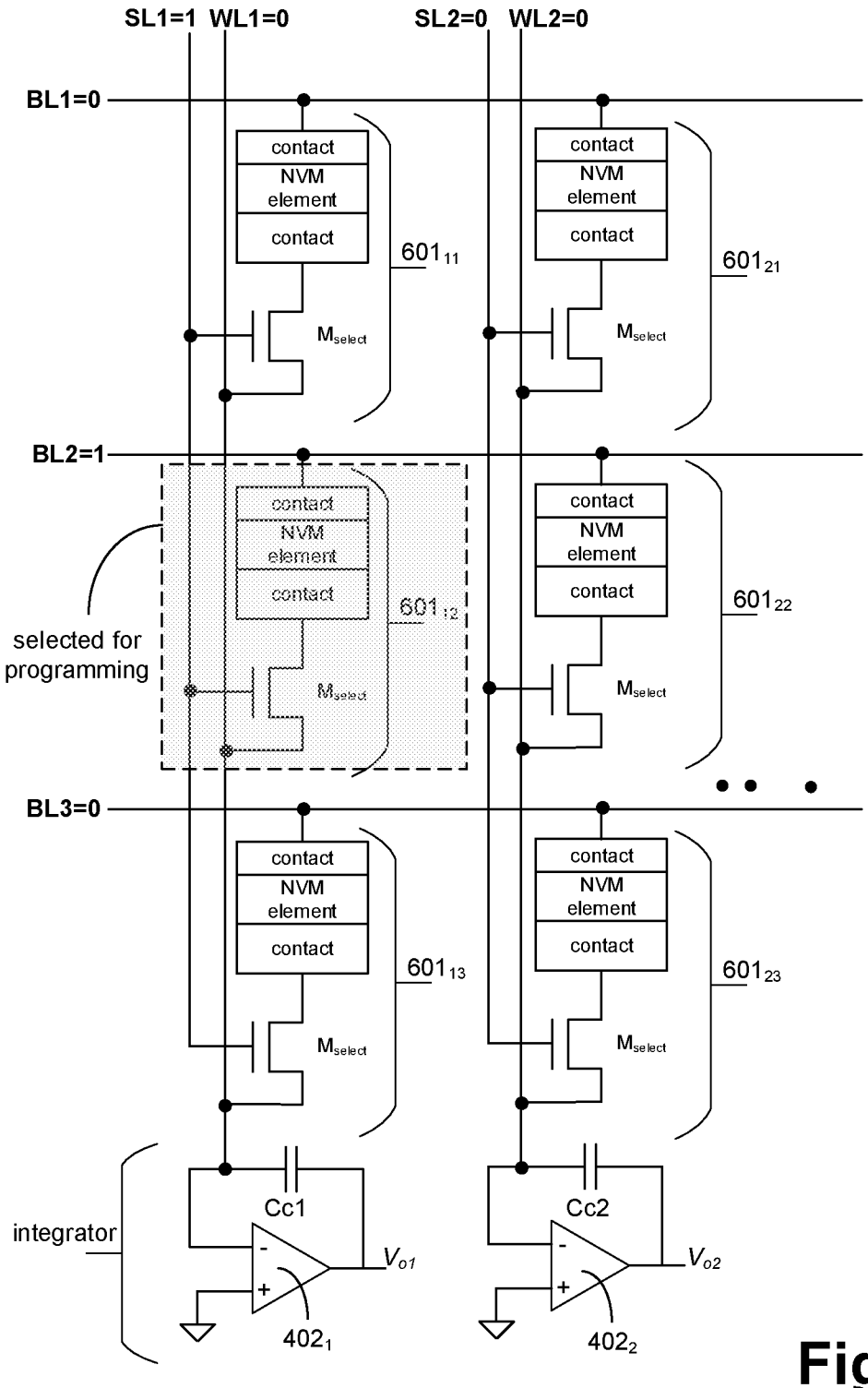

SL1=1
WL1=0
SL2=0
WL2=0
620
BL1=0
BL2=1
BL3=0
contact
NVM element
contact
601_{11}
601_{21}
601_{12}
601_{22}
601_{13}
601_{23}
M_{select}
selected for programming
integrator
Cc1
Cc2
V_{o1}
V_{o2}
402_1
402_2

Fig. 6B

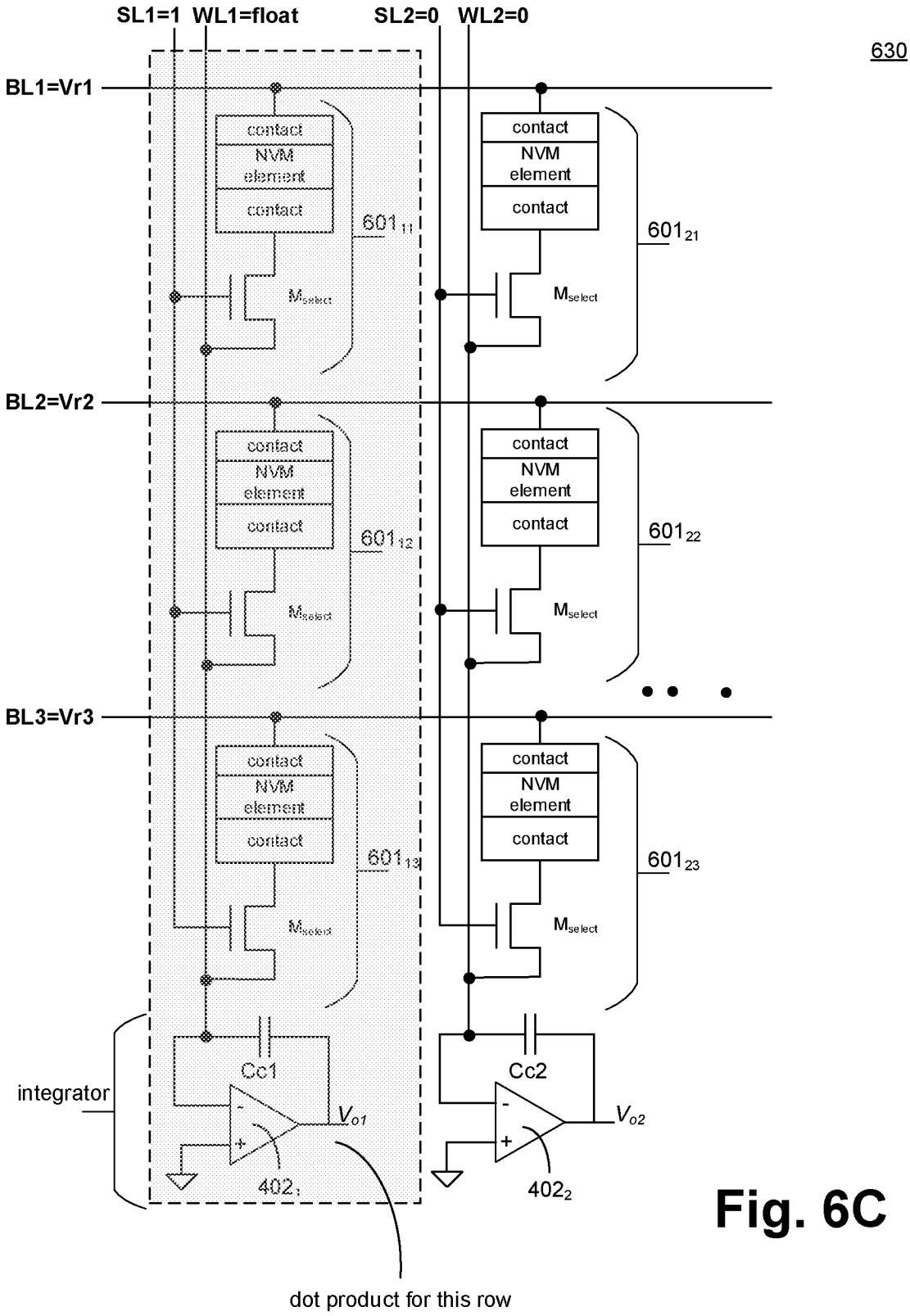

SL1=1
WL1=float
SL2=0
WL2=0
630
BL1=Vr1
BL2=Vr2
BL3=Vr3
contact
NVM element
contact
601_{11}
601_{12}
601_{13}
601_{21}
601_{22}
601_{23}
M_{select}
integrator
Cc1
Cc2
V_{o1}
V_{o2}
402_1
402_2
dot product for this row

Fig. 6C

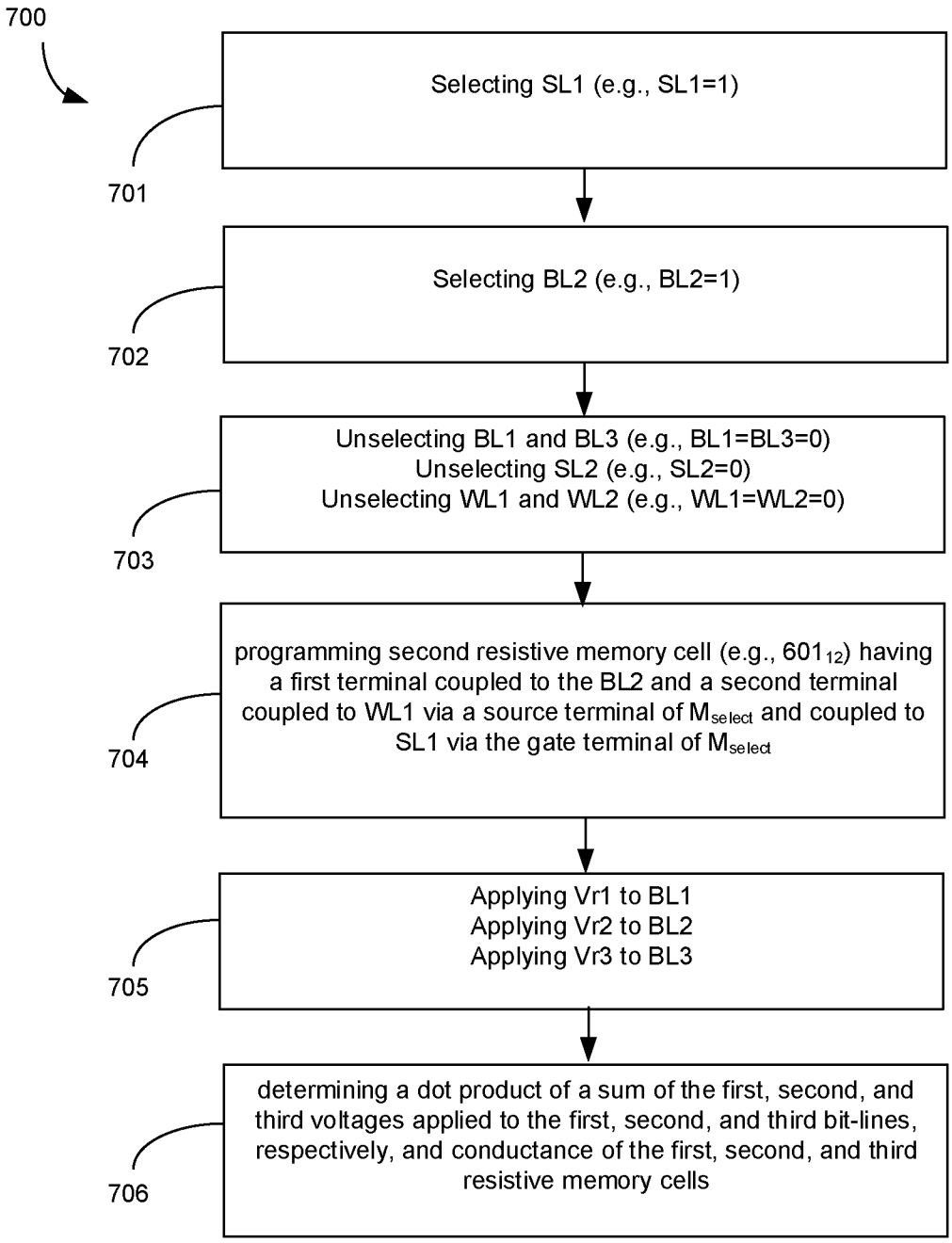

700
Selecting SL1 (e.g., SL1=1)
701
Selecting BL2 (e.g., BL2=1)
702
Unselecting BL1 and BL3 (e.g., BL1=BL3=0)
Unselecting SL2 (e.g., SL2=0)
Unselecting WL1 and WL2 (e.g., WL1=WL2=0)
703
programming second resistive memory cell (e.g., 601$_{12}$) having a first terminal coupled to the BL2 and a second terminal coupled to WL1 via a source terminal of M_{select} and coupled to SL1 via the gate terminal of M_{select}
704
Applying Vr1 to BL1
Applying Vr2 to BL2
Applying Vr3 to BL3
705
determining a dot product of a sum of the first, second, and third voltages applied to the first, second, and third bit-lines, respectively, and conductance of the first, second, and third resistive memory cells
706

Fig. 7

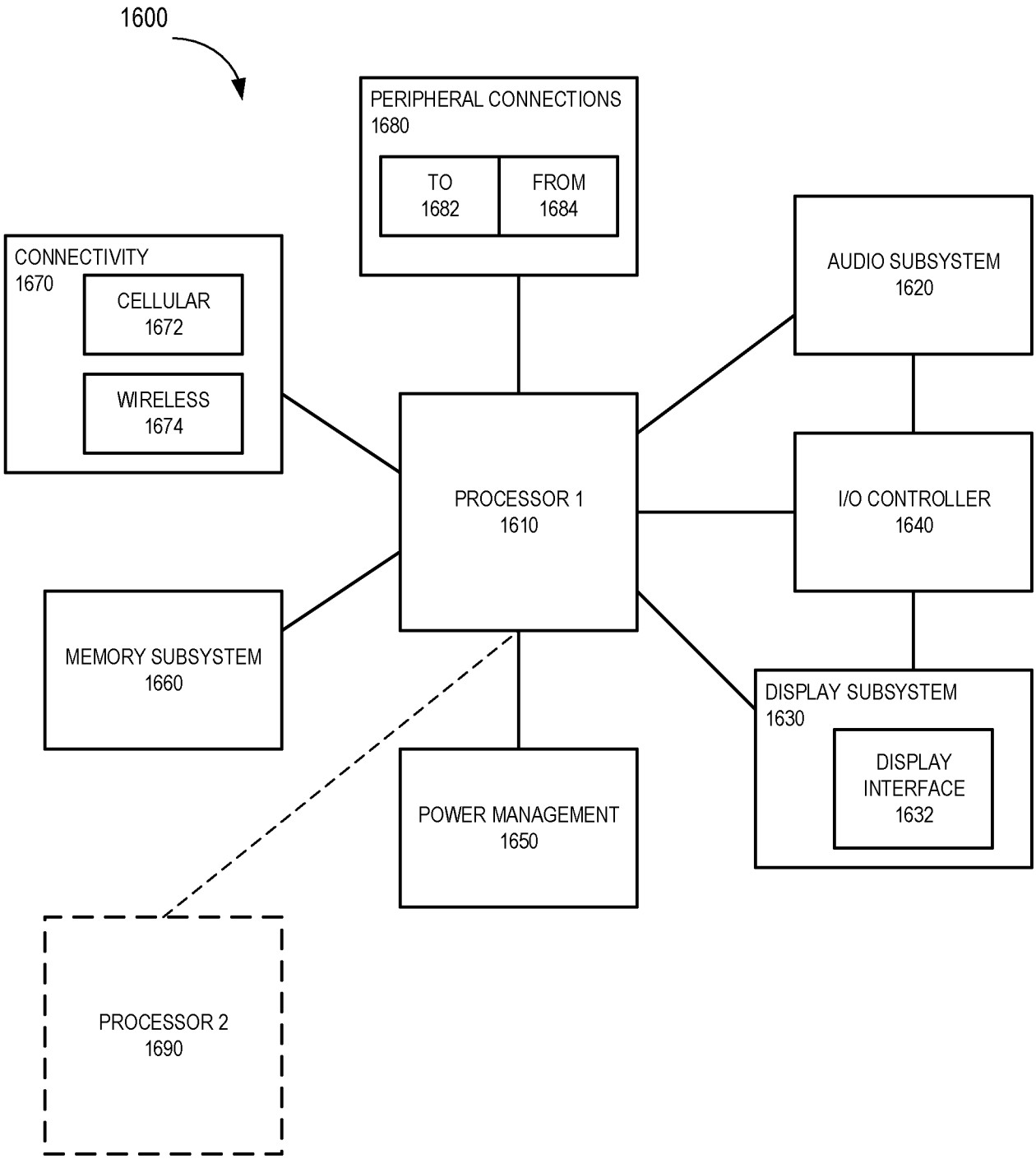

1600
PERIPHERAL CONNECTIONS
1680
TO
1682
FROM
1684
CONNECTIVITY
1670
CELLULAR
1672
WIRELESS
1674
AUDIO SUBSYSTEM
1620
PROCESSOR 1
1610
I/O CONTROLLER
1640
MEMORY SUBSYSTEM
1660
DISPLAY SUBSYSTEM
1630
DISPLAY
INTERFACE
1632
POWER MANAGEMENT
1650
PROCESSOR 2
1690

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/066887

A. CLASSIFICATION OF SUBJECT MATTER

G11C 13/00(2006.01)i, G11C 11/16(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 13/00; G11C 11/02; G11C 11/21; G11C 7/12; G11C 5/02; G11C 11/00; G11C 11/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: word-line, bit-line, resistive, memory, cell, integrator, phase-change, PCM, dot, product

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013-0135925 A1 (ROY E. SCHEUERLEIN) 30 May 2013 See paragraphs [0026], [0037], [0050], [0052], [0055], [0084], [0099]; and figures 1, 4a, 6, 8b.	1-23
Y	US 2013-0028004 A1 (GREGORY STUART SNIDER) 31 January 2013 See paragraphs [0016], [0020]-[0021]; and figure 2.	1-23
A	US 2014-0133211 A1 (HAGOP NAZARIAN et al.) 15 May 2014 See paragraphs [0050]-[0052]; and figure 4.	1-23
A	US 2003-0031045 A1 (KEIJI HOSOTANI) 13 February 2003 See paragraphs [0032]-[0034]; and figure 1.	1-23
A	US 2012-0307542 A1 (CHANG HUA SIAU et al.) 06 December 2012 See paragraphs [0032]-[0039]; and figure 2A.	1-23

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 August 2016 (24.08.2016)	**24 August 2016 (24.08.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
LEE, EUN KYU
Telephone No. +82-42-481-3580

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/066887

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