



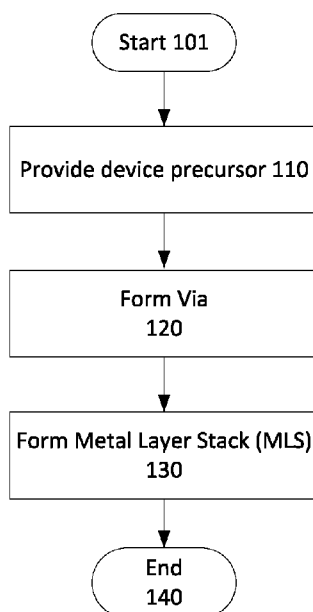
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[Continued on next page]

- (54) **Title:** ROUGHNESS MASK FOR SEMICONDUCTOR DEVICES AND METHODS FOR MAKING THE SAME

FIG. 1

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(57) **Abstract:** Technologies for masking the roughness of surfaces that may be provided during the manufacturing of semiconductor devices are described. Such technologies include methods for forming a roughness mask on relatively rough surfaces of a device precursor. In some embodiments, the roughness mask is designed to provide a relatively uniform and/or smooth surface for the deposition of subsequent layers, relative to a relatively rough surface upon which the roughness mask is disposed. In particular, methods of forming roughness masks in vias or trenches formed in composite dielectric materials are described. Semiconductor devices including such roughness masks are also described.

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ROUGHNESS MASK FOR SEMICONDUCTOR DEVICES AND METHODS FOR MAKING THE SAME

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FIELD

[0001] The present disclosure relates to technologies for masking relatively rough surfaces that may be present during the manufacturing of semiconductor devices. In particular, embodiments of the present disclosure relate to a roughness mask for masking the sidewalls of a dielectric used in a bump under layer metallization process. Methods of making such roughness masks are also described.

BACKGROUND

[0002] The production of interconnects in semiconductor devices often involves the production of vias in one or more dielectric materials. In many instances such vias are produced by the application of wet or dry etching chemistries, which may etch different materials at different rates. As semiconductor devices have grown increasingly complex, composite dielectric materials such as spin on polymer dielectrics have started to become of interest for the production of vias. Although such materials offer advantageous properties, they may be manufactured from multiple different components that may be etched at different rates by a particular etching chemistry. As a result, the etching processes employed to produce vias in such materials may result in the production of a via having a relatively rough surface. As a result, subsequently deposited layers (e.g., in a metal layer stack (MLS)) may be of relatively low quality. That is, such layers may include various defects such as voids, whiskers, hillocks, and the like, any of which may degrade the reliability and/or performance of interconnect or the semiconductor device as a whole.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Features and advantages of embodiments of the claimed subject matter will become apparent as the following Detailed Description proceeds, and upon reference to the Drawings, wherein like numerals depict like parts, and in which:

5 [0004] **FIG. 1** is a flow diagram of example operations of a method of forming a metal layer stack for an interconnect of semiconductor device.

[0005] **FIGS. 2A-2C** stepwise illustrate the formation of an interconnect structure of a semiconductor device including a metal layer stack consistent with the method of FIG. 1.

10 [0006] **FIGS. 3A and 3B** are scanning electron micrograph (SEM) images of a semiconductor device including a metal layer stack formed in manner consistent with the method of FIG. 1.

[0007] **FIG. 4** is a flow diagram of example operations of a method of forming an interconnect structure of a semiconductor device including a roughness mask consistent with the present disclosure.

15 [0008] **FIGS. 5A-5E** stepwise illustrate the formation of an interconnect structure of semiconductor device including a roughness mask consistent with the present disclosure, and in a manner consistent with the method of FIG. 4.

[0009] **FIGS. 6A and 6B** are SEM images of one example of a semiconductor device including a roughness mask consistent with the present disclosure.

20 [0010] Although the following Detailed Description will proceed with reference being made to illustrative embodiments, many alternatives, modifications, and variations thereof will be apparent to those skilled in the art.

DETAILED DESCRIPTION

25 [0011] As noted in the background, interest has grown in the use of composite dielectric materials for the production of vias in semiconductor devices. Such vias may be useful for various applications, such as in inter layer dielectric (ILD) layers, bump under metallization layers, combinations thereof, and the like, the nature and function of which are well understood in the art.

30 [0012] For example, in the manufacture of integrated circuits a flip-chip connection is often used to attach an integrated circuit die (IC die) to a carrier substrate, such as an integrated circuit package (IC package) or a motherboard. Generally, a flip-chip configuration uses an array of metal bumps that are arranged on the surface of the IC die. The metal bumps are aligned with corresponding solder balls on the IC package.

Once aligned, an annealing process is carried out at a temperature above the melting point of the solder to cause the solder balls to reflow and wet the surface of the metal bumps. The solder balls and metal bumps are then rapidly cooled to limit intermixing of their respective materials. Space between and around the interface of the metal bump/solder ball connections may then be filled with an underfill material, such as an epoxy resin.

[0013] With the foregoing in mind, various processes for forming metal bumps on an IC die are known. In some instances for example, electroplating may be used to form metal bumps on exposed regions of a metallization layer of the IC die. For the sake of convenience such exposed regions may be referred to herein as a “pad” or “pads,” but it should be understood that such regions may have any suitable geometry (e.g., lines, dots, etc.). Although electroplating may be used to form metal bumps directly on exposed pads of an IC die, in many instances the IC die is processed in various ways to improve the deposition and/or performance of the metal bumps. For example, one or more barrier and/or dielectric layers may be provided on a surface of the IC die and patterned to form vias that expose a portion of the pads. Subsequently, conductive material may be deposited within the via and processed into a metal bump that can be used to electrically connect the pad with a corresponding portion of an IC package.

[0014] Prior to depositing the conductive material used to form the metal bumps (via electroplating or another process), one or more additional layers may be formed within the via, e.g., to improve adhesion, electrical performance, or for some other reason. For example, one or more barrier layers may be formed in a via, and may function to limit or prevent migration of components of subsequently deposited materials into one of the previously deposited layers, such as one of the dielectric layers. A seed layer may also be deposited (e.g., on top of a barrier layer), and may function to facilitate deposition of the material forming a metal bump, e.g., via electroplating or another process. For the sake of convenience, such barrier and seed layers may be collectively referred to herein as a metal layer stack (MLS), or a MLS layer. In any case, deposition of the material forming the metal bump(s) may proceed in any suitable manner, e.g., on the MLS layer.

[0015] In addition, many integrated circuit devices are formed by forming layers of conductive material and dielectric material on a substrate, such as a silicon wafer. Similar to the techniques described above with regard to flip chip technology, vias

may be defined in the dielectric layers of an integrated circuit and then filled with a conductive material to electrically interconnect the separated conductive layers. As before, an MLS layer may be formed in the via prior to the deposition of conductive material, e.g., to improve performance, facilitate deposition of the conductive material, or for some other reason.

[0016] As explained previously however, production of vias in semiconductor devices is often performed by etching. Specifically, one or more wet or dry etching chemistries may be applied to selectively remove dielectric material from a particular region, resulting in the production of a via or other desired structure. As is well understood in the art, many etching chemistries employed in such processes etch various materials at different rates. Thus, when such chemistries are applied to etch vias in composite dielectric materials, they may etch the various components of the composite dielectric material at different rates. As a result, application of such etching chemistries to composite dielectric materials tend to result in the production of vias including sidewalls that exhibit relatively high (first) average surface roughness, e.g., of greater than or equal to about 10 nanometers (nm) to greater than or equal to 1 micron or even greater than or equal to about 2 microns.

[0017] The inventors have observed that the surface roughness of the sidewalls of a via formed of a composite dielectric material may impact the quality of films that may be subsequently deposited within the via and, in particular, on the sidewalls thereof. Specifically, the inventors observed that MLS layers deposited (e.g., via sputtering) on relatively rough sidewalls of a via formed in a composite dielectric tended to be of low quality. That is, it was observed that MLS layers deposited on relatively rough sidewalls of a via formed in a composite dielectric material tend to include various defects such as whiskers, voids, hillocks, and the like, any of which may compromise the reliability and/or electrical properties of the device in which the via is used.

[0018] With the foregoing in mind, the present disclosure generally relates to technologies for masking the roughness of sidewalls formed in a composite dielectric material. As will be described in detail below, such technologies include methods for forming a roughness mask on the sidewalls of a via formed in a composite dielectric material. Semiconductor devices including such roughness masks are also disclosed.

[0019] For the sake of clarity it is noted that the present disclosure will initially proceed to describe a method of producing an interconnect structure for a

semiconductor device, wherein the interconnect structure includes a via that is formed in a composite dielectric material, and which does not include a roughness mask consistent with the present disclosure. Subsequently, methods of forming a roughness mask within a via formed in a composite dielectric material and semiconductor devices including such a roughness mask will be described.

[0020] It is noted that while the present disclosure focuses on various embodiments in which roughness masks are formed and applied in semiconductor interconnect structures, the technologies described herein are not limited to such use. Indeed it should be understood that the technologies described herein may be useful in a wide variety of applications in semiconductor devices, including but not limited to interlayer dielectric (ILD) layers, bump over metallization layers, combinations thereof, and the like.

[0021] Reference is now made to FIG. 1, which is a flow chart of example operations that may be performed to form an interconnect structure of a semiconductor device, wherein the interconnect structure does not include a roughness mask. For the sake of clarity the various operations of FIG. 1 will be described in conjunction with FIGS. 2A-2C, which stepwise illustrate the formation of an interconnect structure of an semiconductor device that does not include a roughness mask.

[0022] As shown in FIG. 1, method 100 may begin at block 110. Pursuant to block 110, a device precursor may be provided. As used herein, the term “device precursor” is used to refer to a precursor of a semiconductor device or a component thereof, such as but not limited to an integrated circuit, a die, combinations thereof, and one or more subcomponents thereof. Without limitation, in some embodiments the device precursor may be a precursor to the formation of an ILD layer, a bump over metallization layer, or another interconnect structure useful in semiconductor device applications.

[0023] One example of a suitable device precursor is illustrated in FIG. 2A. As shown, device precursor 200 includes a substrate 201 having a device layer 204 formed thereon. One or more metallization layers 205 are formed on device layer 204. One or more barrier layers 210 are formed on device layer 204. In addition, regions of a dielectric material 215 (e.g., a polymer dielectric) may be formed on the surface of barrier layer 210, as shown in FIG. 2A. For example, a printing process may be used to print regions of dielectric material 215 on the surface of barrier layer

210. Alternatively or additionally, dielectric material 215 may be deposited as a conformal layer on the surface of barrier layer 210, and a lithographic or other patterning process may be used to selectively remove portions of the dielectric material, resulting in the structure shown in FIG. 2A. In any case, the structure in
5 FIG. 2A may be subjected to an etching or other process that is designed to selectively remove the exposed surface of barrier layer 210, thereby exposing a portion of metal layer 205 as will be described later in conjunction with FIG. 2B.

[0024] As may be appreciated, device precursor 200 may be particularly suitable for the formation of a bump over metallization structure, such as may be useful in flip-
10 chip applications. As noted previously, however, the technologies described herein are not limited to such applications, and may be used in various other parts of a semiconductor device, including but not limited to an ILD layer.

[0025] Substrate 201 may be any suitable substrate for a semiconductor device. Non-limiting examples of suitable substrates that may be used as substrate 201
15 include substrates made from or including bulk silicon (Si), silicon on insulator, germanium (Ge), gallium arsenide (GaAs), indium antimonide (InSb), SiGe, metals, III-V semiconductor materials, combinations thereof, and the like. Without limitation, in some embodiments substrate 201 is formed from bulk silicon.

[0026] Device layer 204 may be formed on or within an upper portion of substrate
20 201. In general, device layer contains various electronic devices such as but not limited to transistors, capacitors, interconnects, trench isolation structures, combinations thereof, and the like. The nature and function of such structures are well understood in the art, and therefore are not illustrated or described in detail. Moreover it should be understood that device layer 204 may include any suitable
25 combination of electronic structures which may be useful for a desired application.

[0027] Metallization layer 205 generally serves to electrically connect the various devices on substrate 201, e.g., within device layer 204. Accordingly, metallization layer 205 may include metal interconnects, inter level dielectric (ILD) layers used to separate and interconnect the metal interconnects, and/or vias that penetrate through
30 the ILD layers to couple the metal interconnects together. When used, the ILD layers may be formed from various dielectric materials such as carbon doped oxide, silicon dioxide, composite dielectric materials such as but not limited to spin-on-polymer dielectric materials, combinations thereof, and the like. As noted previously, the

technologies described herein may be directly applicable to the formation of such ILD layers, particularly in instances where such layers are formed from or include composite dielectric materials. In particular, the technologies described herein may be particularly useful in an ILD layer that includes one or more vias formed in a composite dielectric material.

[0028] Non-limiting examples of conductive materials that may be used in metallization layer 205 include but are not limited to aluminum, copper, chromium, tin, combinations thereof, and the like. Of course such materials are for the sake of example only, and metallization layer 205 may include any suitable conductive material. Moreover it should be understood that metallization layer 205 may include conductive material that is deposited and/or patterned by any suitable process understood in the art.

[0029] As mentioned above and as shown in FIG. 2A, barrier layer 210 is formed on top of metallization layer 205. In general, barrier layer 210 may function to seal and protect metallization layer 205 and/or other components of the semiconductor device in which device precursor 200 is included from damage and contamination. For example, in some embodiments barrier layer 210 may serve to limit or prevent migration of conductive material from metallization layer 205 into the layer/regions of dielectric material 215. Alternatively or additionally, barrier layer 210 may serve as an etch stop, e.g., to protect metallization layer 205 during the production of a via within the layer/regions of dielectric material 215 (as described later).

[0030] Barrier layer 210 may be formed from any suitable material, including but not limited to interlayer dielectric materials, nitrides, silicon dioxide, polybenzoxazoles, epoxies, silicones, bisbenzocyclobutene, phenolic resins, polyamides, and the like. Without limitation, barrier layer 210 in some embodiments are formed from one or more nitrides, such as but not limited to silicon nitride.

[0031] Barrier layer 210 may be provided on metallization layer 205 in any suitable manner. For example, barrier layer 210 may be provided by depositing a conformal layer (e.g., via chemical vapor deposition, physical vapor deposition, or the like) on metallization layer 205. Following such deposition, a dielectric material 215 may be deposited on the surface of barrier layer 210.

[0032] Dielectric material 215 may be any suitable dielectric material for use in semiconductor device applications, and in particular for use in the production of

semiconductor interconnect structures. Without limitation, in some embodiments dielectric material 215 is a composite dielectric material. As used herein, the term “composite dielectric material” means a dielectric material that includes two or more components that are coupled, mixed, and/or blended together, such that they collectively act as a dielectric material. Non-limiting examples of suitable composite dielectric materials include various composite polymer dielectric materials, including but not limited to polymer dielectrics that include a matrix polymer and one or more different types of filler materials, such as filler particles. As may be appreciated, the composition of such polymer dielectrics may be tailored to provide desirable electronic properties for a particular application.

[0033] As shown in FIG. 2A, dielectric material 215 may be provided on top of barrier layer 210. In this regard, dielectric material 215 may be deposited in any suitable manner. For example, dielectric layer may be deposited using a chemical vapor deposition process, a physical vapor deposition process, a spin on deposition process, combinations thereof, and the like. Without limitation, in some embodiments dielectric material 215 is or includes a composite polymer dielectric that is provided via a spin-on process on the surface (not labeled) of barrier layer 210, as well as surface 207 of metallization layer 205. In further non-limiting embodiments, dielectric layer is or includes a composite polymer dielectric that may be heat cured, e.g., to form a thermoset composite polymer dielectric. In some instances, dielectric material 215 may be deposited in a pattern (e.g., by a printing or other suitable process). Alternatively, dielectric material may be deposited as a layer and subsequently processed into a pattern that exposes a surface of barrier layer 210, as shown in FIG. 2A.

[0034] In any case, the dielectric material 215 may be heat cured, resulting in the structure shown in FIG. 2A. It is noted that for the sake of illustration, the structure of device precursor 200 is shown as including regions of dielectric material 215 that have define a partial via (not labeled), and which include sidewalls that are oriented at an angle relative to the exposed surface of barrier layer 210. It should be understood that such illustration is for the sake of example only, and the sidewalls of the partial via defined by regions of dielectric material 215 may be oriented in any suitable manner relative to the surface of barrier layer 210. For example in some embodiments, the sidewalls of the partial via defined by the regions of dielectric

material may be oriented substantially normal (e.g., about 90 degrees) relative to the surface of barrier layer 210.

[0035] Returning to FIG. 1, once a device precursor such as device precursor 200 is provided, the method may proceed from block 110 to block 120. Pursuant to block 5 120, one or more vias may be formed in the barrier layer 210 of device precursor 200, so as to expose a portion of the underlying metallization layer 210. This concept is shown in FIG. 2B, which illustrates modified device precursor 200'. As shown, modified device precursor 200' includes a via 220 that extends from an upper surface of dielectric material 215 through barrier layer 210, so as to expose a portion of the 10 surface 207 of metallization layer 205.

[0036] Via 220 may be formed in any suitable manner. For example, via 220 may be formed by a photolithographic process, a wet or dry chemical etching process, or a combination thereof. Without limitation, in some embodiments the structure shown in FIG. 2B may be formed by using the regions of dielectric material 215 as a mask for a 15 (e.g., reactive) dry etching process, which may be used to selectively remove at least a portion of the exposed surface of barrier layer 210, thereby exposing surface 207 of metallization layer 205. As may be appreciated, the etching chemistry utilized may be tailored to selectively etch the components of barrier layer 210. The end result may be the formation of via 220, which extends down to and exposes surface 207 of 20 metallization layer 205, with the regions of dielectric material 215 masking barrier layer 210 and other portions of metallization layer 205, as generally shown in FIG. 2B.

[0037] With the foregoing in mind, the etching chemistry utilized during the selective removal of barrier layer 210 may also affect (e.g., etch) the components of dielectric 25 material 215. In instances where dielectric material 215 is a composite dielectric material, for example, exposing device precursor 200 to the aforementioned etching chemistry may also result in the etching of the components of dielectric material 215 at different rates. As a result, via 220 may be formed such that it includes sidewalls that have a relatively rough surface. This concept is illustrated in FIG. 2B, which 30 depicts via 220 as including rough sidewalls 240. For ease of reference, in some instances sidewalls 240 may be referred to herein as including a first via facing surface. It should of course be understood that the drawings are not to scale, and that the illustrated roughness is for the sake of example and explanation only.

[0038] The roughness of sidewalls 240 may vary widely, and may depend on various factors such as etch time, etch temperature, the rate(s) at which the etching chemistry etches the components of dielectric material 215, combination thereof and the like.

That being said, in many instances sidewalls 240 may exhibit a (first) root mean square (RMS_1) roughness ranging from greater than 0 to about 50 nanometers (nm), such as from about 5 nm to about 25 nm, or even about 5 nm to about 10 nm. Alternatively or additionally, sidewalls 240 may exhibit a (first) maximum roughness ($Rmax_1$) ranging from greater than 0 to about 500nm, such as from about 50 to about 100nm. Of course such roughness values are for the sake of example only, and it should be understood that the RMS_1 and $Rmax_1$ may vary widely, and may be larger or smaller than the above noted ranges. In any case, it may be understood that such etching of dielectric material 215 may produce a via with sidewalls having an RMS_1 that may result in the generation of defects (e.g., voids, whiskers, hillocks, etc.) in or during the production of subsequently deposited layers.

[0039] In some instances via 220 may be used to facilitate the alignment and deposition of a conductive material that may function to electrically couple surface 207 of metallization layer 205 with another component. For example in the case of flip chip or other interconnect technology (e.g., in ILD layers), conductive material (e.g., metal balls, traces, bulk metal fill, etc.) may be formed within via 220 via any suitable process, such as via electrodeposition, physical vapor deposition, sputtering, or the like. Non limiting examples of suitable conductive materials that may be used for this purpose include copper, nickel, palladium, gold, a lead/tin alloy, combinations thereof, and the like.

[0040] While such conductive materials may be advantageously used to electrically couple one or more components to surface 207 of metallization layer 205, it may be difficult to deposit such materials directly on the surface 240 of via 220, particularly when dielectric material 215 is or includes a composite dielectric material. Moreover even if conductive material may be deposited directly on surface 240, such materials may exhibit less than desirable adhesion to dielectric material 215. In addition, migration of conductive material into dielectric material 215 may be of concern, as such migration may compromise the electrical properties of dielectric material 215. It may therefore be desirable to form one or more additional layers within via 220 to address one or more of those issues.

[0041] In this regard and returning to FIG. 1, once a via (e.g., via 220) has been formed, the method may proceed from block 120 to block 130. Pursuant to block 130, a metal layer stack may be formed within via 220. This concept is shown in FIG. 2C, which depicts modified device precursor 200'' as including metal layer stack (MLS) 225 on dielectric material 215, and in particular on surface 240 of the sidewalls of via 220.

[0042] MLS 225 may include one or more layers that perform one or more functions. For example, MLS 225 may include a first layer (not separately illustrated), which may be formed directly on the surface of dielectric material 215 and, in particular, on the surface 240 of the sidewalls of via 220. In some embodiments, the first layer of MLS 225 may be in the form of a barrier layer that functions to limit or prevent the migration of conductive material (later deposited within via 220) into dielectric material 215. Moreover, in some embodiments the first layer may serve as a passivation layer that functions to protect dielectric material 215 and/or other components of device precursor 200'', e.g., during the processing of a subsequently deposited conductive layer. Non-limiting examples of suitable barrier layers that may be used in MLS 225 include those formed from titanium, tantalum, titanium nitride, tantalum nitride, and combinations thereof. Of course, other barrier layer materials may be used, as understood in the art.

[0043] MLS 225 in some embodiments may also include a second layer (also not shown), which may be formed on the first layer thereof, e.g., directly on a surface of the first layer. In some embodiments, the second layer may function as a seed layer. In such instances the second layer may function to facilitate the deposition of additional material (e.g., bulk metal, metal balls, etc.) within via 220, e.g., via electrodeposition, sputtering, vapor deposition, or the like. Non-limiting examples of suitable materials that may be used as a seed layer include copper, nickel, tantalum, titanium, combinations and alloys thereof, and the like. Of course, other seed layer materials understood in the art may also be used. Without limitation, in some embodiments MLS 225 includes a barrier layer including titanium or tantalum formed directly on the sidewalls 240 of via 220, and a seed layer including copper, titanium, tantalum, and/or formed directly on the surface of the barrier layer.

[0044] The layer(s) used in MLS 225 may be provided in any suitable manner. In some embodiments, MLS 225 includes both a barrier and a seed layer as previously

described, wherein the barrier and seed layers are formed within via 220 via sputtering or another suitable deposition process. Without limitation, in some embodiments the barrier and seed layers are both provided via a sputtering process, such as but not limited to magnetron sputtering.

- 5 [0045] As shown in FIG. 2C, MLS 225 may substantially conform to the topography of the surface of sidewalls 240 of via 220. This may be particularly true in instances where the layer(s) of MLS 225 are deposited via sputtering. In any case as shown in FIG. 2C, modified device precursor 200'' may include an interface 260 between MLS 225 and dielectric material 215, at which one or more layers of MLS 225 may
- 10 substantially conform to the surface topography of sidewalls 240. In some instances, this surface topography may be carried through MLS 225, such that MLS 225 has a surface 250 which largely mimics the surface topography of the surface of sidewalls 240, as shown in FIG. 2C.

- [0046] As previously explained, when the roughness (e.g., RMS_1 and/or $Rmax_1$) of
- 15 sidewalls 240 is relatively high, the layer(s) in MLS 225 may be of relatively low quality. That is, defects such as voids, hillocks, whiskers, etc., may be generated or present in or proximate to MLS 225. As noted previously, such defects may present various problems, and may undesirably affect the reliability and/or operation of a semiconductor device.

- 20 [0047] To illustrate this concept reference is made to FIG. 3A, which is a scanning electron micrograph of a device precursor manufactured in a manner consistent with FIG. 1 as described above. In particular, the illustrated micrograph is of a device precursor that includes a metallization layer 205 of one or more metals, a barrier layer 210 formed of a hermetic nitride, and a dielectric material 215 of a spin on composite
- 25 polymer dielectric. The device precursor was processed to form a via in a manner consistent with the foregoing description. Sputtering was then performed to deposit a metal layer stack 225 including a barrier layer of titanium nitride and a seed layer of copper within the via. Subsequently, a bulk metal fill 300 was deposited within the via.

- 30 [0048] With the foregoing in mind, FIG. 3B is a magnified view of region A of the device precursor of FIG. 3A. As shown, region A focuses on an interface between MLS 225 and dielectric material 215, proximate a sidewall of via 220 (not labeled). In this region, various defects 270 were observed. Specifically, voids and hillocks

were observed proximate the interface of dielectric material 215 and MLS 225, as well as within MLS 225. As a result, the barrier and seed layers of MLS 225 were of relatively low quality.

5 [0049] With the foregoing in mind reference is made to FIG. 4, which is a flow chart of example operations in accordance with a method of making a device precursor including a roughness mask consistent with the present disclosure. As will become apparent from the following description, the roughness mask may function to improve the quality of an MLS or other layer deposited thereon, e.g., by masking the roughness of the surface of the sidewall of a via formed in a composite dielectric material.

10 [0050] More specifically, in some embodiments the roughness mask may have a (second) RMS roughness (RMS_2) that is less than RMS_1 , i.e., the RMS surface roughness of the surface upon which it is deposited, e.g., of a via sidewall formed in a composite dielectric material. In some instances, RMS_2 is less than RMS_1 by an amount ranging from greater than or equal to about 5%, about 10%, about 15%, about 20%, or even about 25% or more. Put in other terms, in some embodiments RMS_1 may be greater than RMS_2 by greater than or equal to about 5, 10, 15, 20, or even 25% or more.

20 [0051] Similarly, the roughness mask may exhibit a (second) maximum surface roughness ($Rmax_2$) that is less than $Rmax_1$, i.e., the maximum surface roughness of the surface upon which it is deposited, e.g., of a via sidewall formed in a composite dielectric material. For example in some embodiments $Rmax_2$ is less than $Rmax_1$ by greater than or equal to about 5%, 10%, 15%, 20%, or even 25% or more. Put in other terms, in some embodiments $Rmax_1$ may be greater than $Rmax_2$ by greater than or equal to about 5, 10, 15, 20, or even 25% or more.

25 [0052] As shown in FIG. 4, method 400 begins at block 401. The method may then proceed to blocks 110 and 120, respectively. The operations performed pursuant to such blocks are the same as those described above in connection with FIG. 1, and for the sake of brevity are not reiterated in detail. As may be appreciated, the operations pursuant to such blocks may result in the provision of a device precursor 500, as shown in FIG. 5A. Notably, the structure and elements of device precursor 500 are the same as those of device precursor 200' shown in FIG. 2B and described above.

The nature and function of such elements is therefore not described again for the sake of brevity.

[0053] Once a via has been formed pursuant to block 120 of FIG. 4, the method may proceed to block 405. Pursuant to block 405, a roughness mask precursor may be formed on device precursor 400. This concept is shown in FIG. 5B, which depicts modified device precursor 500' as including roughness mask precursor 501. As shown, roughness mask precursor 501 may be in the form of a layer of material that is deposited over various surfaces of device precursor 500, including the upper surface of dielectric material 215, sidewalls 240 of via 220, and the exposed surface 207 of metallization layer 205.

[0054] Roughness mask precursor 501 may be formed of a wide variety of materials which may be suitably used in semiconductor applications. Non-limiting examples of suitable materials that may be used to form roughness mask precursor 501 include various dielectric materials, such as but not limited to dielectric oxides, nitrides, and carbides. In some embodiments, roughness mask precursor may be formed from or include one or more oxides, nitrides, or carbides of silicon (e.g., silicon oxide, silicon dioxide, silicon nitride, silicon carbide). Without limitation, in some embodiments the roughness mask is or includes silicon nitride.

[0055] Roughness mask precursor 501 may be provided in any suitable manner. For example, in some embodiments roughness mask precursor may be deposited on device precursor 500 via a deposition process such as but not limited to chemical vapor deposition, atomic layer deposition, physical vapor deposition, or the like. Without limitation, roughness mask precursor in some embodiments is formed from or includes a layer of dielectric oxide, nitride, or carbide, which has been deposited on device precursor 500 via chemical vapor deposition.

[0056] In any case roughness mask precursor 501 may be deposited on device precursor 500 at a particular deposition temperature. In instances where roughness mask precursor 501 is formed via CVD, for example, its deposition may be carried out at a CVD deposition temperature. The CVD deposition temperature may vary considerably depending on numerous factors, such as the material selected for roughness mask precursor 501, desired deposition rate, physical factors such as adhesion of roughness mask precursor 501 within via 220, desired thickness, etc., combinations thereof, and the like.

[0057] In addition, the deposition temperature may be selected or otherwise determined, for example, based on physical properties of the material making up dielectric material 215. For example, as noted above dielectric material 215 may be formed from a composite polymer dielectric material. As such, dielectric material 215 may exhibit a first glass transition temperature, which may be generally understood as the temperature at which one or more components of dielectric material 215 transitions from a glassy state to a rubbery state. In some instances, the first glass transition temperature may range from greater than or equal to about 200 degrees Celsius (°C), such as from greater than or equal to about 210 °C, about 220 °C, about 230 °C, about 240°C, or even about 250°C.

[0058] In some instances the properties of dielectric material 215 may change if it is exposed to temperatures above the first glass transition temperature. As a result, it may be desirable to control the deposition temperature used during the deposition of roughness mask 501 such that the deposition temperature is less than the first glass transition temperature. That is in some embodiments, it may be desirable to deposit the material of roughness mask precursor 501 at a deposition temperature ranging from less than or equal to about 250 °C, about 240 °C, about 230 °C, about 220°C, about 210 °C, or even about 200 °C. Without limitation, in some embodiments the material of the roughness mask is selected such that it may be deposited at a deposition temperature of less than or equal to about 200°C. One non-limiting example of a material that may be deposited at such a temperature and used as a roughness mask is silicon nitride, though other suitable low temperature dielectric materials (e.g., low temperature nitrides) may also be used.

[0059] The thickness of roughness mask precursor 501 may vary considerably. For example, roughness mask precursor 501 may have a thickness ranging from about 2000 angstroms to about 4000 angstroms (i.e., about 20 to about 40 nanometers (nm)), such as about 2400 to about 3600 angstroms (i.e., about 24 to to 35 nm), about 2800 to about 3200 angstroms (about 28 to about 32 nm), or even about 2900 to about 3100 angstroms (about 29 to about 31nm). In some embodiments, roughness mask precursor 501 has thickness of about 3000 angstroms (30nm). In still further embodiments, roughness mask precursor 501 is formed from silicon nitride that has been deposited to a thickness within the foregoing ranges.

[0060] Consistent with the foregoing description, roughness mask precursor 501 may have a surface 510 that exhibits a (second) average surface roughness that is less than the (first) average surface roughness of sidewalls 240 of via 220, and/or which is less than a (second) roughness threshold. For example, in some embodiments surface 510 of roughness mask precursor 501 (and a subsequently formed roughness mask) may exhibit a (second) root mean square surface roughness (RMS_2) ranging from about 0 to about 50 nanometers (nm), such as from about 5 nm to about 25 nm, or even about 5 nm to about 10 nm, wherein RMS_2 is less than RMS_1 (i.e., the RMS surfaced roughness of sidewalls 240). Alternatively or additionally, the surface of roughness mask precursor 501 (and a subsequently formed roughness mask) may exhibit a (second) maximum roughness ($Rmax_2$) ranging from greater than 0 to about 500nm, such as from about 50 to about 100nm, wherein $Rmax_2$ is less than $Rmax_1$ (i.e., the maximum surface roughness of sidewalls 240). Of course such roughness values are for the sake of example only, and it should be understood that RMS_2 and $Rmax_2$ may vary widely, and may be larger or smaller than the above noted ranges. In any case, RMS_1 and $Rmax_1$ may be greater than RMS_2 and $Rmax_2$, respectively, by an amount ranging from greater than 0 to about 5, 10, 15, 20, or even 25% or more. Without limitation, in some embodiments RMS_1 is greater than RMS_2 by greater than or equal to about 10, 20, or even 25%. Likewise in some embodiments $Rmax_1$ in some embodiments is greater than $Rmax_2$ by greater than or equal to about 10, 20, or even 25% or more.

[0061] Returning to FIG. 4, once a roughness mask precursor has been provided pursuant to block 405, the method may proceed to block 410. Pursuant to block 410, the roughness mask precursor may be processed to form a roughness mask. This concept is shown in FIG. 5C, which depicts modified device precursor 500'' as including roughness mask 515, wherein roughness mask 515 is disposed on sidewalls 240 of via 220. Without limitation and as shown in FIG. 5C, in some embodiments roughness mask 515 may be disposed only on sidewalls 240 of via 220. For ease of reference, roughness mask 515 may be referred to herein as including a second via facing surface, i.e., a surface which faces towards via 220, as opposed to the first via facing surface of sidewalls 240 of dielectric material 215.

[0062] Roughness mask 515 may be formed in any suitable manner. For example, in some embodiments roughness mask may be formed by subjecting device precursor

500' to a reactive dry etching process that is designed to remove the portions of roughness mask precursor 501 that are disposed on the upper surface of dielectric material 215, and at the bottom of via 220 (i.e., in the region proximate surface 207 of metallization layer 205). Alternatively or additionally, roughness mask 515 may be formed by removing the portion of roughness mask precursor 501 on the upper surface of dielectric material 215 via chemical mechanical polishing (CMP), after which an etching process may be employed to remove the portion of roughness mask precursor 501 proximate surface 207 of metallization layer 205. Of course, such methods are for the sake of example only, and any suitable method may be used to form roughness mask 515.

[0063] As further shown in FIG. 5B, roughness mask precursor 501 may be in the form of a layer of material that is deposited on the upper surface of dielectric layer 510, the sidewalls 240 of via 220, and the exposed surface 207 of metallization layer 205.

[0064] Returning to FIG. 4, once a roughness mask has been provided pursuant to block 410, the method may proceed to block 130. Pursuant to such block, a metal layer stack (MLS) may be formed with the via(s) of the device precursor. As the operations pursuant to block 130 are substantially the same as those described above with regard to block 130 of FIG. 1, such operations are not described in detail again. As may be appreciated, the performance of such operations may result in the provision of an MLS layer on the (relatively smooth) surface of the roughness mask, instead of the (relatively rough) surface of the sidewall of a via. This concept is illustrated in FIG. 5D, which depicts MLS layer 225 as being formed over the upper surface of dielectric material 215, on surface 520 of roughness mask 515, and on the surface 207 of metallization layer 205.

[0065] At this point, method 400 may proceed from block 130 to optional block 420, pursuant to which metallization of the via may be performed. Various methods for performing such metallization are understood in the art, and therefore are not described in detail herein. In some embodiments, the operations of optional block 420 may include the deposition of one or more metals (or other conductive materials) via sputtering, vapor deposition, electrodeposition, combinations thereof, and the like. Following such deposition, the resulting deposited metal (which may be in the form of a layer) may be processed, e.g., to form a contact, metal ball, or the like, as desired.

[0066] This concept is shown in FIG. 5E, which depicts modified device precursor 500''' as including a metal fill 530, which may be formed from any suitable conductive material such as those noted above. As may be appreciated, structures similar to those shown in FIG. 5E may be suitable for a variety of applications, such as in interlayer dielectric layers of a semiconductor device, in interconnects of semiconductor device, in a bump under metallization layer of a semiconductor device, combinations thereof, and the like. Of course, such uses are for the sake of example only, and the structure of FIG. 5E may be used in other contexts as would be understood by one of ordinary skill in the art.

10 [0067] As may be appreciated from the foregoing, the quality of MLS layer 225 in FIGS. 5D and 5E may be improved relative to the quality of MLS layer 225 in FIG. 2C. That is, relatively few defects may be formed within or proximate to MLS layer 225 in FIGS. 5D and 5E. Without wishing to be bound by theory, it is believed that this improvement in the quality of the MLS layer is due to the fact that roughness mask 515 may operate to mask the surface roughness and/or other defects that may appear within the surface of the sidewalls 240 of via 220 (i.e., within dielectric material 215). More specifically, it is believed that roughness mask 515 may present a surface that is relatively smooth and/or which contains relatively few defects, as compared to the surface of sidewalls 240 of dielectric material 215. As a result, the MLS layer may adopt the relatively smooth topography of the roughness mask, while limiting or even preventing the generation of defects (e.g., whiskers, hillocks, voids) therein.

[0068] To illustrate this concept, reference is made to FIG. 6A, which is an SEM image of a device precursor prepared in accordance with the method of FIG. 4. In particular, the illustrated micrograph is of a device precursor that includes a metallization layer 205 of one or more metals, a barrier layer 210 formed of a hermetic nitride, a 3000 angstrom thick roughness mask 515 of CVD deposited silicon nitride, and a dielectric material 215 of a spin on composite polymer dielectric. A device precursor including such components and having the same structure as shown in FIG. 5A was prepared and processed to form a via in a manner consistent with the foregoing description. Sputtering was then performed to deposit a metal layer stack 225 including a barrier layer of titanium nitride and a seed layer of copper within the via. Subsequently, a bulk metal fill 530 was deposited within the via.

[0069] Prior to deposition of the roughness mask, Atomic force microscopy was used to measure the RMS and Rmax parameters of the sidewalls 240 (not labeled in FIGS. 6A and 6B) dielectric material 215. Those measurements revealed that the sidewalls exhibited an RMS roughness (RMS_1) of about 7.3 nm, and an Rmax ($Rmax_1$) of about 64.8 nm. Following deposition and processing of the roughness mask 515 (i.e., the creation of a structure consistent with FIG. 5C), atomic force microscopy was performed to measure the RMS and Rmax parameters of the roughness mask. Those measurements revealed that the RMS roughness (RMS_2) of about 5.9 nm and an Rmax roughness ($Rmax_2$) of about 47.8nm. Put in other terms, in this example RMS_2 was about 20% less than RMS_1 , and $Rmax_2$ was about 26% less than RMS_1 .

[0070] With the foregoing in mind, FIG. 6B is a magnified view of region B of the device precursor of FIG. 6A. As shown, region B focuses on an interface between roughness mask 515 and the sidewall 240 of via 220, as well as the surface 520 of roughness mask 515 at an interface between MLS 225 and roughness mask 515. As shown, a defect 530 (in this case, a void) was observed proximate a ridge in the surface of sidewall 240. As further shown, roughness mask 515 obscured defect 530 in this region, and presented a relatively smooth surface 520 for the deposition of MLS 225. As a result, defect 530 was not carried through into MLS 225. Moreover, the surface roughness of MLS 225 in FIG. 6B was less than the surface roughness of MLS 225 observed in FIG. 3B. As a result, MLS 225 of FIG. 6B was determined to be of relatively high quality, as compared to MLS 225 of FIG. 3B.

[0071] Another aspect of the present disclosure relates to semiconductor devices that include one or more layers including a roughness mask consistent with the present disclosure. In some embodiments, the semiconductor devices include an interlayer dielectric layer, wherein the interlayer dielectric includes a composite dielectric that has been processed to form vias or trenches, e.g., in a manner consistent with the description above. In various embodiments, the vias and/or trenches of the interlayer dielectric layer may include a roughness mask on one or more sidewalls thereof. As described above, the roughness mask may provide a relatively smooth and/or uniform surface for the deposition of subsequent layers, e.g., by masking the surface roughness of the underlying sidewall and/or defects contained therein.

[0072] In other embodiments, the semiconductor devices may include a bump under metallization layer, which may be used to facilitate electrical coupling of a first

semiconductor device to a second semiconductor device. In some embodiments, the bump under metallization layer may include a layer of composite dielectric material disposed over a conductive material (e.g., a metal pad), wherein the composite dielectric layer includes vias and/or trenches, as described above. In some

5 embodiments, the vias/trenches may be substantially aligned with or otherwise configured to expose a portion of the underlying conductive material. In such instances a roughness mask may be formed on one or more sidewalls of the trenches and/or voids. As described above, the roughness mask may provide a relatively smooth and/or uniform surface for the deposition of subsequent layers, e.g., by

10 masking the surface roughness of the underlying sidewall and/or defects contained therein. For example, the roughness mask may provide a relatively uniform surface for the deposition of an MLS layer, upon which one or more metal bumps may be formed.

[0073] EXAMPLES:

15 **[0074] Example 1:** According to this example there is provided a method of making a semiconductor device, including: forming a roughness mask on a device precursor including a dielectric layer including at least one via, the via including sidewalls and a bottom, such that the roughness mask is disposed at least on the sidewalls.

20 **[0075] Example 2:** This example includes any or all of the features of example 1, wherein the sidewalls of the via comprise a first via facing surface; the roughness mask is formed on the first via facing surface and includes a second via facing surface; and the first via facing surface is relatively rough, as compared to the second via facing surface.

25 **[0076] Example 3:** This example includes any or all of the features of example 2, wherein: the first via facing surface has a first root mean square surface roughness RMS_1 ; the roughness mask has a second root mean square surface roughness, RMS_2 ; and $RMS_1 > RMS_2$.

30 **[0077] Example 4:** This example includes any or all of the features of example 2, wherein: the device precursor further includes a substrate, a metallization layer on the substrate, and a barrier layer on the metallization layer, wherein the dielectric layer is formed on the barrier layer and has been patterned into regions of the dielectric material; the sidewalls of the via are defined at least in part by the regions of dielectric material; at least a portion of the barrier layer has been removed to expose at least a

portion of the surface of the metallization layer; and the via extends through the barrier layer to the exposed portion of the surface of the metallization layer.

5 [0078] **Example 5:** This example includes any or all of the features of any one of examples 1 to 4, wherein the dielectric material includes a composite dielectric material.

[0079] **Example 6:** This example includes any or all of the features of example 5, wherein the composite dielectric material includes a polymer dielectric.

10 [0080] **Example 7:** This example includes any or all of the features of any one of examples 1 to 6, wherein the roughness mask includes a dielectric oxide, dielectric nitride, dielectric carbide, or one or more combinations thereof.

[0081] **Example 8:** This example includes any or all of the features of example 3, wherein RMS_1 is at least about 10% greater than RMS_2 .

[0082] **Example 9:** This example includes any or all of the features of example 8, wherein RMS_1 is at least about 20% greater than RMS_2 .

15 [0083] **Example 10:** This example includes any or all of the features of example 4, wherein forming the roughness mask includes: forming a roughness mask precursor on an upper surface of the regions of the dielectric material, on the first via facing surface of the sidewalls, and on the exposed surface of the metallization layer; and selectively removing the roughness mask precursor from the upper surface of the regions of the dielectric material and from the exposed surface of the metallization layer.

20 [0084] **Example 11:** This example includes any or all of the features of example 10, wherein selectively removing the roughness mask from the upper surface of the regions of the dielectric material and from the exposed surface of the metallization layer is performed via an etching process.

25 [0085] **Example 12:** This example includes any or all of the features of example 1, wherein: prior to forming the roughness mask, the device precursor includes a substrate, a metallization layer on the substrate, a barrier layer on the metallization layer, and the dielectric layer, wherein the dielectric layer is formed on the barrier layer and has been patterned into regions of the dielectric material and to expose a surface of the barrier layer; and the method further includes selectively removing a

portion of the exposed surface of the barrier layer to expose a portion of the surface of the metallization layer, thereby forming the via.

[0086] Example 13: This example includes any or all of the features example 12, wherein: the regions of dielectric material comprise a composite dielectric material including at least first and second components; the selective removal of a portion of the exposed surface of the barrier layer is performed at least in part with an etching process; and during the etching process, the device precursor is exposed to an etching chemistry that etches the first and second components at different rates.

[0087] Example 14: This example includes any or all of the features of any one of examples 1 to 13, wherein forming the roughness mask is formed via chemical vapor deposition.

[0088] Example 15: This example includes any or all of the features of any one of examples 1 to 14, wherein: the regions of dielectric material have a glass transition temperature T1; forming the roughness mask includes depositing a roughness mask material at a deposition temperature T2; and T2 is less than or equal to T1.

[0089] Example 16: This example includes any or all of the features of example 15, wherein T2 is less than T1.

[0090] Example 17: This example includes any or all of the features of any one of examples 1 to 16, further including forming a metal layer stack within the via, wherein at least a portion of the metal layer stack is formed on the roughness mask.

[0091] Example 18: This example includes any or all of the features of example 17, wherein at least a portion of the metal layer stack is formed directly on the roughness mask.

[0092] Example 19: This example includes any or all of the features of any one of examples 1 to 18, further including forming a metal fill in the via.

[0093] Example 20: According to this example there is provided a semiconductor device including: a dielectric layer including dielectric material; a via in the dielectric layer, the via including sidewalls defined at least in part by the dielectric material; a roughness mask on the sidewalls; and at least one metal layer in the via.

[0094] Example 21: This example includes any or all of the features of example 20, wherein: the sidewalls of the via comprise a first via facing surface; the roughness mask is formed on the first via facing surface and includes a second via facing

surface; and the first via facing surface is relatively rough, as compared to the second via facing surface.

[0095] **Example 22:** This example includes any or all of the features of example 21, wherein: the first via facing surface has a first root mean square surface roughness RMS₁; the second via facing surface has a second root mean square surface roughness, RMS₂; and RMS₁ > RMS₂.

[0096] **Example 23:** This example includes any or all of the features of any one of examples 20 to 23, wherein: the device further includes a substrate, a metallization layer on the substrate, and a barrier layer on the metallization layer, wherein the dielectric layer including the dielectric material is formed on the barrier layer; and the via extends from an upper surface of the dielectric layer to an upper surface of the metallization layers.

[0097] **Example 24:** This example includes any or all of the features of example 22, wherein at least a portion of the upper surface of the metallization layer forms at least a portion of the bottom of the via.

[0098] **Example 25:** This example includes any or all of the features of any one of examples 20 to 24, wherein, the dielectric material includes a composite dielectric material.

[0099] **Example 26:** This example includes any or all of the features of example 25, wherein the composite dielectric material includes a polymer dielectric.

[00100] **Example 27:** This example includes any or all of the features of any one of examples 20 to 26, wherein the roughness mask includes a dielectric oxide, dielectric nitride, dielectric carbide, or one or more combinations thereof.

[00101] **Example 28:** This example includes any or all of the features of example 27, wherein the roughness mask is formed from silicon carbide, silicon nitride, silicon oxide, or one or more combinations thereof.

[00102] **Example 29:** This example includes any or all of the features of example 22, wherein RMS₁ is at least about 10% greater than RMS₂.

[00103] **Example 30:** This example includes any or all of the features of example 29, wherein RMS₁ is at least about 20% greater than RMS₂.

[00104] **Example 31:** This example includes any or all of the features of example 26, wherein the composite dielectric material includes at least first and second components.

[00105] **Example 32:** This example includes any or all of the features of any one of examples 20 to 31, wherein the at least one metal layer includes a metal layer stack, wherein at least a portion of the metal layer stack is formed on the roughness mask.

[00106] **Example 33:** This example includes any or all of the features of example 32, wherein at least a portion of the metal layer stack is formed directly on the roughness mask.

10 [00107] **Example 34:** This example includes any or all of the features of any one of examples 20 to 33, wherein the at least one metal layer includes a metal fill, at least a portion of the metal fill being disposed in the via.

[00108] As used herein, the term “about” when used in conjunction with a numerical value or range, should be understood to refer to +/- 5% of the stated amount or upper and lower bounds of the stated range, unless otherwise expressly indicated. Furthermore in the context of the present disclosure, the terms “on,” when used in conjunction with a first layer should be understood to indicate that the first layer is disposed above another (second)” layer, but not necessarily directly on an upper surface of the second layer. Thus, a first layer may be on a second layer, even if a third (intervening layer) is present between the upper surface of the second layer and the bottom surface of the first layer. In contrast, the term “directly on” should be construed to mean that a first layer is disposed directly on an upper surface of a second layer.

[00109] The terms and expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described (or portions thereof), and it is recognized that various modifications are possible within the scope of the claims. Accordingly, the claims are intended to cover all such equivalents. Various features, aspects, and embodiments have been described herein. The features, aspects, and embodiments are susceptible to combination with one another as well as to variation and modification, as will be understood by those having skill in the art. The present disclosure should, therefore, be considered to encompass such combinations, variations, and modifications.

CLAIMS

What is claimed is:

1. A method of making a semiconductor device, comprising:
forming a roughness mask on a device precursor comprising a dielectric layer comprising at least one via, the via comprising sidewalls and a bottom, such that said roughness mask is disposed at least on said sidewalls.
2. The method of claim 1, wherein
the sidewalls of said via comprise a first via facing surface;
said roughness mask is formed on said first via facing surface and comprises a second via facing surface; and
said first via facing surface is relatively rough, as compared to said second via facing surface.
3. The method of claim 2, wherein:
said first via facing surface has a first root mean square surface roughness RMS_1 ;
said roughness mask has a second root mean square surface roughness, RMS_2 ;
and
 $RMS_1 > RMS_2$.
4. The method of claim 2, wherein:
said device precursor further comprises a substrate, a metallization layer on the substrate, and a barrier layer on the metallization layer, wherein said dielectric layer is formed on said barrier layer and has been patterned into regions of said dielectric material;
the sidewalls of said via are defined at least in part by said regions of dielectric material;
at least a portion of said barrier layer has been removed to expose at least a portion of the surface of the metallization layer; and
said via extends through said barrier layer to the exposed portion of the surface of the metallization layer.

5. The method of any one of claims 1 to 4, wherein said dielectric material comprises a composite dielectric material.
6. The method of claim 4, wherein forming said roughness mask comprises:
forming a roughness mask precursor on an upper surface of said regions of said dielectric material, on said first via facing surface of said sidewalls, and on said exposed surface of said metallization layer; and
selectively removing said roughness mask precursor from the upper surface of said regions of said dielectric material and from the exposed surface of said metallization layer.
7. The method of claim 6, wherein selectively removing said roughness mask from the upper surface of said regions of said dielectric material and from the exposed surface of said metallization layer is performed via an etching process.
8. The method of claim 1, wherein:
prior to forming said roughness mask, said device precursor comprises a substrate, a metallization layer on the substrate, a barrier layer on the metallization layer, and said dielectric layer, wherein said dielectric layer is formed on said barrier layer and has been patterned into regions of said dielectric material and to expose a surface of the barrier layer; and
the method further comprises selectively removing a portion of the exposed surface of the barrier layer to expose a portion of the surface of the metallization layer, thereby forming said via.
9. The method of claim 8, wherein:
said regions of dielectric material comprise a composite dielectric material comprising at least first and second components;
the selective removal of a portion of the exposed surface of the barrier layer is performed at least in part with an etching process; and
during said etching process, the device precursor is exposed to an etching chemistry that etches the first and second components at different rates.

10. The method of claim 1, wherein forming said roughness mask is performed at least in part by chemical vapor deposition.
11. The method of claim 1, wherein:
 - said regions of dielectric material have a glass transition temperature T1;
 - forming said roughness mask comprises depositing a roughness mask material at a deposition temperature T2; and
 - T2 is less than or equal to T1.
12. The method of claim 11, wherein T2 is less than T1.
13. The method of claim 1, wherein said at least one metal layer comprises a metal layer stack, wherein at least a portion of said metal layer stack is formed on said roughness mask.
14. The method of claim 13, wherein at least a portion of said metal layer stack is formed directly on said roughness mask.
15. The method of claim 13, wherein said at least one metal layer further comprises a metal fill in said via, at least a portion of said metal fill being on said metal layer stack.
16. A semiconductor device comprising:
 - a dielectric layer comprising dielectric material;
 - a via in said dielectric layer, the via comprising sidewalls defined at least in part by said dielectric material;
 - a roughness mask on said sidewalls; and
 - at least one metal layer in said via.
17. The semiconductor device of claim 16, wherein:
 - the sidewalls of said via comprise a first via facing surface;
 - said roughness mask is formed on said first via facing surface and comprises a second via facing surface; and

said first via facing surface is relatively rough, as compared to said second via facing surface.

18. The semiconductor device of claim 17, wherein:

said first via facing surface has a first root mean square surface roughness RMS_1 ;

said second via facing surface has a second root mean square surface roughness, RMS_2 ; and

$RMS_2 > RMS_1$.

19. The semiconductor device of claim 16, wherein:

said device further comprises a substrate, a metallization layer on the substrate, and a barrier layer on the metallization layer, wherein said dielectric layer comprising said dielectric material is formed on the barrier layer; and

said via extends from an upper surface of said dielectric layer to an upper surface of the metallization layers.

20. The semiconductor device of claim 19, wherein at least a portion of the upper surface of the metallization layer forms at least a portion of the bottom of said via.

21. The semiconductor device of any one of claims 16 to 20, wherein, said dielectric material comprises a composite dielectric material.

22. The semiconductor device of claim 21, wherein said composite dielectric material comprises at least first and second components.

23. The semiconductor device of claim 16, wherein said at least one metal layer comprises a metal layer stack, wherein at least a portion of said metal layer stack is formed on said roughness mask.

24. The semiconductor device of claim 23, wherein at least a portion of said metal layer stack is formed directly on said roughness mask.

25. The semiconductor device of claim 23, wherein said at least one metal layer further comprises a metal fill, at least a portion of the metal fill being disposed in said via.

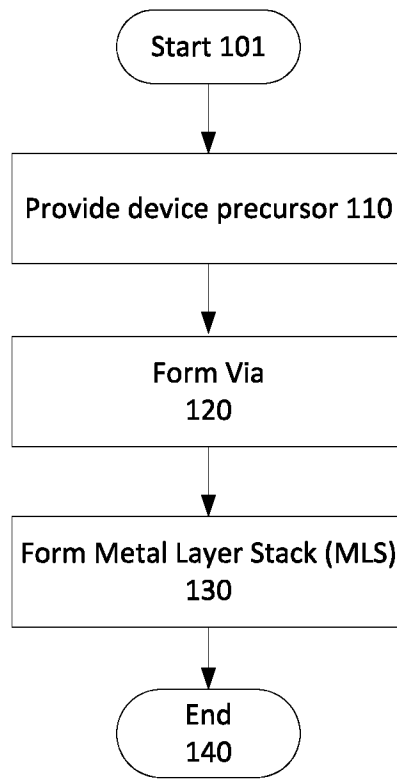
100

FIG. 1

200

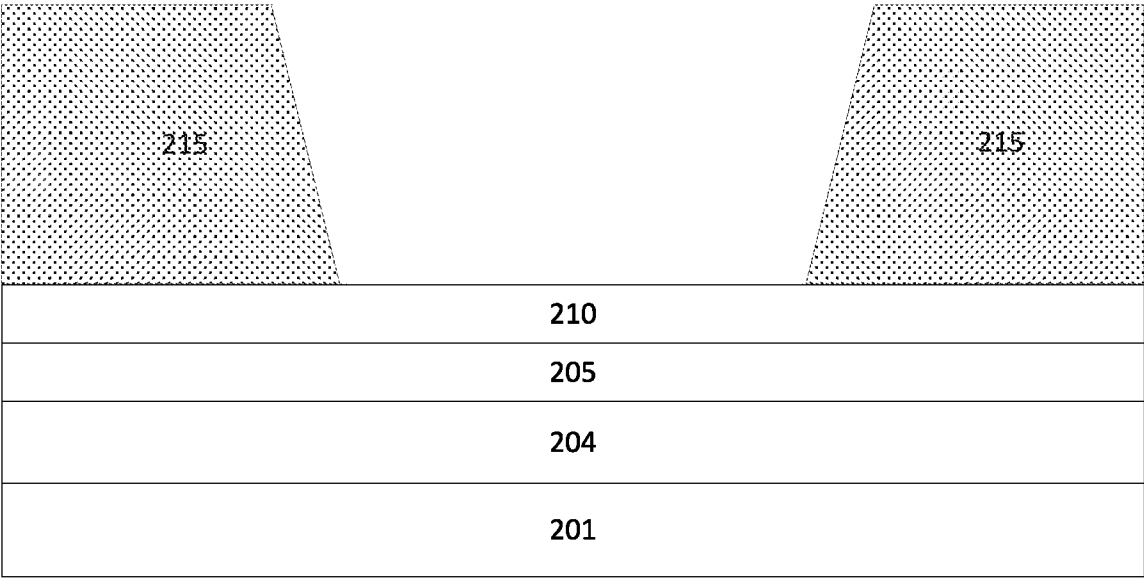


FIG. 2A

200'

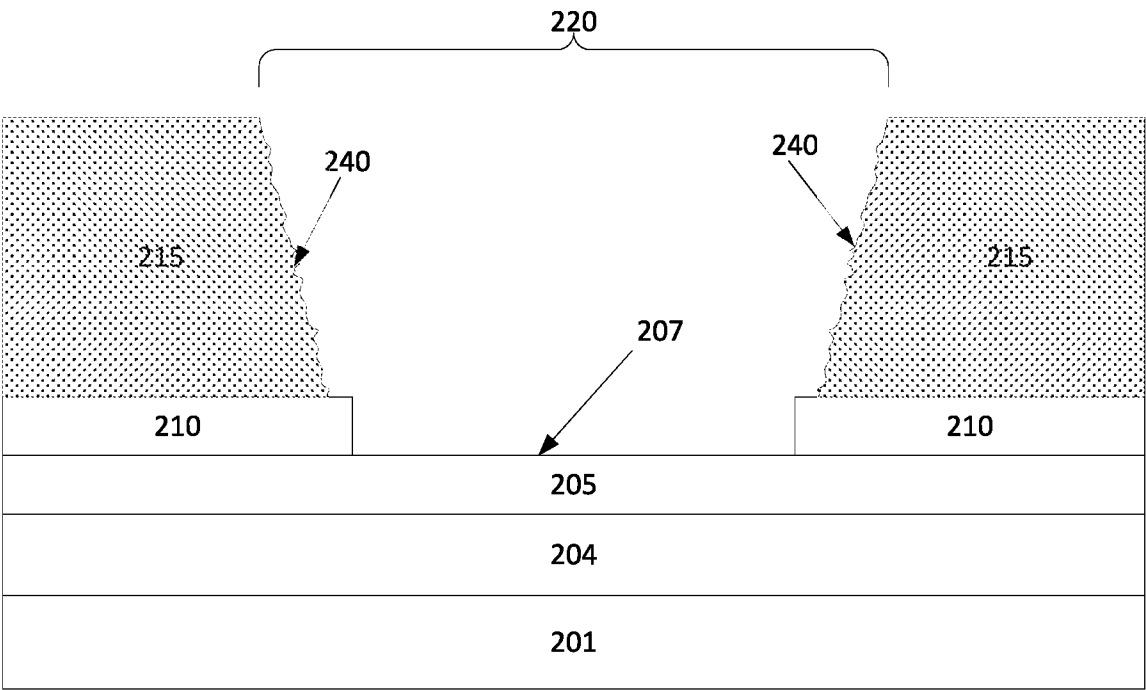


FIG. 2B

200"

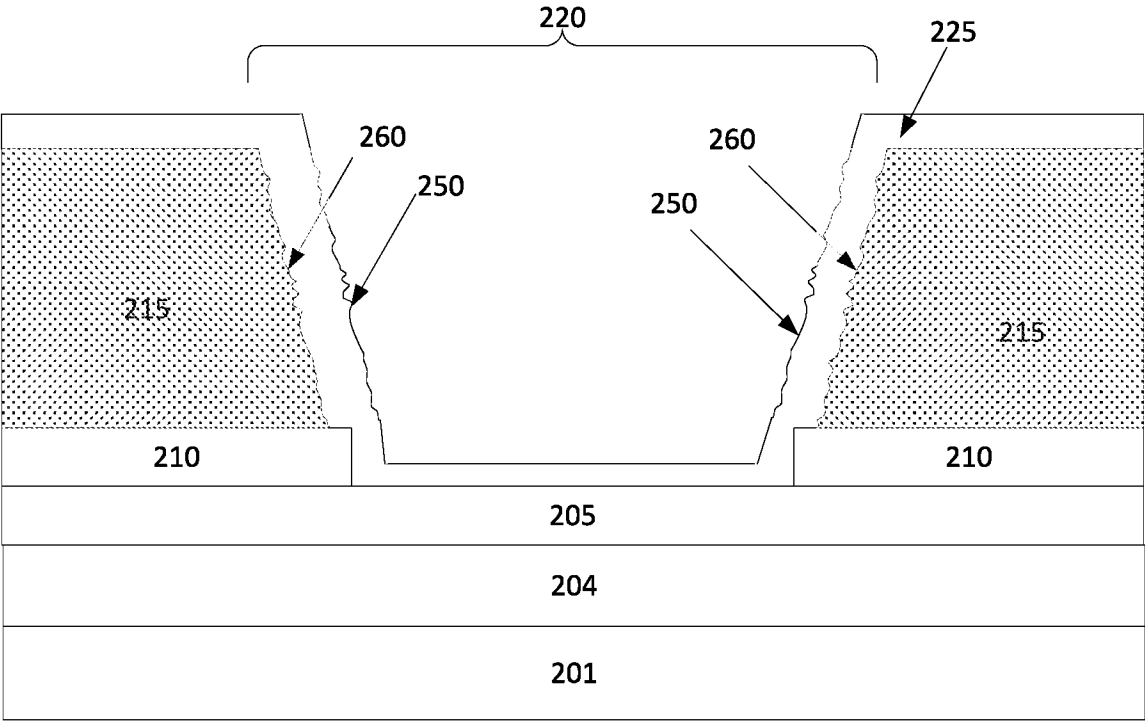


FIG. 2C

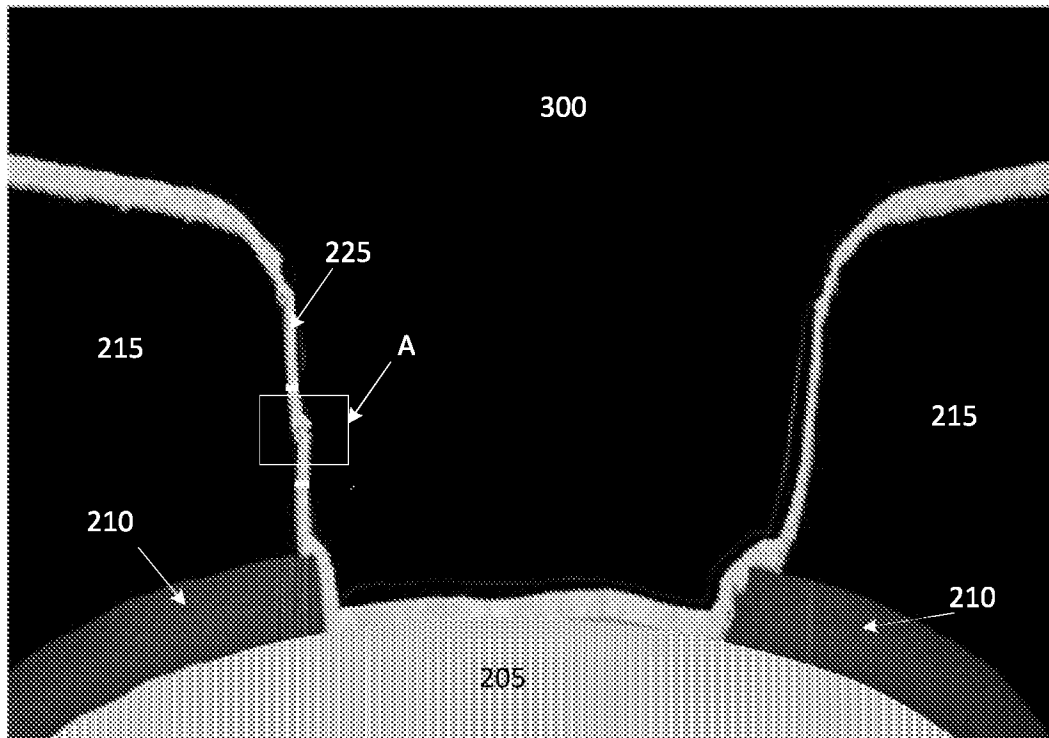


FIG. 3A

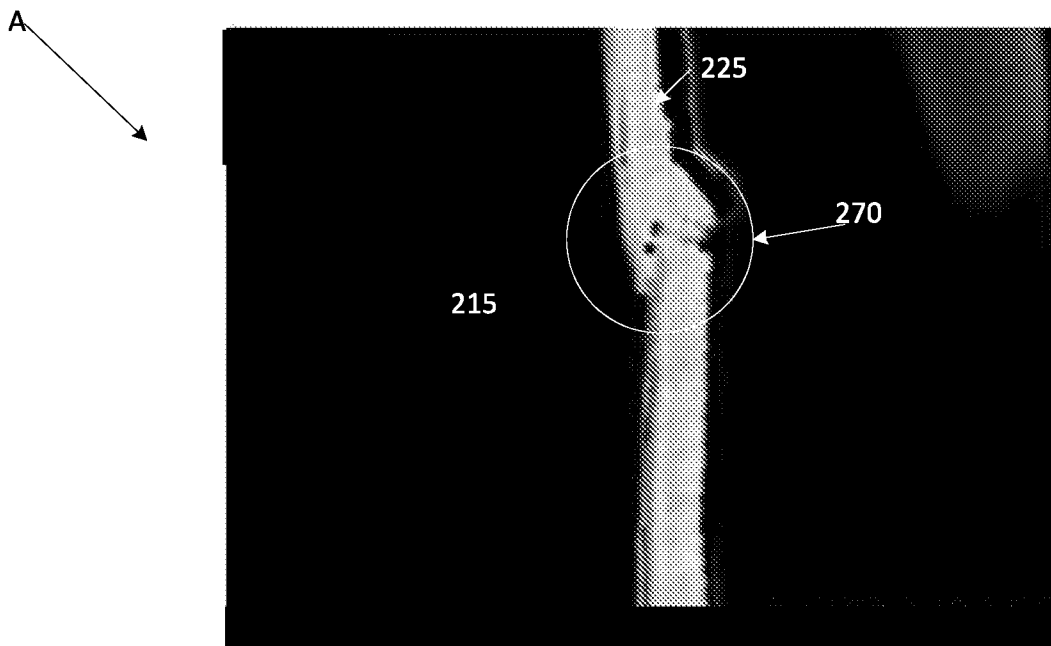


FIG. 3C

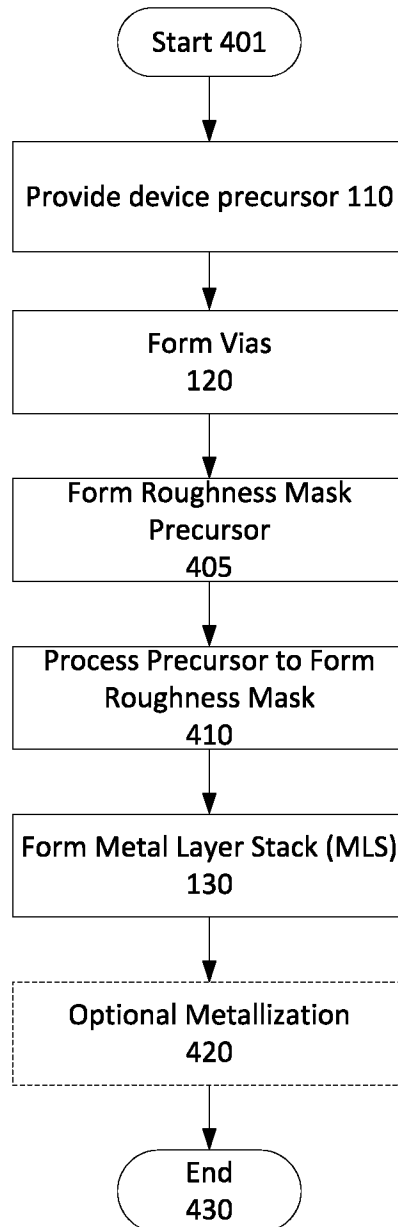
400

FIG. 4

500

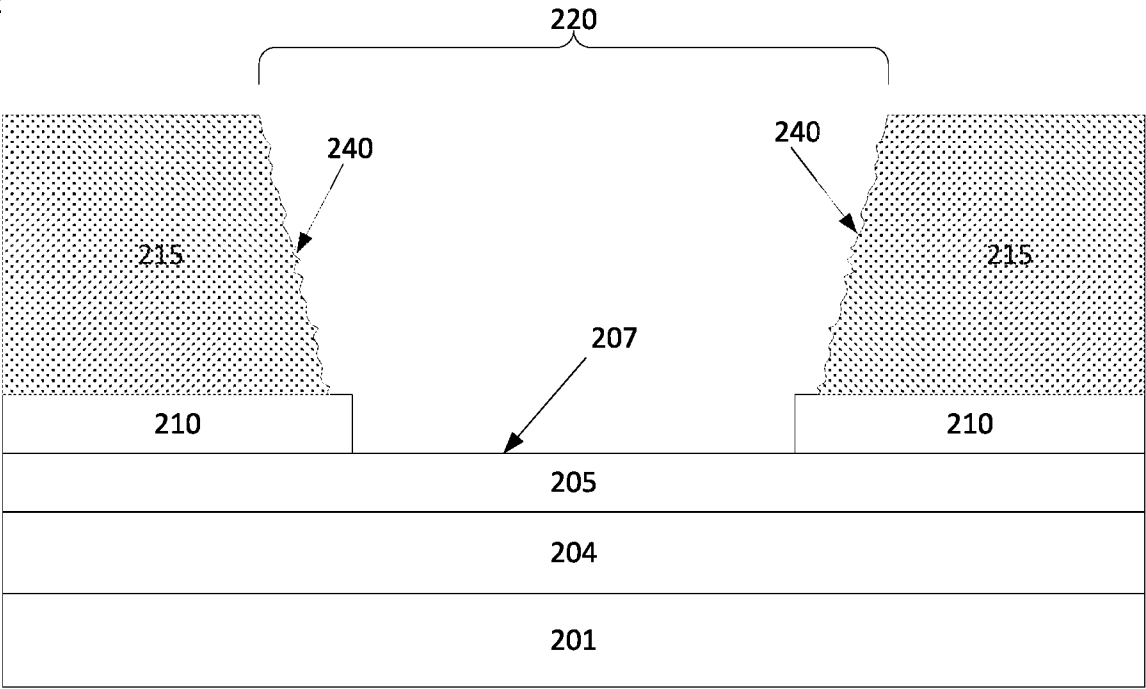


FIG. 5A

500'

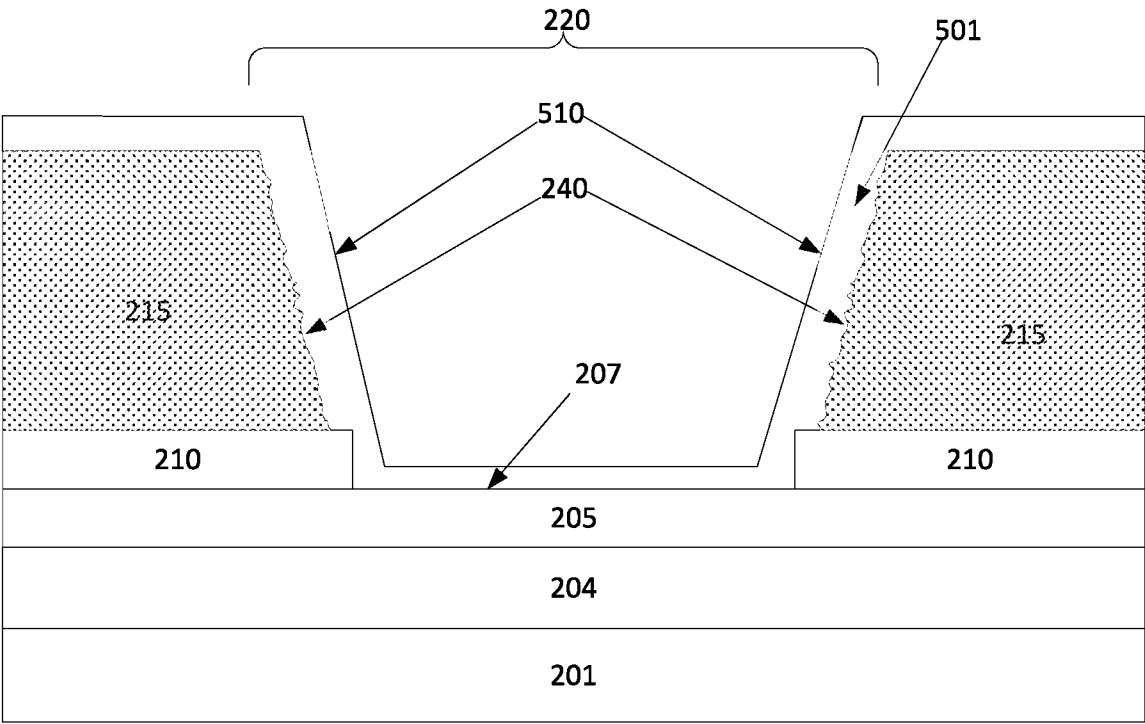


FIG. 5B

500''

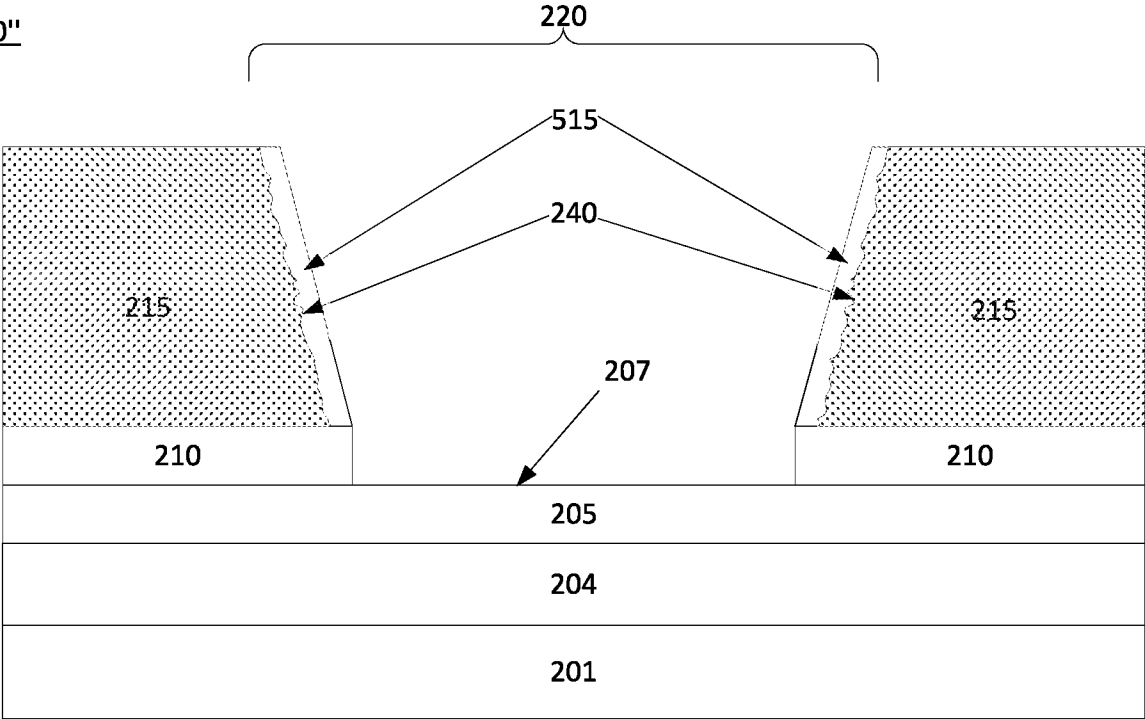


FIG. 5C

500'''

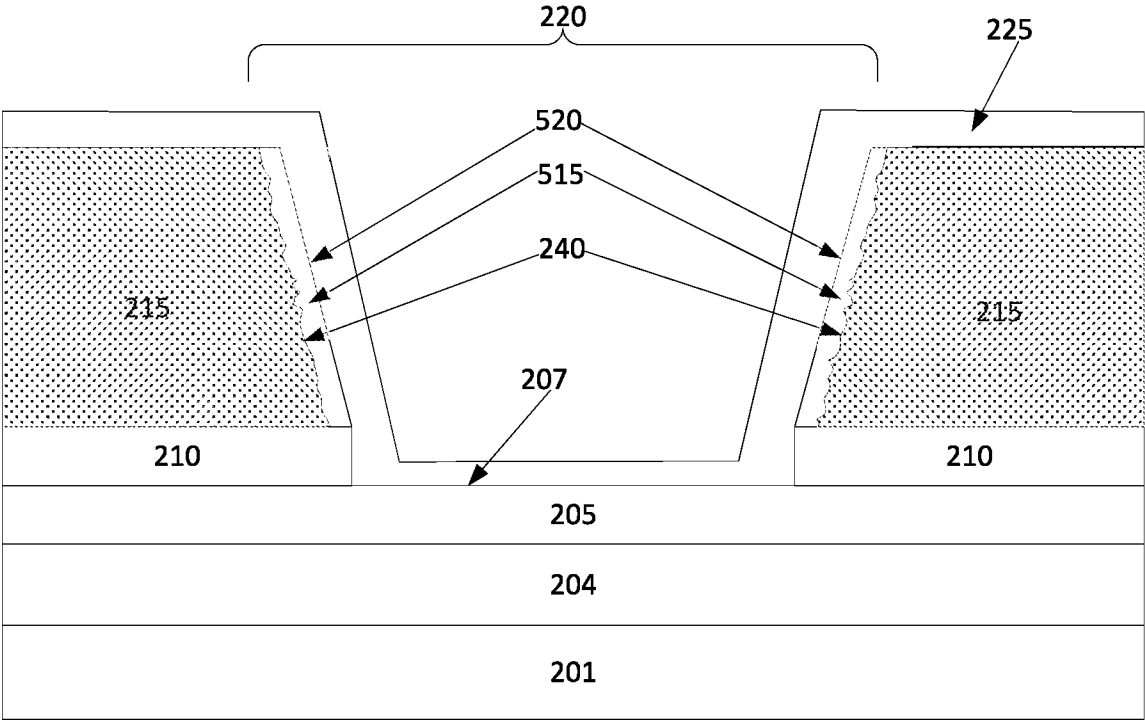


FIG. 5D

500''''

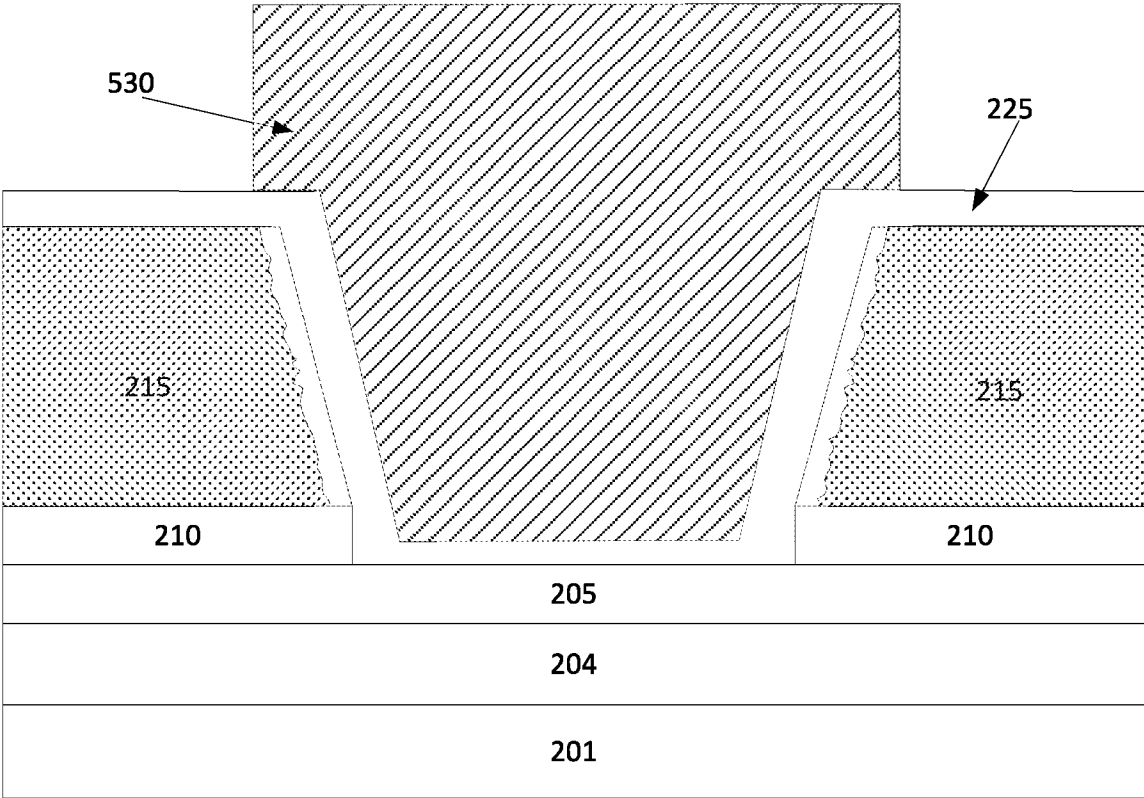


FIG. 5E

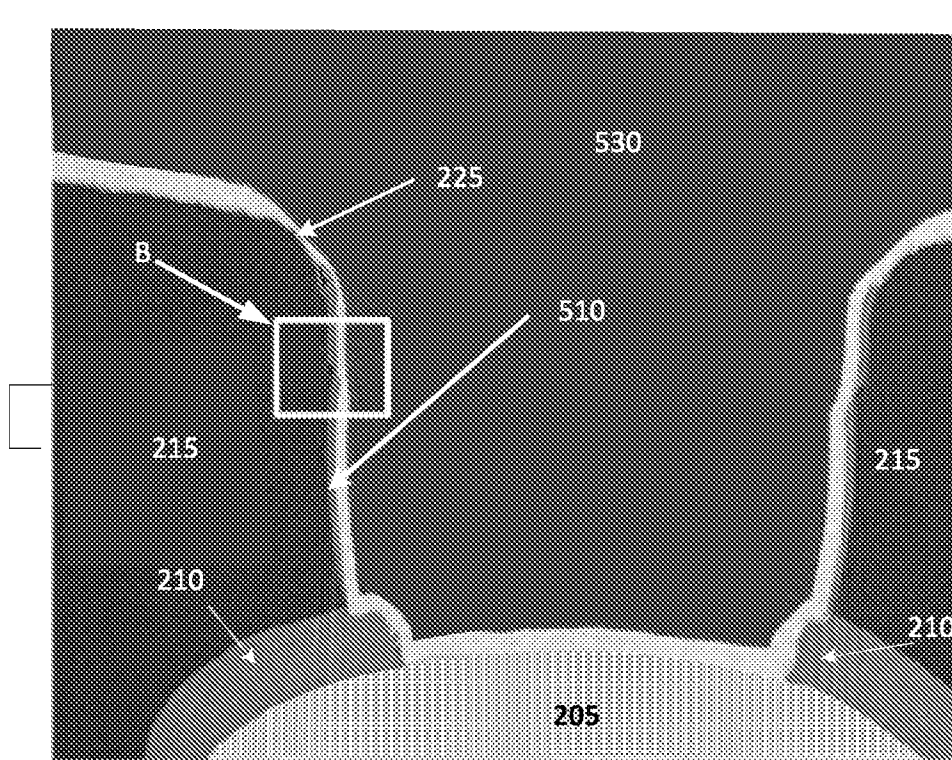


FIG. 6A

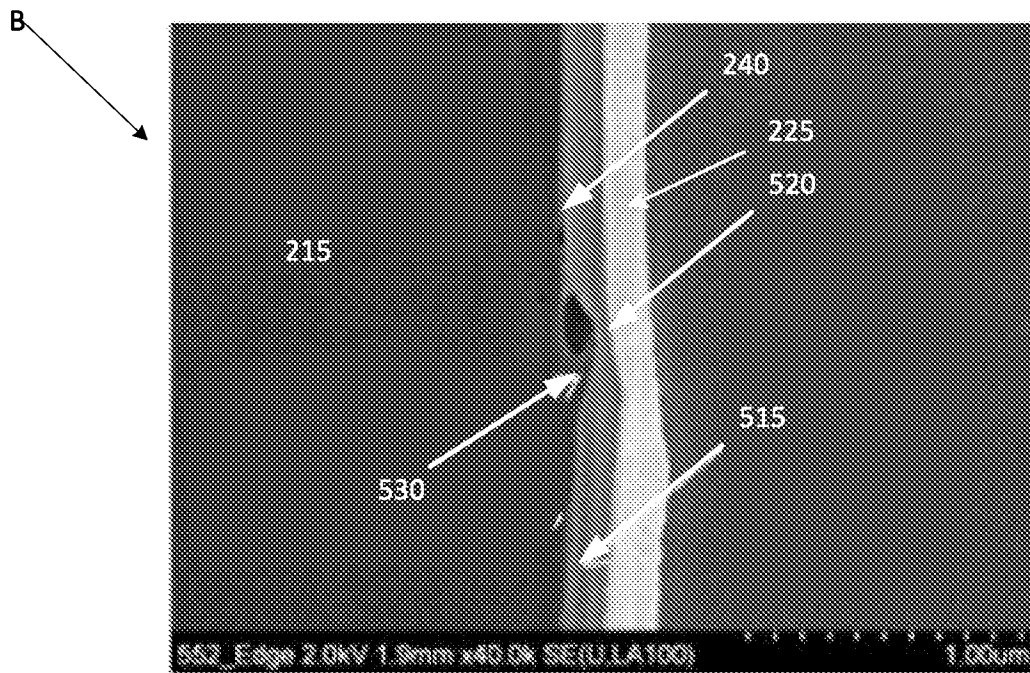


FIG. 6B

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/027(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/027; H01L 23/52; H01L 21/302; H01L 21/3213; H01L 21/4763; H01L 29/40; H01L 21/76; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: etch, via, sidewall, roughness, dielectric

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007-0049007 A1 (CHIH-CHAO YANG et al.) 01 March 2007 See abstract; paragraphs [0023], [0024], [0028]; claim 1; and figures 3-5a, 10, 11.	1, 5, 8-10, 13-16, 19-25
Y		2-4, 6, 7, 17, 18, 11, 12
A		
Y	US 6528386 B1 (SCOTT R. SUMMERFELT et al.) 04 March 2003 See abstract; column 6, lines 56-60; claim 1; and figure 10.	2-4, 6, 7, 17, 18
A	US 2011-0031623 A1 (CHIH-CHAO YANG et al.) 10 February 2011 See abstract; paragraphs [0008]-[0011]; and figures 1A-1E.	1-25
A	US 2010-0025825 A1 (DANIELLE L. DEGRAW et al.) 04 February 2010 See abstract; paragraphs [0036]-[0041]; claim 1; and figures 1A-1F.	1-25
A	WO 2014-144266 A1 (SEMPRIUS, INC.) 18 September 2014 See abstract; paragraphs [012], [013]; claim 1; and figure 1.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

22 June 2016 (22.06.2016)

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/052131

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2009-0194876 A1	06/08/2009
		US 7846834 B2	07/12/2010
		US 8405215 B2	26/03/2013
		WO 2009-098151 A1	13/08/2009
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WO 2014-144266 A1	18/09/2014	US 2014-0264937 A1	18/09/2014