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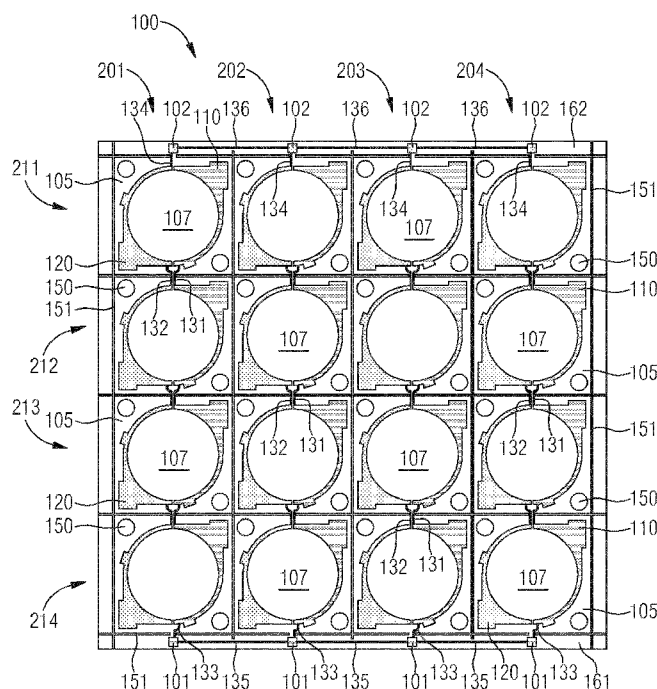
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(54) Title: COMPONENT CARRIER ASSEMBLAGE FOR OPTOELECTRONIC SEMICONDUCTOR COMPONENTS

FIG 2



(57) Abstract: The invention relates to a component carrier assembly for optoelectronic semiconductor components. The component carrier assembly comprises a number of component carriers for arranging optoelectronic semiconductor components. Each component carrier comprises a first contact structure and a second contact structure to which optoelectronic semiconductor components may be electrically connected. The component carrier assembly further comprises a first universal contact which is electrically connected to the first contact structures of the number of component carriers. The component carrier assembly further comprises a second universal contact which is electrically connected to the second contact structures of the number of component carriers. The invention furthermore relates to a method of producing optoelectronic devices.

Description

Component carrier assemblage for optoelectronic semiconductor components

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The invention relates to a component carrier assemblage for optoelectronic semiconductor components. The component carrier assemblage comprises a number of component carriers for arranging optoelectronic semiconductor components. The invention further relates to a method of producing optoelectronic devices.

An optoelectronic device may comprise a component carrier and a plurality of optoelectronic semiconductor components for generating light radiation, the optoelectronic semiconductor components being arranged on the carrier. The carrier may comprise contact structures to which optoelectronic semiconductor components may be electrically connected.

In a concept referred to as chip-on-board (COB), unpackaged optoelectronic semiconductor chips such as LED chips (light emitting diode) are arranged on a component carrier. A device produced in this way is also referred to as COB package or, respectively, COB unit. The carrier may for example be a metal core printed circuit board (MCPCB). The chips may for example be electrically connected to one another and to contact structures of the PCB via bond wires. Strings of chips connected in series may for example be provided.

In a possible method of producing such devices, a component carrier assemblage in the form of a panel is provided which comprises a number of connected component carriers or, respectively, MCPCB units. Optoelectronic semiconductor chips are arranged on the individual carriers, and are electrically connected to one another and to contact structures of the carriers by performing a wire bonding process. A light up test with a low electrical current is carried out after the wire bonding process in which the functionality of the indi-

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vidual units is tested. Defective units may be subjected to a rework process. Subsequent method steps include encapsulating the chips located on the carriers, and singularizing the carrier assemblage into separate optoelectronic devices.

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A component carrier usually comprises two contact pads by means of which the respective optoelectronic device may be contacted. In this way, electrical power may be supplied to the semiconductor chips arranged on the carrier for generat-
10 ing light radiation. The contact pads are also used in the above-mentioned functional test. The test is conducted with a probe card having connector pins. The pins are brought into contact with the contact pads of the individual carriers of the assemblage to provide an electrical connection to a power
15 supply. The tested units are inspected manually by an operator, or with the aid of an automated VI machine (visual inspection). In this way, chips or strings of chips that did not light up may be screened out.

20 Carrying out the functional test is time-consuming, because the carriers of the panel are typically tested one after another by contacting the associated contact pads of the same with the probe card pins. Moreover, for panels having different configurations, in particular different locations of the
25 contact pads of the carriers, different probe cards or a probe card with a sophisticated design comprising a plurality of pins are required to perform the test. Another problem consists in the probe pins potentially damaging the wire bonded units during the test procedure, e.g. caused by a mis-
30 alignment or improper movement of the probe card. This is due to the fact that the contact pads of the carrier units are located closely to the area of the wire bonded semiconductor chips.

35 It is an object of the present invention to provide an improved component carrier assemblage. It is a further object to provide an improved method of producing optoelectronic devices.

These objects are achieved by the features of the independent claims. Further preferred embodiments are disclosed in the dependent claims.

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According to an aspect of the invention, a component carrier assemblage for optoelectronic semiconductor components is provided. The component carrier assemblage comprises a number of component carriers for arranging optoelectronic semiconductor components. Each component carrier comprises a first contact structure and a second contact structure to which optoelectronic semiconductor components may be electrically connected. The component carrier assemblage further comprises a first universal contact and a second universal contact. The first universal contact is electrically connected to the first contact structures of the number of component carriers. The second universal contact is electrically connected to the second contact structures of the number of component carriers.

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The component carrier assemblage which comprises a composite arrangement of component carriers may be singularized into separate component carriers. The component carrier assemblage may be configured in the form of a panel, wherein the component carriers are arranged in a plane next to one another. Singularizing may be carried out in a method of producing optoelectronic devices in which the component carrier assemblage may be applied. In the method, previous to this, optoelectronic semiconductor components are arranged on the component carriers and electrically connected to the first and second contact structures of the same. Component carriers comprising or, respectively, being equipped with optoelectronic semiconductor components are also referred to as active units in the following. The optoelectronic semiconductor components may be configured to generate a light radiation when supplied with electrical power. The optoelectronic semiconductor components may comprise unpackaged optoelectronic semiconductor chips, for example LED chips.

The component carrier assemblage makes it possible to apply respective electrical potentials to all first contact structures and to all second contact structures of the individual component carriers of the carrier assemblage at the same time by using or, respectively, contacting the first and the second universal contact. In this way, several advantages with respect to a light up or, respectively, functional test, which may be carried out after arranging optoelectronic semiconductor components on the carrier assemblage to test the functionality of the active units, may be provided.

In the functional test, a probe card comprising connector pins may be applied in order to contact the first and second universal contact and to establish an electrical connection to a power supply. Consequently, electrical power may be applied to the first and second contact structures of all component carriers or, respectively, active units of the component carrier assemblage at the same time, so that the active units may be jointly tested. In this way, the functional test may be conducted in a relatively small period of time. Thus, the units per hour to be tested may be improved and testing in a method of producing optoelectronic devices may be carried out with an enhanced throughput.

The component carrier assemblage may furthermore be configured in such a way that the first and second universal contact are located relatively far away from the component carriers or, respectively, regions of the carriers on which the optoelectronic semiconductor components are arranged. Consequently, the functional test may be carried out without the problem that a probe card or, respectively, pins of the same damage the active units. The large distance may also simplify a visual inspection of the jointly tested active units.

It is for example possible that semiconductor or, respectively, LED chips such as sapphire chips are arranged on the component carriers and connected to each other and to the

first and second contact structures of the carriers by means of bond wires. Each semiconductor chip may for example comprise two front-side contacts. Several strings of chips connected in series may for example be provided on each of the component carriers. A large distance between the first and second universal contact to the carrier regions on which the semiconductor chips are arranged reduces the risk of die and bond wire defects (e.g. a probe pin causing a sagged or broken bond wire, a probe pin hitting and thus damaging or detaching a chip, etc.).

The functional test may be conducted with a simple probe card comprising only two connector pins to contact the first and second universal contact of the component carrier assemblage. This is possible even for the case that differently designed component carrier assemblages having the above described configuration are to be tested. The different carrier assemblages may for example comprise component carriers having a different size. The different component carrier assemblages may be provided in such a way that the locations of the first and second universal contacts are the same. Consequently, a universal probe card comprising two pins may be used to conduct a functional test with all the different carrier assemblages. A probe card with a sophisticated design comprising a plurality of pins may therefore be replaced. Having a universal probe card to handle different component carrier assemblages may save manufacturing cost. Moreover, using a simple probe card with a reduced number of pins may further help to simplify a visual inspection of tested active units, and may also improve the throughput in testing.

In the following, further possible embodiments of the component carrier assemblage are described. As an example, the first and second universal contact may be configured in the form of contact pads. Moreover, the component carrier assemblage may for example comprise conductor tracks for providing the electrical connection between the universal contacts and the respective contact structures of the component carriers.

In this respect, a possible embodiment of the component carrier assemblage provides that the first contact structures of adjacent component carriers are electrically connected to one another by means of conductor tracks, and that the second contact structures of adjacent component carriers are electrically connected to one another by means of conductor tracks. In this way, a part of the electrical connection between the first universal contact and the first contact structures of the number of component carriers and between the second universal contact and the second contact structures of the number of component carriers may be realized by means of the interconnected first and second contact structures. This allows for a simple electrical connection.

The conductor tracks which may serve as inter-unit traces may extend between the connected first and the connected second contact structures of the adjacent component carriers. The conductor tracks may furthermore be relatively thin and line-shaped. Consequently, singularizing the component carrier assemblage in a method of producing semiconductor devices, in which the carrier assemblage may be divided also in the area of the conductor tracks, may be facilitated.

It is possible that the interconnection of first and second contact structures is provided for groups of adjacent component carriers. This may for example be the case for a possible configuration of the carrier assemblage in which the component carriers are arranged in a plane next to one another in rows and columns. At this, the first and second contact structures of adjacent component carriers of the columns or, respectively, of the rows may be electrically connected to each other by means of respective conductor tracks.

Alternatively, a configuration of the component carrier assemblage may be considered in which all adjacent component carriers are electrically connected to each other by means of respective conductor tracks.

In a further embodiment of the component carrier assemblage, the first and second universal contact are arranged in the area of different edge sides of the component carrier assemblage. This configuration further promotes a simple electrical connection between the first universal contact and the first contact structures of the carriers and between the second universal contact and the second contact structures of the carriers. The arrangement of the first and second universal contact at different edge sides furthermore allows to prevent a faulty contacting of the first and second universal contact with reversed polarity. Moreover, the first and second universal contact may be arranged at a relatively large distance to the carriers or, respectively, active units, thus preventing the risk of damaging active units in a functional test with a high reliability.

It may be provided that the carrier assemblage comprises respective side sections on which the first and second universal contact are arranged. Furthermore, the different edge sides in the area of which the universal contacts are arranged may be opposite edge sides of the carrier assemblage.

In a further embodiment of the component carrier assemblage, the first universal contact is electrically connected to the first contact structure of an adjacent component carrier by means of a conductor track, and the second universal contact is electrically connected to the second contact structure of an adjacent component carrier by means of a conductor track. This configuration further promotes a simple electrical connection. These conductor tracks may be relatively thin and line-shaped, as well, thus facilitating a singularization of the component carrier assemblage.

It may for example be provided that the first and second universal contact are arranged in the area of opposite edge sides on respective side sections of the carrier assemblage, as described above. In the singularization process, the side

sections may be separated from the rest of the carrier assemblage, wherein separating may also take place in the area of the conductor tracks.

5 In a further embodiment, the component carrier assemblage comprises several first and several second universal contacts. The first universal contacts are electrically connected to the first contact structures of the number of component carriers, and the second universal contacts are electrically connected to the second contact structures of the
10 number of component carriers. According to this embodiment of the component carrier assemblage, a functional test may be carried out by using or, respectively, contacting any one of the first and any one of second universal contacts. In this
15 way, a high flexibility is provided with respect to conducting the functional test.

Concerning the aforesaid configuration, a further embodiment provides that the several first and second universal contacts
20 are arranged in the area of opposite edge sides of the component carrier assemblage. The first universal contacts are electrically connected to one another by means of conductor tracks. Likewise, the second universal contacts are electrically connected to one another by means of conductor tracks.
25 In this way, a part of the electrical connection between a first universal contact and the first contact structures of the number of component carriers and between a second universal contact and the second contact structures of the number of component carriers may respectively be realized by means
30 of the interconnected first universal contacts and the interconnected second universal contacts. This allows for a simple electrical connection.

The component carrier assemblage may for example comprise respective side sections on which the several first and the
35 several second universal contacts are arranged.

In a further embodiment of the component carrier assemblage, the component carriers are arranged in rows and columns. In each column, the first contact structures of adjacent component carriers and the second contact structures of adjacent component carriers are electrically connected to one another by means of conductor tracks. The first universal contacts are electrically connected to the first contact structures of component carriers which are arranged at an end of the columns by means of conductor tracks. Likewise, the second universal contacts are electrically connected to the second contact structures of component carriers which are arranged at an opposite end of the columns by means of conductor tracks. This configuration promotes a simple electrical connection between the several first universal contacts and the first contact structures of the component carriers and between the several second universal contacts and the second contact structures of the component carriers.

In the aforesaid embodiment, each column of component carriers may comprise an associated first universal contact and an associated second universal contact, the first and second universal contact being arranged at the two opposite ends of the respective column. In this way, it may for example be considered to singularize the carrier assemblage into sections, each section comprising a column of component carriers and a respective first and second universal contact. Due to the provision of the first and second universal contact at each column of carriers, it is possible after the singularization to subject the separate columns to a functional test.

It is pointed out the wordings "row" and "column" as specified above are applied in order to distinguish different groups or, respectively, different extension directions of groups of component carriers of the component carrier assemblage. A row and a column of component carriers may extend in directions that are perpendicular to each other. Consequently, with respect to the above-mentioned specification,

the wording "row" may be replaced by "column", and the wording "column" may be replaced by "row".

5 In a further embodiment of the component carrier assemblage, each component carrier comprises a component region for arranging optoelectronic semiconductor components. The first and second contact structure of each component carrier enclose the component region. It is for example possible that the component regions of the component carriers have a circular outline.

10 The aforesaid embodiment may for example be considered in order to provide an effective heat dissipation when operating the optoelectronic semiconductor components to generate a light radiation. In this respect, it may be provided that each component carrier of the component carrier assemblage is configured as a so-called metal core board (MCB). In such a configuration, the component carriers comprise a metal layer, for example a copper layer. The above-mentioned component region of each component carrier may be coupled or, respectively, be a part of the metal layer so that optoelectronic semiconductor components or, respectively, chips arranged on the component region may directly dissipate heat.

25 In a further embodiment of the component carrier assemblage, each component carrier comprises a covering layer which partially covers the first and second contact structure of the respective component carrier. In this way, a corrosion or, respectively, oxidization of the first and second contact structures of the component carriers may be largely suppressed. The covering layer may comprise an insulating material such as silicone. The covering layer may furthermore comprise a closed circumferential shape, and may surround the above-mentioned component region.

35 Due to the covering layer partially covering the first and second contact structure of each component carrier, the first and second contact structure of each component carrier may

comprise uncovered regions. The uncovered regions may provide different functional areas of the contact structures.

A possible example is a contact region to which optoelec-
5 tronic semiconductor components may be electrically con-
nected. Each carrier may be provided with two such contact
regions, i.e. belonging to the first and to the second con-
tact structure. For the case that each carrier comprises a
component region having a circular outline, two substantially
10 semi-circular contact regions may be provided which enclose
the respective component region. In this way, optoelectronic
semiconductor chips may be arranged on the component region
and electrically connected to the contact regions by means of
bond wires. The circular configuration makes it possible to
15 arrange semiconductor chips close to the contact regions,
thus facilitating the wire bonding process.

Another example for an uncovered region is a contact pad of a
component carrier by means of which the respective first or
20 second contact structure may be electrically contacted. In
this respect, each carrier may be provided with two such con-
tact pads, i.e. belonging to the first and to the second con-
tact structure. By means of the two contact pads, optoelec-
tronic devices produced from the component carrier assemblage
25 may be contacted.

Further examples for the uncovered regions are a symbol iden-
tifying a contact pad of a component carrier, an area which
may be contacted for a temperature measurement, and/or an
30 alignment mark. Carrying out a temperature measurement may be
considered with respect to a completed optoelectronic device.
Alignment marks may be used in order to facilitate an accu-
rate formation of an encapsulation for optoelectronic semi-
conductor components arranged on a component carrier. In this
35 respect, an enclosing frame structure may be provided, and
the area enclosed by the frame structure may be filled up
with an encapsulation or, respectively, embedding material.

The component carrier assemblage may comprise further features. It is for example possible that the component carrier assemblage comprises recesses in areas between the individual component carriers which substantially enclose the carriers.

5 In this way, singularizing the component carrier assemblage may be facilitated. The recesses may be interrupted in areas of the above-mentioned conductor tracks.

10 A further aspect of the invention relates to a method of producing optoelectronic devices. In the method, a component carrier assemblage is provided. The component carrier assemblage is configured as described above or, respectively, according to one or several of the above-mentioned embodiments. The method further comprises arranging optoelectronic semiconductor components on the component carriers. This may include electrically connecting optoelectronic semiconductor components of the respective component carriers to the first and second contact structures of the same. Optoelectronic semiconductor components may also be electrically connected to one another. The method further comprises conducting a functional test. In the functional test, the first and the second universal contact of the component carrier assemblage are contacted and connected to a power supply. For the case that the component carrier assemblage comprises several first and several second universal contacts, any one of the first and any one of the second universal contacts may be used or, respectively, contacted. The method further comprises providing an encapsulation on the component carriers in order to encapsulate the arranged optoelectronic semiconductor components, and singularizing the component carrier assemblage in order to provide separate optoelectronic devices. Each of the separated optoelectronic devices may comprise a respective component carrier comprising encapsulated optoelectronic semiconductor components or, respectively, chips.

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The configuration of the carrier assemblage comprising the first and second universal contact, the first and second universal contact being electrically connected to the first and

second contact structures of the component carriers, provides several advantages with respect to the functional test. The functional test may be carried out relatively fast. The problem that a probe card applied in the test damages an active unit (i.e. a carrier equipped with optoelectronic semiconductor components) may be prevented. Furthermore, a simple universal probe card may be used in the functional test.

It is pointed out that features and details described above with respect to the component carrier assemblage or its diverse embodiments may also apply to the method of producing optoelectronic devices. This is also the case for other features and details described above, for example concerning the optoelectronic semiconductor components (which may for example be LED chips such as sapphire chips), the electrical connection of the same (for example by means of bond wires), or processes carried out in the fabrication method.

The configurations and features which are described above and/or which are disclosed in the dependent claims may be realized individually or in any combination, except for e.g. cases of clear dependencies or contradicting alternatives.

The accompanying schematic drawings are included in order to provide a further understanding of the present invention and are incorporated into and constitute a part of this specification. The drawings illustrate embodiments of the present invention and together with the description serve to explain principles of the invention. Other embodiments of the present invention and many of the intended advantages of the present invention will be readily appreciated as they will be better understood by reference to the following detailed description.

Figure 1 shows a top view of a component carrier assemblage comprising a number of connected component carriers.

Figure 2 shows a similar top view of the component carrier assemblage, wherein a covering layer of the component carriers is omitted.

5 Figure 3 shows a top view of a single component carrier.

Figure 4 shows a similar top view of the component carrier, wherein a covering layer of the same is omitted.

10 Figure 5 shows a section of the component carrier assemblage in a top view indicating an electrical connection of contact structures of adjacent component carriers by means of conductor tracks.

15 Figure 6 shows a similar section indicating the electrical connection of contact structures of adjacent component carriers, wherein a covering layer of the component carriers is omitted.

20 Figure 7 shows a three-dimensional view of a section of the component carrier assemblage, further indicating the electrical connection of contact structures of adjacent component carriers.

25 Figure 8 shows a similar three-dimensional view of the section of the component carrier assemblage, wherein a covering layer of the component carriers is omitted.

30 Figures 9 and 10 show top views of side areas of the component carrier assemblage indicating an arrangement of interconnected universal contacts of the component carrier assemblage.

35 Figures 11 and 12 show similar top views of the side areas of the component carrier assemblage, wherein a covering layer of the component carriers is omitted.

Figure 13 shows a three-dimensional view of a section of the component carrier assemblage indicating the electrical connection between a universal contact and a contact structure of a component carrier by means of a conductor track, wherein a covering layer of the component carrier is omitted.

Figure 14 shows a top view of a component region of a component carrier comprising a plurality of optoelectronic semiconductor chips which are electrically connected to one another and to contact structures of the component carrier by means of bond wires.

Figure 15 shows a top view of a component carrier comprising a frame which encloses a component region of the component carrier, the frame being used for producing an encapsulation.

Figure 16 shows a flow diagram illustrating steps of a method of producing optoelectronic devices.

The following schematic figures serve to describe possible configurations of a component carrier assemblage 100 for optoelectronic semiconductor components 170. It is pointed out that the figures may not be true to scale. In this sense, components and structures shown in the figures may be scaled up or reduced in size in order to provide a better understanding.

The component carrier assemblage 100 may be provided with respect to a method of producing optoelectronic devices for generating light radiation. Such a fabrication method will be described further below. At first, details concerning the configuration and structure of the carrier assemblage 100 and of its parts will be described. The carrier assemblage 100, which is present in the form of a panel and which may also be referred to as MCPCB panel (metal core printed circuit board) or COB panel (chip-on-board), is configured in such a way that a functional test conducted in the framework of the fabrication method may be facilitated.

Figure 1 shows a top view of the component carrier assemblage 100. Figure 2 shows a similar top view of the carrier assemblage 100, wherein covering layers 140 being arranged on the carrier assemblage 100 are omitted for illustrative purposes. The carrier assemblage 100 comprises a number of connected component carriers 105 which are arranged in a plane next to one another. In the fabrication method, the carrier assemblage 100 is singularized into the individual carriers 105 or, respectively, optoelectronic devices comprising the carriers 105.

As shown in Figures 1 and 2, the illustrated component carrier assemblage 100 comprises sixteen component carriers 105. The connected carriers 105 are arranged in four rows 211, 212, 213, 214 and four columns 201, 202, 203, 204. Each carrier 105 has a rectangular or, respectively, square outline and comprises a respective component region 107 at a front side having a circular outline for arranging optoelectronic semiconductor components 170 (cf. Figures 3 and 14). The optoelectronic semiconductor components 170 are configured to generate a light radiation when supplied with electrical energy. As will be described further below, the optoelectronic semiconductor components 170 to be arranged on the carriers 105 may be unpackaged optoelectronic semiconductor chips 170.

Each component carrier 105 comprises two separate metallic contact structures 110, 120 in the area of the front side, as shown in Figure 2, to which the optoelectronic semiconductor components 170 may be electrically connected. Moreover, each carrier 105 comprises a respective covering layer 140 at the front side. The covering layer 140 of each carrier 105 partially covers the two contact structures 110, 120, so that the contact structures 110, 120 comprise uncovered regions. This aspect becomes apparent by comparing Figure 1 with Figure 2. The uncovered regions provide or, respectively, serve as different functional areas of the two contact structures 110, 120.

In the following, further details concerning a single component carrier 105 of the component carrier assemblage 100 are described with respect to the top views of Figures 3 and 4.

5 This description may substantially apply to all carriers 105 of the assemblage 100. Similar to Figures 1 and 2, Figure 3 shows a component carrier 105 with its covering layer 140, wherein Figure 4 shows the respective carrier 105 without the covering layer 140. In Figure 3, the shapes of the partially
10 covered contact structures 110, 120 are indicated by means of dashed lines. This also applies to conductor tracks 131, 132 depicted in Figures 3, 4, which are also partially covered by the covering layer 140. By means of the conductor tracks 131, 132, contact structures 110, 120 of adjacent carriers 105 of
15 the columns 201, 202, 203, 204 are electrically interconnected, as will be described in more detail further below.

As shown in Figure 4, the two contact structures 110, 120 of the illustrated component carrier 105 substantially have the
20 same shape and enclose the circular component region 107 of the carrier 105. The contact structures 110, 120 are arranged in a common plane (cf. also Figure 8). Each contact structure 110, 120 comprises a partial area having substantially the form of a part of a circular ring, and a wider partial area
25 extending towards a corner of the component carrier 105. At this, the two contact structures 110, 120 extend to two diagonally opposite corners of the carrier 105.

In the following, the two contact structures 110, 120 are also referred to as first contact structure 110 and second contact structure 120. The first contact structure 110 may be
30 provided for a connection with a positive pole, and the second contact structure may be provided for a connection with a negative pole of a DC power supply. The two contact structures 110, 120 comprise a suitable metallic material such as
35 copper.

As shown in Figure 3, the covering layer 140 of the component carrier 105 has a closed circumferential shape and surrounds the component region 107. The covering layer 140 comprises respective openings, the openings exposing partial regions of the two contact structures 110, 120. The covering layer 140 comprises an insulating material such as silicone. The silicone material may have a white colour, which may be realized by including TiO_2 particles in the silicone material. By means of the covering layer 140, a corrosion or, respectively, oxidization of the covered parts of the contact structures 110, 120 may be prevented.

Concerning the uncovered regions, two pentagonal openings are provided in the covering layer 140 in the area of the above-mentioned corner areas of the two contact structures 110, 120, so that each contact structure 110, 120 comprises a respective uncovered region 111, 121, as shown in Figure 3. The uncovered regions 111, 121 serve as contact pads 111, 121 of the component carrier 105. The pentagonal contact pads 111, 121 are arranged at diagonally opposite corners of the carrier 105. By means of the contact pads 111, 121, the contact structures 110, 120 of the carrier 105 and thus an optoelectronic device being produced from the carrier assemblage 100 and comprising the carrier 105 may be electrically contacted. In accordance with the first and second contact structure 110, 120, the contact pad 111 of the first contact structure 110 is also referred to as first contact pad 111, and the contact pad 121 of the second contact structure 120 is also referred to as second contact pad 121 in the following.

The other diagonally opposite corners of the component carrier 105 are provided with holes 150 extending through the carrier 105 from the front side to an opposite back side. The two holes 150 may be used to receive screws. In this way, the component carrier 105 and thus an optoelectronic device comprising the carrier 105 may be attached to a further carrier device. It is furthermore possible to attach further components to the carrier 105 (not depicted).

As further illustrated in Figure 3, the two contact structures 110, 120 additionally comprise inner uncovered regions 112, 122 which are adjacent to the component region 107 or, respectively, directly enclose the component region 107. The uncovered regions 112, 122 have a substantially semi-circular outline. These regions 112, 122 serve as contact regions 112, 122 of the two contact structures 110, 120 to which optoelectronic semiconductor components 170 may be electrically connected by means of bond wires 171 (cf. Figure 14). In accordance with the first and second contact structure 110, 120, the contact region 112 of the first contact structure 110 is also referred to as first contact region 112, and the contact region 122 of the second contact structure 120 is also referred to as second contact region 122 in the following.

Figure 3 further illustrates line-shaped openings of the covering layer 140 at which the two contact structures 110, 120 are uncovered, so that alignment marks 114, 115, 124 are provided. With respect to the line-shaped alignment marks 114, 124, the contact structures 110, 120 comprise respective outwardly projecting partial areas, as shown in Figure 4. The other alignment mark 115 is provided in the area of the corner area of the first contact structure 110. The alignment marks 114, 115, 124 are arranged on a circle surrounding the component region 107 in a distance to the two contact regions 112, 122. The alignment marks 114, 115, 124 are used with respect to the formation of an encapsulation carried out in the method of producing optoelectronic devices.

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As shown in Figure 3, the covering layer 140 comprises a further opening in the area of the corner area of the first contact structure 110, so that a dot-like uncovered region 119 is provided. This region 119 may be contacted in order to measure the temperature of the component carrier 105 or, respectively, an optoelectronic device comprising the carrier 105.

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The covering layer 140 comprises a further opening in the area of the corner area of the first contact structure 110, so that a cross-shaped uncovered region 117 is provided, as shown in Figure 3. This region 117 serves as a symbol or, respectively, "+"-symbol identifying the contact pad 111. As described above, the first contact structure 110 may be provided for a connection with a positive pole, and the second contact structure 120 may be provided for a connection with a negative pole of a DC power supply. Consequently, the first contact pad 111 may also be referred to as positive pad, +ve pad or p-pad 111. The second contact pad 121 may also be referred to as negative pad, -ve pad or n-pad 121. In this regard, the region 117 identifies the respective polarity of the first contact structure 110 and thus of the associated first contact pad 111.

The component carrier 105 may for example be a so-called metal core board (MCB). In this respect, the component carrier 105 may comprise a metal layer, for example comprising copper, which serves as a heat sink and provides an enhanced heat dissipation when operating optoelectronic semiconductor components 170 to generate a light radiation (not depicted). The component region 107 may be thermally coupled or, respectively, be part of the metal layer so that semiconductor components 170 arranged on the component region 107 may effectively dissipate heat. The metal layer may be partially surrounded by an insulating material, e.g. an epoxy laminate material usually used for MCPCBs.

The component carrier arrangement 100 shown in Figures 1, 2 and comprising a number of such connected component carriers 105 is provided with recesses 151 on the front side. The front-side recesses 151 substantially enclose the individual component carriers 105. Recesses 152 are also provided on the opposite back side of the carrier assemblage 100 (cf. Figures 7 and 8). The recesses 151, 152 are provided to facilitate a singularization process carried out in the fabrication method in order to divide the processed component carrier assemblage

100 into separate optoelectronic devices, each optoelectronic device comprising a respective component carrier 105.

The component carrier assemblage 100 shown in Figures 1, 2
5 further comprises four isolated universal contacts 101 and four isolated universal contacts 102 at the front side. The universal contacts 101 are arranged in the area of an edge side of the component carrier assemblage 100, and the other
10 universal contacts 102 are arranged in the area of an opposite edge side of the assemblage 100. The component carrier assemblage 100 comprises respective side sections 161, 162 on which the universal contacts 101, 102 are arranged. The universal contacts 101, 102 are furthermore arranged adjacent to
15 component carriers 105 being located at the ends of the columns 201, 202, 203, 204. In this way, each column 201, 202, 203, 204 comprises a respective universal contact 101 and a respective universal contact 102.

Each universal contact 101 is electrically connected to the
20 first contact structures 110 of all component carriers 105. The universal contacts 101, which are provided in the form of rectangular contact pads (cf. Figure 10), are therefore referred to as first universal contacts 101 in the following.
In accordance with the positive contact pads 111 of the individual carriers 105, the first universal contacts 101 may
25 also be referred to as positive universal contact pads 101.

Each universal contact 102 is electrically connected to the second contact structures 120 of all component carriers 105.
30 The universal contacts 102, which are provided in the form of rectangular contact pads, as well (cf. Figure 9), are therefore referred to as second universal contacts 102 in the following. In accordance with the negative contact pads 121 of the individual carriers 105, the second universal contacts
35 102 may also be referred to as negative universal contact pads 102.

The configuration of the component carrier assemblage 100 comprising the universal contacts 101, 102 makes it possible to apply respective electrical potentials to all first contact structures 110 and to all second contact structures 120 of the component carriers 105 at the same time. For this purpose, any one of the first universal contacts 101 and any one of the second universal contacts 102 may be used or, respectively, contacted. In this way, several advantages are provided with respect to a functional test carried out in the framework of the method of producing optoelectronic devices, as will be described in more detail further below. At this point, details regarding the electrical connection between the universal contacts 101, 102 and the contact structures 110, 120 of the component carriers 105 are explained.

A part of the electrical connection between the first universal contacts 101 and the first contact structures 110 and between the second universal contacts 102 and the second contact structures 120 is realized by means of an electrical connection or, respectively, interconnection of the first and second contact structures 110, 120 of the component carriers 105. In this respect, in each column 201, 202, 203, 204, the first contact structures 110 of adjacent component carriers 105 are electrically connected to each other by means of conductor tracks 131. Similarly, the second contact structures 120 of adjacent component carriers 105 in each column 201, 202, 203, 204 are electrically connected to each other by means of conductor tracks 132. This can be seen from Figures 1 to 4, and is shown in more detail in the section views of Figures 5, 6 and the three-dimensional views of Figures 7, 8. Similar to the preceding figures, Figures 5, 7 depict the covering layers 140 of the component carriers 105, wherein in Figures 6, 8, the covering layers 140 are omitted.

By means of a conductor track 131, the first contact structures 110 of two adjacent carriers 105 are directly electrically connected to each other. The conductor track 131 extends in an area between the connected contact structures

110. By means of a conductor track 132, the second contact structures 120 of two adjacent carriers 105 are directly electrically connected to each other. The conductor track 132 extends in an area between the connected contact structures 120. This configuration applies to all adjacent carriers 105 of the respective columns 201, 202, 203, 204.

The conductor tracks 131, 132 which are arranged in the area of the front side of the component carrier assemblage 100 are relatively thin conductive traces and comprise straight and curved line-shaped sections. Due to the thin and line-shaped configuration, the above-mentioned singularization process may be facilitated, as well. The conductor tracks 131, 132 are partially covered by the covering layers 140 of the component carriers 105 (cf. Figures 5, 7). Furthermore, the front-side recesses 151 are interrupted in the area of the conductor tracks 131, 132 (cf. Figures 6, 8).

The Figures 9 to 12 show section views of opposite sides of the component carrier assemblage 100 in the area of which the first and second universal contacts 101, 102 are located on side sections 161, 162, thus illustrating further details of the electrical connection between the first and second universal contacts 101, 102 and the first and second contact structures 110, 120 of the component carriers 105. Similar to the preceding figures, Figures 9, 10 depict the covering layers 140 of the component carriers 105, wherein in the Figures 11, 12, the covering layers 140 are omitted.

In each column 201, 202, 203, 204, a first universal contact 101 is directly electrically connected to a first contact structure 110 of an adjacent component carrier 105 by means of a conductor track 133, the respective carrier 105 being located at a column end (cf. Figures 10, 12). Similarly, in each column 201, 202, 204, 204, a second universal contact 102 is directly electrically connected to a second contact structure 120 of an adjacent component carrier 105 by means of a conductor track 134, the respective carrier 105 being

located at an opposite column end (cf. Figures 9, 11). Comparable to the conductor tracks 131, 132 by means of which the interconnection of the contact structures 110, 120 is provided, the conductor tracks 133, 134 are relatively thin line-shaped traces, thus promoting the singularization process.

The conductor tracks 133 comprise straight and curved sections, as can be seen from Figure 12 and the additional three-dimensional illustration of Figure 13 in which the covering layer 140 of the depicted component carrier 105 is omitted. The other conductor tracks 134 are solely straight-line, as shown in Figure 11. The conductor tracks 133, 134 which are arranged in the area of the front side of the carrier assemblage 100 are also partially covered by the covering layers 140 of the component carriers 105. Furthermore, the front-side recesses 151 are interrupted in the area of the conductor tracks 133, 134.

As further shown in Figures 9 to 12, the first and second universal contacts 101, 102 located in the area of opposite edges of the component carrier assemblage 100 are furthermore electrically connected to each other by means of conductor tracks 135, 136. The conductor tracks 135, 136 which are arranged at the front side of the carrier assemblage 100 are thin straight-line conductive traces. The conductor tracks 135, 136 are arranged on the side sections 161, 162 of the carrier assemblage 100 and extend between the universal contacts 101, 102. By means of each conductor track 135, two first universal contacts 101 are directly electrically connected to each other. By means of each conductor track 136, two second universal contacts 102 are directly electrically connected to each other.

The conductor tracks 131, 132, 133, 134, 135, 136 provide a simple electrical connection between all first universal contacts 101 and all first contact structures 110 of the component carriers 105, and between all second universal contacts

102 and all second contact structures 120 of the component carriers 105 of the carrier assemblage 100. In this way, several advantages are made possible with respect to a light up or, respectively, functional test. Details of this and further details will be described in the following with respect to a possible method of producing optoelectronic devices, in which the carrier assemblage 100 may be applied.

Figure 16 shows a flow diagram illustrating steps of the fabrication method. In a first step 301, initial components such as the component carrier assemblage 100 comprising the connected carriers 105 and a plurality of optoelectronic semiconductor components 170 to be mounted on the carrier assemblage 100 are provided. The optoelectronic semiconductor components 170, which are schematically shown in Figure 14, are unpackaged optoelectronic semiconductor chips 170, in particular LED chips (light emitting diode) such as for example sapphire chips. Each semiconductor chip 170 comprises two front-side contacts to which bond wires 171 may be connected. It is the front side or, respectively, a part of the front side of a semiconductor chip 170 by means of which a light radiation generated when operating the chip 170 is substantially emitted. The semiconductor chips 170 may be manufactured in a known manner and may comprise components such as a semiconductor layer sequence with an active zone for generating light radiation, a conversion layer for converting the radiation as the case may be, etc.

A further step 302 of the fabrication method (cf. Figure 16) comprises arranging the optoelectronic semiconductor chips 170 on the component regions 107 of the component carriers 105 and electrically connecting the chips 170 to one another and to the first and second contact structures 110, 120 of the component carriers 105 by means of bond wires 171. For this purpose, the semiconductor chips 170 or, respectively, back sides of the same being opposite to the front sides, are attached on the component regions 107 of the carriers 105 for

example by means of an adhesive. Subsequently, a wire bonding process is carried out.

Figure 14 illustrates a possible arrangement and electrical connection of semiconductor chips 170 with respect to a single component carrier 105 or, respectively, a component region 107 of the same. The depicted configuration may be provided for all component carriers 105 of the carrier assemblage 100. As shown in Figure 14, several (i.e. five) strings of semiconductor chips 170 electrically connected in series by means of bond wires 171 are provided. Semiconductor chips 170 at the ends of the strings are connected to the first and second contact regions 112, 122 of the contact structures 110, 120 by means of bond wires 171, as well. The strings are connected in parallel via the contact structures 110, 120. The circular configuration of the component region 107 and of the enclosing contact regions 112, 122 makes it possible to arrange semiconductor chips 170 close to the contact regions 112, 122, thus facilitating the wire bonding process.

In a further step 303 (cf. Figure 16), a functional test is conducted in order to test the functionality of the component carriers 105 being equipped with the semiconductor chips 170. For this purpose, any one of the first common contacts 101 and any one of the second common contacts 102 of the component carrier assemblage 100 may be contacted, and a low voltage or, respectively, current may be applied to the contacted universal contacts 101, 102. In this way, electrical power may be supplied to the first and second contact structures 110, 120 of all carriers 105 at the same time, which may therefore be jointly tested.

In the functional test, a simple probe card comprising two pins may be applied in order to contact the respective universal contacts 101, 102 of the carrier assemblage 100 and to provide an electrical connection to a DC power supply (not depicted). Thus, active units comprised of component carriers 105 and semiconductor chips 170 which have a proper configu-

ration and electrical connection or, respectively, semiconductor chips 170 of the same, may light up. The jointly tested units 105, 170 may be manually inspected or by means of a VI machine (visual inspection). Defective units 105, 170 may be recognized, and may be subjected to a rework process. This may be repeated, if necessary, several times. These processes are carried out in the framework of the step 303.

Instead of testing component carriers one after another, as in the case of a conventional component carrier assemblage, the configuration of the component carrier assemblage 100 makes it possible to test all component carriers 105 or, respectively, active units 105, 170 at the same time. Consequently, a functional test may be carried out in a small period of time. It is furthermore possible to test several carrier assemblages 100 being equipped with semiconductor chips 170 with a high throughput. Moreover, as described above, the functional test may be conducted by using any one of the first universal contacts 101 and any one of the second universal contacts 102. This allows for a high test flexibility.

Another advantage is that the universal contacts 101, 102 which are arranged in the area of opposite edge sides of the carrier assemblage 100 are located relatively far away from the carriers 105 or, respectively, the component regions 107 comprising the wire-bonded semiconductor chips 170. This holds true in comparison to the first and second contact pads 111, 121 of the individual carriers 105 which are located closer to the component regions 107. Consequently, a functional test may be carried out with a high reliability and without the problem that the applied probe card or, respectively, pins of the same damage the active units 105, 170. The large distance and the usage of a simple probe card having two probe pins may also simplify a visual inspection.

Afterwards, further processes are carried out which are summarized in a step 304 of the flow diagram of Figure 16. This includes the provision of an encapsulation on the component

carriers 105 in the area of the component regions 107 in order to encapsulate the semiconductor chips 170. For this purpose, ring-shaped frames 180 enclosing the component regions 170 are arranged on the carriers 105 of the carrier assemblage 100, as shown in Figure 15 for a single component carrier 105. At this, the alignment marks 114, 115, 124 may be used for a precise arrangement of the frames 180. The frames 180 may for example comprise silicone. Subsequently, in each case the area enclosed by a frame 180 is filled up with an embedding material, for example a silicone material (not depicted).

The step 304 (cf. Figure 16) furthermore includes singularizing the processed component carrier assemblage 100 into separate optoelectronic devices (not depicted). In this process, the component carrier assemblage 100 is divided or, respectively, cut or sawn in the area of the recesses 151, 152, and therefore also in the area of the conductor tracks 131, 132, 133, 134. Side sections, including the side sections 161, 162 with the universal contacts 101, 102, are also separated from the component carriers 105.

Each of the optoelectronic devices produced in this way comprises a respective component carrier 105 carrying encapsulated optoelectronic semiconductor chips 170 in the area of the component region 107. The holes 150 extending through the carrier 105 of a device may be used to receive screws. In this way, other components (e.g. a housing part) may be fixed to the carrier 105, and the optoelectronic device may be fixed to a further carrier device. By means of the two contact pads 111, 121, the optoelectronic device may be electrically contacted.

The configuration of the component carrier assemblage 100 with the universal contacts 101, 102 provides further advantages. In the carrier assemblage 100, each column 201, 202, 203, 204 of interconnected component carriers 105 comprises an associated first universal contact 101 and an associated

second universal contact 102. The first and second universal contact 101, 102 are arranged at the two opposite ends of the respective columns 201, 202, 203, 204 and are electrically connected to a first or second contact structure 110, 120 of the respective adjacent component carriers 105 by means of a conductor track 133, 134 (cf. Figures 1, 2). Thus, it may be considered, after providing the encapsulation, to first of all singularize the carrier assemblage 100 into sections, each section comprising a column 201, 202, 203, 204 of carriers 105 and a respective first and second universal contact 101, 102. Due to the presence of a first and second universal contact 101, 102 at each column 201, 202, 203, 204, it is possible to subject the individual columns 201, 202, 203, 204 to a functional test. Afterwards, the column sections may be further separated into individual optoelectronic devices.

A further advantage is that different component carrier assemblages 100 having different designs, for example different sizes of the component carriers 105, may be tested by means of the same probe card. For this purpose, the different component carrier assemblages 100 may be configured in such a way that the positions of the universal contacts 101, 102 are the same. Consequently, a simple universal probe card comprising two pins may be used to conduct a functional test with all the different component carrier assemblages 100. The application of a universal probe card allows to save manufacturing cost, and to simplify the visual inspection.

The component carrier assemblage 100 and the components of the same explained with reference to the figures represent possible embodiments, or embodiments by way of example, of the invention. In addition to the embodiments described and illustrated, further embodiments of a carrier assemblage or, respectively, arrangement which may comprise modifications or combinations of the features described are conceivable.

In this respect, it is pointed out that the above-mentioned materials and numerical data are examples which may be re-

placed by other materials and specifications. As an example, it is possible to provide a component carrier assemblage 100 having a different number of connected carriers 105.

5 This is also the case for the number of universal contacts 101, 102. In this regard, it is for example possible to provide a component carrier assemblage 100 having only one isolated first universal contact 101 and only one isolated second universal contact 102. In a configuration like this, the
10 two universal contacts 101, 102 may be arranged in the area of opposite edge sides of the carrier assemblage 100. Conductor tracks may be provided by means of which the universal contacts 101, 102 may be electrically connected to component carriers 105 located at the respective edge sides of the as-
15 semblage 100.

Variations and/or modifications are also conceivable for the depicted geometries and shapes of structures of the component carrier assemblage 100, for example the contact structures
20 110, 120, the conductor tracks, etc.

It is further pointed out that instead of semiconductor chips 170 comprising two front-side contacts, other semiconductor chips, for example comprising a front-side and a back-side
25 contact or comprising two back-side contacts may be applied. For such semiconductor chips, a component carrier assemblage 100 or, respectively, component carriers 105 of the same may be provided with contact structures 110, 120 having a matched configuration.

30

The contact structures 110, 120 of each carrier 105 may for example comprise contact pads to which back-side contacts of semiconductor chips, the chips having one or two back-side contacts, may be attached by means of a solder material. Arranging semiconductor chips on the carrier 105 may include a
35 soldering or, respectively, reflow soldering process. In this way, the semiconductor chips may be attached on a respective carrier 105 and electrically connected to one another and to

the contact structures 110, 120. For the case that semiconductor chips comprising a front-side and a back-side contact are applied, the contact structures 110, 120 may comprise further contact areas or, respectively, pads. These contact pads may be connected to the front-side contacts of the chips by means of bond wires.

It is further pointed out the wordings "row" and "column" used above are applied in order to distinguish different groups or, respectively, different extension direction of groups of component carriers 105. As shown in Figures 1, 2, a row and a column extend in directions that are perpendicular to each other. Consequently, with respect to the above-mentioned specification, the wording "row" may be replaced by "column", and the wording "column" may be replaced by "row".

It is further pointed out that a functional test in which universal contacts 101, 102 are contacted may also be conducted after providing an encapsulation.

While the invention has been described in detail with reference to specific embodiments thereof, it will be apparent to one of ordinary skill in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof. Accordingly, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Reference Numbers

	100	component carrier assemblage
	101, 102	universal contact
5	105	component carrier
	107	component region
	110	contact structure
	111	contact pad
	112	contact region
10	114, 115	alignment mark
	117	symbol
	119	region
	120	contact structure
	121	contact pad
15	122	contact region
	124	alignment mark
	131, 132	conductor track
	133, 134	conductor track
	135, 136	conductor track
20	140	covering layer
	150	hole
	151, 152	recess
	161, 162	side section
	170	semiconductor chip
25	171	bond wire
	180	frame
	201, 202	column
	203, 204	column
	211, 212	row
30	231, 214	row
	301, 302	method step
	303, 304	method step
	305, 306	method step

Claims

1. A component carrier assemblage (100) for optoelectronic semiconductor components (170), comprising:

5 a number of component carriers (105) for arranging optoelectronic semiconductor components (170), each component carrier (105) comprising a first contact structure (110) and a second contact structure (120) to which optoelectronic semiconductor components (170) may be electrically connected;

10 a first universal contact (101) which is electrically connected to the first contact structures (110) of the number of component carriers (105); and

15 a second universal contact (102) which is electrically connected to the second contact structures (120) of the number of component carriers (105).

- 20 2. The component carrier assemblage according to claim 1, wherein the first contact structures (110) of adjacent component carriers (105) are electrically connected to one another by means of conductor tracks (131), and wherein the second contact structures (120) of adjacent component carriers (105) are electrically connected to one another by means of conductor tracks (132).

- 30 3. The component carrier assemblage according to any one of the preceding claims, wherein the first and second universal contact (101, 102) are arranged in the area of different edge sides of the component carrier assemblage (100).

- 35 4. The component carrier assemblage according to any one of the preceding claims, wherein the first universal contact (101) is electrically connected to the first contact structure (110) of

an adjacent component carrier (105) by means of a conductor track (133), and wherein the second universal contact (102) is electrically connected to the second contact structure (120) of an adjacent component carrier (105) by means of a conductor track (134).

5. The component carrier assemblage according to any one of the preceding claims,

comprising several first and several second universal contacts (101, 102), wherein the first universal contacts (101) are electrically connected to the first contact structures (110) of the number of component carriers (105), and wherein the second universal contacts (102) are electrically connected to the second contact structures (120) of the number of component carriers (105).

6. The component carrier assemblage according to claim 5, wherein the first and second universal contacts (101, 102) are arranged in the area of opposite edge sides of the component carrier assemblage (100), wherein the first universal contacts (101) are electrically connected to one another by means of conductor tracks (135), and wherein the second universal contacts (102) are electrically connected to one another by means of conductor tracks (136).

7. The component carrier assemblage according to claim 6, wherein the component carriers (105) are arranged in rows and columns, wherein in each column (201, 202, 203, 204) the first contact structures (110) of adjacent component carriers (105) and the second contact structures (120) of adjacent component carriers (105) are electrically connected to one another by means of conductor tracks (131, 132), wherein the first universal contacts (101) are electrically connected to the first contact structures (110) of component carriers (105) which are arranged at an end of the columns (201, 202, 203, 204)

by means of conductor tracks (133), and wherein the second universal contacts (102) are electrically connected to the second contact structures (120) of component carriers (105) which are arranged at an opposite end of the columns (201, 202, 203, 204) by means of conductor tracks (134).

8. The component carrier assemblage according to any one of the preceding claims,
wherein each component carrier (105) comprises a component region (107) for arranging optoelectronic semiconductor components (170), the first and second contact structure (110, 120) enclosing the component region (107).

9. The component carrier assemblage according to any one of the preceding claims,
wherein each component carrier (105) comprises a covering layer (140) which partially covers the first and second contact structure (110, 120) of the respective component carrier (105).

10. The component carrier assemblage according to claim 9,
wherein the first and second contact structure (110, 120) of each component carrier (105) comprise uncovered regions providing one of the following:

a contact region (112, 122) to which optoelectronic semiconductor components (170) may be electrically connected;

a contact pad (111, 121) by means of which the respective first or second contact structure (110, 120) may be electrically contacted;

a symbol (117) identifying a contact pad (111);

a region (119) which may be contacted for a temperature

measurement; and

an alignment mark (114, 115, 124).

- 5 11. A method of producing optoelectronic devices, comprising:

providing a component carrier assemblage (100) according to any one of the preceding claims;

10

arranging optoelectronic semiconductor components (170) on the component carriers (105) of the component carrier assemblage (100);

15

conducting a functional test, wherein the first and second universal contact (101, 102) of the component carrier assemblage (100) are connected to a power supply;

20

providing an encapsulation in order to encapsulate the arranged optoelectronic semiconductor components (170); and

singularizing the component carrier assemblage (100) in order to provide separate optoelectronic devices.

25

FIG 1

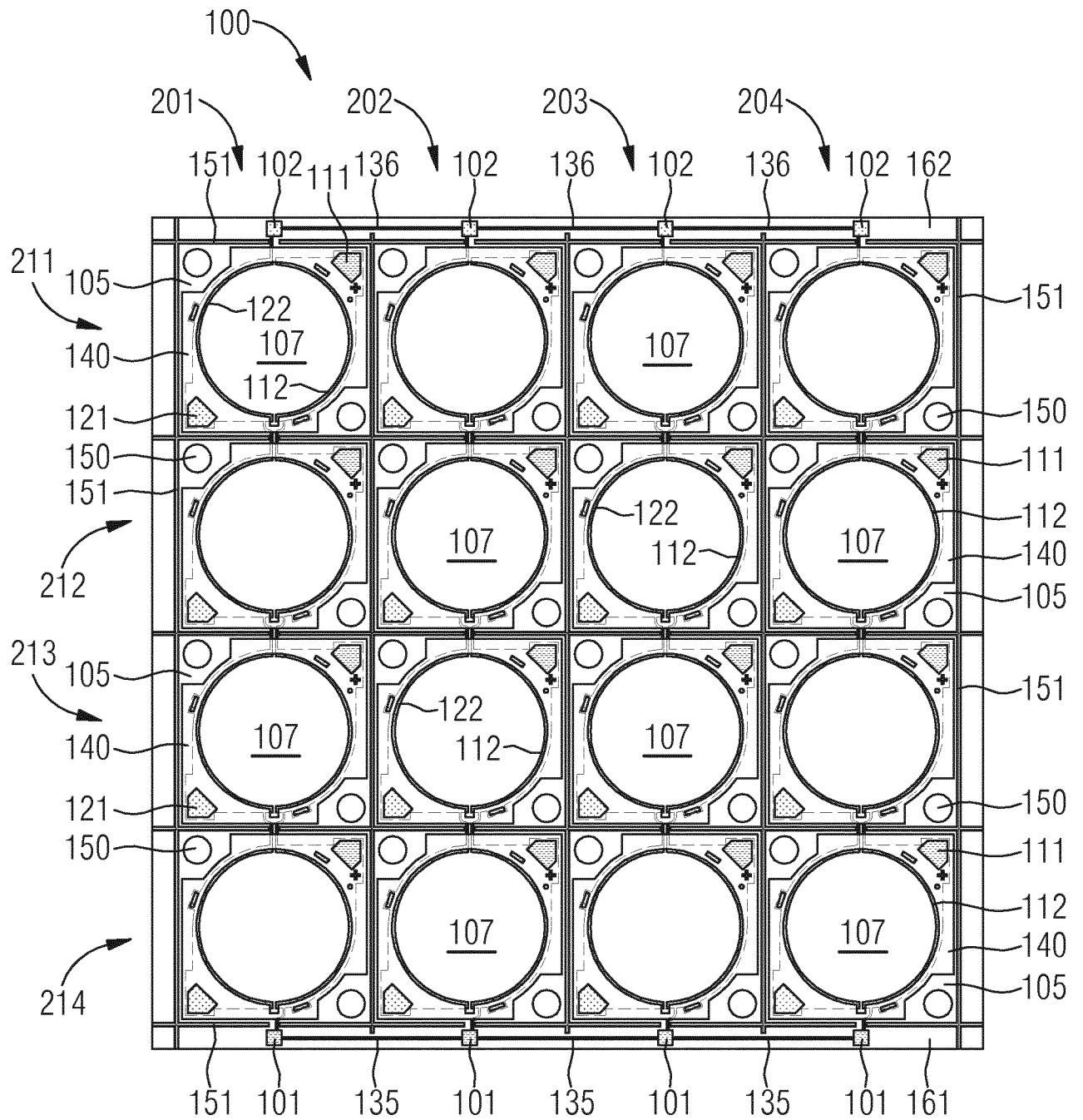


FIG 2

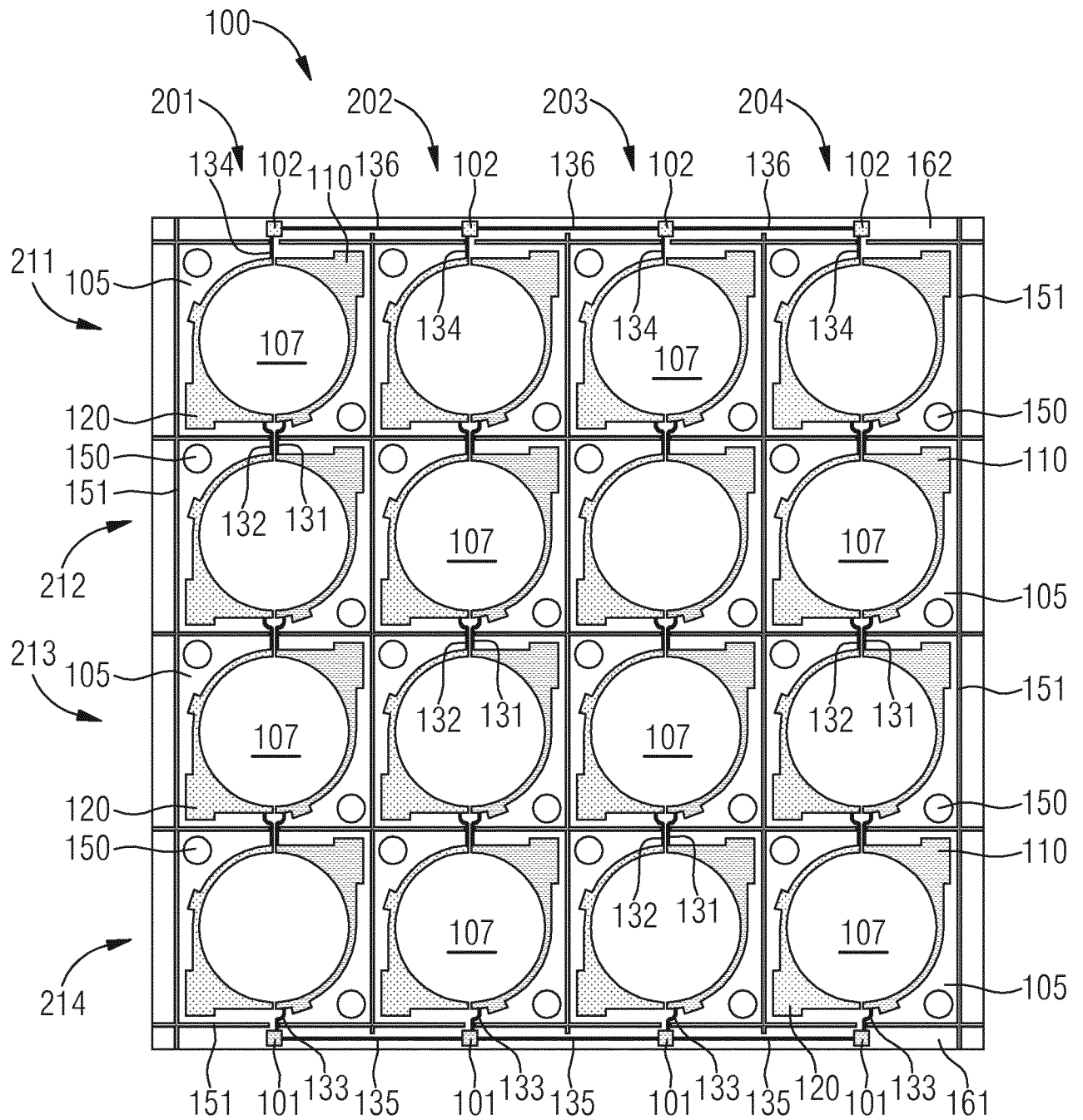


FIG 3

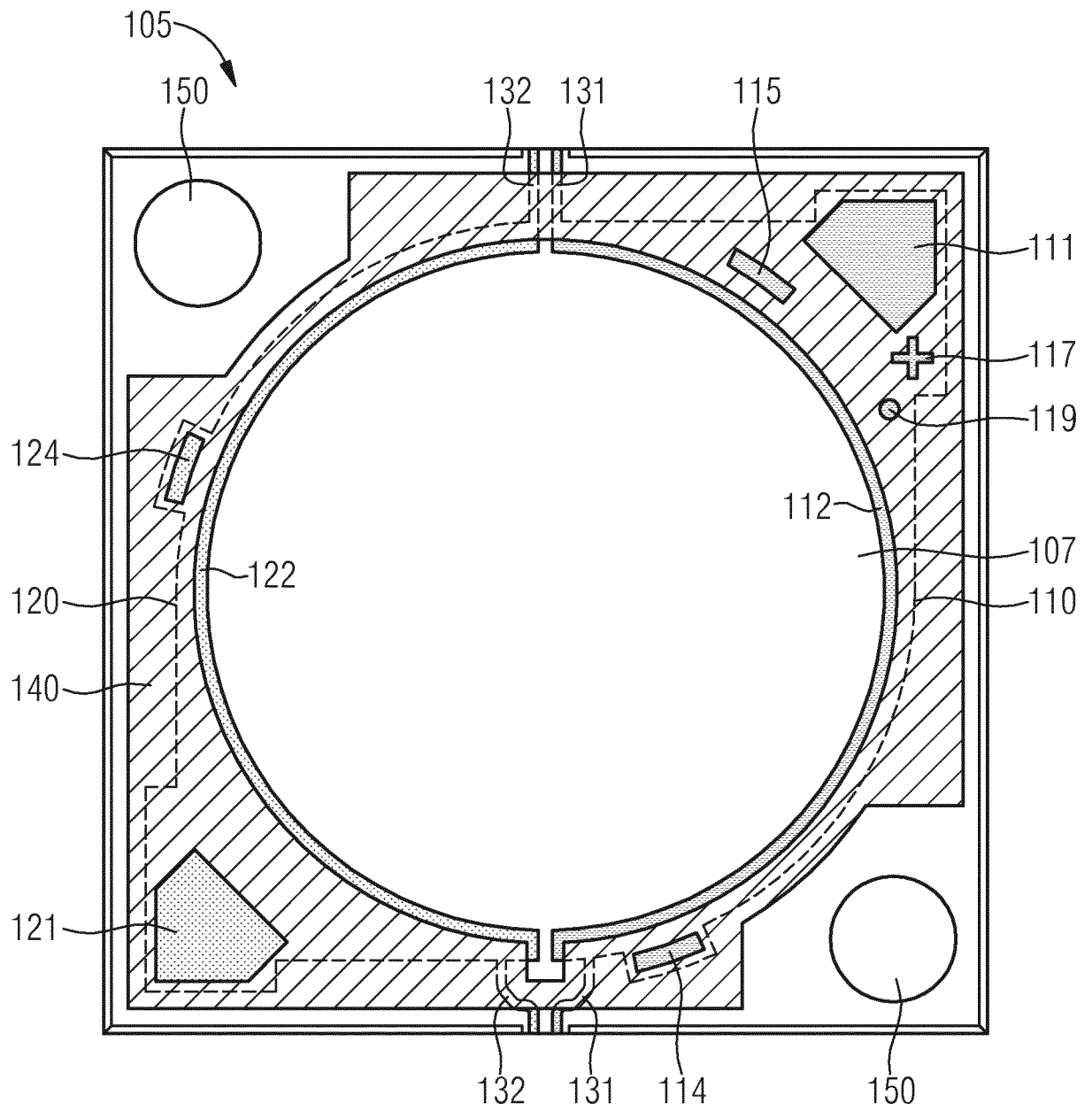


FIG 4

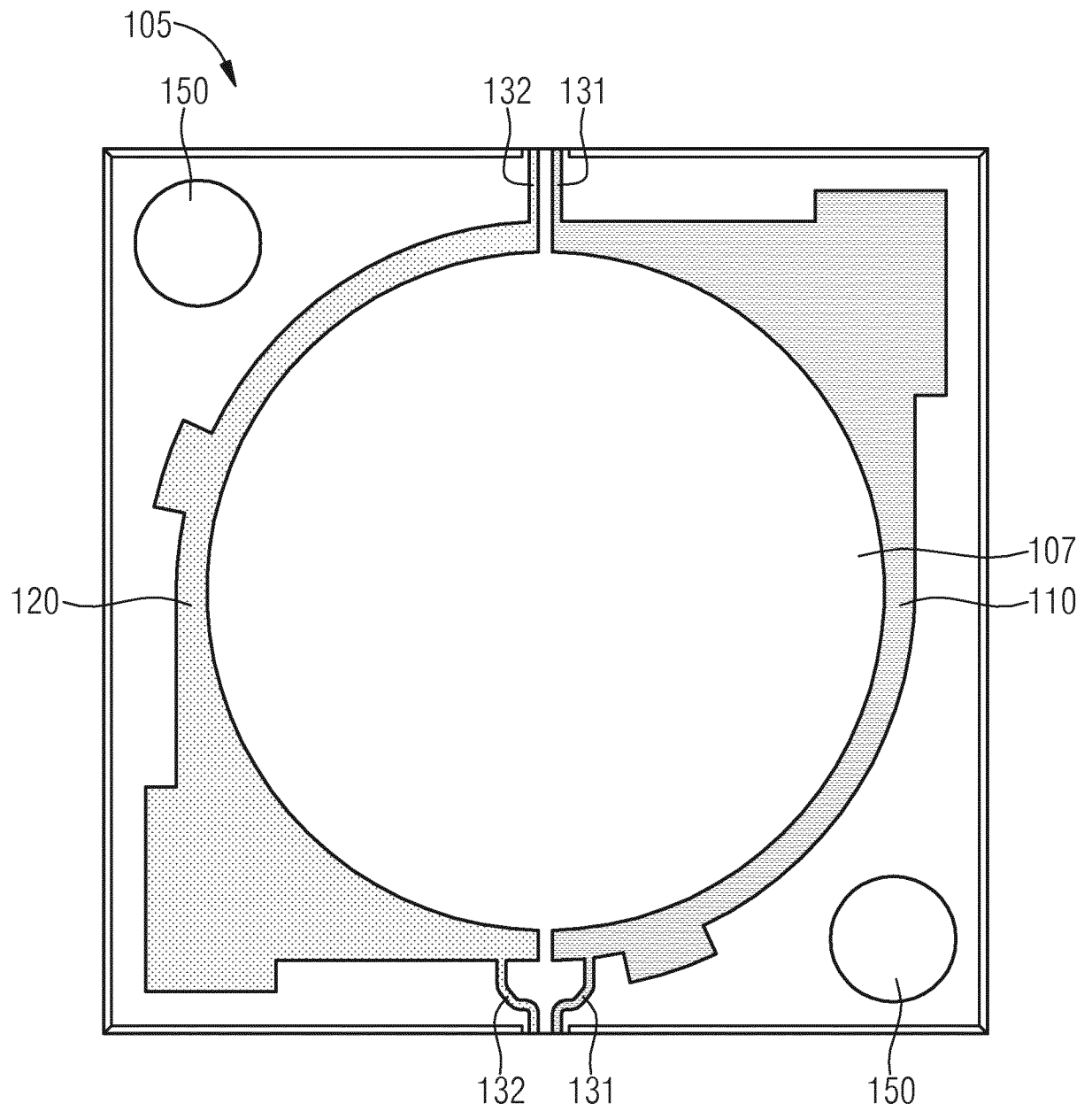


FIG 5

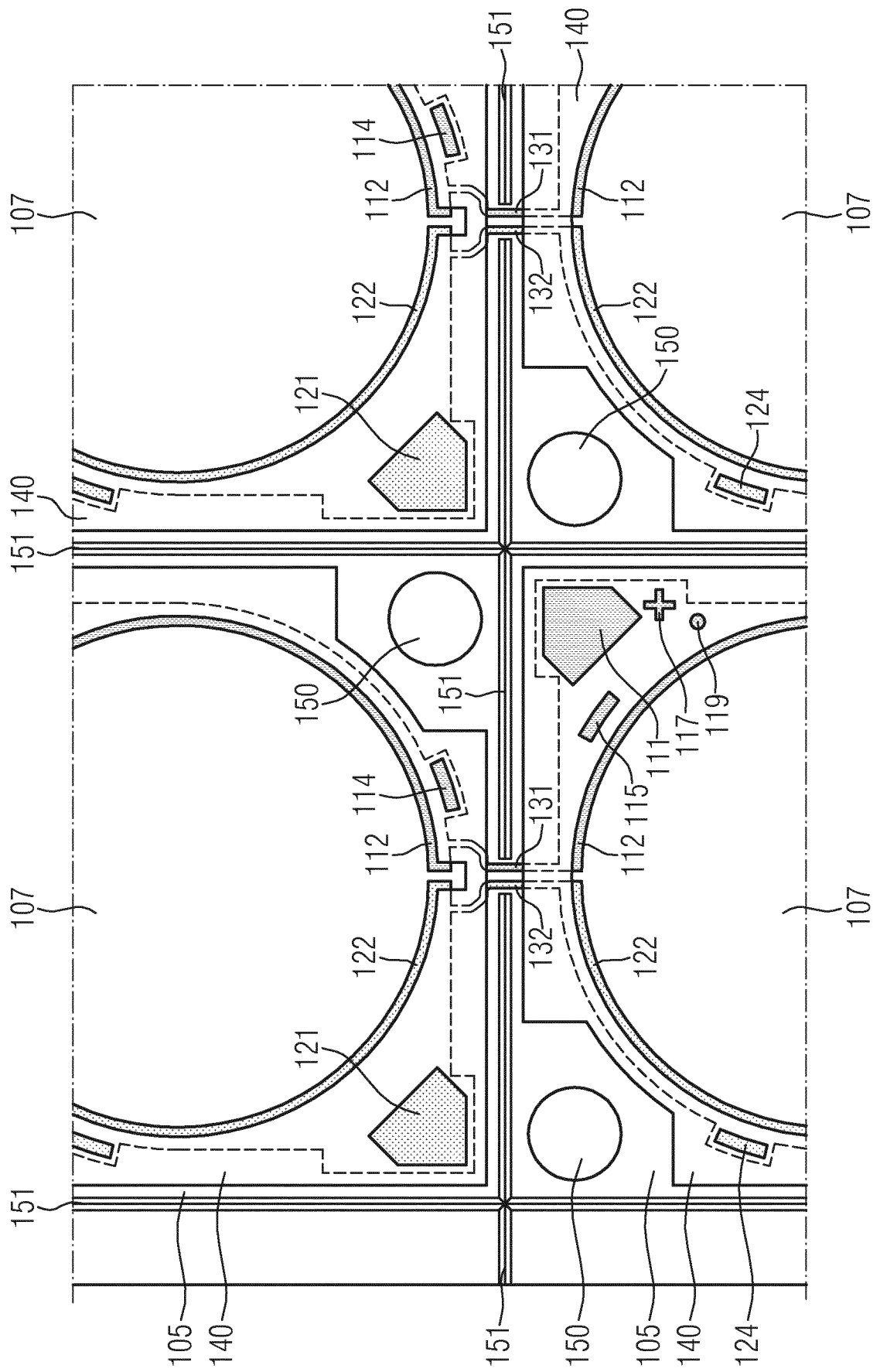


FIG 6

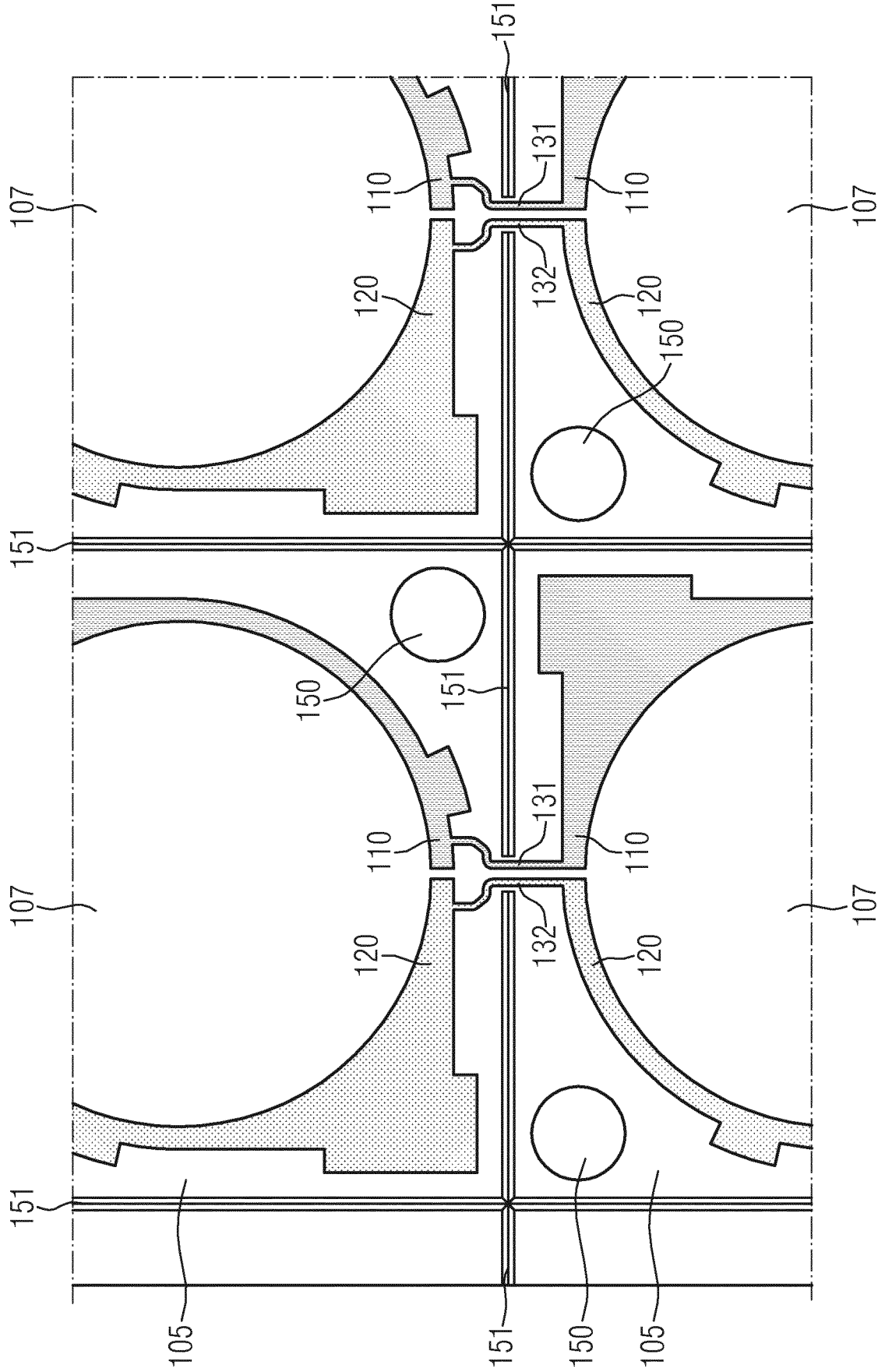


FIG 7

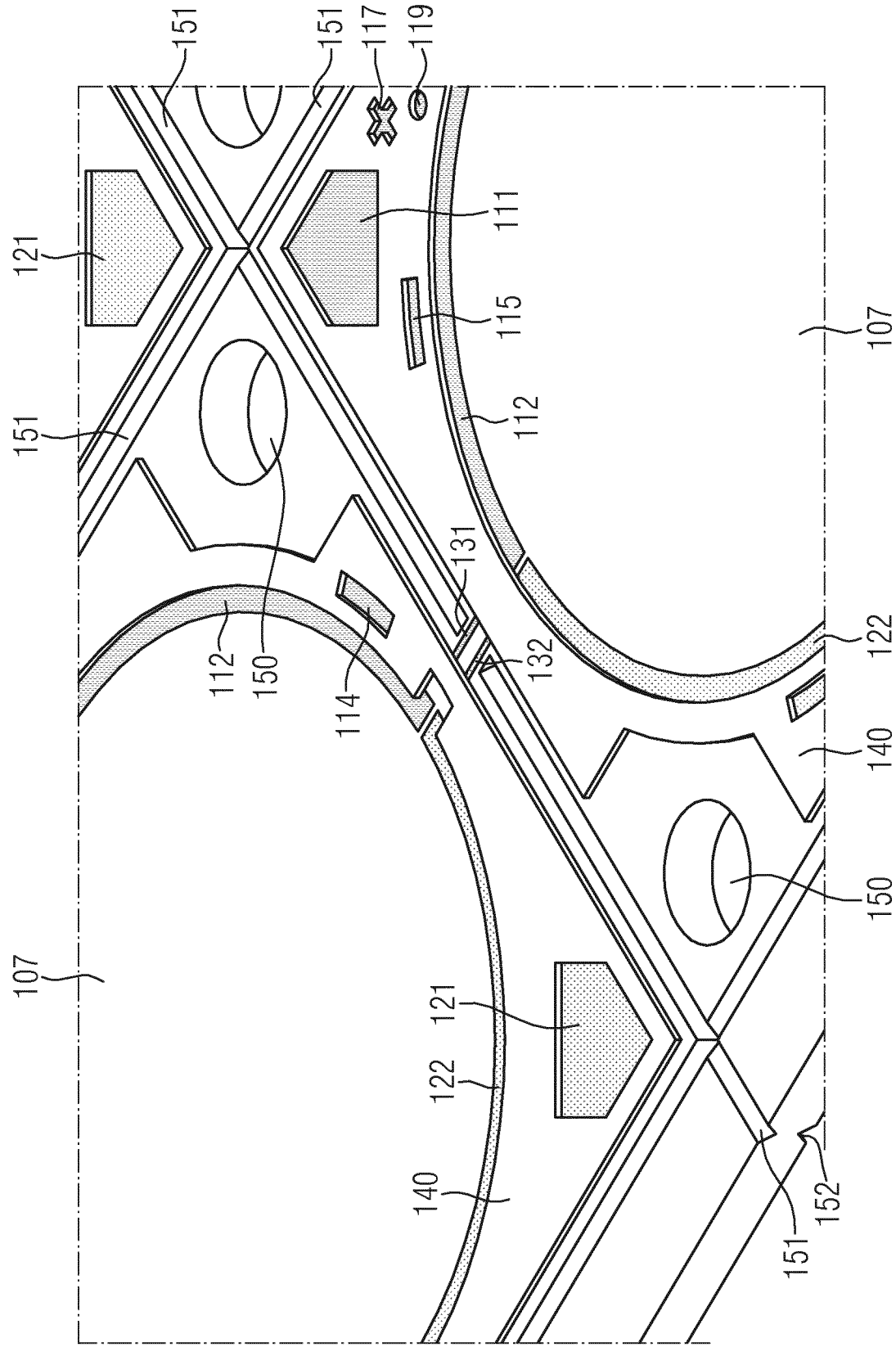


FIG 8

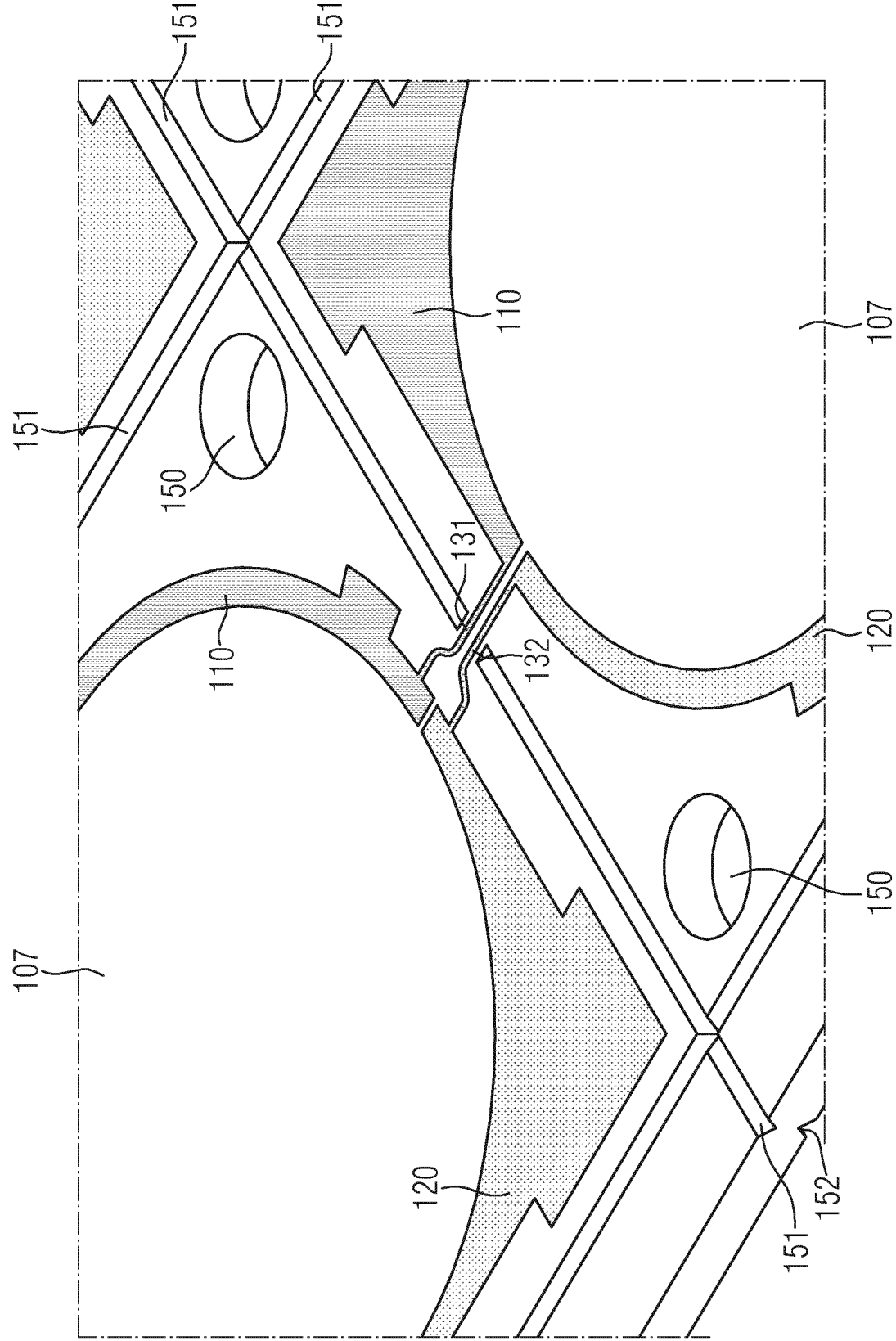


FIG 9

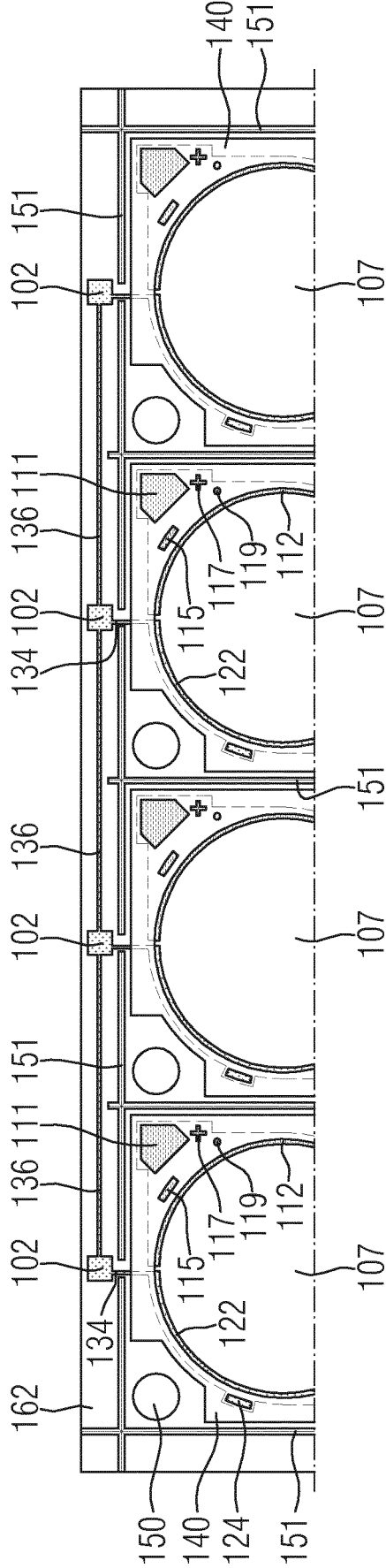


FIG 10

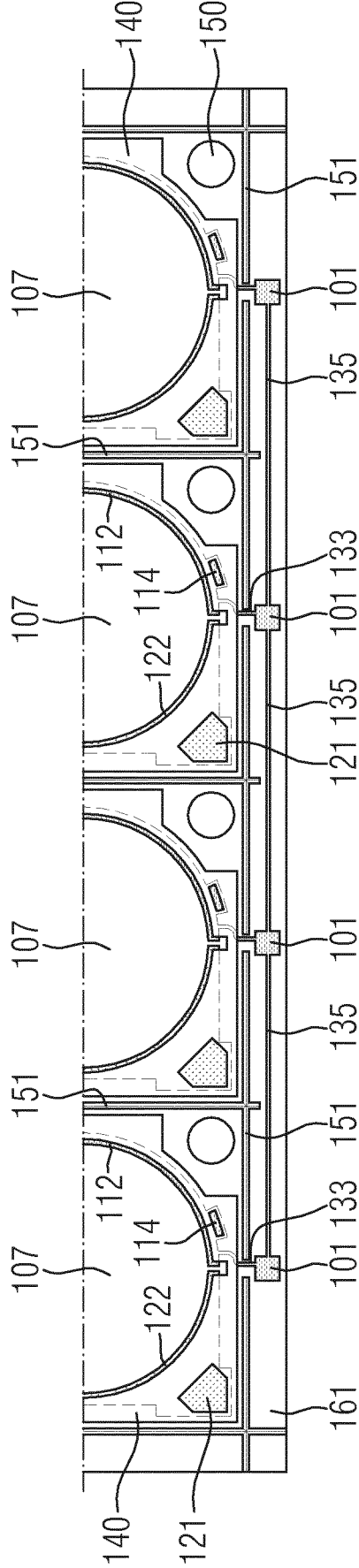


FIG 11

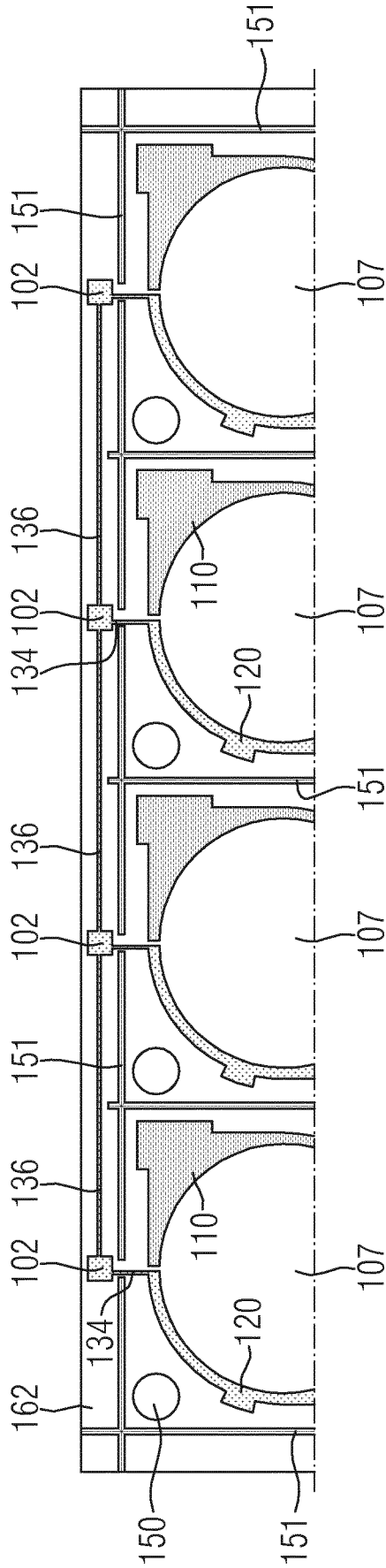


FIG 12

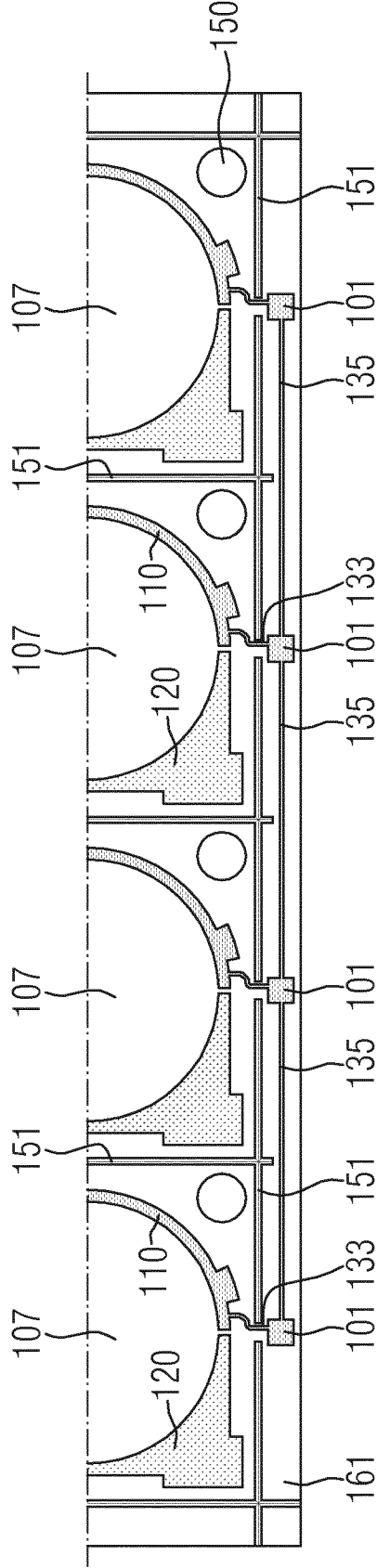


FIG 13

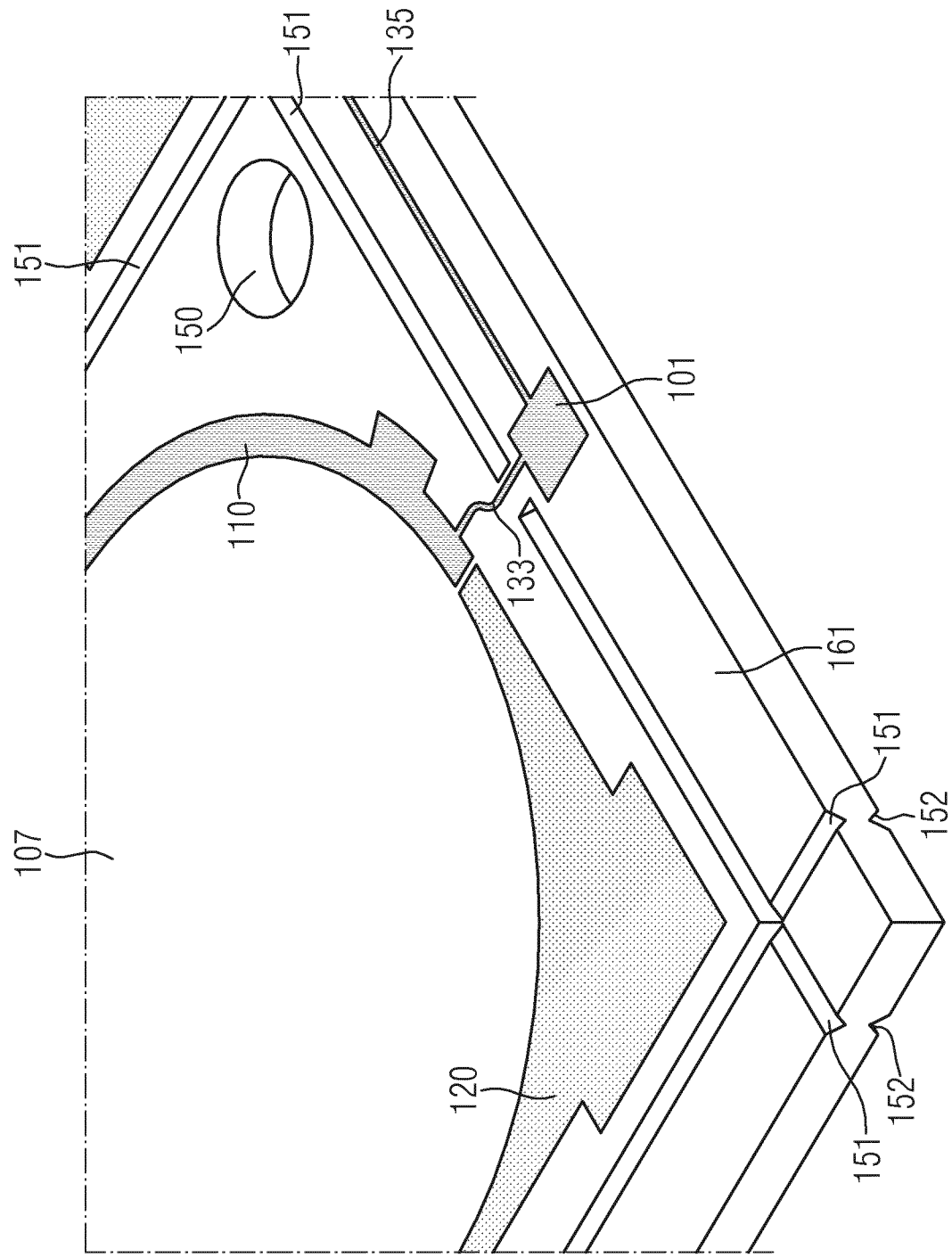


FIG 14

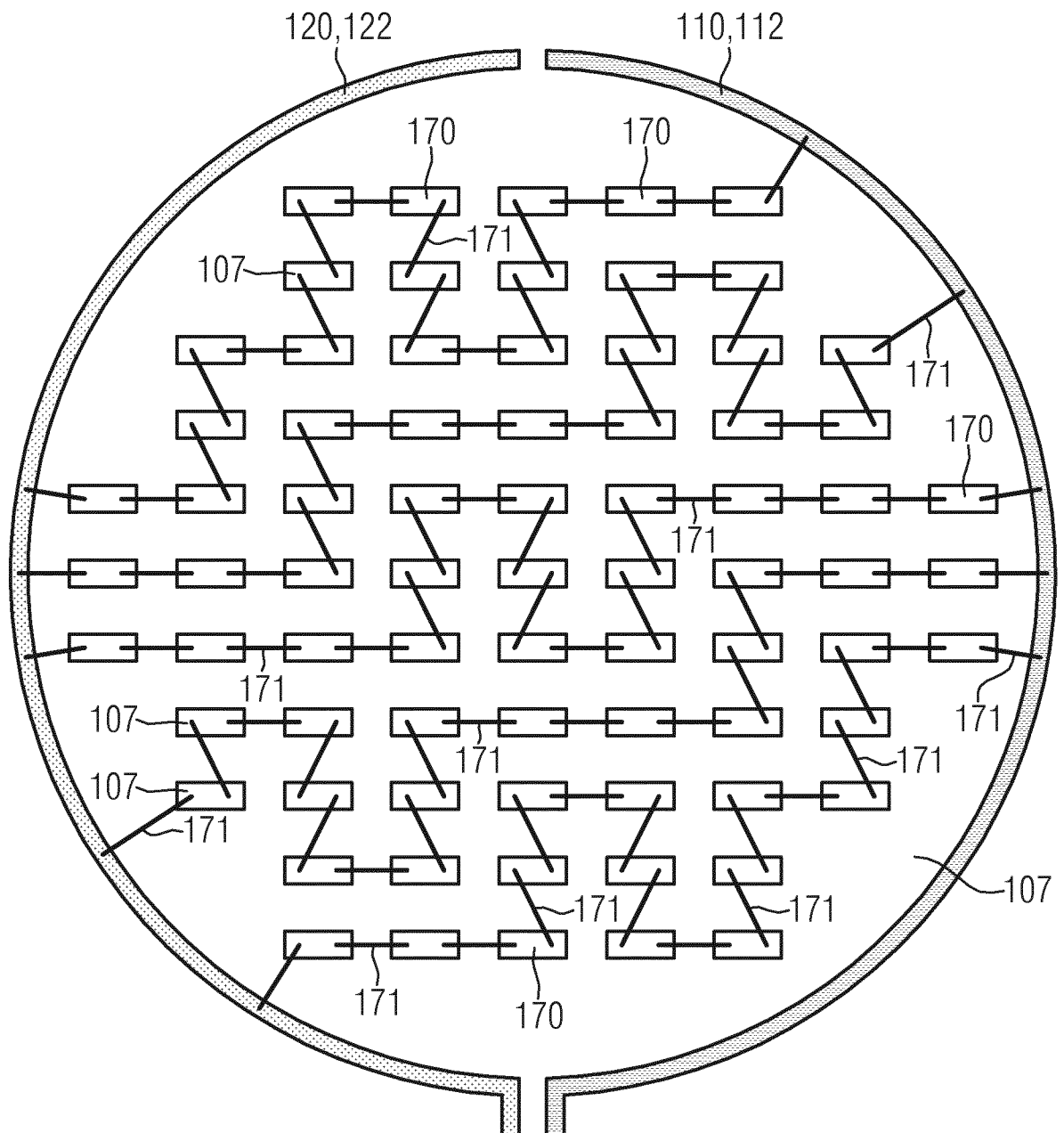


FIG 15

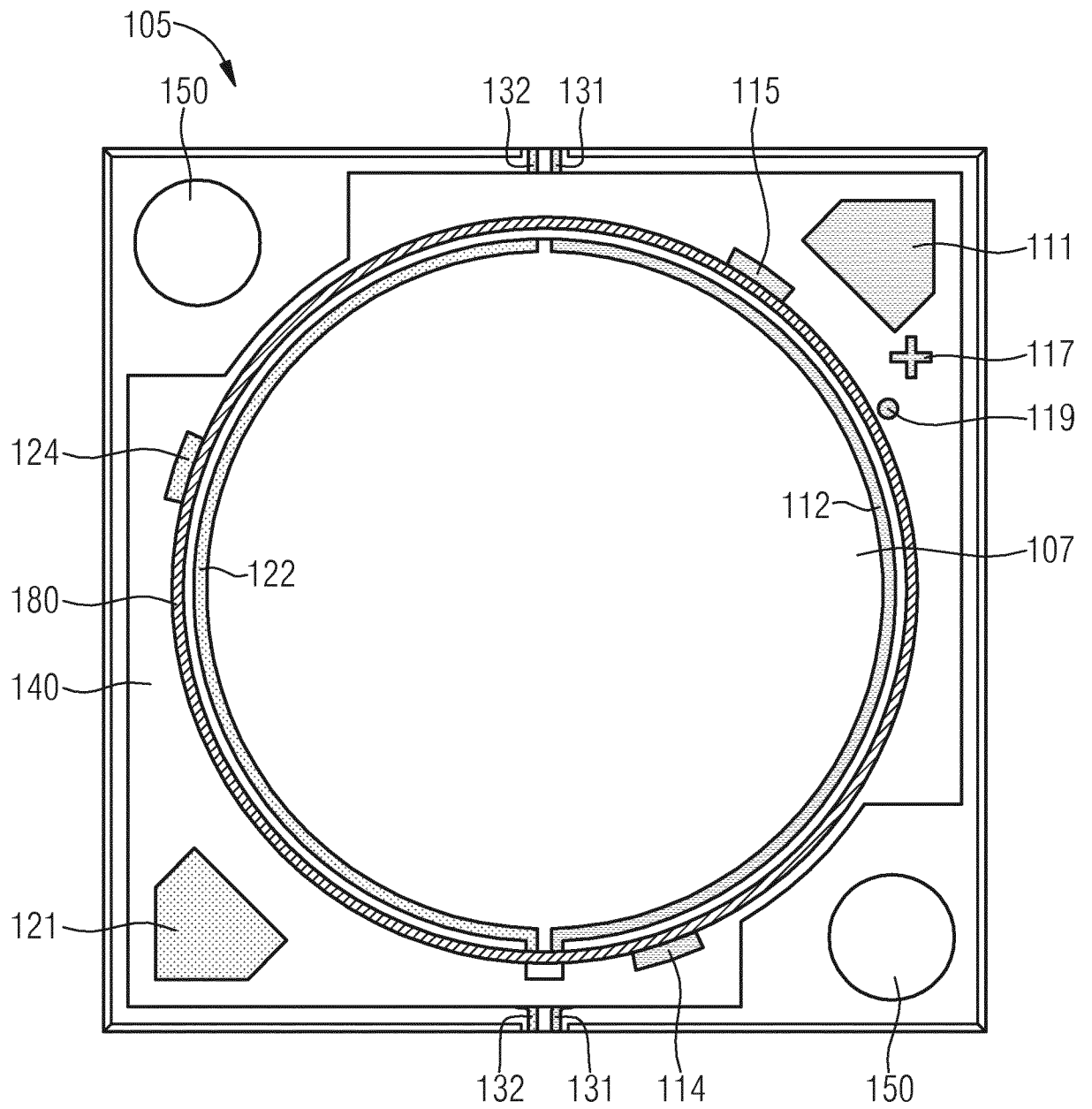
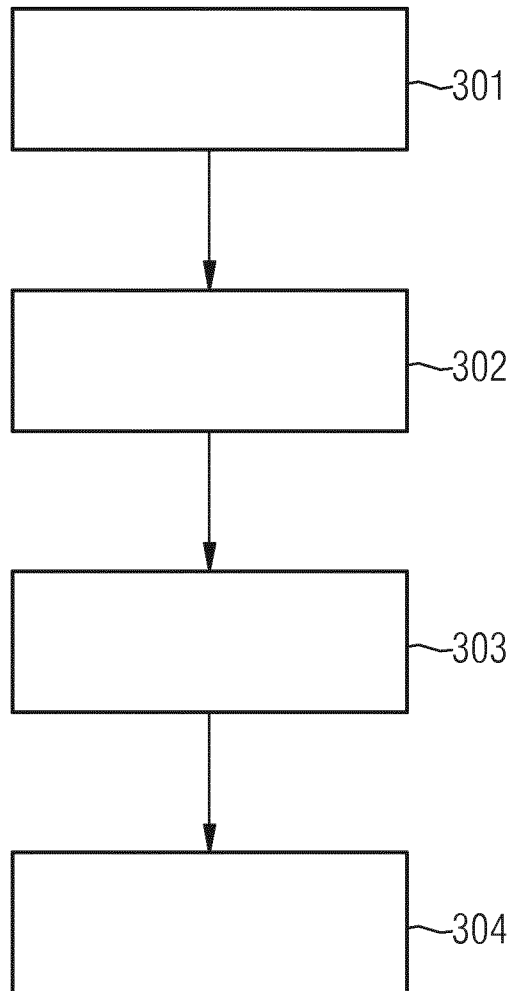


FIG 16



INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2013/066282

A. CLASSIFICATION OF SUBJECT MATTER

INV. H05K1/02 H05K3/00
 ADD. G01R31/26 H01L21/782

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05K G01R H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/249776 A1 (JI WON-SOO [KR] ET AL) 4 October 2012 (2012-10-04) paragraph [0046] - paragraph [0082]; figures 3-8 -----	1-11
X	CA 2 389 631 A1 (CHIN YOON [CA]) 6 December 2003 (2003-12-06) page 1, line 21 - page 7, line 2 -----	1-11
X	US 2006/221608 A1 (ISHIZUKA MASAHIRO [JP] ET AL) 5 October 2006 (2006-10-05) paragraph [0007] - paragraph [0010]; figures 1-6 paragraph [0020] - paragraph [0040] -----	1-11
A	US 4 426 773 A (HARGIS BILLY M [US]) 24 January 1984 (1984-01-24) the whole document -----	1-11



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

19 March 2014

Date of mailing of the international search report

01/04/2014

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