



(51) International Patent Classification:

H01L 29/78 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:

PCT/CN2019/080340

(22) International Filing Date:

29 March 2019 (29.03.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; 12500 Ti Boulevard, MS 3999, Dallas, Texas 75243 (US).(71) Applicant (for JP only): **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-shinjuku 6-chome, Shinjuku-ku, Tokyo 160-8366 (JP).(72) Inventors: **YANG, Hong**; 4616 Breckinridge Boulevard, Richardson, Texas 75082 (US). **SRIDHAR, Seetharaman**; 4424 Cedar Elm Circle, Richardson, Texas 75082 (US). **CHEN, Yaping**; No. 28, Er Huan Lu Dong Yi Duan, Chengdu, Sichuan 610051 (CN). **MA, Fei**; 518 Wenxin Road, Pixian, Chengdu, Sichuan 611730 (CN). **LIU, Yunlong**; 421 Taishan North Road, Pixian, Chengdu, Sichuan 610031 (CN). **KIM, Sunglyong**; 1516 Jamison Drive, Allen, Texas 75013 (US).(74) Agent: **LEE AND LI - LEAVEN IPR AGENCY LTD.**; Unit 2202, Tower A, Beijing Marriott Center, No. 7, Jian Guo Men South Avenue, Beijing 100005 (CN).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,

(54) Title: TRENCH SHIELD ISOLATION LAYER

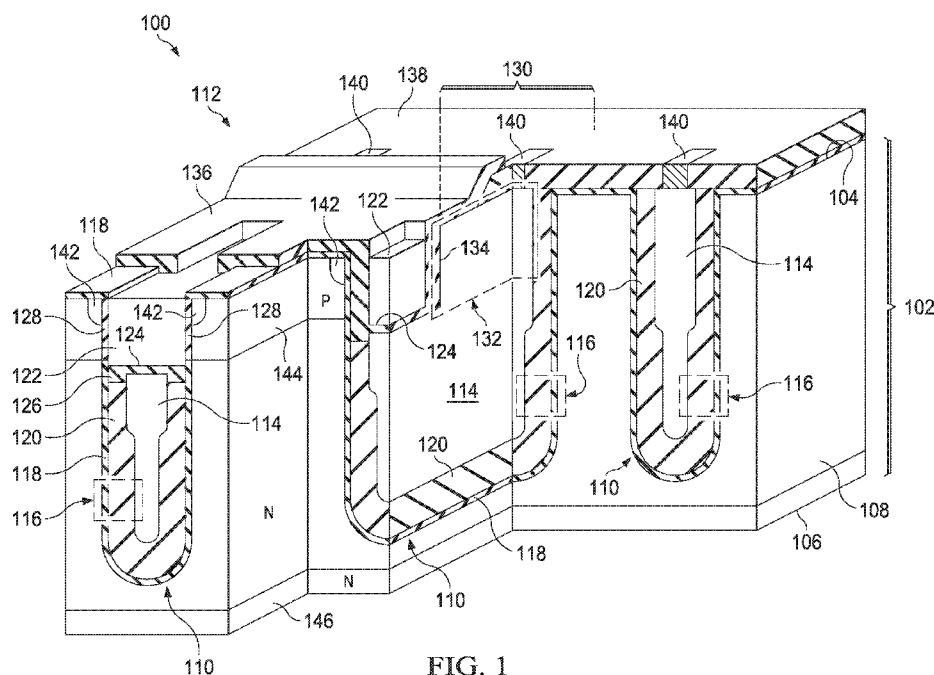


FIG. 1

(57) **Abstract:** A semiconductor device (100) has a semiconductor material (108) in a substrate (102). The semiconductor device (100) has an MOS transistor (112). A trench (110) in the substrate (102) extends from a top surface (104) of the substrate (102) into the semiconductor material (108). A shield (114) is disposed in the trench (110). The shield (114) has a contact portion (132) which extends toward a top surface of the trench (110). A gate (122) of the MOS transistor (112) is disposed in the trench (110) over the shield (114). The gate (122) is electrically isolated from the shield (114). The gate (122) is electrically isolated from the contact portion (132) of the shield (114) by a shield isolation layer (136) which covers an angled surface (134) of the contact portion (132) extending toward the top of the trench (110). Methods of forming the semiconductor device (100) are disclosed.



HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

— *with international search report (Art. 21(3))*

TRENCH SHIELD ISOLATION LAYER

FIELD

[0001] This disclosure relates to the field of semiconductor devices. More particularly, this disclosure relates to isolation layers in microelectronic devices/integrated circuits/semiconductor devices.

BACKGROUND

[0002] Some semiconductor devices include a transistor with a gate in a trench in the semiconductor substrate, and a shield in the trench below the gate. Such a configuration is common in vertical metal oxide semiconductor (MOS) transistors. A portion of the shield extends to a top of the trench, to provide an area for an electrical connection to the shield. Forming the shield and the gate to be electrically isolated from each other, while maintaining the size of the transistor below a target size, has been difficult to achieve in production.

SUMMARY

[0003] The present disclosure introduces a semiconductor device which includes a metal oxide semiconductor (MOS) transistor having a trench in a substrate. The substrate includes a semiconductor material extending to the trench. A shield is disposed in the trench. A contact portion of the shield extends toward a top surface of the trench. A gate is disposed in the trench over the shield. The gate is electrically isolated from the shield. The gate is electrically isolated from the contact portion of the shield by a shield isolation layer which covers an angled surface of the shield contact portion extending toward the top of the trench. The semiconductor device is formed by removing at least a portion of a shield liner in the trench in a region for the gate, and forming the shield isolation layer on the surface of the shield extending toward the top of the trench, prior to forming the gate.

BRIEF DESCRIPTION OF THE VIEWS OF THE DRAWINGS

[0004] FIG. 1 is a cross section of an example semiconductor device with a shield and a gate separated by a shield isolation layer.

[0005] FIG. 2A through FIG. 2N are cross sections of a semiconductor device with a shield and a gate separated by a shield isolation layer, depicted in stages of an example method of formation.

[0006] FIG. 3A and FIG. 3B are cross sections of a semiconductor device with a shield and a gate separated by a shield isolation layer, depicted in stages of another example method of formation.

DETAILED DESCRIPTION

[0007] The present disclosure is described with reference to the attached figures. The figures are not drawn to scale and they are provided merely to illustrate the disclosure. Several aspects of the disclosure are described below with reference to example applications for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide an understanding of the disclosure. The present disclosure is not limited by the illustrated ordering of acts or events, as some acts may occur in different orders and/or concurrently with other acts or events. Furthermore, not all illustrated acts or events are required to implement a methodology in accordance with the present disclosure.

[0008] A semiconductor device has a trench in a substrate. The substrate includes a semiconductor material, which extends to the trench. The semiconductor device includes a metal oxide semiconductor (MOS) transistor. A shield of the MOS transistor is disposed in the trench, along a bottom of the trench and extending toward a top of the trench, for example, at an end of the trench. The shield is separated from the semiconductor material of the substrate by a shield liner which is electrically non-conductive. An electrical connection to the shield may be located at the top of the trench, where the shield extends toward the top of the trench. The shield has an angled surface where the shield extends toward the top of the trench. A gate of the MOS transistor is disposed in the trench, over the shield. The gate is separated from the angled surface of the shield by a shield isolation layer which includes a dielectric material.

[0009] The semiconductor device is formed by forming the shield liner in the trench, and forming the shield on the shield liner, extending to a top of the trench. A portion of the shield is removed from the trench, leaving the shield extending along a

bottom of the trench, and extending toward the top of the trench with the angled surface. At least a portion of the trench liner is removed where exposed by the shield. A shield isolation layer is formed on the shield, covering the angled surface of the shield that extends toward the top of the trench. The gate is formed in the trench, so that the gate is separated from the angled surface of the shield by the shield isolation layer.

[0010] It is noted that terms such as top, bottom, over, and below may be used in this disclosure. These terms should not be construed as limiting the position or orientation of a structure or element, but should be used to provide spatial relationship between structures or elements.

[0011] FIG. 1 is a cross section of an example semiconductor device with a shield and a gate separated by a shield isolation layer. The semiconductor device 100 includes a substrate 102 having a top surface 104 and a bottom surface 106, located opposite from the top surface 104. The substrate 102 includes a semiconductor material 108, such as silicon. The semiconductor material 108 may extend from the top surface 104 to the bottom surface 106, as depicted in FIG. 1. The substrate 102 has one or more trenches 110 extending from the top surface 104 into the semiconductor material 108. References in the singular tense include the plural, and vice versa, unless otherwise noted. The trenches 110 may optionally be connected at a point not shown in FIG. 1, to provide a single trench 110. The semiconductor material 108 extends to the trenches 110. The trenches 110 may be 0.5 microns to 2 microns wide, for example, and may have ratios of depth to width, referred to as aspect ratios, of 3:1 to 10:1, for example.

[0012] The semiconductor device 100 includes an MOS transistor 112. The MOS transistor 112 includes a shield 114 disposed in the trenches 110. The shield 114 is electrically conductive, and may include, for example, polycrystalline silicon, sometime referred to as polysilicon. The polycrystalline silicon may be doped during deposition, or may be implanted with dopants after deposition, to reduce an electrical resistivity of the shield 114. The shield 114 is separated from the semiconductor material 108 by a shield liner 116 which is electrically non-conductive. In this example, the shield liner 116 may include a first liner 118 of thermal silicon dioxide, contacting the semiconductor material 108, and a second liner 120 of a deposited dielectric material, contacting the first liner 118. The thermal silicon dioxide in the first liner 118 may be characterized by a

stoichiometric composition of silicon dioxide, that is, SiO_2 , and a hydrogen content less than 5 atomic percent. The first liner 118 may have a thickness of 20 nanometers to 200 nanometers in the trenches 110, for example. The first liner 118 may optionally extend over the top surface 104 of the substrate 102, as indicated in FIG. 1. The second liner 120 may include silicon dioxide, and may have an etch rate, in aqueous buffered hydrofluoric acid, that is at least twice an etch rate, in the same aqueous buffered hydrofluoric acid, of the first liner 118. The shield liner 116 may vary in thickness, having a higher thickness proximate to a bottom of the shield 114 than proximate to a top of the shield 114. By way of example, the shield liner 116 may have a thickness of 200 nanometers to 400 nanometers proximate to the bottom of the shield 114, and may have a thickness of 60 nanometers to 200 nanometers proximate to the top of the shield 114. Having a varying thickness of the shield liner 116 may advantageously reduce an electric field in the semiconductor material 108 between the trenches 110 during operation of the MOS transistor 112. The term “proximate to” is understood in this context to refer to a vertical distance that is less than a lateral width of the trenches 110. The terms “lateral” and “laterally” refer to a direction parallel to the top surface 104 of the substrate 102. The terms “vertical” and “vertically” refer to a direction perpendicular to the top surface 104.

[0013] The MOS transistor 112 includes a gate 122 in the trenches 110. The shield 114 extends under the gate 122 in the trenches 110. The gate 122 may include polycrystalline silicon, for example, with appropriate dopants to attain a desired threshold potential during operation of the MOS transistor 112. A gate bottom surface 124 of the gate 122 is separated from the shield 114 by a lateral insulator 126. The lateral insulator 126 may include silicon dioxide, for example. The gate 122 extends to proximate to a top of the trenches 110, that is, proximate to the top surface 104 of the substrate 102. Proximate to the top surface 104, in this example, is understood to mean a vertical distance between a top of the gate 122 and the top surface 104 is less than a lateral width of one of the trenches 110. The gate 122 is separated from the semiconductor material 108 by a gate dielectric layer 128, which contacts the gate 122 and the semiconductor material 108.

[0014] One or more contact portions 132 of the shield 114 extend toward the top of that trench 110, that is, toward the top surface 104. The contact portions 132 of the shield 114 may be located, for example, at ends 130 of the trenches 110. The contact portion 132 of the shield 114 has an angled surface 134 adjacent to the gate 122 that extends from below the gate bottom surface 124 to proximate to the top of the trench 110. A plane of the angled surface 134 intersects the top surface 104 of the substrate 102 at an angle of 45 degrees to 90 degrees, with 90 degrees being perpendicular to the top surface 104. The angled surface 134 of the contact portion 132 of the shield 114 is separated from the gate 122 by a shield isolation layer 136, which is electrically non-conductive. The shield isolation layer 136 contacts the gate 122 and the angled surface 134 of the contact portion 132 of the shield 114. The shield isolation layer 136 may extend laterally between the gate bottom surface 124 and the shield 114 for a distance sufficient to provide complete coverage of the angled surface 134 of the contact portion 132 of the shield 114, but does not extend a length of each of the trenches 110. By way of example, the shield isolation layer 136 may extend laterally between the gate bottom surface 124 and the shield 114 for 1 micron to 5 microns. The shield isolation layer 136 may include silicon dioxide, with a hydrogen content less than 15 atomic percent. The shield isolation layer 136 may extend over the top surface 104 of the substrate, as shown in FIG. 1. The shield isolation layer 136 may be 100 nanometers to 300 nanometers thick, for example. The shield isolation layer 136 may advantageously reduce leakage current between the gate 122 and the contact portion 132 of the shield 114 during operation of the MOS transistor 112, compared to relying on an extension of the gate dielectric layer 128 to isolate the gate 122 from the contact portion 132 of the shield 114.

[0015] The shield isolation layer 136 may extend onto a top dielectric layer 138. The top dielectric layer 138 may include silicon dioxide, and may be 300 nanometers to 1 micron thick, for example. An edge of the top dielectric layer 138 adjacent to the contact portion 132 of the shield 114 may be tapered, as depicted in FIG. 1. Contacts 140 may extend through the top dielectric layer 138 to provide electrical connections to the contact portion 132 of the shield 114.

[0016] The MOS transistor 112 of this example includes a source 142 in the semiconductor material 108, contacting the gate dielectric layer 128. The source 142 has

a first conductivity type, for example, n-type. The MOS transistor 112 of this example includes a body 144 in the semiconductor material 108, contacting the gate dielectric layer 128 and the source 142. The body 144 has a second conductivity type, opposite from the first conductivity type; in this example, the body 144 may be p-type, as indicated in FIG. 1. The MOS transistor 112 of this example includes a drain contact region 146 in the semiconductor material 108 below the trenches 110, extending to the bottom surface 106 of the substrate 102. The drain contact region 146 has the first conductivity type, which is n-type in this example, as indicated in FIG. 1. The semiconductor material 108 between the body 144 and the drain contact region 146 may have the first conductivity type, n-type in this example, and may provide a drain drift region for the MOS transistor 112.

[0017] FIG. 2A through FIG. 2N are cross sections of a semiconductor device with a shield and a gate separated by a shield isolation layer, depicted in stages of an example method of formation. Referring to FIG. 2A, formation of the semiconductor device 200 includes acquiring a substrate 202. The substrate 202 may be implemented as a semiconductor wafer, such as a silicon wafer, optionally with an epitaxial layer, for example. The substrate 202 has a top surface 204 and a bottom surface 206 located opposite from the top surface 204. The substrate 202 includes a semiconductor material 208, such as silicon. The semiconductor material 208 may extend from the top surface 204 to the bottom surface 206, as depicted in FIG. 2A.

[0018] The substrate 202 includes an area for an MOS transistor 212. In the area for the MOS transistor 212, one or more trenches 210 are formed in the substrate 202. The trenches 210 extend from the top surface 204 into the semiconductor material 208. The one or more trenches 210 may optionally be connected at a point not shown in FIG. 2A, to provide a single trench 210. The trenches 210 may extend to proximate to the bottom surface 206 of the substrate 202, as depicted in FIG. 2A. Alternatively, the trenches 210 may extend through the semiconductor material 208 to the bottom surface 206. The trenches 210 may be 0.5 microns to 2 microns wide, for example, and may have aspect ratios of 3:1 to 10:1, for example.

[0019] A first liner 218 is formed on the semiconductor material 208 in the trenches 210. The first liner 218 of this example is formed by a thermal oxidation

process at a temperature above 800 °C, so that the first liner 218 includes primarily thermal silicon dioxide having a stoichiometric composition of silicon dioxide, that is, SiO₂, and a hydrogen content less than 5 atomic percent. The first liner 218 may have a thickness of 20 nanometers to 200 nanometers in the trenches 210, for example. The first liner 218 may extend over the top surface 204 of the substrate 202, as depicted in FIG. 2A.

[0020] Referring to FIG. 2B, a second liner 220 is formed on the trenches 210 on the first liner 218. The second liner 220 may be formed by a thermal chemical vapor deposition (CVD) process using tetraethyl orthosilicate (TEOS), Si(OC₂H₅)₄, sometimes referred to as tetraethoxysilane. The thermal CVD process may be implemented as a sub-atmospheric chemical vapor deposition (SACVD) process, for example, or as an atmospheric pressure chemical vapor deposition (APCVD) process. Alternatively, the second liner 220 may be formed by a plasma enhanced chemical vapor deposition (PECVD) process, using TEOS. The second liner 220 includes primarily silicon dioxide. The second liner 220 is formed at a temperature sufficiently low so that the second liner 220 has an etch rate, in aqueous buffered hydrofluoric acid, that is at least twice an etch rate, in the same aqueous buffered hydrofluoric acid, of the first liner 218. By way of example, the second liner 220 may be formed below 600 °C. The second liner 220 may be formed to have a greater thickness proximate to bottoms of the trenches 210 than proximate to tops of the trenches 210, as depicted in FIG. 2B. The second liner 220 may be formed in two or more steps to attain a desired thickness profile in the trenches 210. The second liner 220 may be removed from over the top surface 204 of the substrate 202, as indicated in FIG. 2B, or may extend over the top surface 204, similarly to the first liner 218. A combination of the first liner 218 and the second liner 220 provides a shield liner 216 in the trenches 210.

[0021] A shield 214 is formed in the trenches 210 on the shield liner 216, extending to proximate to the top surface 204 of the substrate 202. The shield 214 is electrically conductive, and is electrically isolated from the semiconductor material 208 by the shield liner 216. The shield 214 may be formed by thermal or plasma decomposition of silane or disilane, so that the shield 214 may include primarily polycrystalline silicon. The shield 214 may be formed at a temperature that is

sufficiently low so as to maintain the etch rate of the second liner 220, in aqueous buffered hydrofluoric acid, above twice the etch rate of the first liner 218. By way of one example, the shield 214 may be formed of undoped polycrystalline silicon at 600 °C to 620 °C, and subsequently implanted with dopants and annealed to provide a desired electrical resistivity in the shield 214. By way of another example, the shield 214 may be formed of doped polycrystalline silicon at 500 °C to 580 °C by including dopant reagents with the silane or disilane.

[0022] Referring to FIG. 2C, a top dielectric layer 238 is formed over the top surface 204 of the substrate 202. The top dielectric layer 238 is patterned to expose the shield 214 in the trenches 210. The top dielectric layer 238 may include silicon dioxide, and may be 300 nanometers to 1 micron thick, for example. The top dielectric layer 238 may be formed by a thermal CVD process using TEOS, or by a PECVD process using TEOS, at a temperature that is sufficiently low so as to maintain the etch rate of the second liner 220, in aqueous buffered hydrofluoric acid, above twice the etch rate of the first liner 218. An edge of the top dielectric layer 238 adjacent to the shield 214 may be tapered, as depicted in FIG. 2C, using an erodable etch mask, and etching the top dielectric layer 238 using an isotropic plasma etch process.

[0023] Referring to FIG. 2D, a shield etch mask 248 is formed over the top surface 204 of the substrate 202, covering one or more contact portions 232 of the shield 214, which may be located, for example, at ends 230 of the trenches 210, and exposing the shield 214 past the contact portion 232. The shield etch mask 248 may include photoresist, and may be formed by a photolithographic process. The shield etch mask 248 may include hard mask materials, such as silicon nitride or amorphous carbon. In an alternate version of this example, the shield etch mask 248 may be used to provide an etch mask for both the top dielectric layer 238 and the shield 214, advantageously reducing fabrication cost and complexity of the semiconductor device 200.

[0024] A portion of the shield 214 is removed where exposed by the shield etch mask 248, leaving the shield 214 along a bottom portion of the trenches 210. The portion of the shield 214 may be removed by a reactive ion etch (RIE) process using chlorine or bromine. The portion of the shield 214 may be removed by a timed etch process, to remove a desired amount of the shield 214. The process of removing the portion of the

shield 214 leaves the contact portion 232 with an angled surface 234 extending proximate to the top surface 204 of the substrate 202. The process of removing the portion of the shield 214 also leaves at least a portion of the shield liner 216 in the trenches 210, extending to the top surface 204, as depicted in FIG. 2D.

[0025] Referring to FIG. 2E, the shield etch mask 248 of FIG. 2D is removed. The shield etch mask 248 may be removed by an oxygen plasma process, such as an asher process or a downstream asher process, or an ozone process, followed by a wet clean process using an aqueous mixture of sulfuric acid and hydrogen peroxide. Other methods for removing the shield etch mask 248 are within the scope of this example. The shield etch mask 248 may be used to provide an etch mask for the top dielectric layer 238, before being removed, as noted above.

[0026] Referring to FIG. 2F, the second liner 220 is removed from the trenches 210 where exposed by the shield 214. The second liner 220 may be removed by a wet etch using an aqueous solution of buffered hydrofluoric acid, for example a 1 percent solution of buffered hydrofluoric acid. At least a portion of the first liner 218 remains in the trenches 210, extending up to the top surface 204 of the substrate 202, due to the lower etch rate of the first liner 218 in the buffered hydrofluoric acid solution than the second liner 220. The wet etch to remove the second liner 220 may be a timed etch process, to remove the second liner 220 where exposed by the shield 214, while reducing etching of the second liner 220 between the shield 214 and the first liner 218. Forming the second liner 220 to have an etch rate at least twice that of the first liner 218 may advantageously enable complete removal of the second liner 220 where exposed by the shield 214 while leaving a continuous portion of the first liner 218 on the semiconductor material 208 in the trenches 210, preventing erosion of the semiconductor material 208. The process of removing the second liner 220 where exposed by the shield 214 may result in grooves 250 in the second liner 220 along the angled surface 234 of the contact portion 232 of the shield 214, between the contact portion 232 and the first liner 218, as depicted in FIG. 2F. The grooves 250 may expose edges of the contact portion 232 of the shield 214 along the angled surface 234. These edges may be difficult to electrically isolate from a subsequently-formed gate 222, shown in FIG. 2N, by a subsequently-formed gate dielectric layer 228, shown in FIG. 2L, alone.

[0027] Referring to FIG. 2G, a conformal layer 252 is formed over the top dielectric layer 238 and the top surface 204 of the substrate 202, extending into the trenches 210 and covering the shield 214, including the angled surface 234 of the contact portion 232 of the shield 214. The conformal layer 252 fills in the grooves 250 of FIG. 2F in the second liner 220 along the angled surface 234 of the contact portion 232 of the shield 214. The conformal layer 252 includes primarily silicon dioxide, and is formed, in this example, by a thermal CVD process using TEOS, such as an SACVD process or an APCVD process, or a PECVD process using TEOS, at a temperature sufficiently low so that the conformal layer 252 has an etch rate, in aqueous buffered hydrofluoric acid, that is at least twice an etch rate, in the same aqueous buffered hydrofluoric acid, of the first liner 218. By way of example, the conformal layer 252 may be formed at approximately 600 °C. The conformal layer 252 is formed to be conformal in the trenches 210, that is, an average thickness of the conformal layer 252 on angled surfaces of the trenches 210 is 50 percent to 125 percent of an average thickness of the conformal layer 252 on horizontal surfaces in the trenches 210.

[0028] Referring to FIG. 2H, an isolation etch mask 254 is formed over the conformal layer 252. The isolation etch mask 254 extends over the contact portion 232 of the shield 214 and into the trenches 210 past the angled surface 234 of the contact portion 232. The isolation etch mask 254 does not cover the shield 214 throughout the trenches 210. The isolation etch mask 254 may extend over the shield 214 past the angled surface 234 a lateral distance of 1 micron to 5 microns, for example, to allow for undercut of the conformal layer 252 while maintaining complete coverage of the angled surface 234. The isolation etch mask 254 may include photoresist, and may be formed by a photolithographic process. Alternatively, the isolation etch mask 254 may include a polymer, and may be formed by an additive process, such as an ink jet process or a material extrusion process.

[0029] Referring to FIG. 2I, the conformal layer 252 of FIG. 2H is removed where exposed by the isolation etch mask 254 to form a shield isolation layer 236 of the conformal layer 252 covered by the isolation etch mask 254. The conformal layer 252 may be removed by a wet etch using an aqueous solution of buffered hydrofluoric acid, for example a 1 percent solution of buffered hydrofluoric acid. The conformal layer 252

may be removed by a wet etch similar to that used to remove a portion of the second liner 220 as disclosed in reference to FIG. 2F. The process of removing the conformal layer 252 is performed so as to leave at least a portion of the first liner 218 in the trenches 210, extending up to the top surface 204 of the substrate 202, due to the lower etch rate of the conformal layer 252 in the buffered hydrofluoric acid solution than the second liner 220. The wet etch to remove the conformal layer 252 may be a timed etch process, to reduce undercut of the conformal layer 252 and to reduce etching of the second liner 220 between the shield 214 and the first liner 218. Forming the conformal layer 252 to have an etch rate at least twice that of the first liner 218 may advantageously enable complete removal of the conformal layer 252 where exposed by the isolation etch mask 254 while leaving a continuous portion of the first liner 218 on the semiconductor material 208 in the trenches 210, preventing erosion of the semiconductor material 208.

[0030] Referring to FIG. 2J, the isolation etch mask 254 of FIG. 2I is removed. The isolation etch mask 254 may be removed by an oxygen plasma process followed by a wet clean process, such as the process described for removal of the shield etch mask 248, disclosed in reference to FIG. 2F.

[0031] The shield isolation layer 236 may optionally be heated after the isolation etch mask 254 is removed, to reduce an etch rate of the shield isolation layer 236 in an aqueous solution of buffered hydrofluoric acid, prior to removing the first liner 218 where exposed by the second liner 220 and the shield isolation layer 236. For example, the shield isolation layer 236 may be heated to 800 °C to 900 °C, for 5 minutes to 60 minutes. Alternatively, formation of the semiconductor device 200 may be continued without heating the shield isolation layer 236.

[0032] The shield isolation layer 236 covers the angled surface 234 of the contact portion 232 of the shield 214, and extends into the grooves in the second liner 220 along the angled surface 234 of the contact portion 232 of the shield 214. The shield isolation layer 236 may be formed to extend laterally on the shield 214 for a distance sufficient to provide complete coverage of the angled surface 234.

[0033] Referring to FIG. 2K, the first liner 218 is removed in the trenches 210 where exposed by the second liner 220 and by the shield isolation layer 236. The first liner may be removed by an aqueous solution of buffered hydrofluoric acid, which may

also remove a portion of the second liner 220 and a portion of the shield isolation layer 236. The top surface 204 of the substrate 202 may remain covered by silicon dioxide after the first liner 218 is removed in the trenches 210, as depicted in FIG. 2K. Alternatively, removal of the first liner 218 in the trenches 210 may result in removal of silicon dioxide from a portion or all of the top surface 204 where exposed by the shield isolation layer 236 and the top dielectric layer 238. Forming the first liner 218 to be thinner than the second liner 220 and thinner than the shield isolation layer 236 may advantageously enable removal of the first liner 218 without significant degradation of the second liner 220 and the shield isolation layer 236.

[0034] Referring to FIG. 2L, a gate dielectric layer 228 is formed on the semiconductor material 208 in the trenches 210 where exposed by the first liner 218. The gate dielectric layer 228 may be formed by a thermal oxidation process, and may have a thickness of 5 nanometers to 500 nanometers, for example. Other methods for forming the gate dielectric layer 228 are within the scope of this example. Forming the gate dielectric layer 228 may result in forming a dielectric layer, not shown in FIG. 2L, on the shield 214 in the trenches 210.

[0035] Referring to FIG. 2M, a lateral insulator 226 may be formed over the shield 214 in the trenches 210. The lateral insulator 226 electrically isolates the shield 214 from a subsequently-formed gate 222, shown in FIG. 2N.

[0036] Referring to FIG. 2N, the gate 222 is formed in the trenches 210, contacting the gate dielectric layer 228. The gate 222 may include polycrystalline silicon, and may be formed by thermal or plasma decomposition of silane or disilane, for example. The gate 222 may be formed by a process similar to that used to form the shield 214. The gate 222 is isolated from the contact portion 232 of the shield 214 by the shield isolation layer 236. The shield isolation layer 236 may limit a low leakage current between the gate 222 and the shield 214 to a desired value during operation of the MOS transistor 212. Formation of the semiconductor device 200 is continued by forming a source, body, drain contact region, and contacts, not shown in FIG. 2N, to provide a structure similar to the semiconductor device 100 of FIG. 1.

[0037] FIG. 3A and FIG. 3B are cross sections of a semiconductor device with a shield and a gate separated by a shield isolation layer, depicted in stages of another

example method of formation. Referring to FIG. 3A, the semiconductor device 300 is formed in and on a substrate 302 having a top surface 304 and a bottom surface 306 located opposite from the top surface 304, and a semiconductor material 308 between the top surface 304 and the bottom surface 306. One or more trenches 310 are formed in the substrate 302 in an area for an MOS transistor 312. The trenches 310 extend into the semiconductor material 308 from the top surface 304. A shield liner 316 is formed in the trenches 310, including a first liner 318 and a second liner 320. A shield 314 is formed in the trenches 310; in this example, the shield 314 may include two or more separate pieces, arranged vertically in the trenches 310. A contact portion 332 of the shield 314 extends to proximate to the top surface 304, while a remainder of the shield 314 is recessed vertically in the trenches 310 from the top surface 304, to allow room for a subsequently-formed gate in the trenches 310. The contact portion 332 of the shield 314 has an angled surface 334 that is exposed in the trenches 310. A top dielectric layer 338 may be formed over the top surface 304 outside of the trenches 310, as depicted in FIG. 3A.

[0038] In this example, a shield isolation layer 336 is formed on the angled surface 334 by an additive process. For the purposes of this disclosure, an additive process may be understood to dispose nanoparticles in an area for the shield isolation layer 336, and not dispose the nanoparticles outside of the area for the shield isolation layer 336, so that it is not necessary to remove a portion of the disposed nanoparticles to produce a final desired shape of the shield isolation layer 336. Additive processes may enable forming films in desired areas without photolithographic processes and subsequent etch processes, thus advantageously reducing fabrication cost and complexity. Examples of additive processes include binder jetting, material jetting, directed energy deposition, material extrusion, powder bed fusion, sheet lamination, vat photopolymerization, direct laser deposition, electrostatic deposition, laser sintering, electrochemical deposition, cold spraying, thermal spraying, and photo-polymerization extrusion. By way of example, the additive process may use an ink jet apparatus 356 to dispense a dielectric precursor 358 onto the semiconductor device 300. In one example, the dielectric precursor 358 may include nanoparticles of silicon dioxide, in a liquid binder including TEOS. In another example, the dielectric precursor 358 may include nanoparticles of silicon dioxide,

silicon nitride, aluminum oxide, titanium dioxide, or other dielectric material, in a solvent binder. The dielectric precursor 358 may include materials which have a low etch rate in aqueous buffered hydrofluoric acid, such as silicon nitride, to reduce degradation of the shield isolation layer 336 during subsequent removal of the first liner 318. The shield isolation layer 336 may be formed to extend over the top dielectric layer 338 to a lateral perimeter of the semiconductor device 300, as indicated in FIG. 3A. Alternatively, the shield isolation layer 336 may be formed to extend partway onto the top dielectric layer 338, similar to the shield isolation layer 236 of FIG. 2N.

[0039] Referring to FIG. 3B, the shield isolation layer 336 is heated to remove volatile material such as binders or solvents, and to adhere nanoparticles in the shield isolation layer 336 to each other. The shield isolation layer 336 may be heated by a radiant heating process 360, as depicted schematically in FIG. 3B. Alternatively, the shield isolation layer 336 may be heated by a furnace process, a forced air convection heating process, or a hot plate process. Formation of the semiconductor device 300 is continued as disclosed in reference to FIG. 2K through FIG. 2N.

[0040] Various features of the examples disclosed herein may be combined in other manifestations of example semiconductor devices. For example, the MOS transistor 112 of FIG. 1 may have a single part shield similar to the shield 214 of FIG. 2B or a multiple part shield similar to the shield 314 of FIG. 3A. The MOS transistor 112 of FIG. 1 may have a shield isolation layer similar to the shield isolation layer 236 of FIG. 2J or the shield isolation layer 336 of FIG. 3A.

[0041] While various embodiments of the present disclosure have been described above, it should be understood that they have been presented by way of example only and not limitation. Numerous changes to the disclosed embodiments can be made in accordance with the disclosure herein without departing from the spirit or scope of the disclosure. Thus, the breadth and scope of the present invention should not be limited by any of the above described embodiments. Rather, the scope of the disclosure should be defined in accordance with the following claims and their equivalents.

What is claimed is:

1. A semiconductor device, comprising:

a substrate having a top surface and a bottom surface located opposite from the top surface, the substrate having a semiconductor material between the top surface and the bottom surface;

a shield in a trench in the substrate, the trench extending from the top surface, the shield being electrically conductive, wherein the semiconductor material extends to the trench, wherein the shield is separated from the semiconductor material by a shield liner in the trench, the shield liner being electrically non-conductive;

a metal oxide semiconductor (MOS) transistor, the MOS transistor including:

a gate in the trench, the shield extending under the gate, wherein the gate is electrically isolated from the shield; and

gate dielectric layer in the trench, the gate dielectric layer separating the gate from the semiconductor material; and

a shield isolation layer which separates the gate from an angled surface of a contact portion of the shield, the angled surface extending toward the top surface of the substrate, the shield isolation layer being electrically non-conductive, wherein the shield isolation layer does not extend the length of the trench.

2. The semiconductor device of claim 1, wherein the shield isolation layer includes silicon dioxide.

3. The semiconductor device of claim 1, wherein the shield liner includes a first liner contacting the semiconductor material of the substrate, and a second liner contacting the shield, the first liner having a stoichiometric composition of silicon dioxide (SiO_2), wherein the second liner includes silicon dioxide, and has an etch rate, in aqueous buffered hydrofluoric acid, that is at least twice an etch rate, in the same aqueous buffered hydrofluoric acid, of the first liner.

4. The semiconductor device of claim 1, wherein the shield includes polycrystalline silicon.

5. The semiconductor device of claim 1, wherein the gate includes polycrystalline silicon.

6. The semiconductor device of claim 1, wherein the shield isolation layer extends onto the top surface of the substrate.

7. The semiconductor device of claim 1, wherein the shield isolation layer extends into a groove between the contact portion of the shield and the semiconductor material.

8. A method of forming a semiconductor device, comprising:

acquiring a substrate having a top surface and a bottom surface located opposite from the top surface, the substrate having a semiconductor material between the top surface and the bottom surface;

forming a trench in the substrate into the semiconductor material from the top surface;

forming a shield liner in the trench on a surface of the semiconductor material, the shield liner being electrically non-conductive;

forming a shield of a metal oxide semiconductor (MOS) transistor in the trench on the shield liner, the shield being electrically conductive;

removing a portion of the shield from the trench from the top surface, so that the shield extends toward the top surface of the substrate at a contact portion of the shield, the contact portion having an angled surface extending toward the top surface of the substrate;

forming a shield isolation layer on the shield, the shield isolation layer covering the angled surface of the contact portion of the shield, the shield isolation layer being electrically non-conductive, wherein the shield isolation layer does not extend the length of the trench;

forming a gate dielectric layer of the MOS transistor in the trench on the semiconductor material; and

forming a gate of the MOS transistor in the trench, the gate contacting the gate dielectric layer, the gate being separated from the angled surface of the contact portion of the shield by the shield isolation layer.

9. The method of claim 8, wherein forming the shield isolation layer includes forming a conformal layer covering the angled surface of the contact portion of the shield, the conformal layer being electrically non-conductive.

10. The method of claim 9, wherein forming the shield isolation layer includes forming an etch mask over the conformal layer.

11. The method of claim 10, wherein forming the shield isolation layer includes removing the conformal layer where exposed by the etch mask using aqueous buffered hydrofluoric acid.

12. The method of claim 8, wherein forming the shield liner includes forming a first liner on the semiconductor material by a thermal oxidation process.

13. The method of claim 12, wherein forming the shield liner includes forming a second liner on the first liner using a thermal chemical vapor deposition (CVD) process using tetraethyl orthosilicate (TEOS).

14. The method of claim 8, wherein forming the shield isolation layer leaves a portion of the shield liner in the trench on the semiconductor material.

15. The method of claim 8, further including removing at least a portion of the shield liner from the trench where exposed by the shield, after removing the portion of the shield from the trench, and prior to forming the shield isolation layer.

16. The method of claim 8, wherein forming the shield isolation layer includes heating the shield isolation layer at a temperature above 800 °C.

17. The method of claim 16, wherein heating the shield isolation layer is performed concurrently with forming the gate dielectric layer.

18. The method of claim 8, wherein forming the gate includes forming polycrystalline silicon in the trench on the gate dielectric layer.

19. The method of claim 8, wherein:
removing the portion of the shield liner forms a groove along the angled surface, between the contact portion of the shield and the semiconductor material; and
forming the shield isolation layer fills the groove with dielectric material.

20. The method of claim 8, wherein forming the shield isolation layer is performed using an additive process.

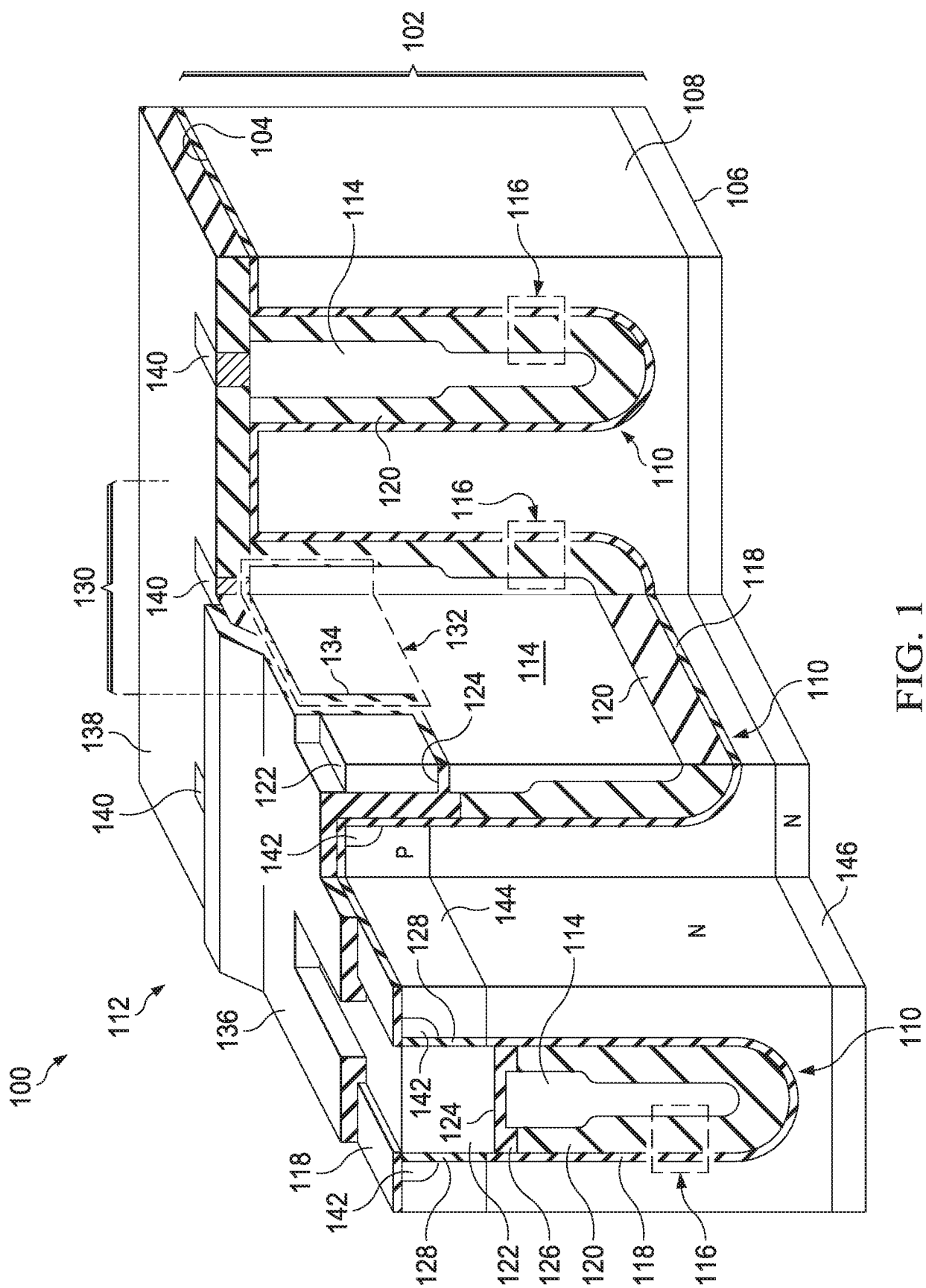
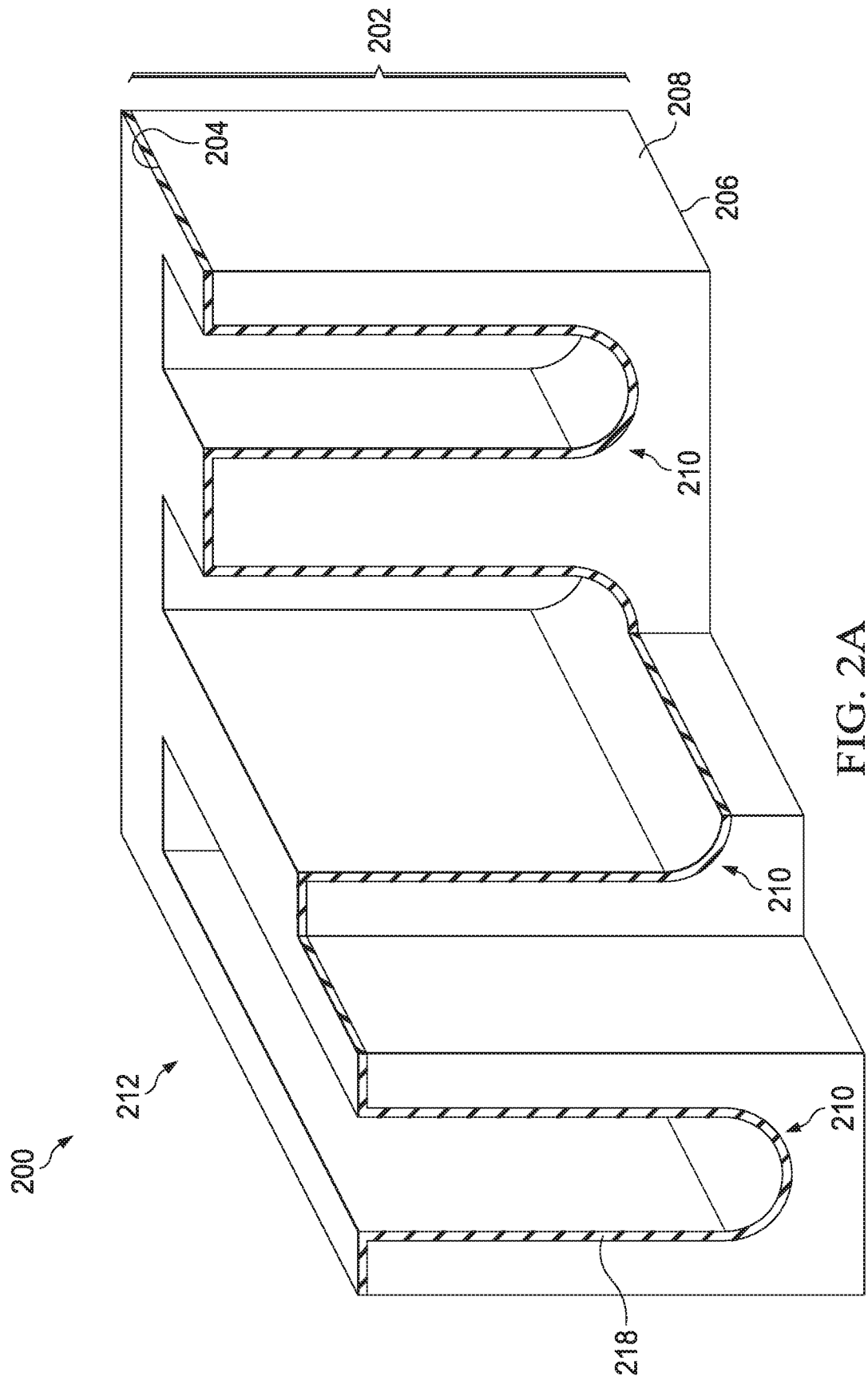


FIG. 1



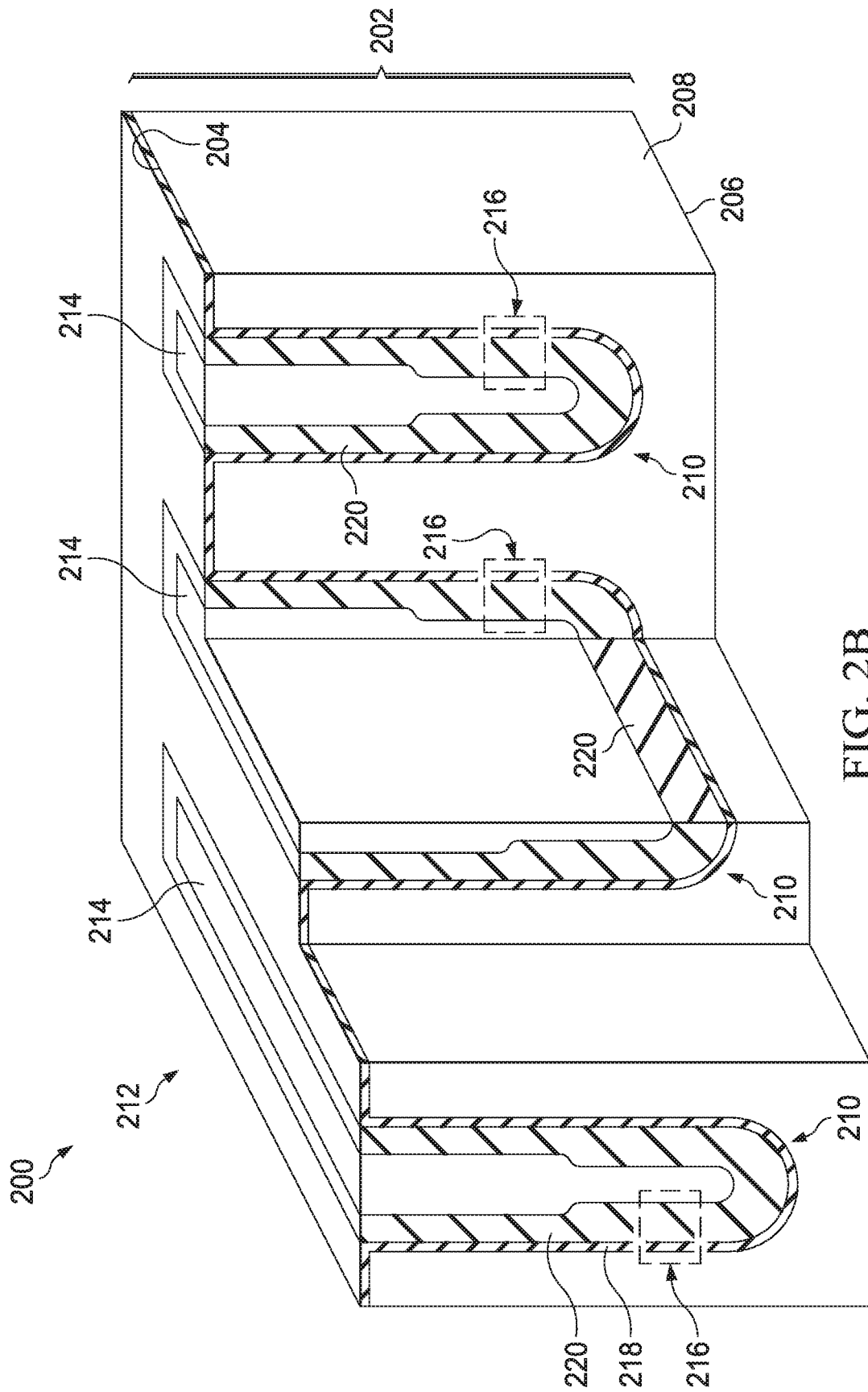


FIG. 2B*

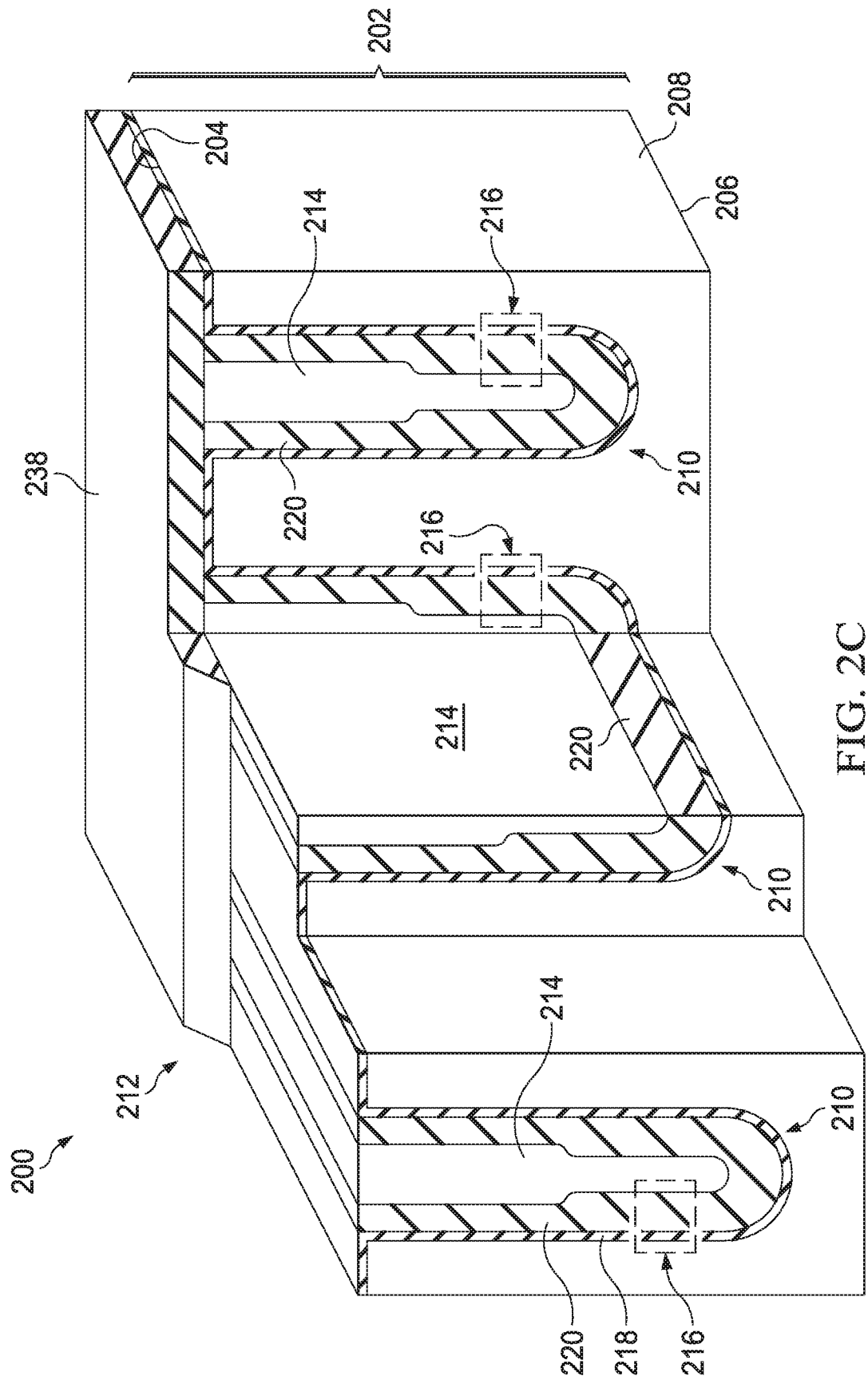


FIG. 2C

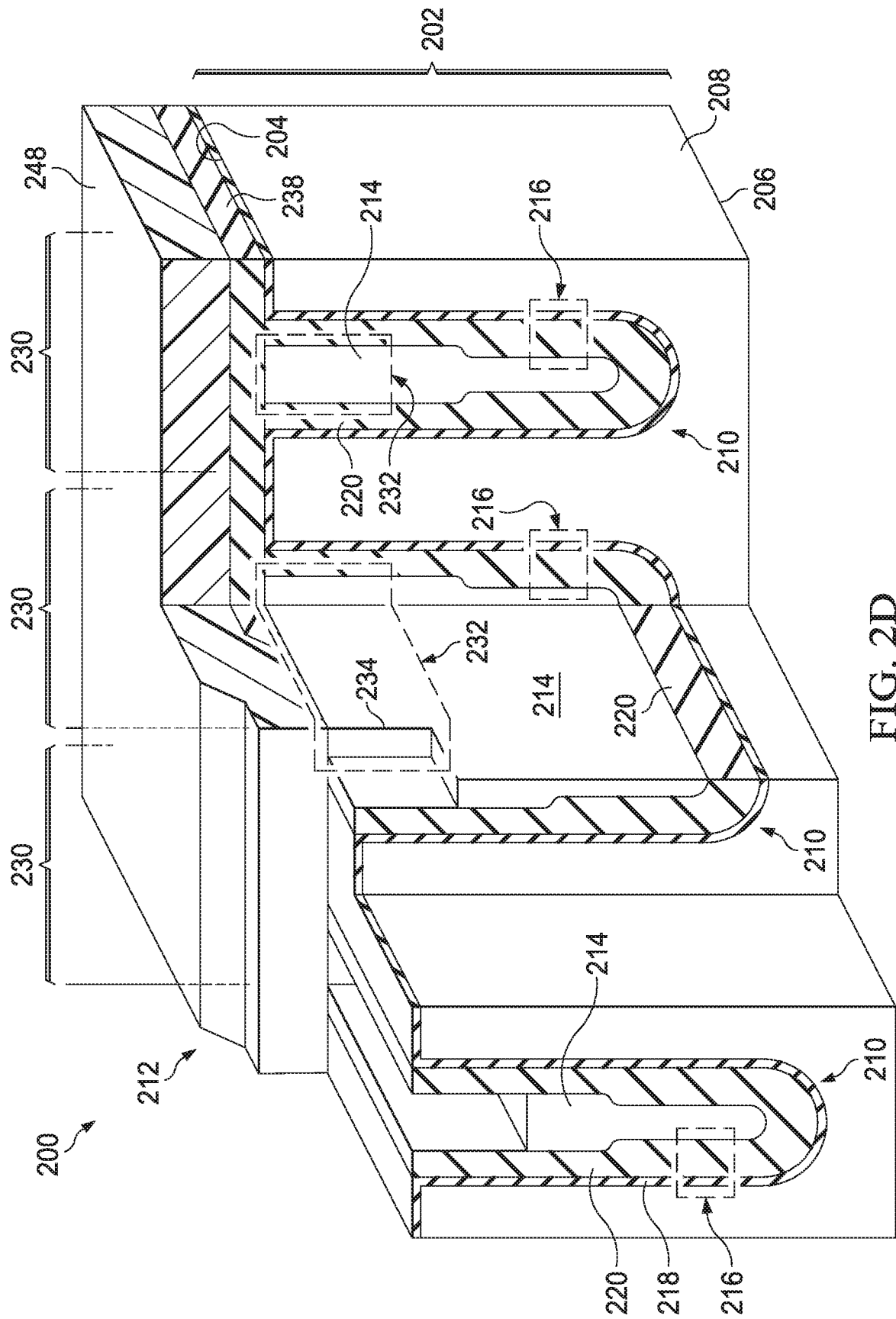


FIG. 2D

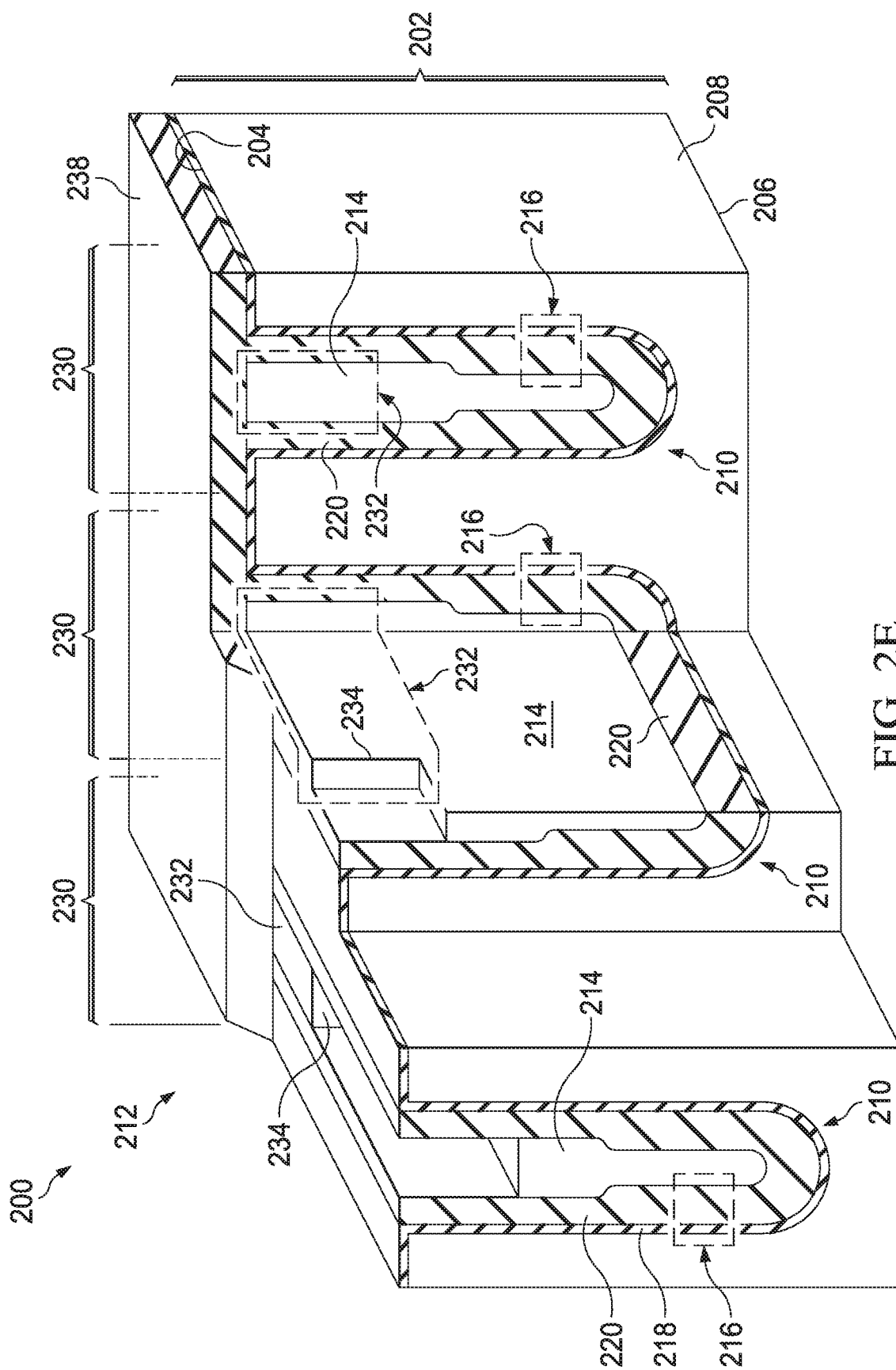


FIG. 2E

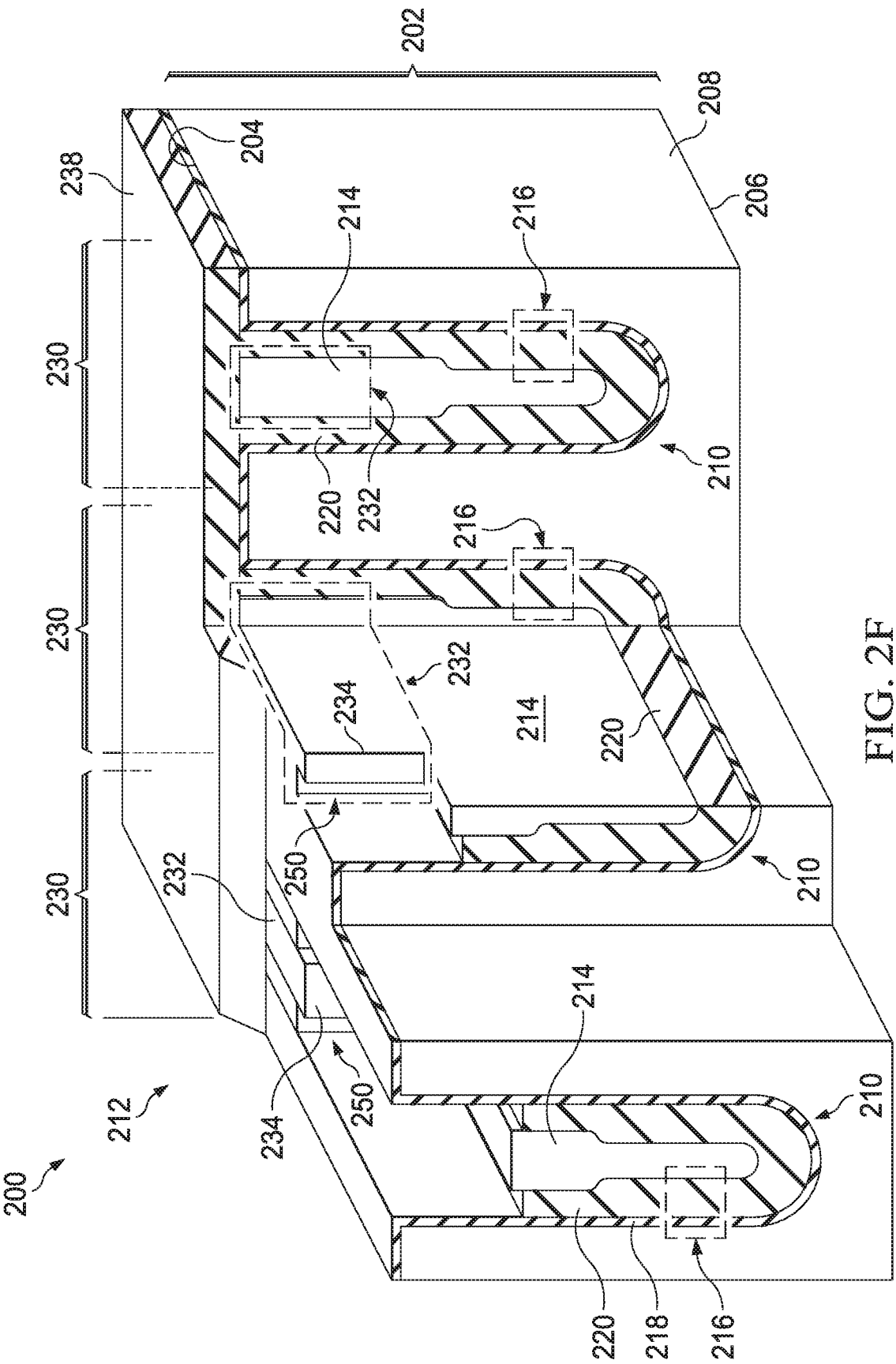


FIG. 2F

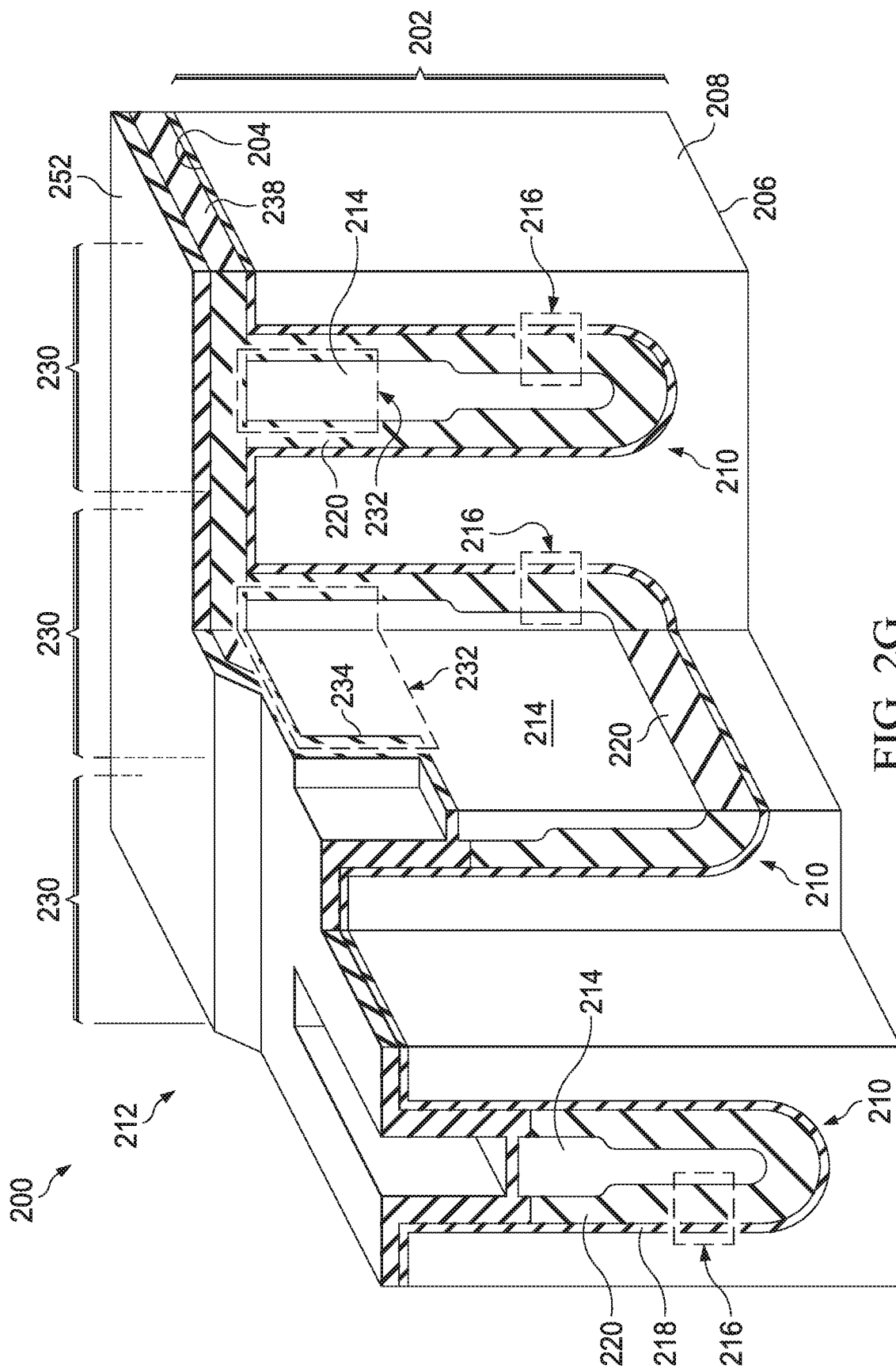


FIG. 2G

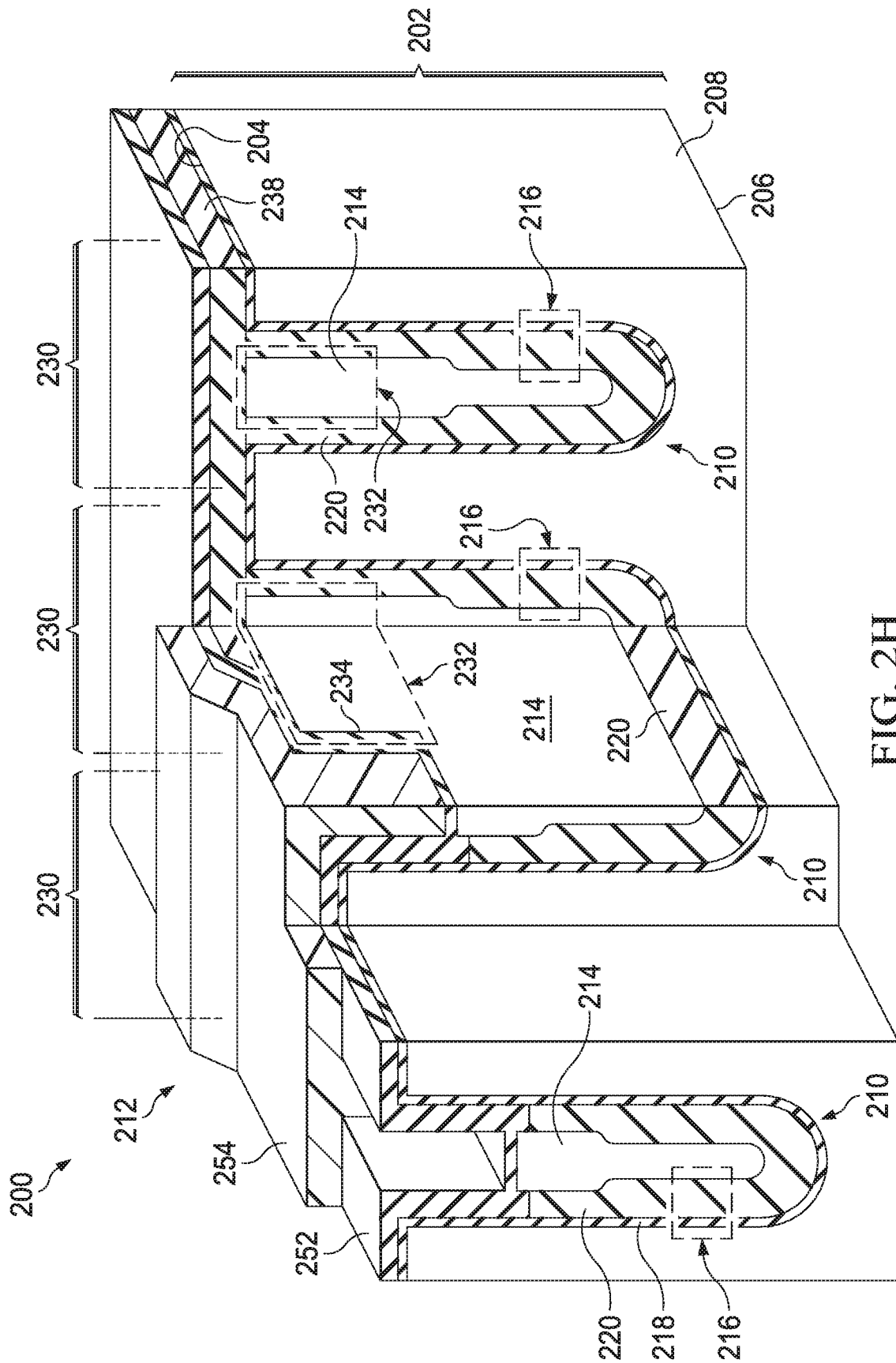
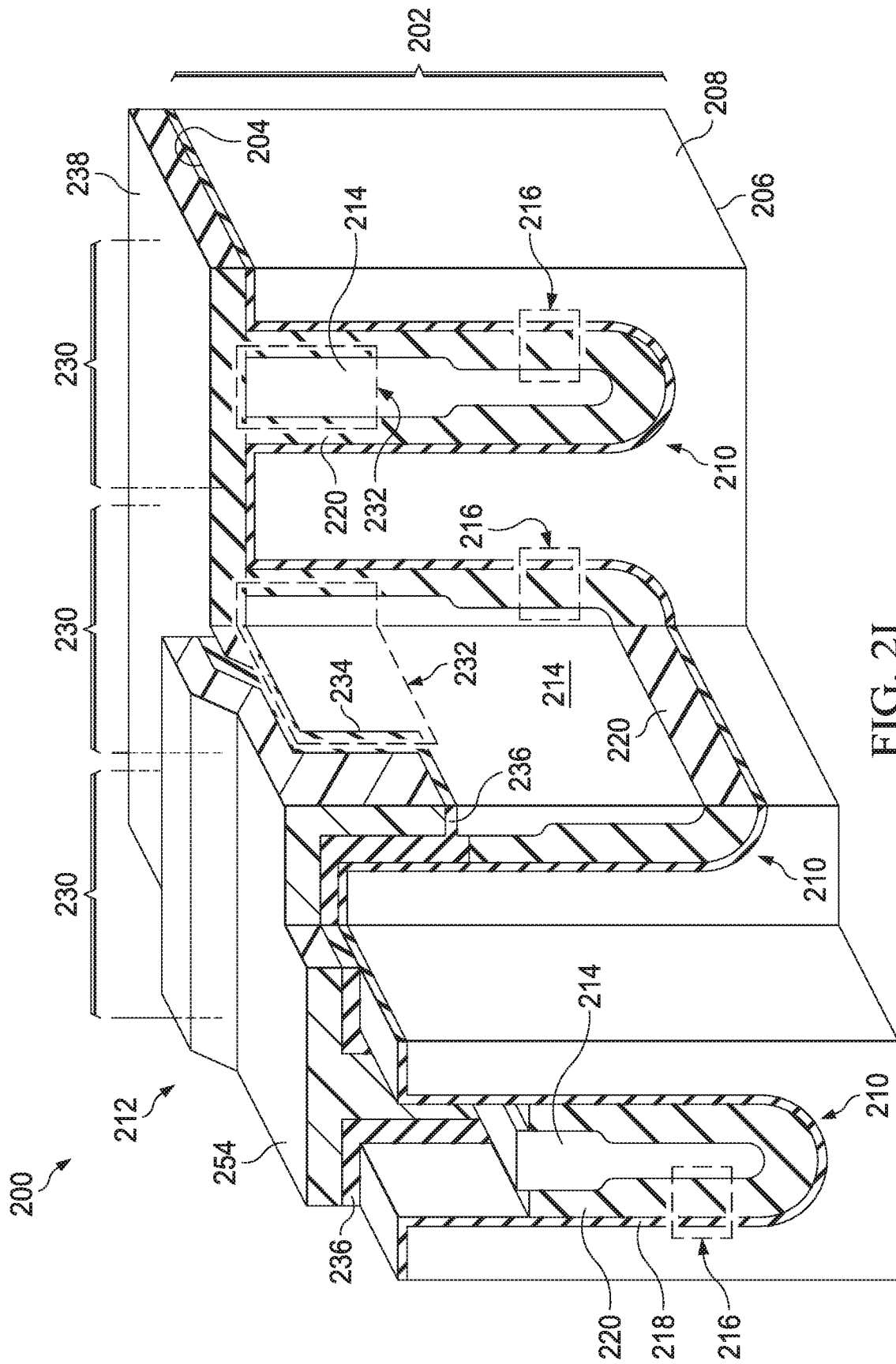


FIG. 2H



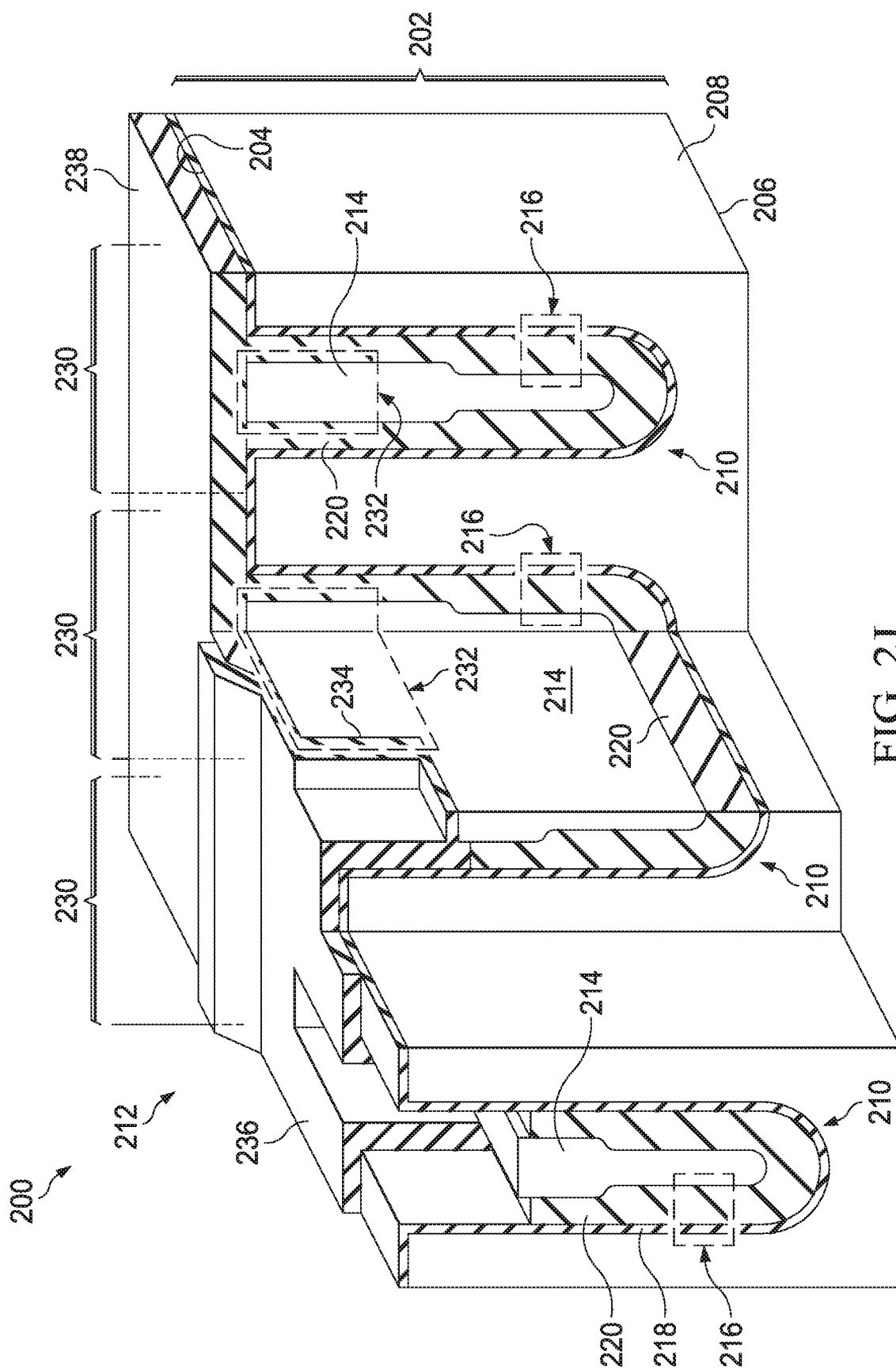


FIG. 2J

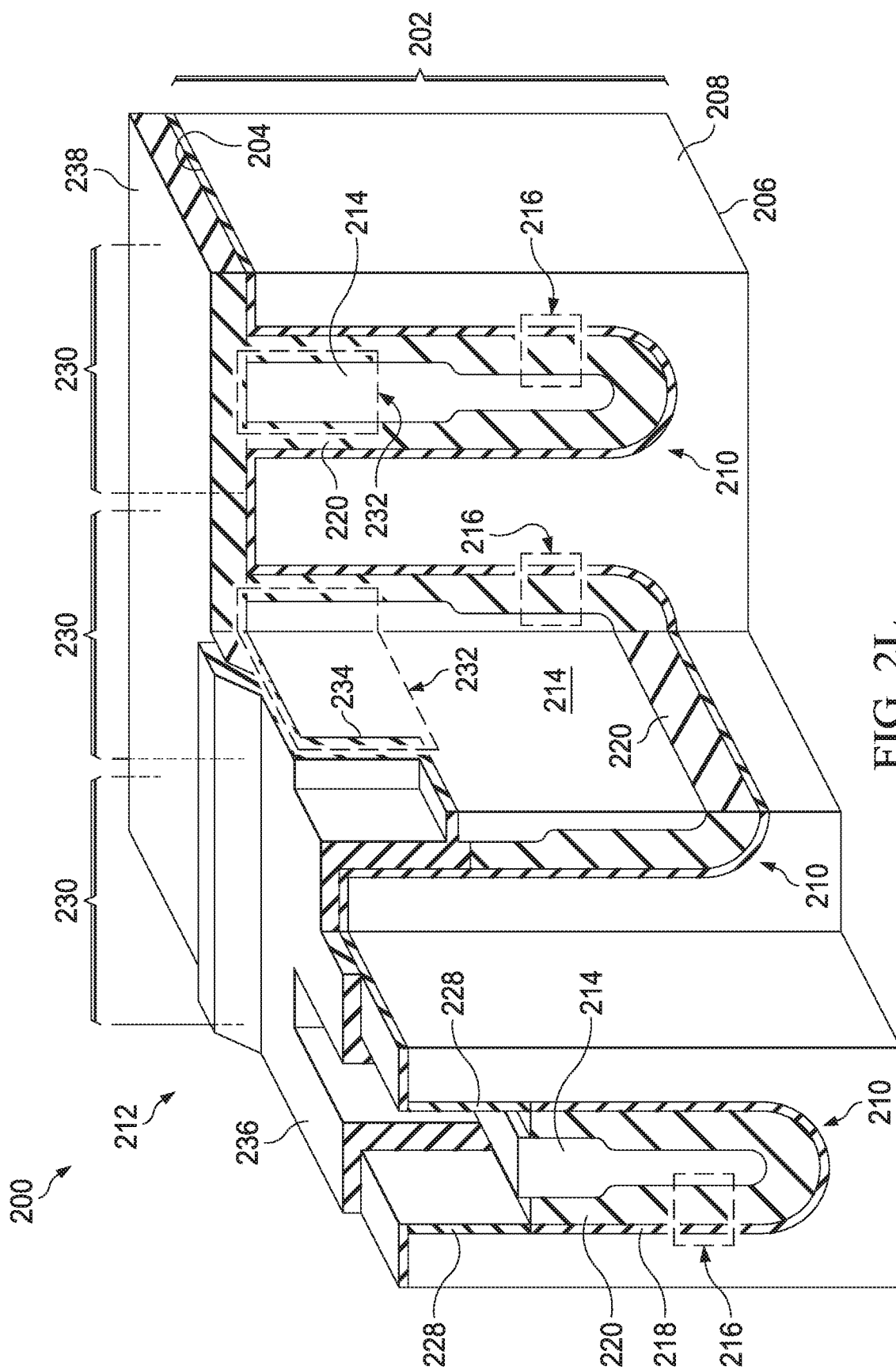


FIG. 2L

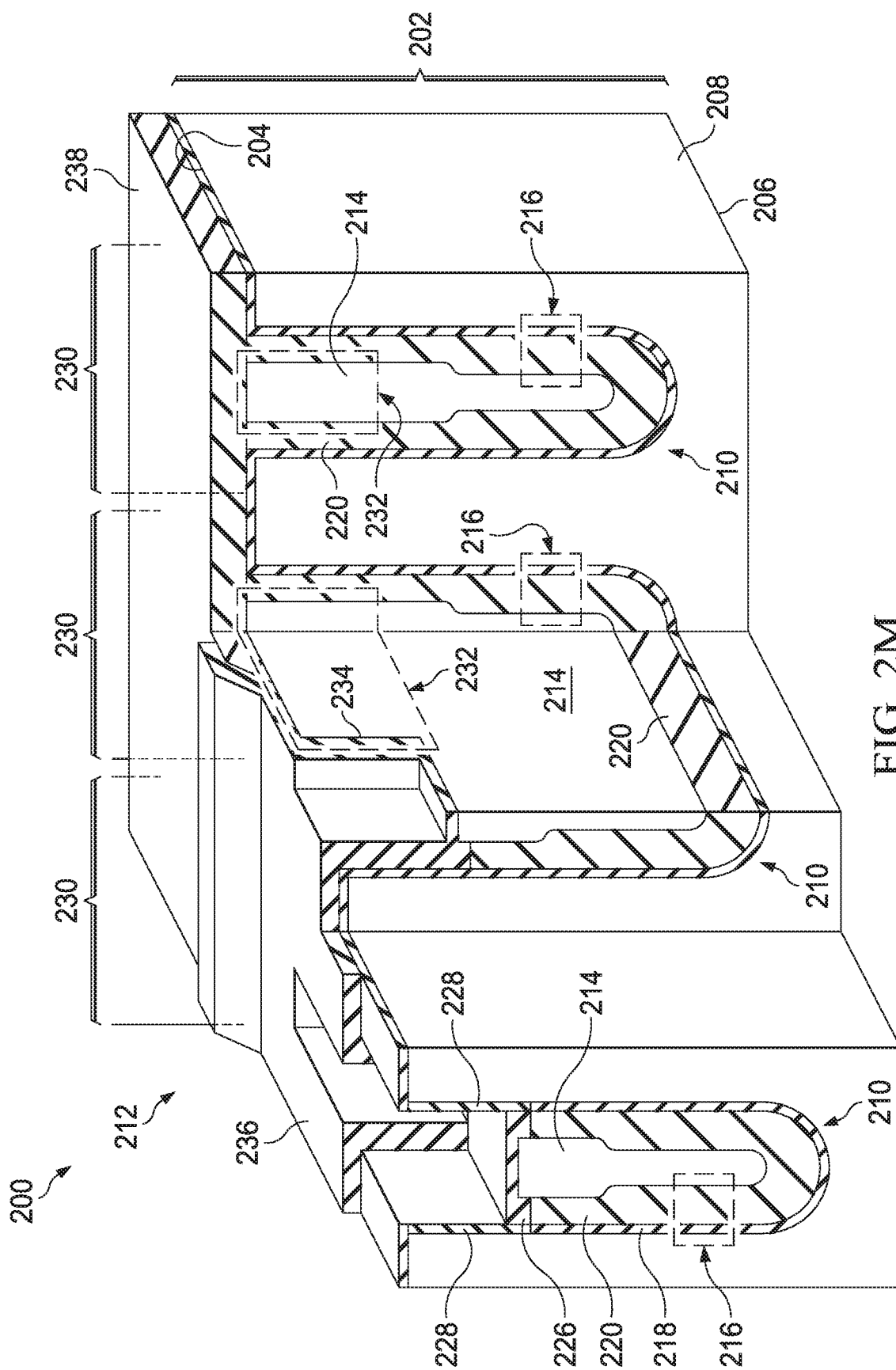


FIG. 2M

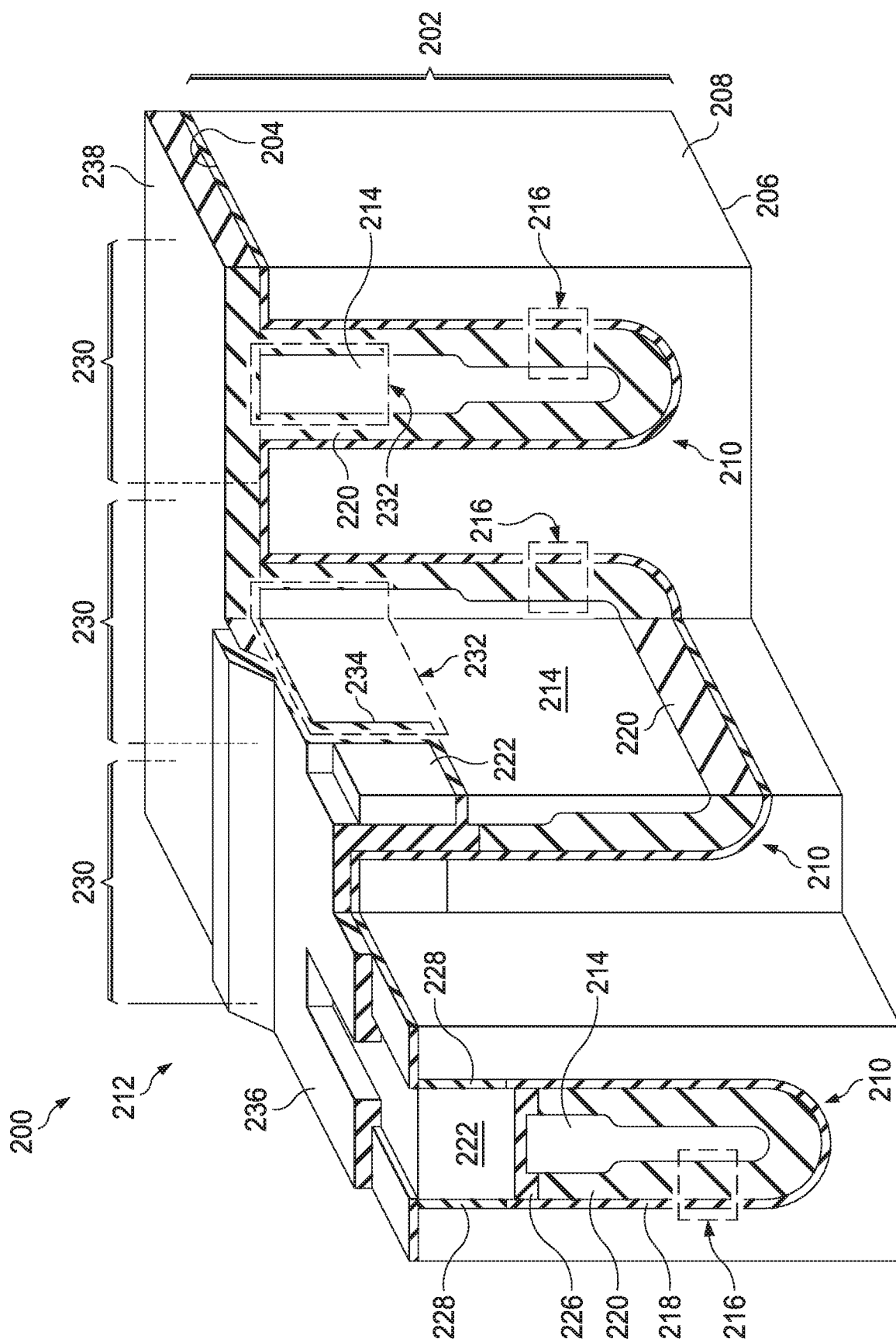


FIG. 2N

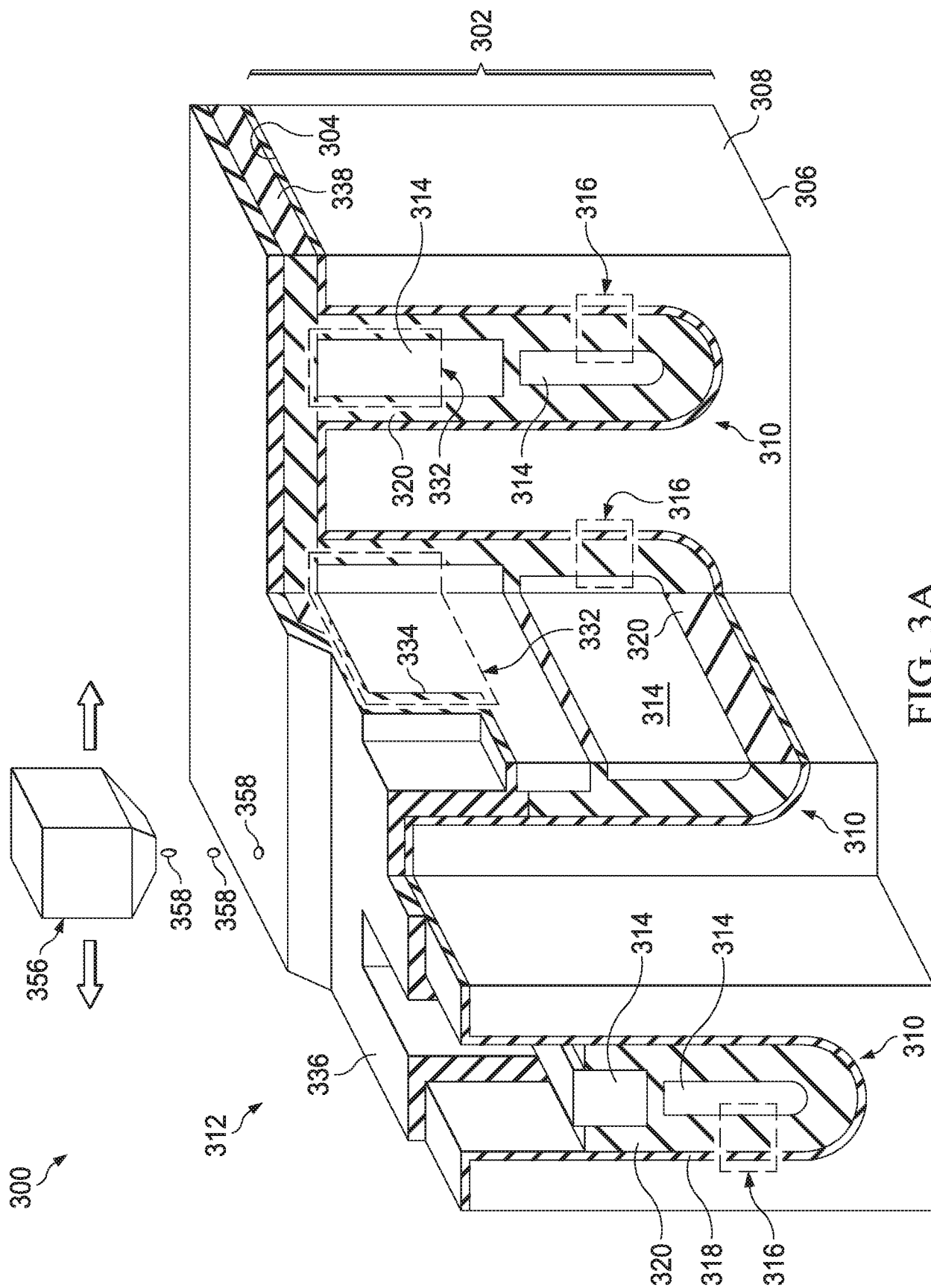


FIG. 3A

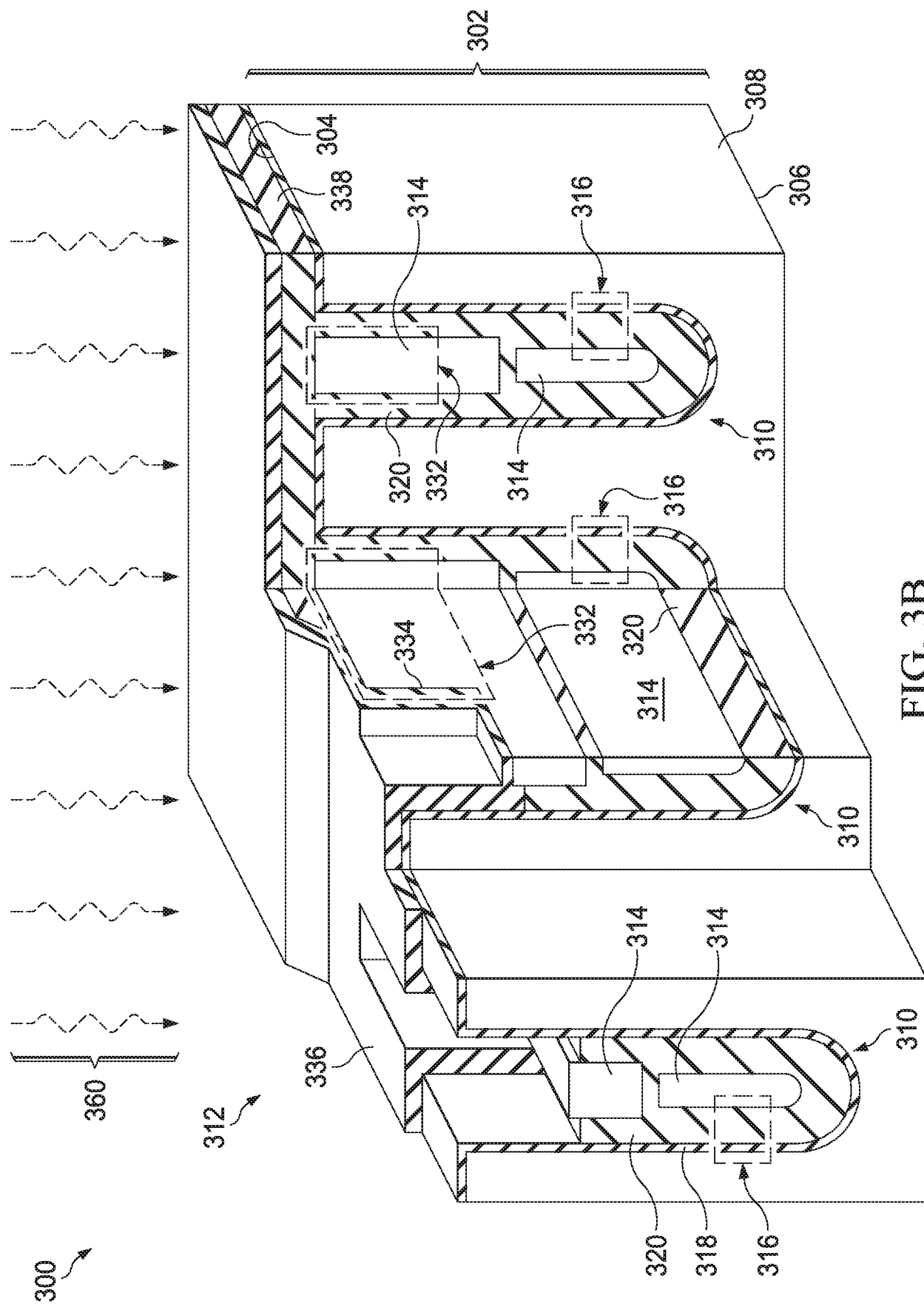


FIG. 3B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/080340

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i; H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC, CNKI, IEEE: MOS, metal, oxide, semiconductor, trench, groove, isolat+, dielectric, insulator, shield +, poly+, silicon, gate, thermal, oxidation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 103887342 A (SILERGY SEMICONDUCTOR TECHNOLOGY HANGZHO) 25 June 2014 (2014-06-25) paragraphs [0038]-[0067], figures 1-11b	1-20
A	CN 102130169 A (SHANGHAI HUAHONG NEC ELECTRONICS CO., LTD.) 20 July 2011 (2011-07-20) the whole document	1-20
A	CN 109216452 A (CSMC TECHNOLOGIES FAB2 CO., LTD.) 15 January 2019 (2019-01-15) the whole document	1-20
A	CN 102610568 A (ALPHA & OMEGA SEMICONDUCTOR INC.) 25 July 2012 (2012-07-25) the whole document	1-20
A	CN 104022043 A (AIR CHINA CHONGQING MICROELECTRONICS CO., LTD.) 03 September 2014 (2014-09-03) the whole document	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

12 December 2019

Date of mailing of the international search report

02 January 2020

Name and mailing address of the ISA/CN

National Intellectual Property Administration, PRC
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
100088
China

Authorized officer

LUO,Huijing

Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961204

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/080340

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 8642425 B2 (SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC) 04 February 2014 (2014-02-04) the whole document	1-20

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/080340

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	103887342	A	25 June 2014	CN	103887342	B	02 November 2018
CN	102130169	A	20 July 2011	CN	102130169	B	23 October 2013
CN	109216452	A	15 January 2019	None			
CN	102610568	A	25 July 2012	US	8476676	B2	02 July 2013
				TW	I445161	B	11 July 2014
				US	2013299872	A1	14 November 2013
				CN	102610568	B	10 December 2014
				US	2012187472	A1	26 July 2012
				US	8772828	B2	08 July 2014
				TW	201232760	A	01 August 2012
CN	104022043	A	03 September 2014	CN	104022043	B	16 June 2017
US	8642425	B2	04 February 2014	US	2013323921	A1	05 December 2013